TE0820 Test Board

Revision v.56

Exported on 2019-12-19

Online version of this document:

https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=92995380

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4 Overview

ZynqMP PS Design with Linux Example and simple frequency counter to measure SI5338 Reference CLK with Vivado HW-Manager.
Wiki Resources page: http://trenz.org/te0820-info

4.1 Key Features

- Vivado 2018.3
- PetaLinux
- SD
- ETH
- USB
- I2C
- RTC
- FMeter
- MAC from EEPROM
- User LED (PCB REV03 only)
- Modified FSBL for SI5338 programming
- Special FSBL for QSPI programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2019-10-29	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_09_20191029071045.zip TE0820-test_board-vivado_2018.3-build_09_20191029071028.zip	John Hartfiel	• New assembly variants
2019-08-09	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_07_20190809084040.zip TE0820-test_board-vivado_2018.3-build_07_20190809083901.zip	John Hartfiel	• bugfix fsbl (removed second PSU init)

Date	Vivado	Project Built	Authors	Description
2019-06-19	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_06_20190619073300.zip TE0820-test_board-vivado_2018.3-build_06_20190619073243.zip	John Hartfiel	• new assembly variants • USB2 only (change PS IP and device tree) • FSBL changes
2019-04-01	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_03_20190401130135.zip TE0820-test_board-vivado_2018.3-build_03_20190401130123.zip	John Hartfiel	• renamed ...D variantes to ...A
2019-02-21	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_01_20190221103025.zip TE0820-test_board-vivado_2018.3-build_01_20190221102913.zip	John Hartfiel	• TE Script update • rework of the FSBLs • SI5338 CLKBuilder Pro Project • some additional Linux features • MAC from EEPROM • new assembly variants • remove special compiler flags, which was needed in 2018.2
2018-10-31	2018.2	TE0820-test_board_noprebuilt-vivado_2018.2-build_03_20181031164506.zip TE0820-test_board-vivado_2018.2-build_03_20181031164452.zip	John Hartfiel	• new assembly variants • update optional petalinux startup init script

2018-09-12	2018.2	TE0820-test_board_noprebuilt-vivado_2018.2-build_03_20180912094615.zip
		TE0820-test_board-vivado_2018.2-build_03_20180912094558.zip
			John Hartfiel	• correction:
				  • TE0820-03-4EV-1EA has 2GB DDR, now 2GB instead of 1GB is initialised
				  • small changes on DDR setup of TE0820-02-2EG-1EE

Date	Vivado	Project Built	Authors	Description
2018-08-15	2018.2	TE0820-test_board-vivado_2018.2-build_01_20180706212937.zip TE0820-test_board_noprebuilt-vivado_2018.2-build_01_20180706212952.zip	John Hartfiel	• different design for REV03 • small petalinux changes • IO renaming • additional notes for FSBL generated with Win SDK • changed *.bif
2018-06-19	2017.4	TE0820-test_board-vivado_2017.4-build_10_20180619160713.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_10_20180619160728.zip	John Hartfiel	• bugfix board part files BANK1 MIO voltages • Add "dummy" PS USB3 parameter so solve problems with some USB2 devices
2018-05-24	2017.4	TE0820-test_board-vivado_2017.4-build_10_20180524151356.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_10_20180524151342.zip	John Hartfiel	• solved Linux Flash issue • new assembly variant
2018-04-25	2017.4	TE0820-test_board-vivado_2017.4-build_07_20180425134435.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_07_20180425134459.zip	John Hartfiel	• new assembly variants
2018-02-06	2017.4	TE0820-test_board-vivado_2017.4-build_06_20180206203359.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_06_20180206203414.zip	John Hartfiel	• solved JTAG/Linux issue

Date	Vivado	Project Built	Authors	Description
2018-02-01	2017.4	TE0820-test_board-vivado_2017.4-build_05_20180201084319.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_05_20180201094724.zip	John Hartfiel	• board part csv update
2018-01-24	2017.4	TE0820-test_board-vivado_2017.4-build_05_20180124085247.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_05_20180124085303.zip	John Hartfiel	• rework board part files • solved USB, QSPI and PHy issue
2017-11-21	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171121160552.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171121160606.zip	John Hartfiel	• solved SD SDX Cards Problem • Separate csv name for all assembly variants
2017-11-20	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171120162931.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171120162851.zip	John Hartfiel	• solved SD WP Problem
2017-10-19	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171019104824.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171019104837.zip	John Hartfiel	• initial release

Table 1: Design Revision History

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Flash access on Linux	Device tree is not correct on Linux	add compatibility to "com patible “jedec,spi-nor”"	**Solved** with 20180524 update
USB UART Terminal is blocked / SDK Debugging is blocked	This happens only with 2017.4 Linux , when JTAG connection is established on Vivado HW Manager.	Do not use HW Manager connection, or if debugging is nessecary: 1. Boot linux with usb terminal 2. From the terminal: root root mount ifconfig eth0 3. Open two new SSH terminals via ethernet: root root , run user application ... 4. Exit and close the usb terminal	**Solved** with 20180206 update

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vivado	2018.3	needed
SDK	2018.3	needed
PetaLinux	2018.3	needed
SI ClockBuilder Pro	---	optional

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[1]

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
~~TE0820-ES1~~	~~es1~~	~~REV01~~	~~1GB~~	~~64MB~~	~~4GB~~	~~NA~~	Not longer supported by vivado
TE0820-02-02EG-1E	2eg_1e_1gb	REV02	1GB	64MB	4GB	NA	NA
TE0820-02-02EG-1E3	2eg_1e_1gb	REV02	1GB	64MB	4GB	2.5 mm connectors	NA
TE0820-02-02CG-1E	2cg_1e_1gb	REV02	1GB	64MB	4GB	NA	NA
TE0820-02-03EG-1E	3eg_1e_1gb	REV02	1GB	64MB	4GB	NA	NA
TE0820-02-03EG-1E3	3eg_1e_1gb	REV02	1GB	64MB	4GB	2.5 mm connectors	NA
TE0820-02-03CG-1E	3cg_1e_1gb	REV02	1GB	64MB	4GB	NA	NA
TE0820-02-02EG-1EA	2eg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA

1 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-02-02EG-1EL	2eg_1e_1gb	REV02	1GB	128MB	4GB	2.5 mm connectors	NA
TE0820-02-02CG-1EA	2cg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA
TE0820-02-03EG-1EA	3eg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA
TE0820-02-03EG-1EL	3eg_1e_1gb	REV02	1GB	128MB	4GB	2.5 mm connectors	NA
TE0820-02-03CG-1EA	3cg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA
TE0820-02-04CG-1EA	4cg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA
TE0820-03-04EV-1EA	4ev_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02CG-1EA	2cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02EG-1EA	2eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02EG-1EL	2eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-03-03CG-1EA	3cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-04CG-1EA	4cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-03EG-1EA	3eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-03EG-1EL	3eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-2AI21FA	2cg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BE21FL	2eg_1e_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-03-3AI210A	3cg_1i_2gb	REV03	2GB	128MB	0GB	NA	NA
TE0820-03-3BE21FA	3eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-3BE21FL	3eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-02CG-1ED	2cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-03-2AE21FA	2cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BE21FA	2eg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3AE21FA	3cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3AI21FA	3cg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4AE21FA	4cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4DE21FA	4ev_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4DI21FA	4ev_1i_2gb	REV03	2GB	128MB	8GB	NA	NA

Table 4: Hardware Modules
Design supports following carriers:

Carrier Model	Notes
TE0701	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers[2]
TE0703	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 cm carriers [3] • Used as reference carrier.
TE0705	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers[4]

2 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers
3 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers
4 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers

Carrier Model	Notes
TE0706	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers[5]
TEBA0841	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers[6] • No SD Slot available, pins goes to Pin Header • For TEBA0841 REV01, please contact TE support

Table 5: Hardware Carrier

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct typ
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI
Cooler	It's recommended to use cooler on ZynqMP device

Table 6: Additional Hardware

4.5 Content

For general structure and of the reference design, see Project Delivery - Xilinx devices[7]

4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

Table 7: Design sources

5 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers
6 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices

4.5.2 Additional Sources

Type	Location	Notes
SI5338	<design name>/misc/Si5338	SI5338 Project with current PLL Configuration
init.sh	<design name>/sd/	Additional Initialization Script for Linux

Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebult content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0820 "Test Board" Reference Design[8]

8 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0820/Reference_Design/2018.3/test_board

5 Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

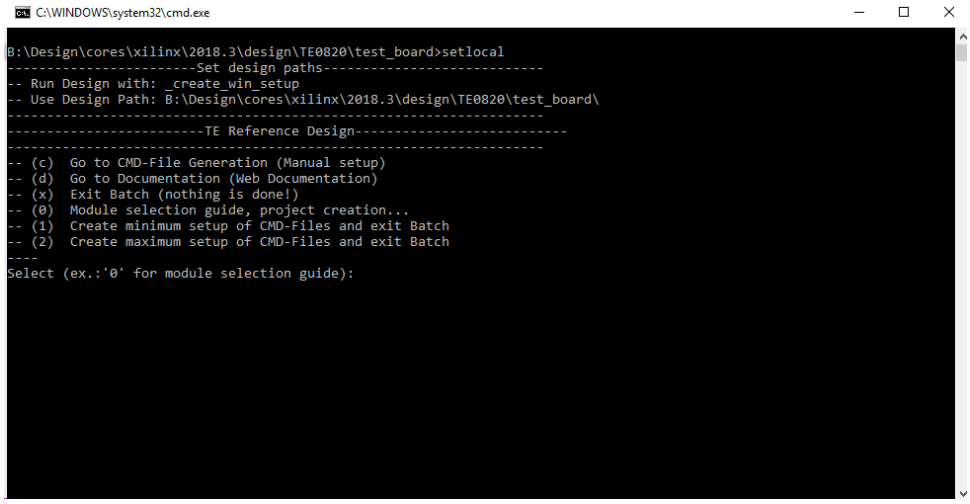
See also:

- Xilinx Development Tools[9]
- Vivado Projects - TE Reference Design[10]
- Project Delivery.[11]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[12]

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
   a. (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd" Note: Select correct one, see TE Board Part Files[13]
5. Create HDF and export to prebuilt folder

9 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides
10 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design
11 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices
12 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDelivery-Xilinxdevices-Currentlylimitationsoffunctionality
13 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (bl31.elf, uboot.elf and image.ub) with exported HDF
   a. HDF is exported to "prebuilt\hardware\<short name>"
      Note: HW Export from Vivado GUI create another path as default workspace.
      Create Linux images on VM, see PetaLinux KICKstart[14]
      i. Use TE Template from /os/petalinux
         Note: run init_config.sh before you start petalinux config. This will set correct temporary path variable.
7. Add Linux files (bl31.elf, uboot.elf and image.ub) to prebuilt folder
   a. "prebuilt\os\petalinux\default" or "prebuilt\os\petalinux\<short name>"
      Notes: Scripts select "prebuilt\os\petalinux\<short name>", if exist, otherwise "prebuilt\os\petalinux\default"
8. Generate Programming Files with HSI/SDK
   a. Run on Vivado TCL: TE::sw_run_hsi
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
      Note: See SDK Projects[15]

14 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
15 https://wiki.trenz-electronic.de/display/PD/SDK+Projects

6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging[16]

Note: Depending on CPLD Firmware and Boot Mode settings, QSPI boot with Linux image on SD or complete SD Boot is possible.

6.1.1 QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
   optional "TE::pr_program_flash_binfile -swapp hello_te0820" possible
4. Copy image.ub on SD-Card
   - For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
5. Insert SD-Card

6.1.2 SD

Use this description for CPLD Firmware with SD Boot selectable.

1. Copy image.ub and Boot.bin on SD-Card.
   - For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Insert SD-Card in SD-Slot.

6.1.3 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section Programming(see page 20)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card or QSPI as Boot Mode (Depends on used programming variant)
   Note: See TRM of the Carrier, which is used.
4. Power On PCB
   Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD/QSPI Flash into OCM, 2. FSBL loads ATF(bl31.elf) and U-boot from SD into DDR, 3. U-boot load Linux from SD into DDR

16 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging

6.2.1 Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root
3. You can use Linux shell now.
   a. I2C 0 Bus type: i2cdetect -y -r 0
   b. RTC check: dmesg | grep rtc
   c. ETH0 works with udhcpc
   d. USB type "lsusb" or connect USB2.0 device
4. Option Features
   a. Webserver to get access to Zynq
      i. insert IP on web browser to start web interface
   b. init.sh scripts
      i. add init.sh script on SD, content will be load automatically on startup (template included in ./misc/SD)

6.2.2 Vivado HW Manager

SI5338_CLK0 Counter:

1. Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).
   a. Set radix from VIO signals to unsigned integer.
      Note: Frequency Counter is inaccurate and displayed unit is Hz

SI5338 CLK is configured to 200MHz by default.

PCB REV03 Design:

- User LED, see: TE0820 CPLD[17]

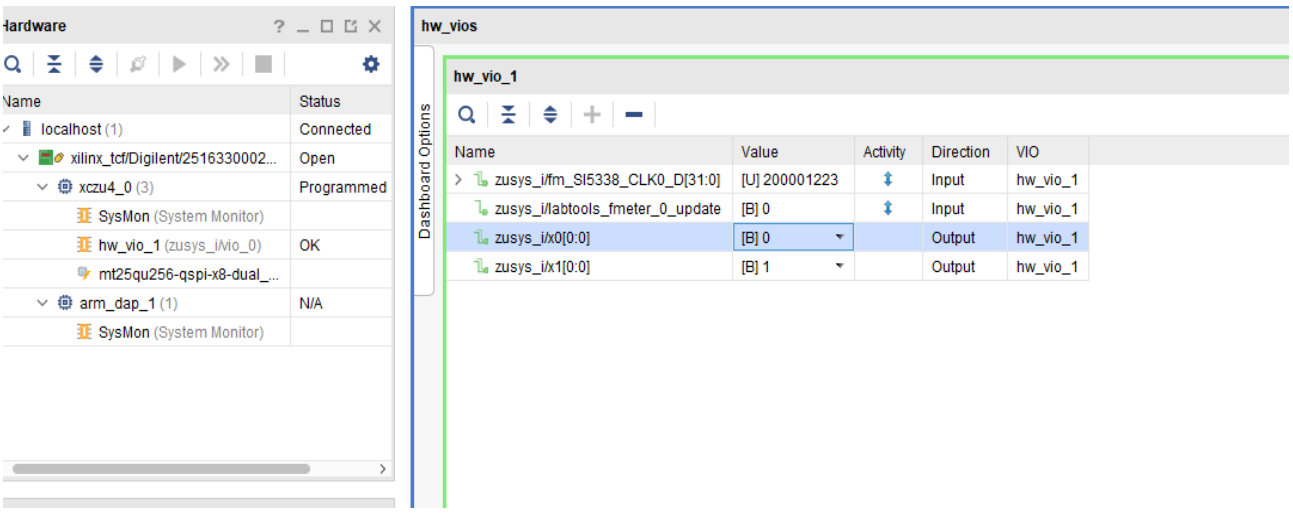


Figure 1: Vivado Hardware Manager

17 https://wiki.trenz-electronic.de/display/PD/TE0820+CPLD#TE0820CPLD-LED

PCB REV01, REV02 Design:

- PHY LEDS, see: TE0820-REV01_REV02 CPLD[18]
- CPLD Firmware, see: TE0820-REV01_REV02 CPLD[19]

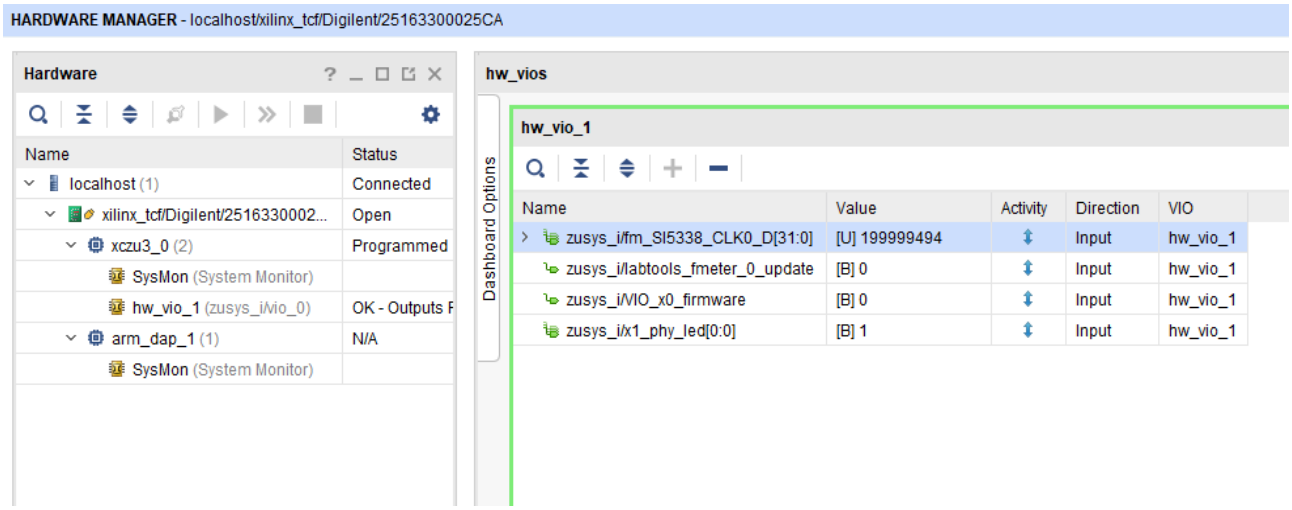


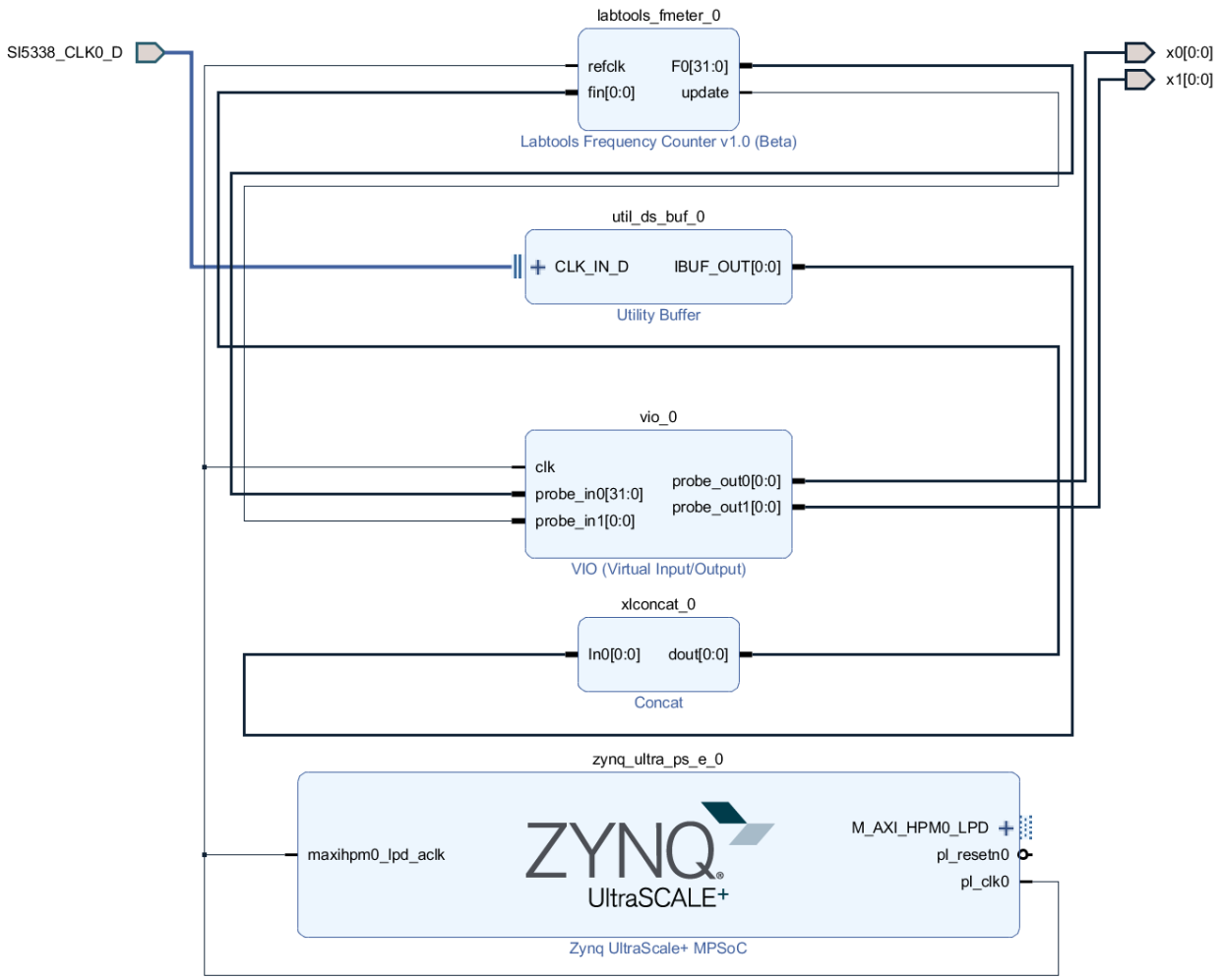
Figure 2: Vivado Hardware Manager PCB REV01,REV02

18 https://wiki.trenz-electronic.de/display/PD/TE0820-REV01_REV02+CPLD#TE0820-REV01_REV02CPLD-X0/X1Pin
19 https://wiki.trenz-electronic.de/display/PD/TE0820-REV01_REV02+CPLD#TE0820-REV01_REV02CPLD-X0/X1Pin

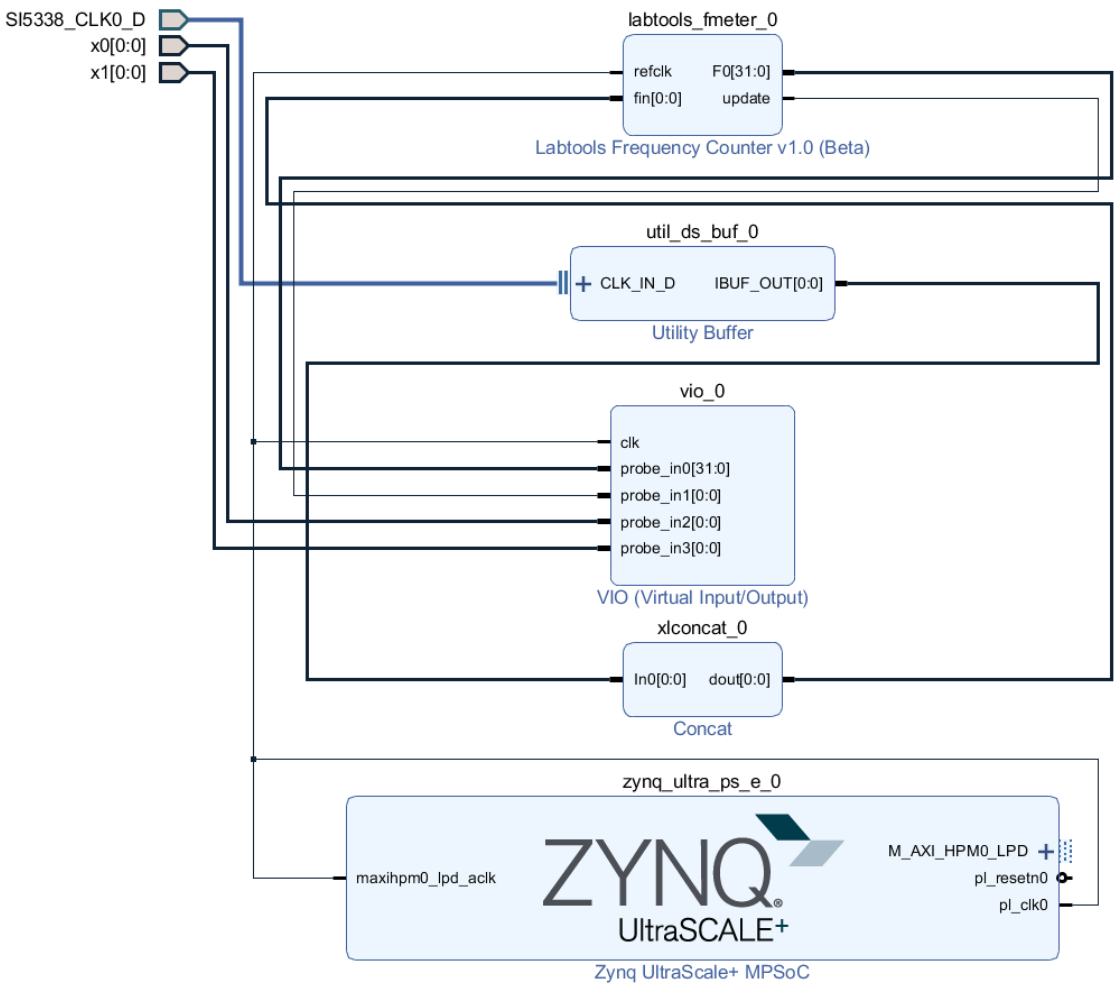
7 System Design - Vivado

7.1 Block Design

7.1.1 PCB REV03



7.1.2 PCB REV01 REV02



7.1.3 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
I2C0	MIO
UART0	MIO

Type	Note
GPIO0	MIO
SWDT0..1	
TTC0..3	
GEM3	MIO
USB0	MIO, USB2 only

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design
```

7.2.2 Design specific constrain

_i_io.xdc

```
set_property PACKAGE_PIN K9 [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property IOSTANDARD LVDS [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property DIFF_TERM TRUE [get_ports {SI5338_CLK0_D_clk_p[0]}]

set_property PACKAGE_PIN H1 [get_ports {x0[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x0[0]}]
set_property PACKAGE_PIN J1 [get_ports {x1[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x1[0]}]
```

8 Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects[20]

8.1 Application

Template location: ./sw_lib/sw_apps/

8.1.1 zynqmp_fsbl

TE modified 2018.3 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c(search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)\n\
- General Changes:
    - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te_*
    - Si5338 Configuration
    - ETH+OTG Reset over MIO

8.1.2 zynqmp_fsbl_flash

TE modified 2018.3 FSBL

General:

- Modified Files: xfsbl_initialisation.c, xfsbl_hw.h, xfsbl_handoff.c, xfsbl_main.c
- General Changes:
    - Display FSBL Banner
    - Set FSBL Boot Mode to JTAG
    - Disable Memory initialisation

8.1.3 zynqmp_pmufw

Xilinx default PMU firmware.

8.1.4 hello_te0820

Hello TE0820 is a Xilinx Hello World example as endless loop instead of one console output.

20 https://wiki.trenz-electronic.de/display/PD/SDK+Projects

8.1.5 u-boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart[21]

9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- CONFIG_SUBSYSTEM_PRIMARY_SD_PSU_SD_1_SELECT=y
- CONFIG_SUBSYSTEM_ETHERNET_PSU_ETHERNET_3_MAC=""

9.2 U-Boot

Start with **petalinux-config -c u-boot**
Changes:

- CONFIG_ENV_IS_NOWHERE=y
- CONFIG_ENV_IS_IN_SPI_FLASH is not set

Change platform-top.h:

21 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart

```
#include <configs/platform-auto.h>
#define CONFIG_SYS_BOOTM_LEN 0xF000000

#define DFU_ALT_INFO_RAM \
                "dfu_ram_info=" \
        "setenv dfu_alt_info " \
        "image.ub ram $netstart 0x1e00000\0" \
        "dfu_ram=run dfu_ram_info && dfu 0 ram 0\0" \
        "thor_ram=run dfu_ram_info && thordown 0 ram 0\0"

#define DFU_ALT_INFO_MMC \
        "dfu_mmc_info=" \
        "set dfu_alt_info " \
        "${kernel_image} fat 0 1\\\\;" \
        "dfu_mmc=run dfu_mmc_info && dfu 0 mmc 0\0" \
        "thor_mmc=run dfu_mmc_info && thordown 0 mmc 0\0"

/*Required for uartless designs */
#ifndef CONFIG_BAUDRATE
#define CONFIG_BAUDRATE 115200
#ifdef CONFIG_DEBUG_UART
#undef CONFIG_DEBUG_UART
#endif
#endif

/*Define CONFIG_ZYNQMP_EEPROM here and its necessaries in u-boot menuconfig if you
had EEPROM memory. */
#define CONFIG_ZYNQMP_EEPROM
#ifdef CONFIG_ZYNQMP_EEPROM
#define CONFIG_SYS_I2C_EEPROM_ADDR_LEN  1
#define CONFIG_CMD_EEPROM
#define CONFIG_ZYNQ_EEPROM_BUS          0
#define CONFIG_ZYNQ_GEM_EEPROM_ADDR     0x50
#define CONFIG_ZYNQ_GEM_I2C_MAC_OFFSET  0xFA
#endif
```

9.3 Device Tree

```
/include/ "system-conf.dtsi"
/ {
};


/* SDIO */

&sdhci1 {
   disable-wp;
   no-1-8-v;
};

/* ETH PHY */
&gem3 {

    status = "okay";
  ethernet_phy0: ethernet-phy@0 {
        compatible = "marvell,88e1510";
        device_type = "ethernet-phy";
            reg = <1>;
    };
};
/* USB 2.0 */

/* USB  */
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    maximum-speed = "high-speed";
    /delete-property/phy-names;
    /delete-property/phys;
    /delete-property/snps,usb3_lpm_capable;
     snps,dis_u2_susphy_quirk;
    snps,dis_u3_susphy_quirk;
};

&usb0 {
    status = "okay";
    /delete-property/ clocks;
    /delete-property/ clock-names;
    clocks = <0x3 0x20>;
    clock-names = "bus_clk";
};
```

```
/* QSPI PHY */
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};
```

9.4 Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_CPU_IDLE is not set (only needed to fix JTAG Debug issue)
- CONFIG_CPU_FREQ is not set (only needed to fix JTAG Debug issue)
- CONFIG_CPU_FREQ_DEFAULT_GOV_USERSPACE is not set (only needed to fix JTAG Debug issue)
- CONFIG_EDAC_CORTEX_ARM64=y

9.5 Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- CONFIG_i2c-tools=y
- CONFIG_busybox-httpd=y (for web server app)

9.6 Applications

9.6.1 startup

Script App to load init.sh from SD Card if available.

See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files

9.6.2 webfwu

Webserver application accemble for Zynq access. Need busybox-httpd

10 Additional Software

10.1 SI5338

File location <design name>/misc/Si5338/Si5338-*.slabtimeproj

General documentation how you work with these project will be available on Si5338[22]

22 https://wiki.trenz-electronic.de/display/PD/Si5338

11 Appx. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2019-12-19	v.57[23]	John Hartfiel[24]	• new assembly variants
2019-08-09	v.55	John Hartfiel	• bugfix fsbl
2019-06-19	v.54	John Hartfiel	• design changes • new variants
2019-04-01	v.53	John Hartfiel	• some notes • renamed ..D variants to ...A
2018-09-21	v.47	John Hartfiel	• 2018.3 release finished (include design reworks)
2018-10-31	v.43	John Hartfiel	• Update Design files for 2GB variants • rebuilt petalinux for optional init script
2018-09-12	v.41	John Hartfiel	• Update Design files for 2GB variants
2018-07-11	v.40	John Hartfiel	• add notes to ES1
2018-07-06	v.38	John Hartfiel	• 2018.2 release finished
2018-06-19	v.34	John Hartfiel	• Design Files Update
2018-02-13	v.29	John Hartfiel	• Design Files Update
2018-02-06	v.27	John Hartfiel	• Design Files Update

23 https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=43680892
24 https://wiki.trenz-electronic.de/display/~j.hartfiel

Date	Document Revision	Authors	Description
2018-01-29	v.26	John Hartfiel	• Update Known Issues
2018-01-24	v.25	John Hartfiel	• Release 2017.4
2018-01-10	v.24	John Hartfiel	• Update Known Issues
2017-12-20	v.23	John Hartfiel	• Typo correction • Update HW Module Table Description
2017-11-21	v.19	John Hartfiel	• Design Update
2017-11-20	v.18	John Hartfiel	• Design Update • Add Variants with 128MB Flash
2017-11-13	v.16	John Hartfiel	• Update Carrier sections
2017-11-06	v.15	John Hartfiel	• Typo corrected
2017-10-23	v.13	John Hartfiel	• Update Key Features section • Style Update Additional Software section
2017-10-19	v.9	John Hartfiel	• Release 2017.2
2017-09-11	v.1	John Hartfiel[25]	Initial release
	All	John Hartfiel[26]	

Table 10: Document change history.

25 https://wiki.trenz-electronic.de/display/~j.hartfiel
26 https://wiki.trenz-electronic.de/display/~j.hartfiel

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2019-06-07

27 http://guidance.echa.europa.eu/
28 https://echa.europa.eu/candidate-list-table
29 http://www.echa.europa.eu/