TE0820 Test Board

Revision v.65

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Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0820+Test+Board

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4 Overview

ZynqMP PS Design with Linux Example and simple frequency counter to measure SI5338 Reference CLK with Vivado HW-Manager.
Wiki Resources page: http://trenz.org/te0820-info

4.1 Key Features

- Vitis/Vivado 2020.2
- PetaLinux
- SD
- ETH
- USB
- I2C
- RTC
- FMeter
- MAC from EEPROM
- User LED (PCB REV03 only)
- Modified FSBL for SI5338 programming
- Special FSBL for QSPI programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2020-06-01	2020.2	TE0820-test_board-vivado_2020.2-build_5_20210601084124.zip TE0820-test_board_noprebuilt-vivado_2020.2-build_5_20210601092528.zip	John Hartfiel	• 2020.2 release • new assembly variants
2020-04-08	2019.2	TE0820-test_board_noprebuilt-vivado_2019.2-build_10_20200408073458.zip TE0820-test_board-vivado_2019.2-build_10_20200408073444.zip	John Hartfiel	• script update • new assembly variants
2020-03-25	2019.2	TE0820-test_board_noprebuilt-vivado_2019.2-build_8_20200325083817.zip TE0820-test_board-	John Hartfiel	• script update • Board Part update (minor changes)

Date	Vivado	Project Built	Authors	Description
		vivado_2019.2-build_8_20200325083750.zip		
2020-01-22	2019.2	TE0820-test_board_noprebuilt-vivado_2019.2-build_3_20200122154341.zip TE0820-test_board-vivado_2019.2-build_3_20200122154318.zip	John Hartfiel	• script update for linux user
2020-01-14	2019.2	TE0820-test_board-vivado_2019.2-build_3_20200114081551.zip TE0820-test_board_noprebuilt-vivado_2019.2-build_3_20200114081612.zip	John Hartfiel	• add fsbl_flash binary • Vitis script updates (include linux domain and prebuilt linux files for vitis) • prebuilt binary export on selection guide
2019-12-19	2019.2	TE0820-test_board-vivado_2019.2-build_1_20191219075647.zip TE0820-test_board_noprebuilt-vivado_2019.2-build_1_20191219080228.zip	John Hartfiel	• 2019.2 update • Vitis support
2019-10-29	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_09_20191029071045.zip TE0820-test_board-vivado_2018.3-build_09_20191029071028.zip	John Hartfiel	• new assembly variants
2019-08-09	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_07_20190809084040.zip TE0820-test_board-vivado_2018.3-build_07_20190809083901.zip	John Hartfiel	• bugfix fsbl (removed second PSU init)
2019-06-19	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_06_20190619073300.zip TE0820-test_board-	John Hartfiel	• new assembly variants • USB2 only (change PS IP and device tree) • FSBL changes

Date	Vivado	Project Built	Authors	Description
		vivado_2018.3-build_06_20190619073243.zip		
2019-04-01	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_03_20190401130135.zip TE0820-test_board-vivado_2018.3-build_03_20190401130123.zip	John Hartfiel	• renamed ...D variants to ...A
2019-02-21	2018.3	TE0820-test_board_noprebuilt-vivado_2018.3-build_01_20190221103025.zip TE0820-test_board-vivado_2018.3-build_01_20190221102913.zip	John Hartfiel	• TE Script update • rework of the FSBLs • SI5338 CLKBuilder Pro Project • some additional Linux features • MAC from EEPROM • new assembly variants • remove special compiler flags, which was needed in 2018.2
2018-10-31	2018.2	TE0820-test_board_noprebuilt-vivado_2018.2-build_03_20181031164506.zip TE0820-test_board-vivado_2018.2-build_03_20181031164452.zip	John Hartfiel	• new assembly variants • update optional petalinux startup init script

2018-09-12	2018.2	TE0820-test_board_noprebuilt-vivado_2018.2-build_03_20180912094615.zip
		TE0820-test_board-vivado_2018.2-build_03_20180912094558.zip
			John Hartfiel	• correction:
				  • TE0820-03-4EV-1EA has 2GB DDR, now 2GB instead of 1GB is initialised
				  • small changes on DDR setup of TE0820-02-2EG-1EE

2018-08-15	2018.2	TE0820-test_board-vivado_2018.2-build_01_20180706212937.zip TE0820-test_board_noprebuilt-vivado_2018.2-build_01_20180706212952.zip	John Hartfiel	• different design for REV03 • small petalinux changes • IO renaming • additional notes for FSBL generated with Win SDK • changed *.bif

Date	Vivado	Project Built	Authors	Description
2018-06-19	2017.4	TE0820-test_board-vivado_2017.4-build_10_20180619160713.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_10_20180619160728.zip	John Hartfiel	• bugfix board part files BANK1 MIO voltages • Add "dummy" PS USB3 parameter so solve problems with some USB2 devices
2018-05-24	2017.4	TE0820-test_board-vivado_2017.4-build_10_20180524151356.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_10_20180524151342.zip	John Hartfiel	• solved Linux Flash issue • new assembly variant
2018-04-25	2017.4	TE0820-test_board-vivado_2017.4-build_07_20180425134435.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_07_20180425134459.zip	John Hartfiel	• new assembly variants
2018-02-06	2017.4	TE0820-test_board-vivado_2017.4-build_06_20180206203359.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_06_20180206203414.zip	John Hartfiel	• solved JTAG/Linux issue
2018-02-01	2017.4	TE0820-test_board-vivado_2017.4-build_05_20180201084319.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_05_20180201094724.zip	John Hartfiel	• board part csv update
2018-01-24	2017.4	TE0820-test_board-vivado_2017.4-build_05_20180124085247.zip TE0820-test_board_noprebuilt-vivado_2017.4-build_05_20180124085303.zip	John Hartfiel	• rework board part files • solved USB, QSPI and PHY issue

Date	Vivado	Project Built	Authors	Description
2017-11-21	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171121160552.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171121160606.zip	John Hartfiel	• solved SD SDX Cards Problem • Separate csv name for all assembly variants
2017-11-20	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171120162931.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171120162851.zip	John Hartfiel	• solved SD WP Problem
2017-10-19	2017.2	TE0820-test_board-vivado_2017.2-build_05_20171019104824.zip TE0820-test_board_noprebuilt-vivado_2017.2-build_05_20171019104837.zip	John Hartfiel	• initial release

Table 1: Design Revision History

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Flash access on Linux	Device tree is not correct on Linux	add compatibility to "compatible “jedec,spi-nor”"	**Solved** with 20180524 update
USB UART Terminal is blocked / SDK Debugging is blocked	This happens only with 2017.4 Linux , when JTAG connection is established on Vivado HW Manager.	Do not use HW Manager connection, or if debugging is necessary: 1. Boot linux with usb terminal 2. From the terminal: root root mount ifconfig eth0 3. Open two new SSH terminals via ethernet:	**Solved** with 20180206 update

Issues	Description	Workaround	To be fixed version
		root root , run user application ... 4. Exit and close the usb terminal	

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2020.2	needed, Vivado is included into Vitis installation
PetaLinux	2020.2	needed
SI ClockBuilder Pro	---	optional

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[1]

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
~~TE0820-ES1~~	~~es1~~	~~REV01~~	~~1GB~~ -	~~64MB~~	~~4GB~~	~~NA~~	Not longer supported by vivado
TE0820-02-02EG-1E	2eg_1e_1gb	REV02	1GB	64MB	4GB	NA	NA

1 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-02-02EG-1E3	2eg_1e_1gb	REV02	1GB	64MB	4GB	2.5 mm connectors	NA
TE0820-02-02CG-1E	2cg_1e_1gb	REV02	1GB	64MB	4GB	NA	NA
TE0820-02-03EG-1E	3eg_1e_1gb	REV02	1GB	64MB	4GB	NA	NA
TE0820-02-03EG-1E3	3eg_1e_1gb	REV02	1GB	64MB	4GB	2.5 mm connectors	NA
TE0820-02-03CG-1E	3cg_1e_1gb	REV02	1GB	64MB	4GB	NA	NA
TE0820-02-02EG-1EA	2eg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA
TE0820-02-02EG-1EL	2eg_1e_1gb	REV02	1GB	128MB	4GB	2.5 mm connectors	NA
TE0820-02-02CG-1EA	2cg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA
TE0820-02-03EG-1EA	3eg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA
TE0820-02-03EG-1EL	3eg_1e_1gb	REV02	1GB	128MB	4GB	2.5 mm connectors	NA
TE0820-02-03CG-1EA	3cg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-02-04CG-1EA	4cg_1e_1gb	REV02	1GB	128MB	4GB	NA	NA
TE0820-03-04EV-1EA	4ev_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02CG-1EA	2cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02EG-1EA	2eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-02EG-1EL	2eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-03CG-1EA	3cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-04CG-1EA	4cg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-03EG-1EA	3eg_1e_2gb	REV03	2GB	128MB	4GB	NA	NA
TE0820-03-03EG-1EL	3eg_1e_2gb	REV03	2GB	128MB	4GB	2.5 mm connectors	NA
TE0820-03-2AI21FA	2cg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BE21FL	2eg_1e_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-03-3AI210A	3cg_1i_2gb	REV03	2GB	128MB	0GB	NA	NA
TE0820-03-3BE21FA	3eg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3BE21FL	3eg_1e_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-03-02CG-1ED	2cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2AE21FA	2cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BE21FA	2eg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3AE21FA	3cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-3AI21FA	3cg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4AE21FA	4cg_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4DE21FA	4ev_1e_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-4DI21FA	4ev_1i_2gb	REV03	2GB	128MB	8GB	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-03-4DE21FL	4ev_1e_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-03-4AE21FI	4cg_1e_x_2gb	REV03	2GB	128MB	8GB	without ETH PHY	NA
TE0820-03-4DE21FC	4ev_1e_2gb	REV03	2GB	128MB	8GB	without encryption NCNR	NA
TE0820-03-4AI21FI	4cg_1i_x_2gb	REV03	2GB	128MB	8GB	without ETH PHY	NA
TE0820-03-5DR21FA	5ev_1q_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BI21FA	2eg_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-03-2BI21FL	2eg_1i_2gb	REV03	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-03-5DI21FA	5ev_1i_2gb	REV03	2GB	128MB	8GB	NA	NA
TE0820-04-2AE21FA	2cg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2AI21FA	2cg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BE21FA	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BE21FAJ	2eg_1e_2gb	REV04	2GB	128MB	8GB	without spacers	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-04-2BE21FL*	2eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-04-2BE21-V1	2eg_1e_2gb	REV04	2GB	128MB	8GB	NA	Customised
TE0820-04-2BI21FA	2eg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-2BI21FL	2eg_1i_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-04-3AE21FA	3cg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-3AI21FA	3cg_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-3AI21FAT	3cg_1i_2gb	REV04	2GB	128MB	8GB	NA	Customer supplied
TE0820-04-3BE21FA	3eg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-3BE21FL	3eg_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-04-3BE21KA	3eg_1e_2gb	REV04	2GB	128MB	64GB	NA	NA
TE0820-04-4AE21FA	4cg_1e_2gb	REV04	2GB	128MB	8GB	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0820-04-4AI21FI	4cg_1i_x_2gb	REV04	2GB	128MB	8GB	without ETH PHY	NA
TE0820-04-4BI21KL	4eg_1i_2gb	REV04	2GB	128MB	64GB	2.5 mm connectors	NA
TE0820-04-4DE21FA	4ev_1e_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-4DE21FL	4ev_1e_2gb	REV04	2GB	128MB	8GB	2.5 mm connectors	NA
TE0820-04-4DI21FA	4ev_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-5DI21FA	5ev_1i_2gb	REV04	2GB	128MB	8GB	NA	NA
TE0820-04-5DR21FA	5ev_1q_2gb	REV04	2GB	128MB	8GB	NA	NA

Table 4: Hardware Modules

*used as reference

Design supports following carriers:

Carrier Model	Notes
TE0701	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers[2]
TE0703*	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 cm carriers [3] • Used as reference carrier.
TE0705	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers[4]

2 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers
3 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers
4 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers

Carrier Model	Notes
TE0706	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers[5]
TEBA0841	• Important: See restrictions on usage with 7 Serie Carriers: 4 x 5 SoM Carriers[6] • No SD Slot available, pins goes to Pin Header • For TEBA0841 REV01, please contact TE support

Table 5: Hardware Carrier

*used as reference

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct typ
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI
Cooler	It's recommended to use cooler on ZynqMP device

Table 6: Additional Hardware

4.5 Content

For general structure and of the reference design, see Project Delivery - Xilinx devices[7]

4.5.1 Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

5 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers
6 https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Carriers
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices

Type	Location	Notes
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
SI5338	<project folder>\misc\Si5338	SI5338 Project with current PLL Configuration
init.sh	<project folder>\sd\	Additional Initialization Script for Linux

Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Boot Source	*.scr	Distro Boot file
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform -Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File

File	File-Extension	Description
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebuilt content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0820 "Test Board" Reference Design[8]

8 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0820/Reference_Design/2020.2/test_board

5 Design Flow

> Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- Xilinx Development Tools[9]
- Vivado Projects - TE Reference Design[10]
- Project Delivery.[11]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[12]

> **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
------------------------Set design paths----------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
------------------------------------------------------------------
-------------------------TE Reference Design---------------------------
------------------------------------------------------------------
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.

9 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides
10 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design
11 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices
12 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality

- optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

  ⚠ Note: Select correct one, see also Vivado Board Part Flow[13]

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "\prebuilt\hardware\")

```
\prebuilt\hardware\")">
TE::hw_build_design -export_prebuilt
```

ⓘ Using Vivado GUI is the same, except file export to prebuilt folder.

5. Create and configure your PetaLinux project with exported .xsa-file, see PetaLinux KICKstart[14]
   - use TE Template from "<project folder>\os\petalinux"
   - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>" . **Note:** HW Export from Vivado GUI creates another path as default workspace.
6. Configure the **boot.scr** file as needed, see Distro Boot with Boot.scr[15]
7. Copy PetaLinux build image files to prebuilt folder
   - copy **u-boot.elf, bl31.elf**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

     ⓘ "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

8. Generate Programming Files with Vitis

run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE
Scripts on Vivado TCL)
```

⚠ TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis[16]

13 https://wiki.trenz-electronic.de/display/PD/Vivado+Board+Part+Flow
14 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
15 https://wiki.trenz-electronic.de/display/PD/Distro+Boot+with+Boot.scr
16 https://wiki.trenz-electronic.de/display/PD/Vitis

6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging[17]

Note: Depending on CPLD Firmware and Boot Mode settings, QSPI boot with Linux image on SD or complete SD Boot is possible.

6.1.1 Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select create and open delivery binary folder

   ⓘ Note: Folder "<project folder>/_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

6.1.2 QSPI-Boot mode

Option for **Boot.bin** on QSPI Flash and **image.ub** and **boot.scr** on **SD** or **USB**.

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

   run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

   ```
   TE::pr_program_flash -swapp u-boot
   TE::pr_program_flash -swapp hello_te0820 (optional)
   ```

   ⚠ To program with Vitis/Vivado GUI, use special FSBL (fsbl_flash) on setup

3. Copy **image.ub** and **boot.scr** on **SD** or **USB**
   - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder,see: Get prebuilt boot binaries(see page 24)
   - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
4. Set Boot Mode to **QSPI-Boot** and insert **SD** or **USB**.
   - Depends on Carrier, see carrier TRM.

17 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging

6.1.3 SD-Boot mode

1. Copy **image.ub**, **boot.src** and **Boot.bin** on **SD**
   - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder, see: Get prebuilt boot binaries(see page 24)
   - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
2. Set Boot Mode to SD-Boot.
   - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

6.1.4 JTAG

Not used on this example.

6.2 Usage

1. Prepare HW like described on section Programming(see page 24)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)

   Note: See TRM of the Carrier, which is used.

   Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.
   The boot options described above describe the common boot processes for this hardware; other boot options are possible.
   For more information see Distro Boot with Boot.scr[18]

4. Power On PCB
   boot process

   1. ZynqMP Boot ROM loads FSBL from SD/QSPI into OCM,

   2. FSBL init the PS, programs the PL using the bitstream and loads PMU, ATF and U-boot from SD/QSPI into DDR,

   3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

6.2.1 Linux

1. Open Serial Console (e.g. putty)
   - Speed: 115200
   - select COM Port

     Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)

2. Linux Console:

18 https://wiki.trenz-electronic.de/display/PD/Distro+Boot+with+Boot.scr

```
petalinux login: root
Password: root
```

Note: Wait until Linux boot finished

3. You can use Linux shell now.

```
i2cdetect -y -r 0   (check I2C 0 Bus)
dmesg | grep rtc    (RTC check)
udhcpc              (ETH0 check)
lsusb               (USB check)
```

4. Option Features
    - Webserver to get access to Zynq
        - insert IP on web browser to start web interface
    - init.sh scripts
        - add init.sh script on SD, content will be load automatically on startup (template included in "<project folder>\misc\SD")

6.2.2 Vivado HW Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder)

- Control:
    - User LED (PCB REV03 and newer)
- Monitoring:
    - SI5338_CLK0 Counter:
        - Set radix from VIO signals to unsigned integer.
          Note: Frequency Counter is inaccurate and displayed unit is Hz
        - SI5338 CLK is configured to 200MHz by default.

PCB REV03 Design:

- User LED, see: TE0820 CPLD[19]

19 https://wiki.trenz-electronic.de/display/PD/TE0820+CPLD#TE0820CPLD-LED

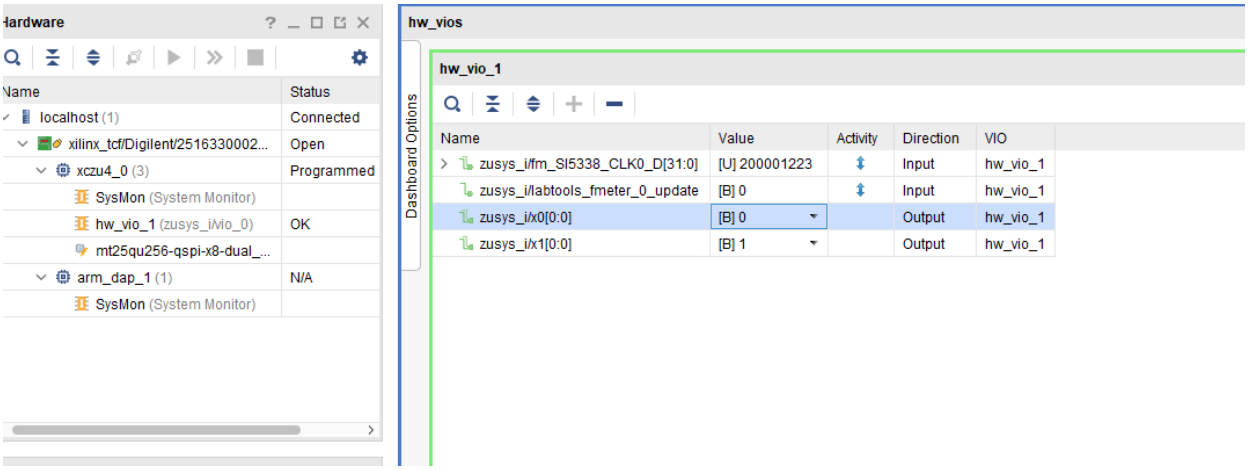

Figure 1: Vivado Hardware Manager

PCB REV01, REV02 Design:

- PHY LEDS, see: TE0820-REV01_REV02 CPLD[20]
- CPLD Firmware, see: TE0820-REV01_REV02 CPLD[21]

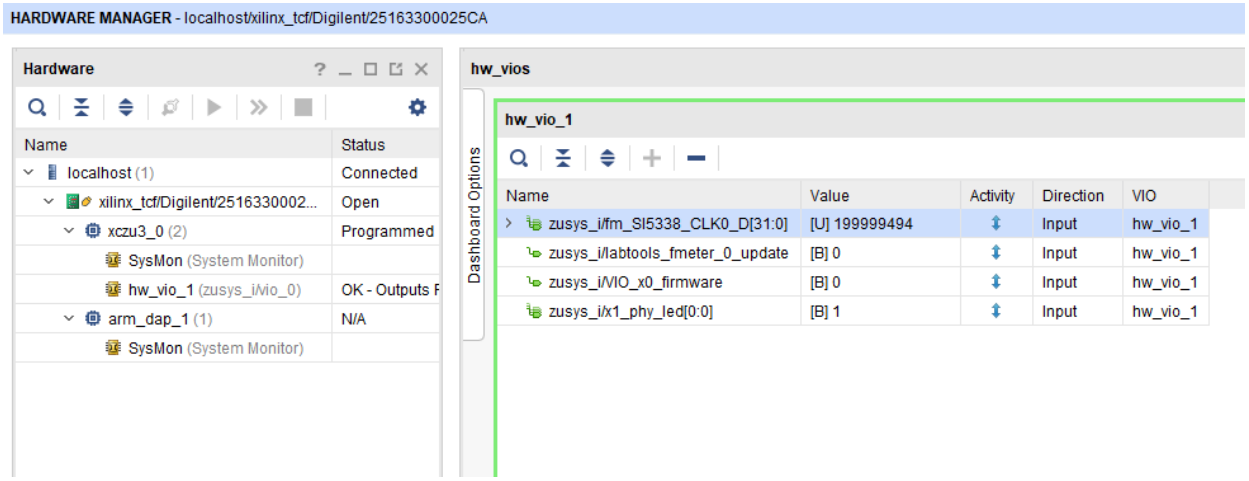

Figure 2: Vivado Hardware Manager PCB REV01,REV02

20 https://wiki.trenz-electronic.de/display/PD/TE0820-REV01_REV02+CPLD#TE0820REV01_REV02CPLD-X0/X1Pin
21 https://wiki.trenz-electronic.de/display/PD/TE0820-REV01_REV02+CPLD#TE0820REV01_REV02CPLD-X0/X1Pin

7 System Design - Vivado

7.1 Block Design

7.1.1 PCB REV03

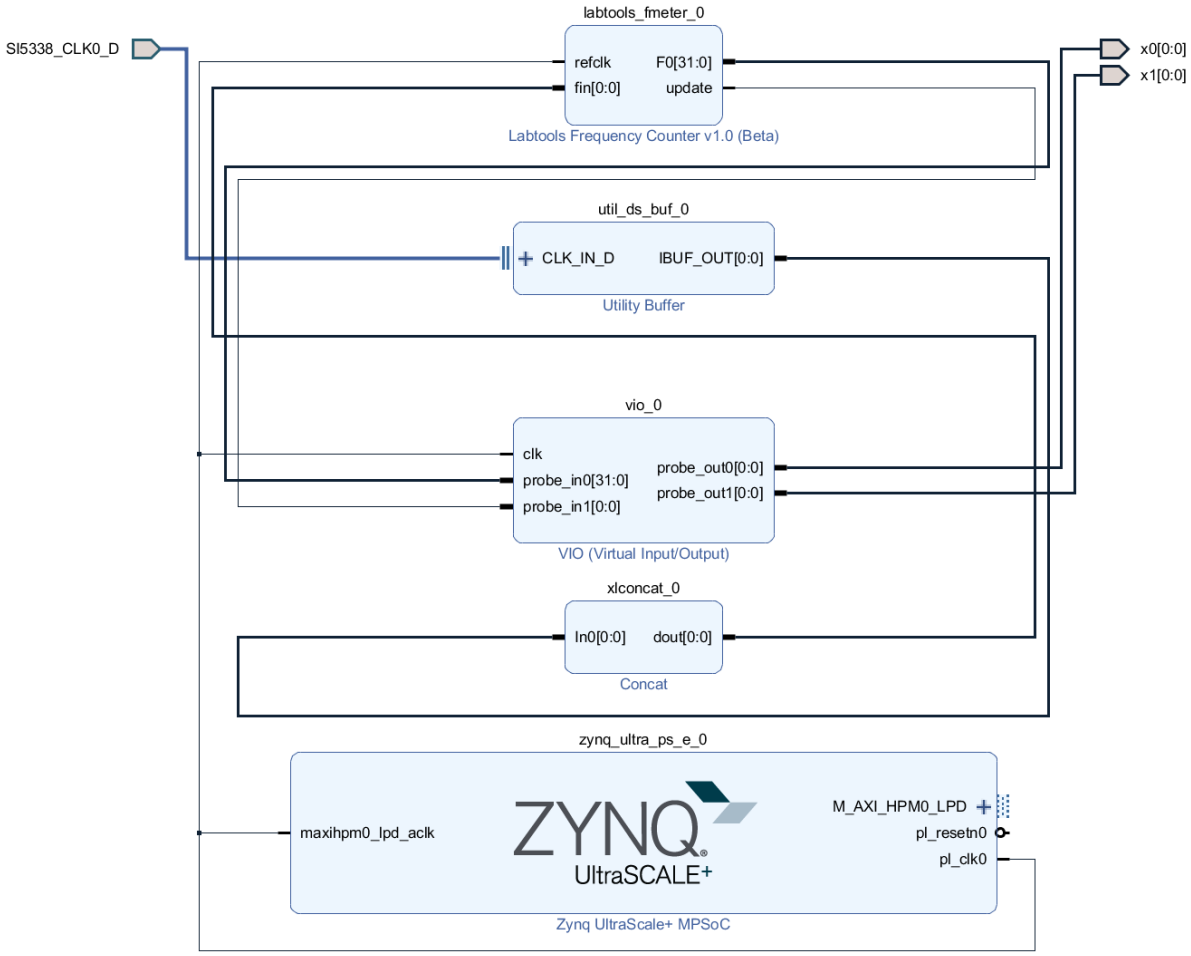

Figure 3: Block Design PCB REV03

7.1.2 PCB REV01 REV02

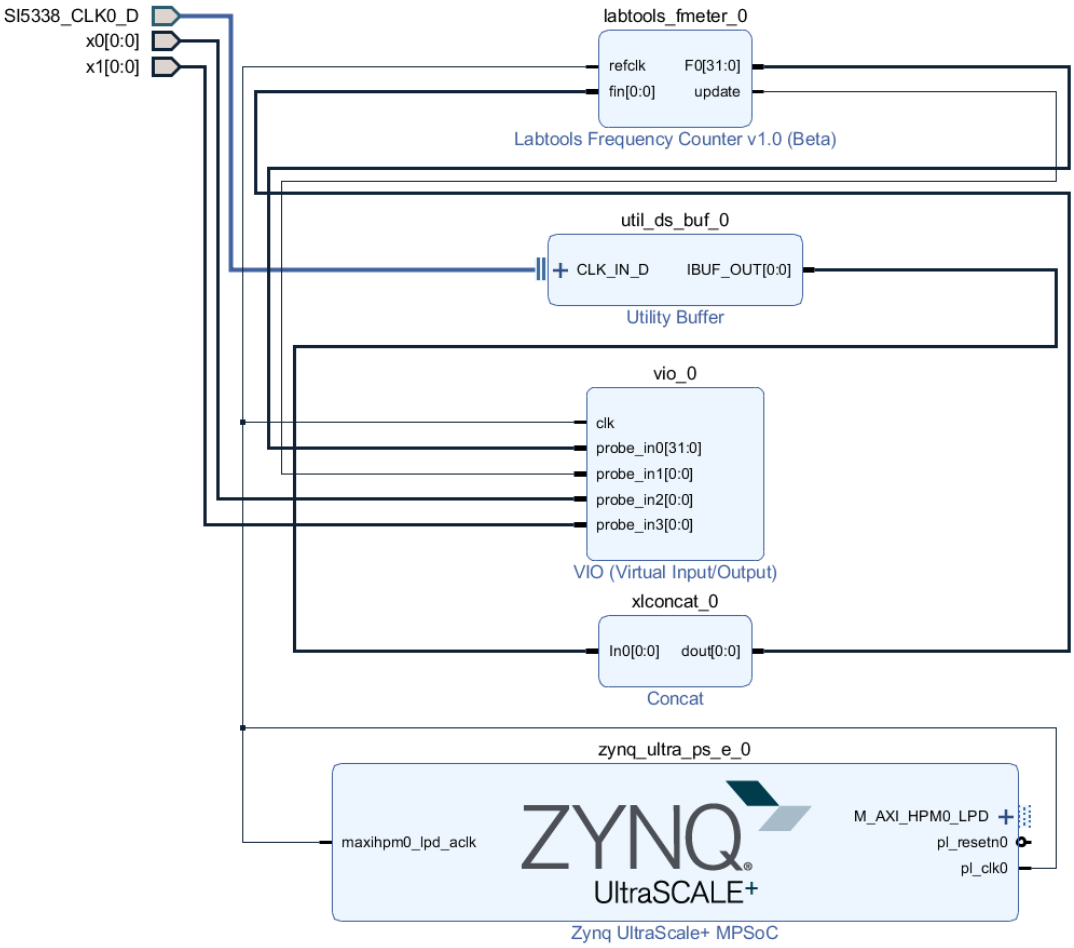

Figure 4: Block Design PCB REV01 REV02

7.1.3 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
I2C0	MIO
UART0	MIO

Type	Note
GPIO0	MIO
SWDT0..1	
TTC0..3	
GEM3	MIO
USB0	MIO, USB2 only

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen_common.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design
```

7.2.2 Design specific constrain

_i_io.xdc

```
set_property PACKAGE_PIN K9 [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property IOSTANDARD LVDS [get_ports {SI5338_CLK0_D_clk_p[0]}]
set_property DIFF_TERM TRUE [get_ports {SI5338_CLK0_D_clk_p[0]}]

set_property PACKAGE_PIN H1 [get_ports {x0[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x0[0]}]
set_property PACKAGE_PIN J1 [get_ports {x1[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {x1[0]}]
```

8 Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis[22]

8.1 Application

Template location: "<project folder>\sw_lib\sw_apps\"

8.1.1 zynqmp_fsbl

TE modified 2020.2 FSBL

General:

- Modified Files: xfsbl_main.c, xfsbl_hooks.h/.c, xfsbl_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te_xfsbl_hooks.h/.c (for hooks and board)
- General Changes:
    - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te_*
    - Si5338 Configuration
    - ETH+OTG Reset over MIO

8.1.2 zynqmp_fsbl_flash

TE modified 2020.2 FSBL

General:

- Modified Files: xfsbl_initialisation.c, xfsbl_hw.h, xfsbl_handoff.c, xfsbl_main.c
- General Changes:
    - Display FSBL Banner
    - Set FSBL Boot Mode to JTAG
    - Disable Memory initialisation

8.1.3 zynqmp_pmufw

Xilinx default PMU firmware.

8.1.4 hello_te0820

Hello TE0820 is a Xilinx Hello World example as endless loop instead of one console output.

8.1.5 u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

22 https://wiki.trenz-electronic.de/display/PD/Vitis

9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart[23]

9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- CONFIG_SUBSYSTEM_PRIMARY_SD_PSU_SD_1_SELECT=y
- CONFIG_SUBSYSTEM_ETHERNET_PSU_ETHERNET_3_MAC=""

9.2 U-Boot

Start with **petalinux-config -c u-boot**
Changes:

- CONFIG_I2C_EEPROM=y
- CONFIG_ZYNQ_GEM_I2C_MAC_OFFSET=0xFA
- CONFIG_SYS_I2C_EEPROM_ADDR=0x50
- CONFIG_SYS_I2C_EEPROM_BUS=0
- CONFIG_SYS_EEPROM_SIZE=256
- CONFIG_SYS_EEPROM_PAGE_WRITE_BITS=0
- CONFIG_SYS_EEPROM_PAGE_WRITE_DELAY_MS=0
- CONFIG_SYS_I2C_EEPROM_ADDR_LEN=1
- CONFIG_SYS_I2C_EEPROM_ADDR_OVERFLOW=0
- CONFIG_SD_BOOT=y

Change platform-top.h:

9.3 Device Tree

```
/include/ "system-conf.dtsi"
/ {
  chosen {
    xlnx,eeprom = &eeprom;
  };
};
/*emmc*/
&sdhci0 {
    // disable-wp;
    no-1-8-v;

};
/* SDIO */
```

23 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart

```
&sdhci1 {
   disable-wp;
   no-1-8-v;
};

/* ETH PHY */
&gem3 {

    status = "okay";
  ethernet_phy0: ethernet-phy@0 {
        compatible = "marvell,88e1510";
        device_type = "ethernet-phy";
            reg = <1>;
    };
};
/* USB 2.0 */

/* USB  */
&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    maximum-speed = "high-speed";
    /delete-property/phy-names;
    /delete-property/phys;
    /delete-property/snps,usb3_lpm_capable;
     snps,dis_u2_susphy_quirk;
    snps,dis_u3_susphy_quirk;
};

&usb0 {
    status = "okay";
    /delete-property/ clocks;
    /delete-property/ clock-names;
    clocks = <0x3 0x20>;
    clock-names = "bus_clk";
};




/* QSPI PHY */
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

&i2c0 {
  eeprom: eeprom@50 {
     compatible = "atmel,24c08";
```

```
      reg = <0x50>;
  };
};
```

9.4 Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_CPU_IDLE is not set (only needed to fix JTAG Debug issue)
- CONFIG_CPU_FREQ is not set (only needed to fix JTAG Debug issue)
- CONFIG_EDAC_CORTEX_ARM64=y

9.5 Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- CONFIG_i2c-tools=y
- CONFIG_busybox-httpd=y (for web server app)
- CONFIG_packagegroup-petalinux-utils(util-linux,cpufrequtils,bridge-utils,mtd-utils,usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)

9.6 Applications

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps\"

9.6.1 startup

Script App to load init.sh from SD Card if available.

9.6.2 webfwu

Webserver application suitable for Zynq access. Need busybox-httpd

10 Additional Software

10.1 SI5338

File location "<project folder>\misc\Si5338\Si5338-*.slabtimeproj"

General documentation how you work with these project will be available on Si5338[24]

24 https://wiki.trenz-electronic.de/display/PD/Si5338

11 Appx. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2021-06-09	v.65(see page 6)	@ Manuela Strücker[25]	• document style update
2021-06-01	v.64	John Hartfiel	• 2020.2 update • new assembly variants • document style update
2020-05-07	v.62	John Hartfiel	• update programming section
2020-04-08	v.61	John Hartfiel	• script update • new assembly variants
2020-03-25	v.60	John Hartfiel	• script update
2020-01-21	v.59	John Hartfiel	• Script update for linux user
2020-01-14	v.58	John Hartfiel	• Script update, new features • doc update • add missing binary files
2019-12-19	v.57	John Hartfiel	• 2019.2 release
2019-10-29	v.56	John Hartfiel	• new assembly variants
2019-08-09	v.55	John Hartfiel	• bugfix fsbl
2019-06-19	v.54	John Hartfiel	• design changes

25 https://wiki.trenz-electronic.de/display/~m.struecker

Date	Document Revision	Authors	Description
			• new variants
2019-04-01	v.53	John Hartfiel	• some notes • renamed ..D variants to ...A
2018-09-21	v.47	John Hartfiel	• 2018.3 release finished (include design reworks)
2018-10-31	v.43	John Hartfiel	• Update Design files for 2GB variants • rebuilt petalinux for optional init script
2018-09-12	v.41	John Hartfiel	• Update Design files for 2GB variants
2018-07-11	v.40	John Hartfiel	• add notes to ES1
2018-07-06	v.38	John Hartfiel	• 2018.2 release finished
2018-06-19	v.34	John Hartfiel	• Design Files Update
2018-02-13	v.29	John Hartfiel	• Design Files Update
2018-02-06	v.27	John Hartfiel	• Design Files Update
2018-01-29	v.26	John Hartfiel	• Update Known Issues
2018-01-24	v.25	John Hartfiel	• Release 2017.4
2018-01-10	v.24	John Hartfiel	• Update Known Issues
2017-12-20	v.23	John Hartfiel	• Typo correction • Update HW Module Table Description
2017-11-21	v.19	John Hartfiel	• Design Update
2017-11-20	v.18	John Hartfiel	• Design Update

Date	Document Revision	Authors	Description
			• Add Variants with 128MB Flash
2017-11-13	v.16	John Hartfiel	• Update Carrier sections
2017-11-06	v.15	John Hartfiel	• Typo corrected
2017-10-23	v.13	John Hartfiel	• Update Key Features section • Style Update Additional Software section
2017-10-19	v.9	John Hartfiel	• Release 2017.2
2017-09-11	v.1	@ John Hartfiel[26]	Initial release
	All	@ John Hartfiel[27], Manuela Strücker[28]	

Table 10: Document change history.

11.2 Legal Notices

11.3 Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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26 https://wiki.trenz-electronic.de/display/~j.hartfiel
27 https://wiki.trenz-electronic.de/display/~j.hartfiel
28 https://wiki.trenz-electronic.de/display/~m.struecker

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RoHS

29 http://guidance.echa.europa.eu/
30 https://echa.europa.eu/candidate-list-table
31 http://www.echa.europa.eu/

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2019-06-07