


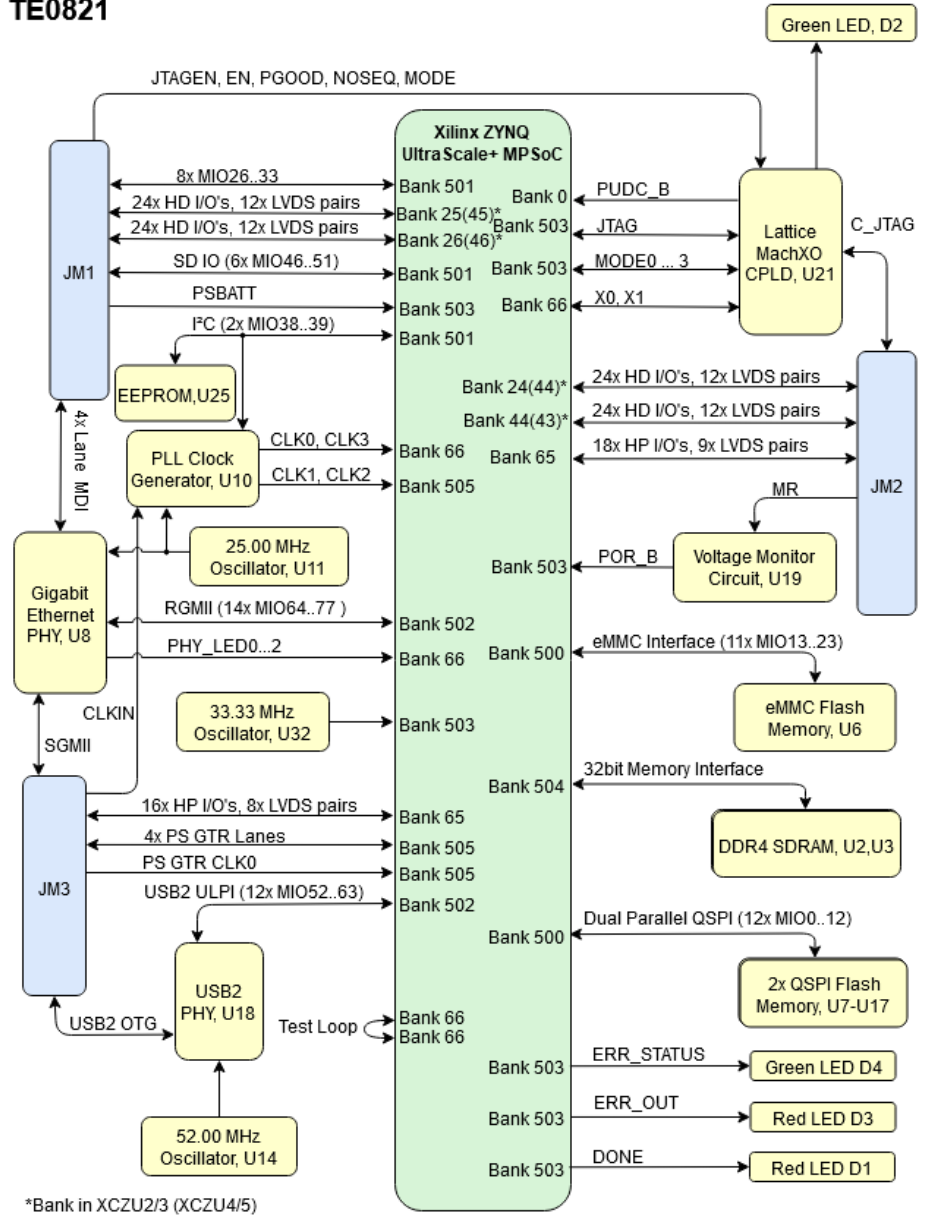
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Schematics and other handouts serve for informational purposes only!

	Title: Module TE0821		
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	Date: 14.08.2020	Copyright: Trenz Electronic GmbH / TT	Page 1 of 24
	Filename: Legal Notices Modules.SchDoc		

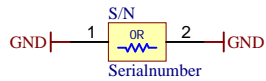
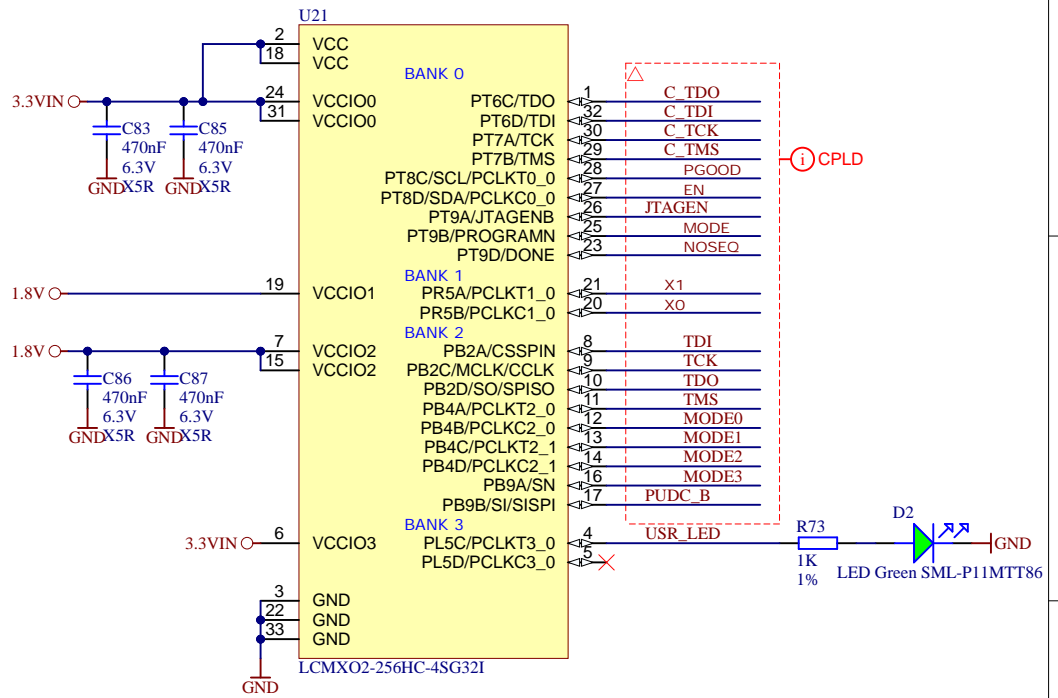
TE0821



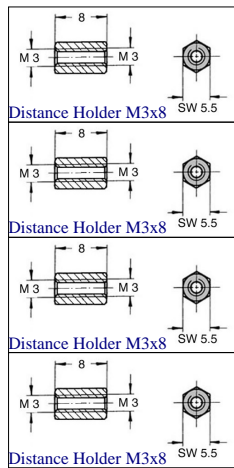
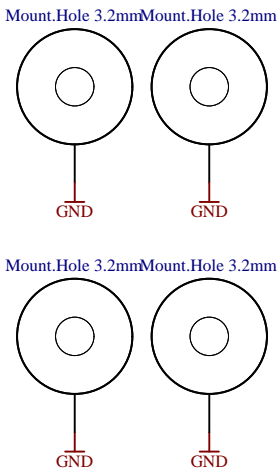
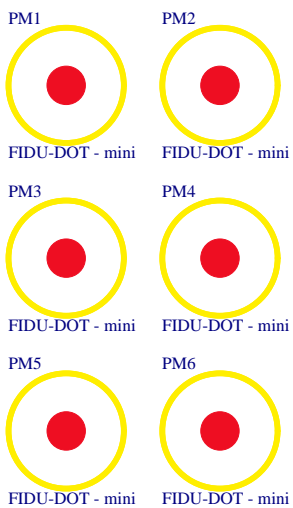
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		A4	Number: TE0821 2AE21FA Rev. 01
Date: 18.01.2022		Copyright: 2015 Trenz Electronic GmbH	
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Filename: TE0821-Overview.SchDoc			

U_USB-PHY USB-PHY.SchDoc
U_ETH-PHY ETH-PHY.SchDoc
U_B_HD B_HD.SchDoc
U_B64 B64.SchDoc
U_B65 B65.SchDoc
U_B66 B66.SchDoc
U_CONFIG CONFIG.SchDoc
U_B_MIO B_MIO.SchDoc
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U_CLK CLK.SchDoc
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U_PS_DDR PS_DDR.SchDoc
U_ZU_POWER ZU_POWER.SchDoc
U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_DDR4-RAM_2 DDR4-RAM_2.SchDoc
U_DDR4-RAM DDR4-RAM.SchDoc
U_POWER POWER.SchDoc
U_POWER_1 POWER_1.SchDoc
U_Revision_changes Revision Changes.SchDoc



Serial
Serialnumber 6,3 x 6,3mm

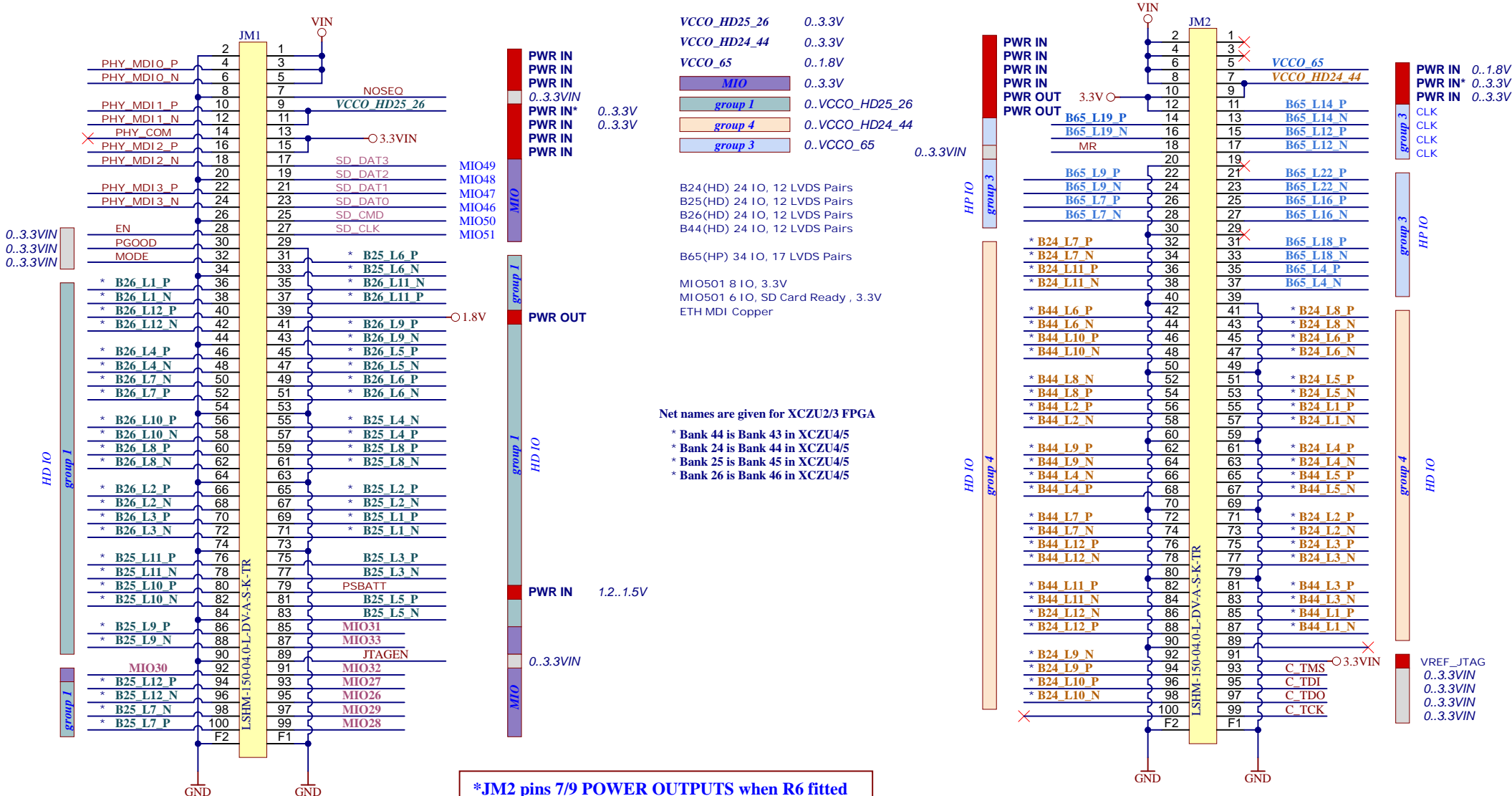


Special notes:

Component RC0201FR-0710KL removed



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***JM2 pins 7/9 POWER OUTPUTS when R6 fitted**

VCCO_HD24_44 ~~R6~~ 0.3.3V
OR
1%

***JM1 pins 9/11 POWER OUTPUTS when R89 fitted**

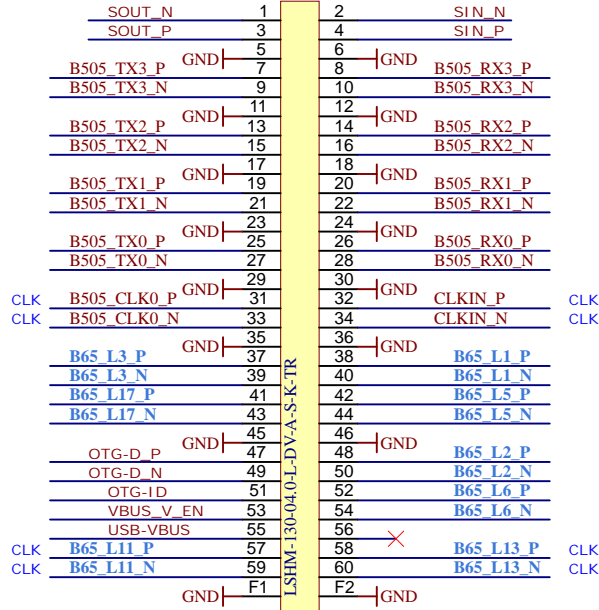
VCCO_HD25_26 ~~R89~~ 0.3.3V
OR
1%



Title: Module TE0821 - B2B Connectors		
A4	Number: TE0821 2AE21FA	Rev. 01
Date: 04.07.2019	Copyright: 2015 Trenz Electronic GmbH	Page 4 of 24
Filename: B2B-Connectors.SchDoc		

USB OTG
 ETH SGMII
 PS_GTR 4 Lanes
 PS_GTR CLK IN
 PLL CLK IN

JM3



HP IO
 group 3
 USB
 HP IO

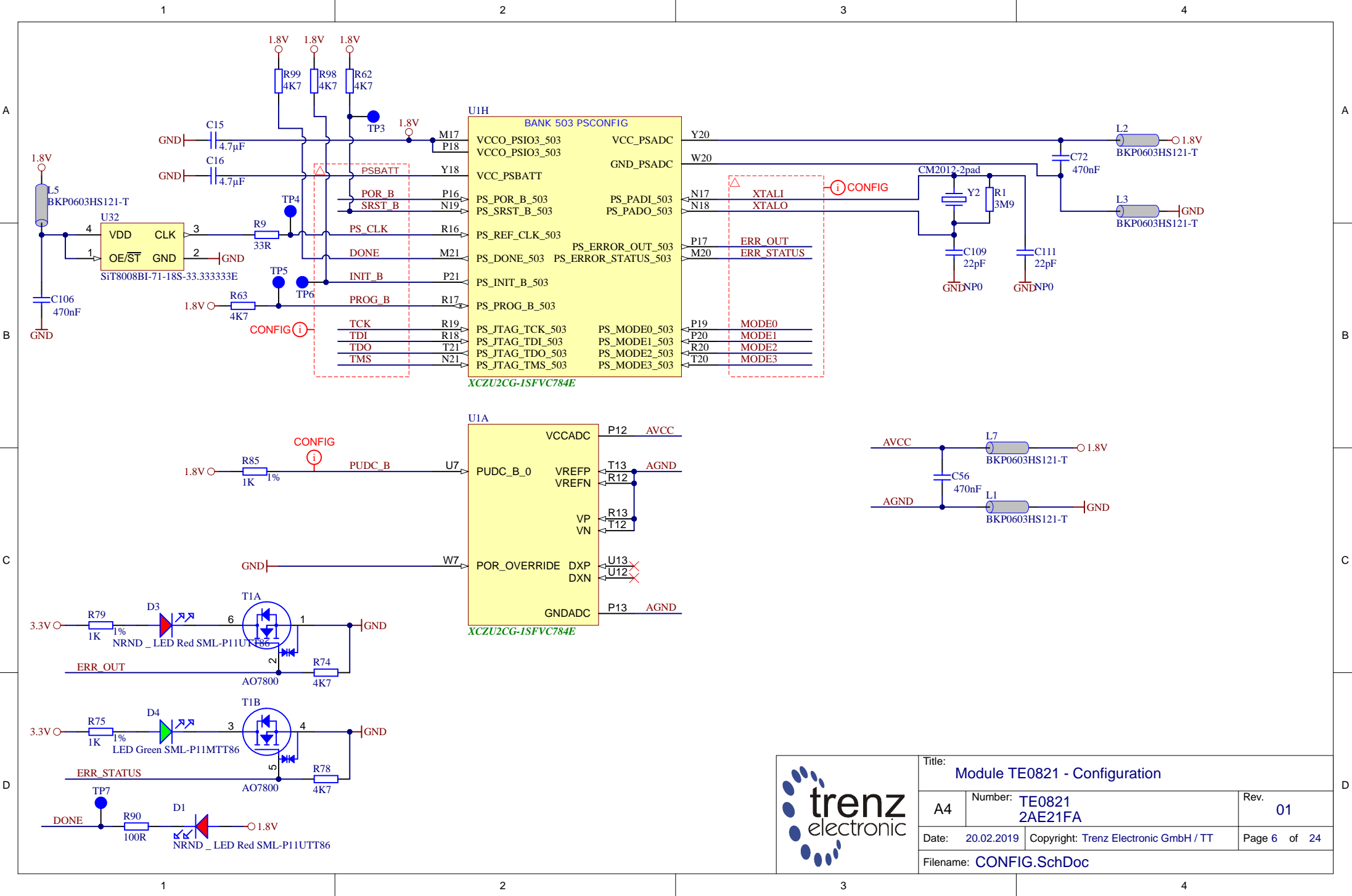
group 3
 group 3
 group 3

X

X

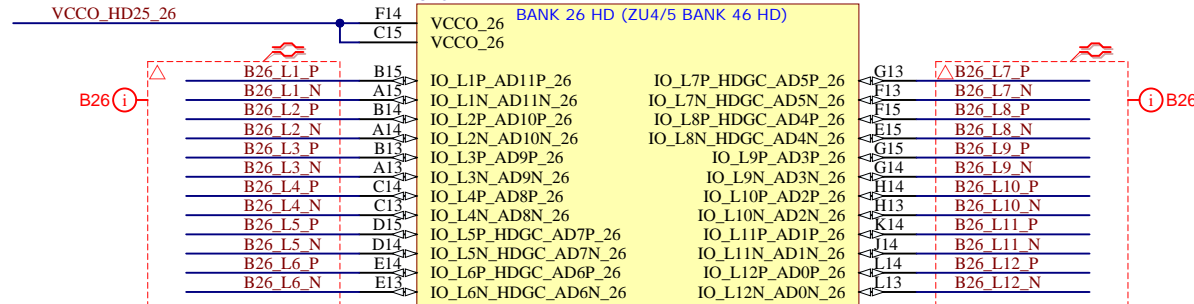


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Date: 20.02.2019	Copyright: 2015 Trenz Electronic GmbH	Page 5 of 24
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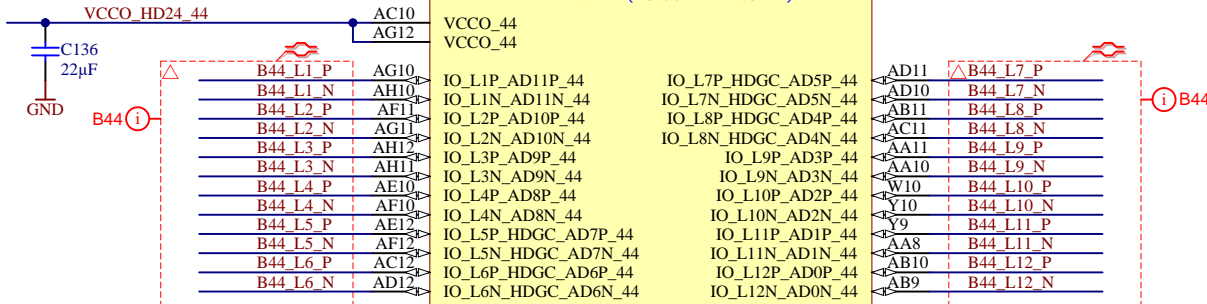


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Date: 20.02.2019	Copyright: Trenz Electronic GmbH / TT	Page 6 of 24
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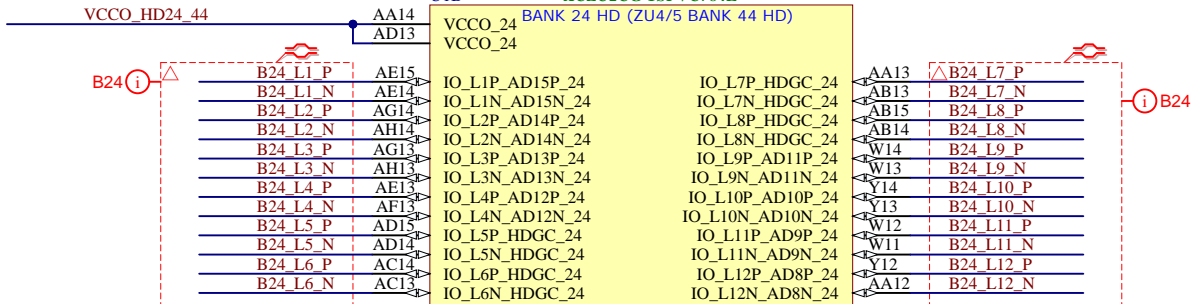
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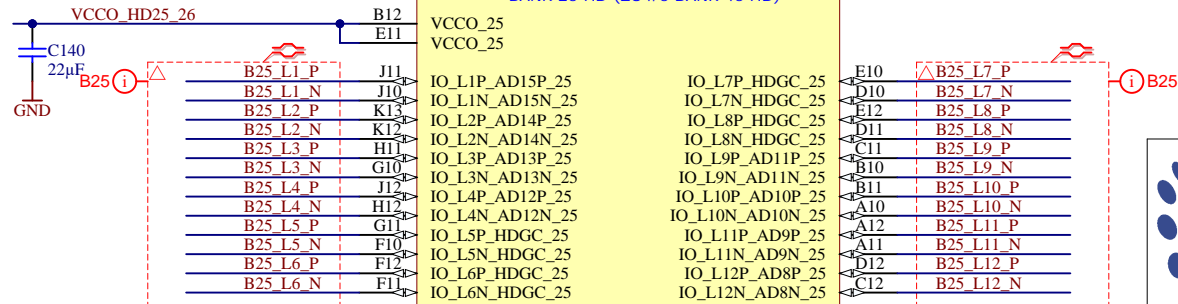
BANK 44 HD (ZU4/5 BANK 43 HD)



UIB XCZU2CG-1SFVC784E



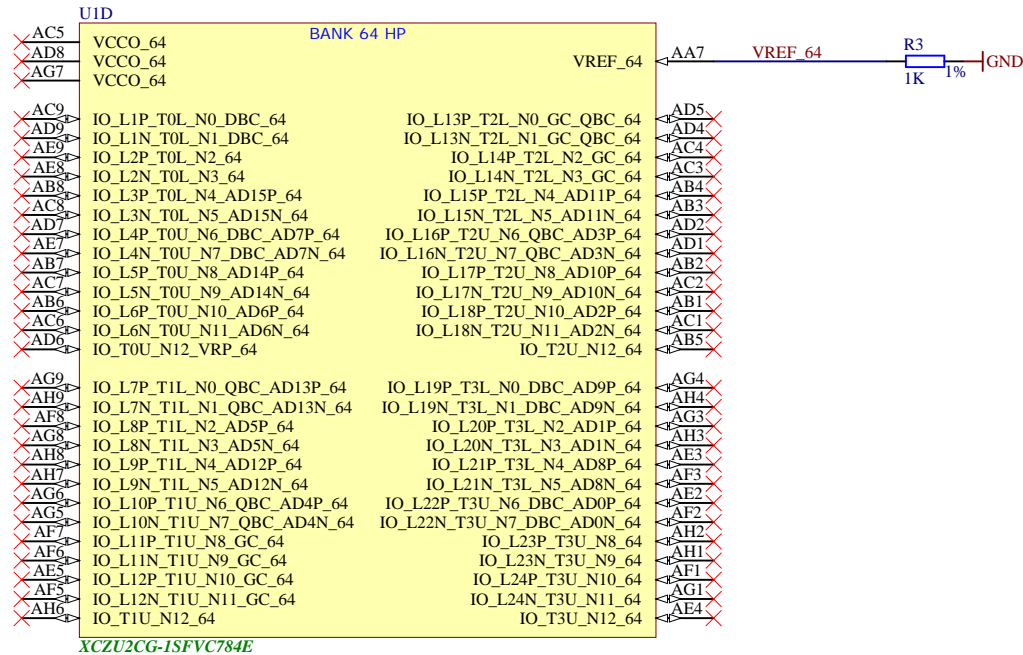

BANK 25 HD (ZU4/5 BANK 45 HD)



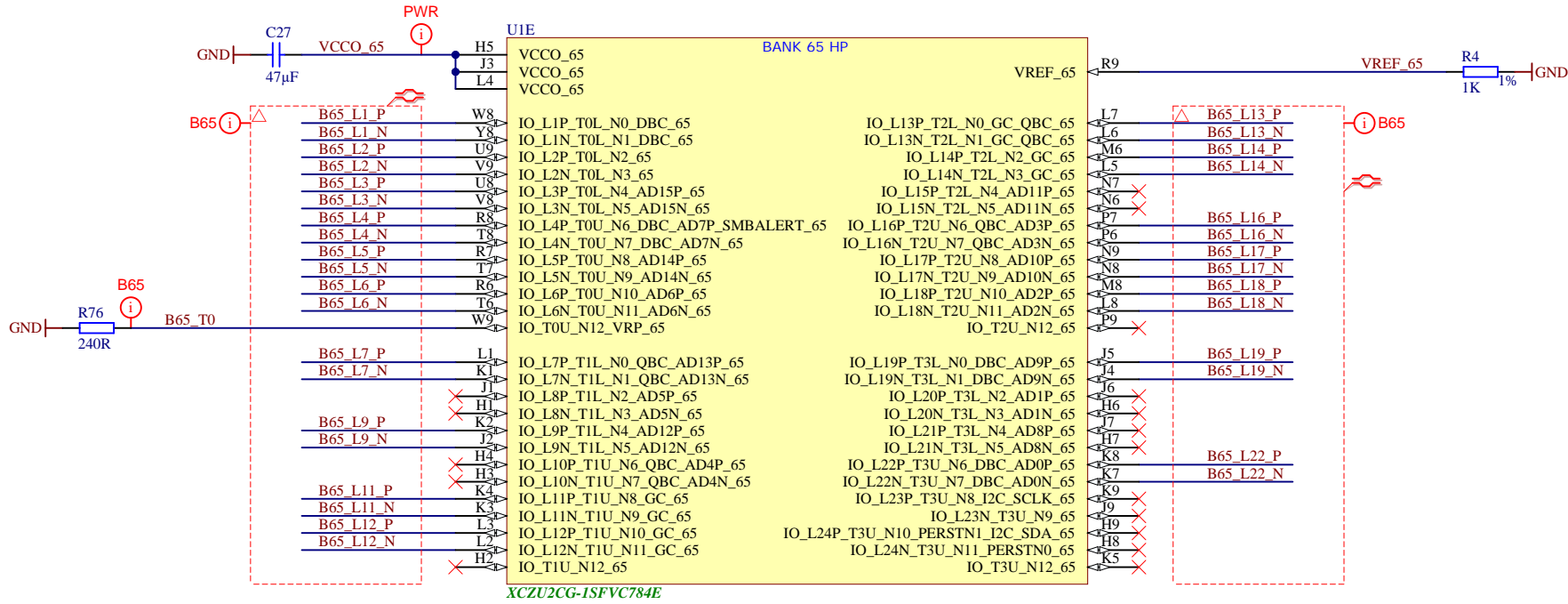
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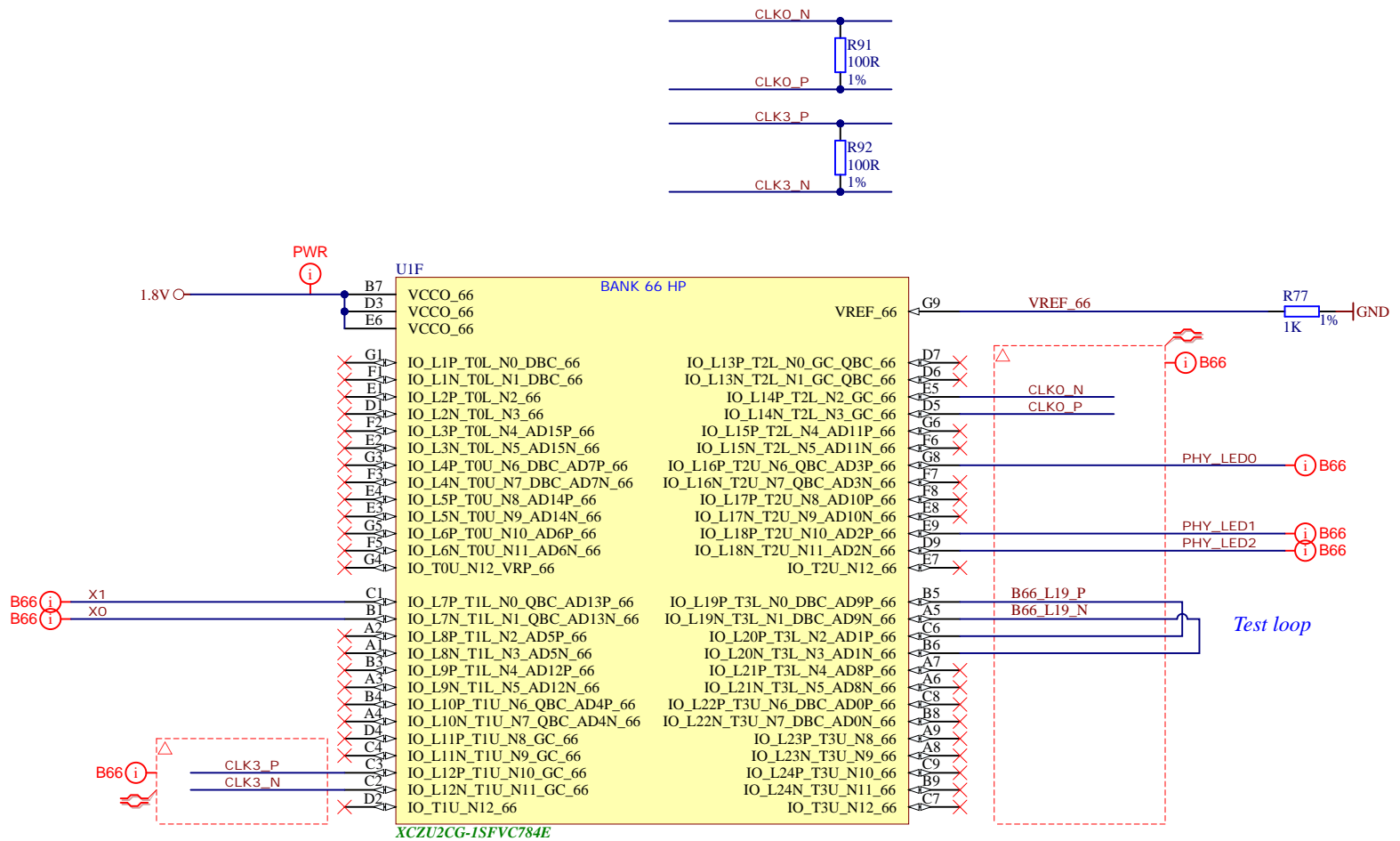
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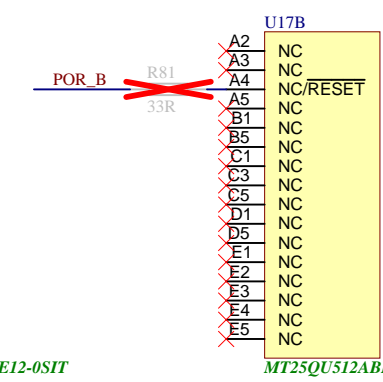
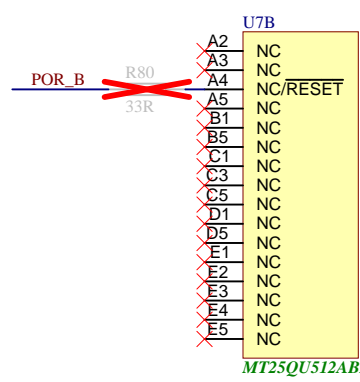
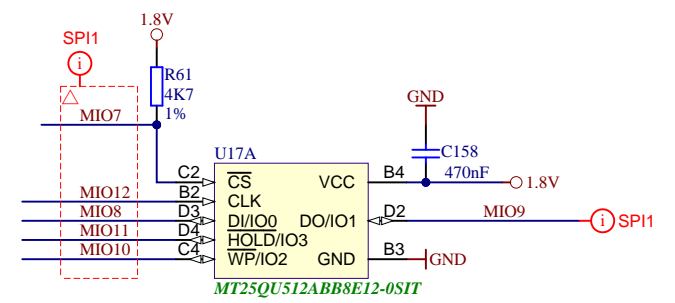
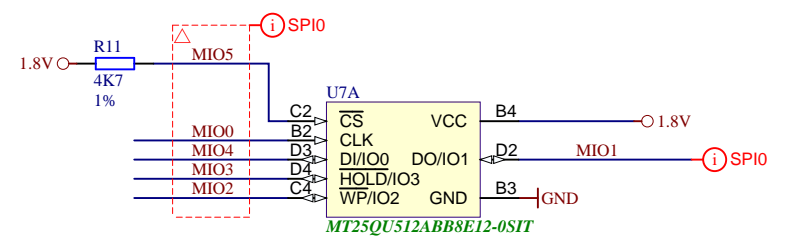
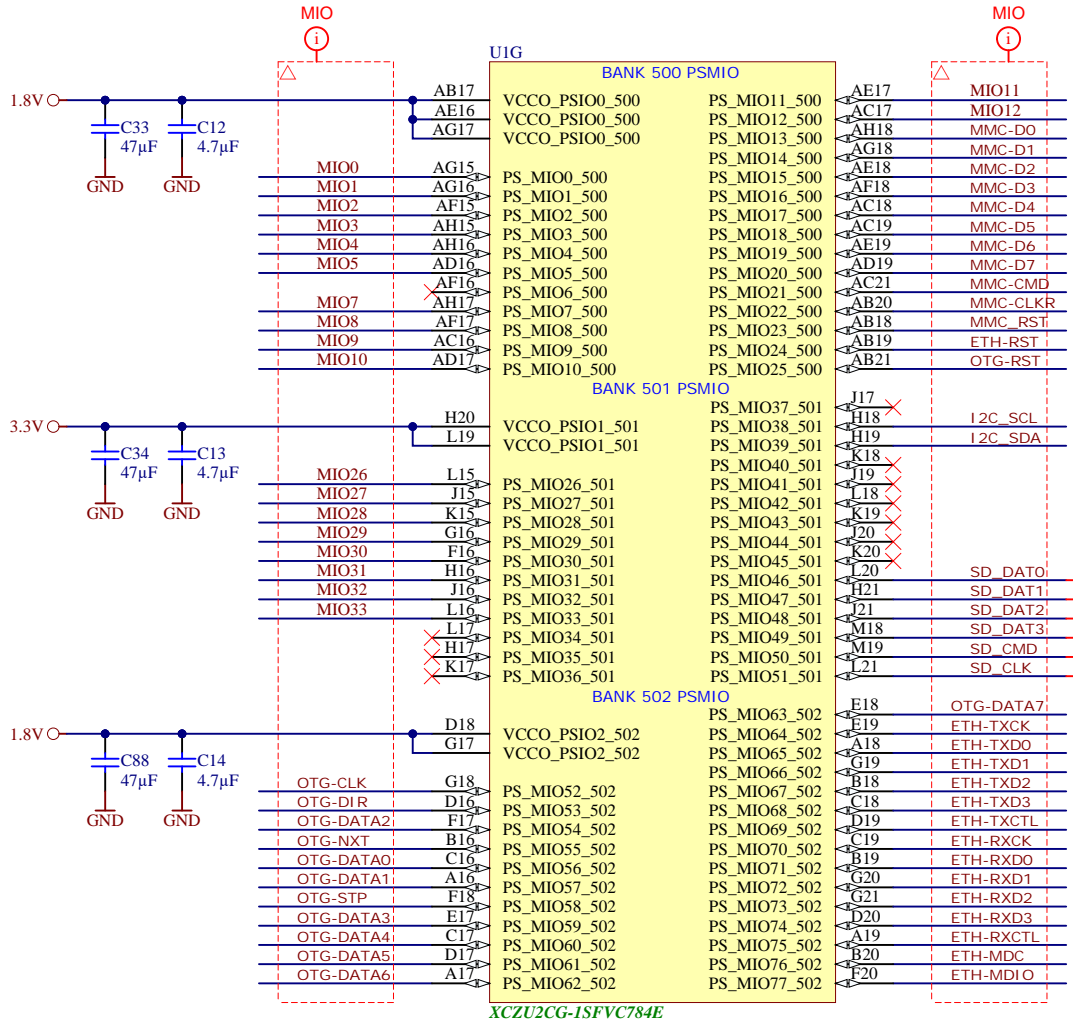
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Title: Module TE0821 - B65		
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Filename: B66.SchDoc		



			Title: Module TE0821 - MIO Banks	
			A4	Number: TE0821 2AE21FA
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Filename: B_MIO.SchDoc				

A

B

C

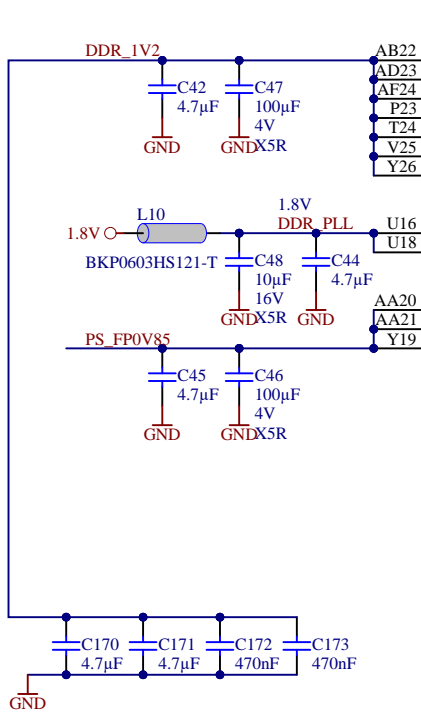
D

A

B

C

D



U1I

BANK 504 PSDDR

VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0 P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0 N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
	PS_DDR_A3_504	AA28	DDR4-A3
	PS_DDR_A4_504	Y27	DDR4-A4
	PS_DDR_A5_504	AA27	DDR4-A5
	PS_DDR_A6_504	Y22	DDR4-A6
	PS_DDR_A7_504	AA23	DDR4-A7
	PS_DDR_A8_504	AA22	DDR4-A8
	PS_DDR_A9_504	AB23	DDR4-A9
	PS_DDR_A10_504	AA25	DDR4-A10
	PS_DDR_A11_504	AA26	DDR4-A11
	PS_DDR_A12_504	AB25	DDR4-A12
	PS_DDR_A13_504	AB26	DDR4-A13
	PS_DDR_A14_504	AB24	DDR4-A14
	PS_DDR_A15_504	AC24	DDR4-A15
	PS_DDR_A16_504	AC23	DDR4-A16
	PS_DDR_A17_504	AC22	DDR4-A17
	PS_DDR_CS_N0_504	W27	DDR4-CS
	PS_DDR_CS_N1_504	V26	
	PS_DDR_BA0_504	V23	DDR4-BA0
	PS_DDR_BA1_504	W22	DDR4-BA1
	PS_DDR_BG0_504	W24	DDR4-BG0
	PS_DDR_BG1_504	V22	DDR4-BG1
	PS_DDR_PARITY_504	V24	DDR4-PAR
	PS_DDR_RAM_RST_N_504	U23	DDR4-RESET
	PS_DDR_ACT_N_504	Y23	DDR4-ACT
	PS_DDR_ALERT_N_504	U25	DDR4-ALERT
	PS_DDR_ZQ_504	U24	
	PS_DDR_ODT0_504	U28	DDR4-ODT0
	PS_DDR_ODT1_504	U26	

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U1J

BANK 504 PSDDR

DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504	T22
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504	R22
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504	P22
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504	N22
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504	T23
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504	P24
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	R24
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	N24
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504	H24
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504	J24
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504	M24
DQ11	AD23	PS_DDR_DQ11_504	PS_DDR_DQ43_504	K24
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504	J22
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504	H22
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504	K22
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504	J22
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504	M25
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504	M26
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504	L25
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504	L26
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504	K28
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504	L28
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504	M28
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504	N28
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504	J28
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504	K27
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504	H28
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504	H27
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504	G26
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504	G25
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504	K25
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504	J25
		PS_DDR_DQ64_504	PS_DDR_DQ64_504	T28
		PS_DDR_DQ65_504	PS_DDR_DQ65_504	R28
		PS_DDR_DQ66_504	PS_DDR_DQ66_504	P28
		PS_DDR_DQ67_504	PS_DDR_DQ67_504	P27
		PS_DDR_DQ68_504	PS_DDR_DQ68_504	P26
		PS_DDR_DQ69_504	PS_DDR_DQ69_504	R25
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		PS_DDR_DQ71_504	PS_DDR_DQ71_504	T25
		PS_DDR_DQ8_504	PS_DDR_DM0_504	AG20
		PS_DDR_DM0_504	PS_DDR_DM1_504	AE23
		PS_DDR_DM1_504	PS_DDR_DM2_504	AE25
		PS_DDR_DM2_504	PS_DDR_DM3_504	AE28
		PS_DDR_DM3_504	PS_DDR_DM4_504	R23
		PS_DDR_DM4_504	PS_DDR_DM5_504	H23
		PS_DDR_DM5_504	PS_DDR_DM6_504	L27
		PS_DDR_DM6_504	PS_DDR_DM7_504	H26
		PS_DDR_DM7_504	PS_DDR_DM8_504	T26

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Title: Module TE0821 - PS DDR		
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Filename: PS_DDR.SchDoc		

1

2

3

4

A

A

B

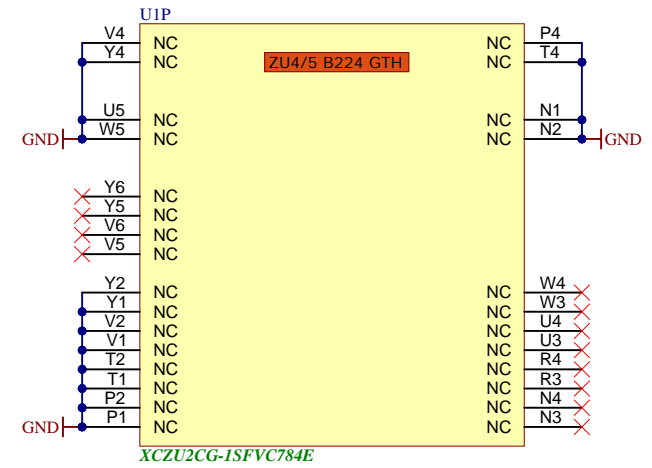
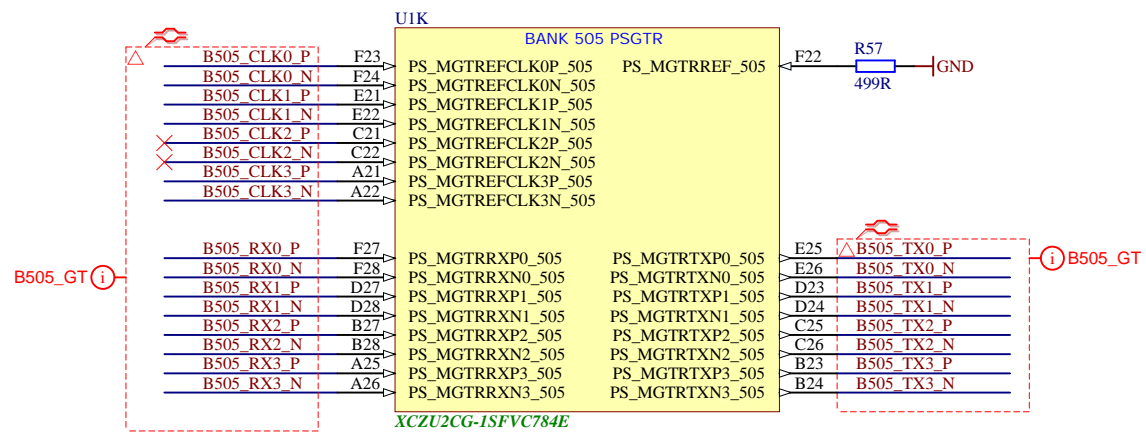

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C

C

D

D

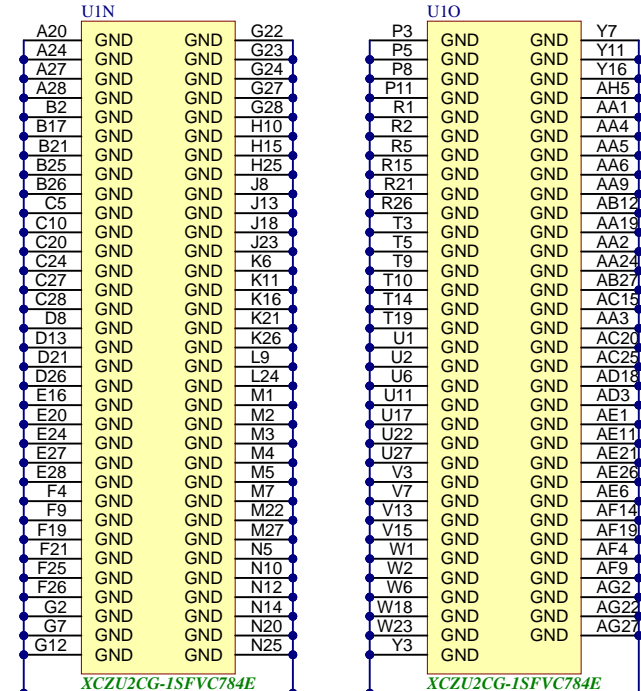
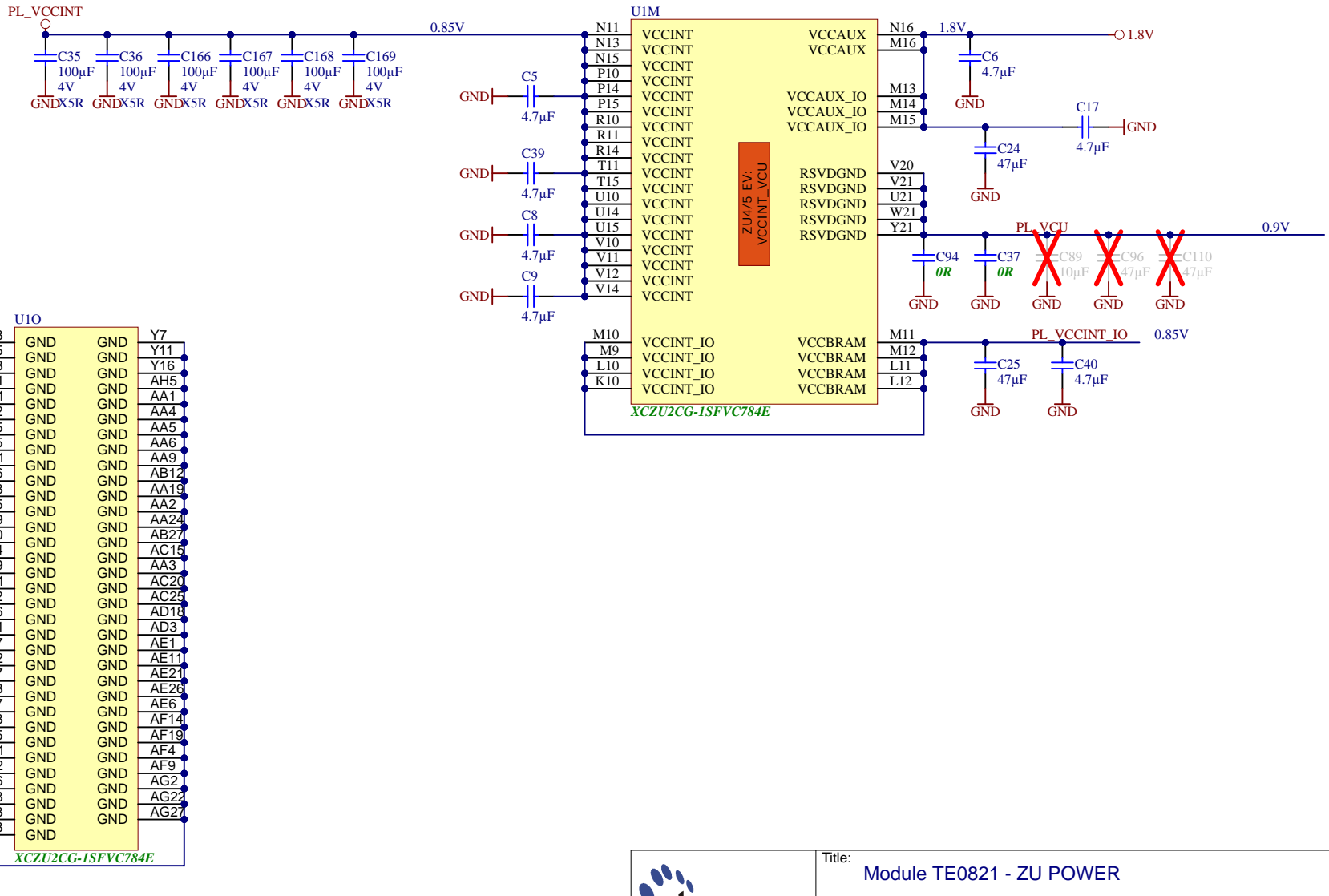
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Date: 20.02.2019	Copyright: Trenz Electronic GmbH / TT	Page 13 of 24
Filename: B_PS_GT.SchDoc		

1

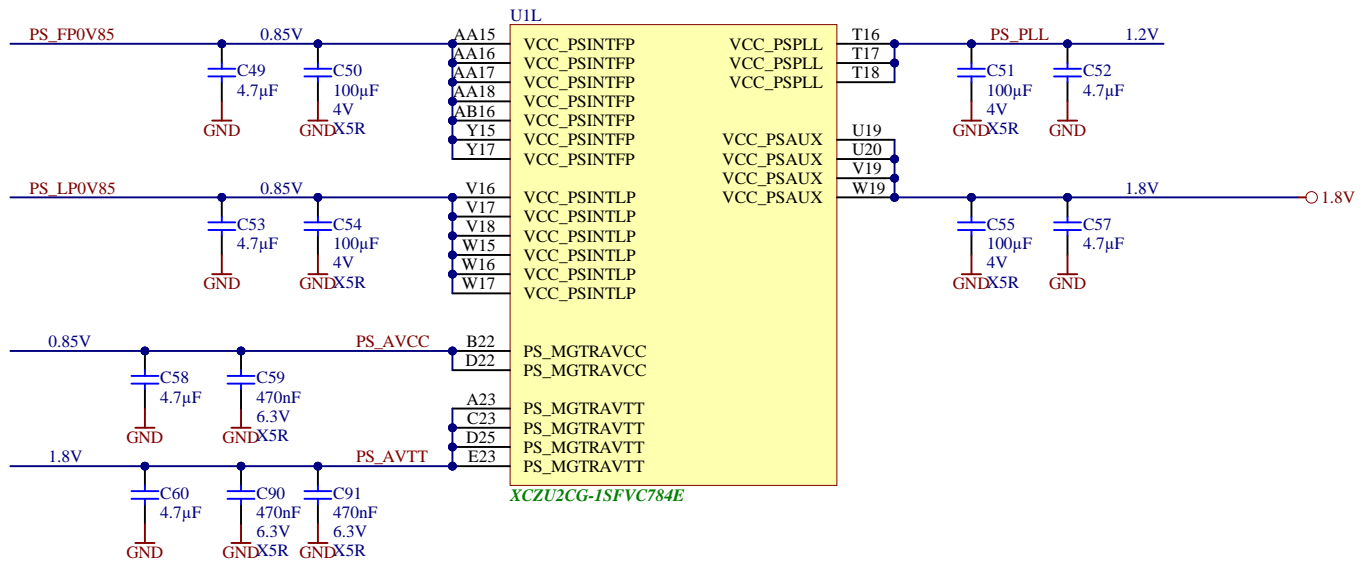
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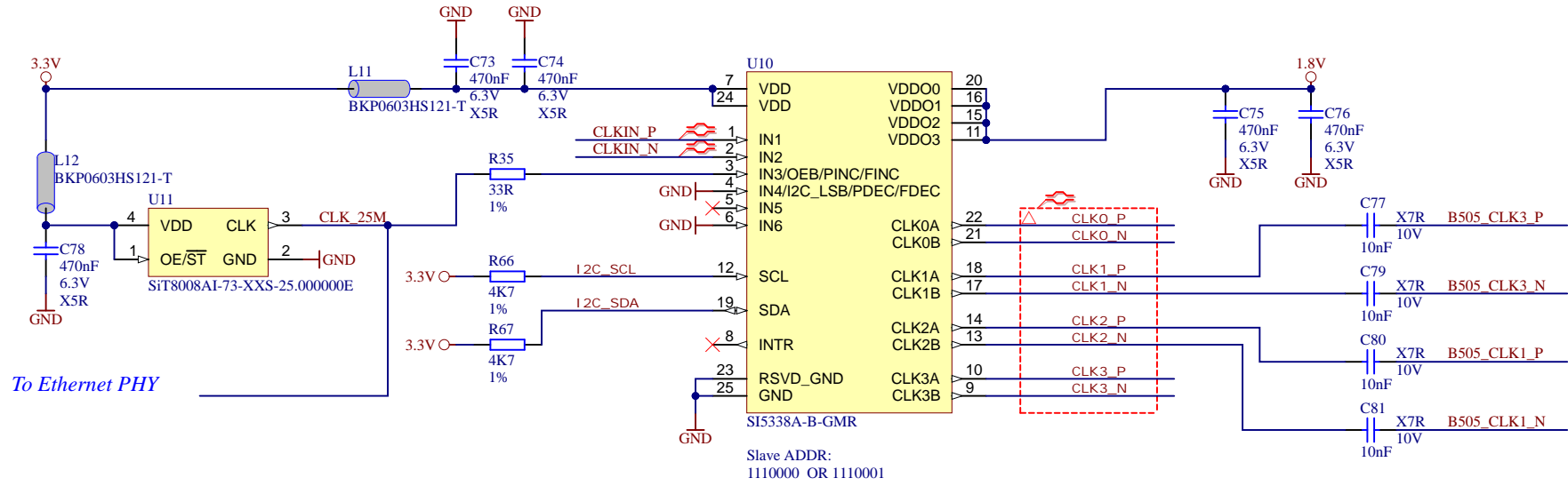
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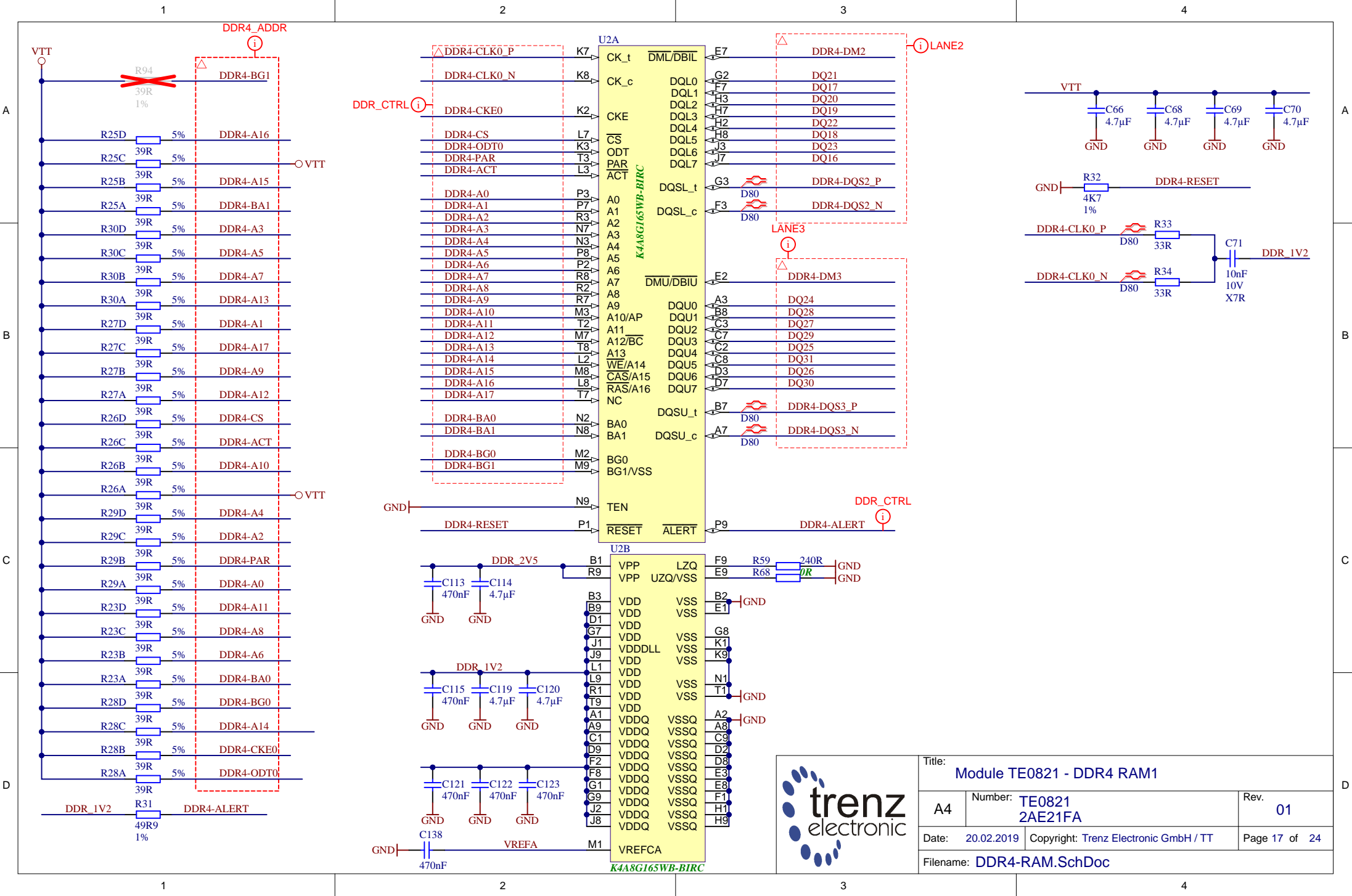
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Date: 20.02.2019	Copyright: Trenz Electronic GmbH / TT	
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Filename: ZU_POWER.SchDoc		



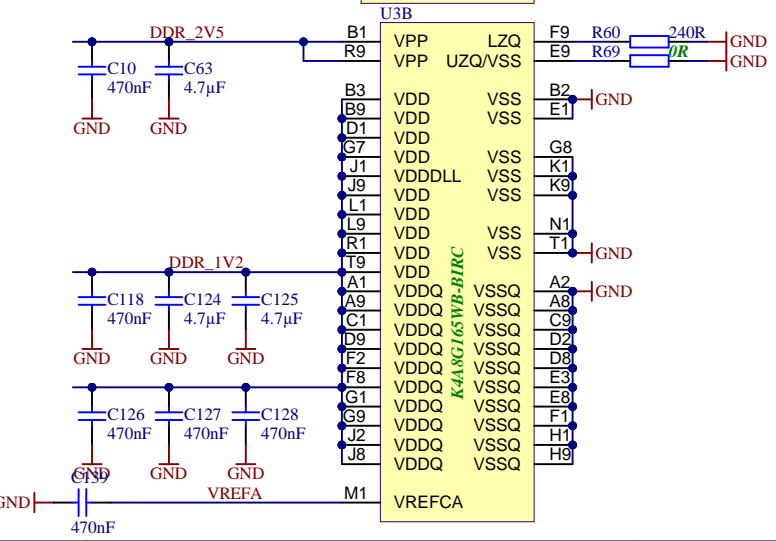
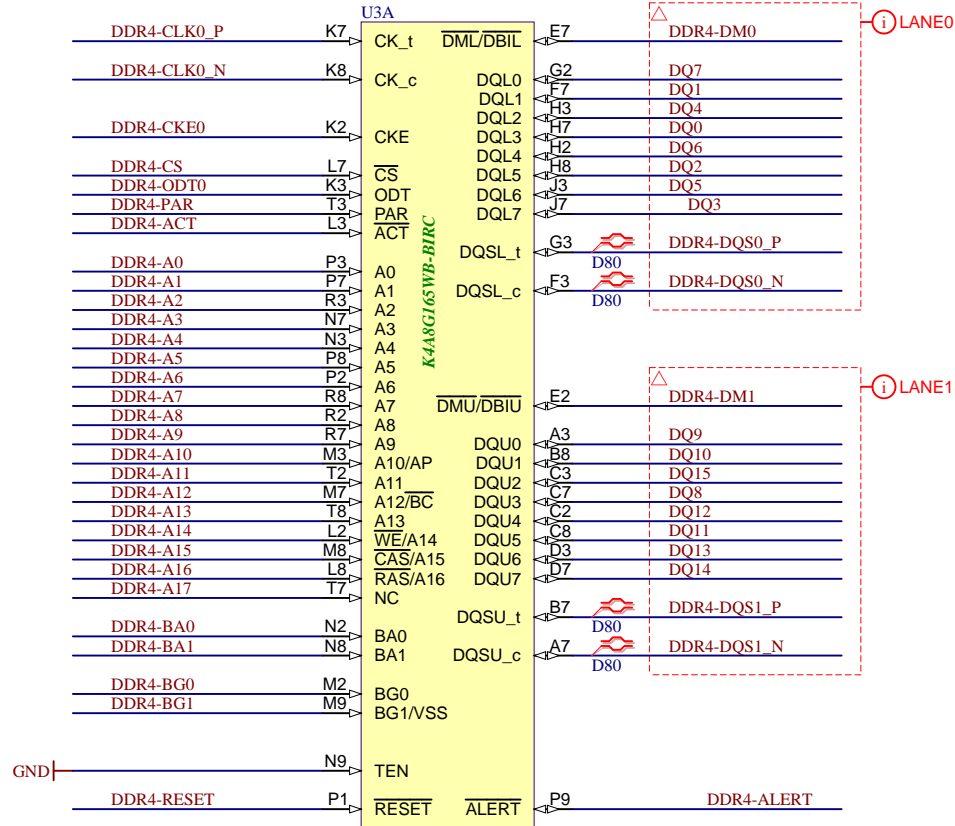
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	Date: 20.02.2019	Copyright: Trenz Electronic GmbH / TT	
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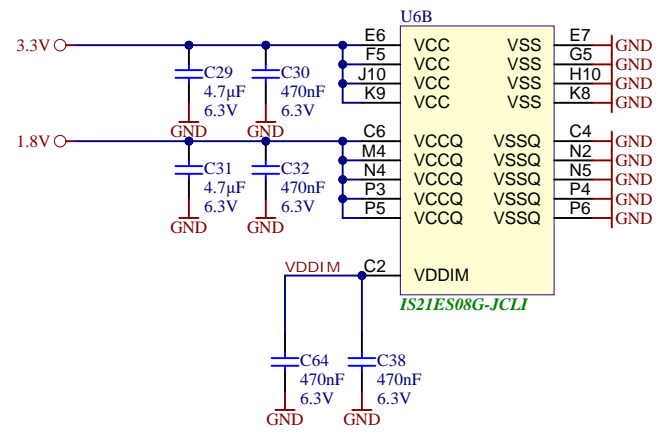
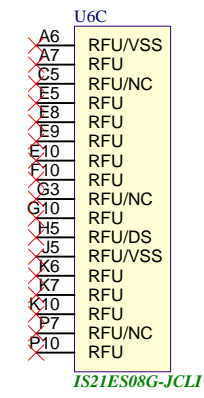
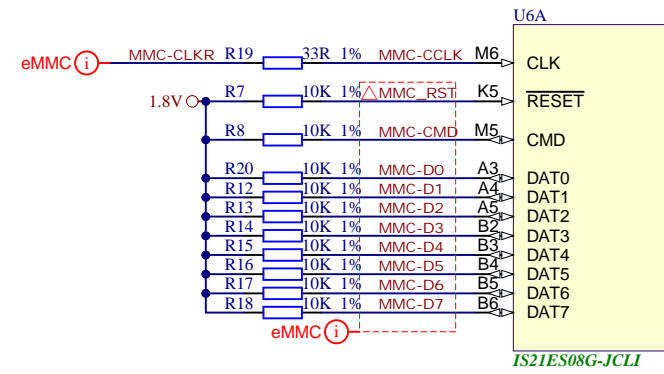
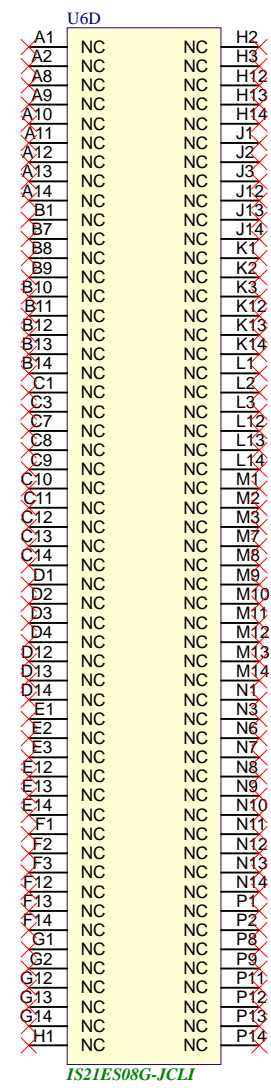

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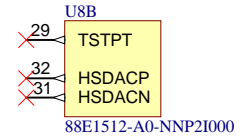
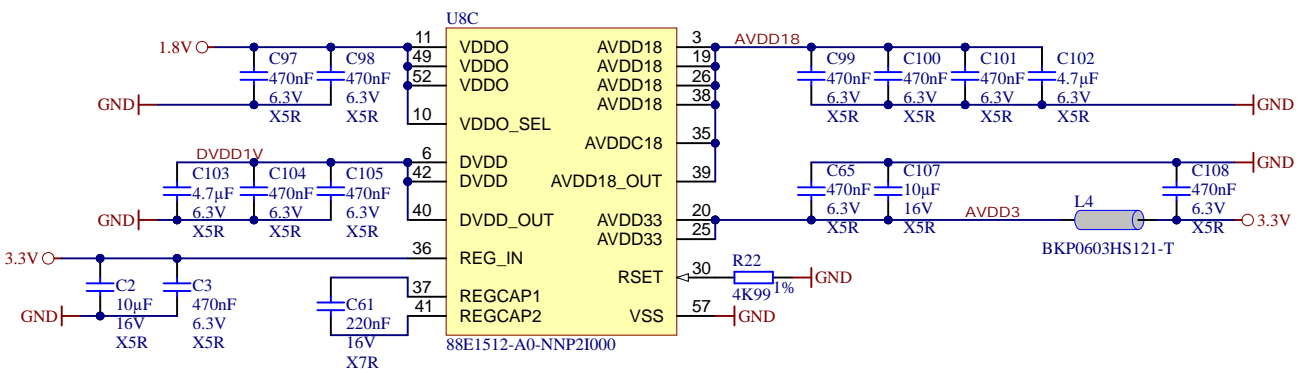
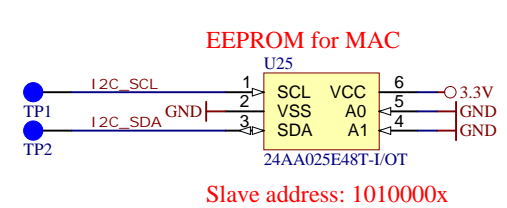
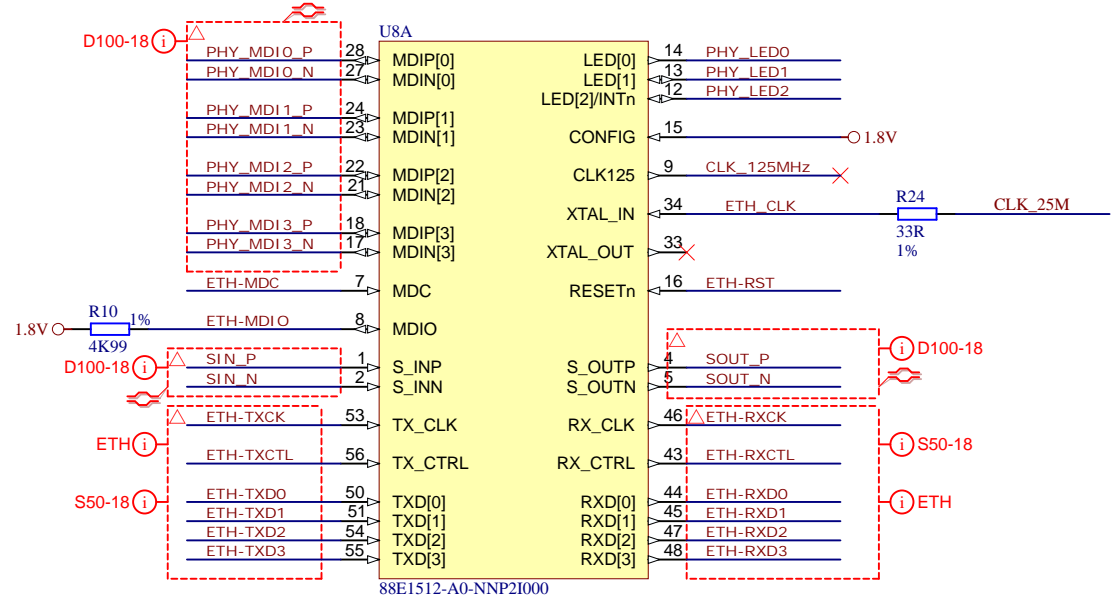
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Filename: DDR4-RAM.SchDoc		



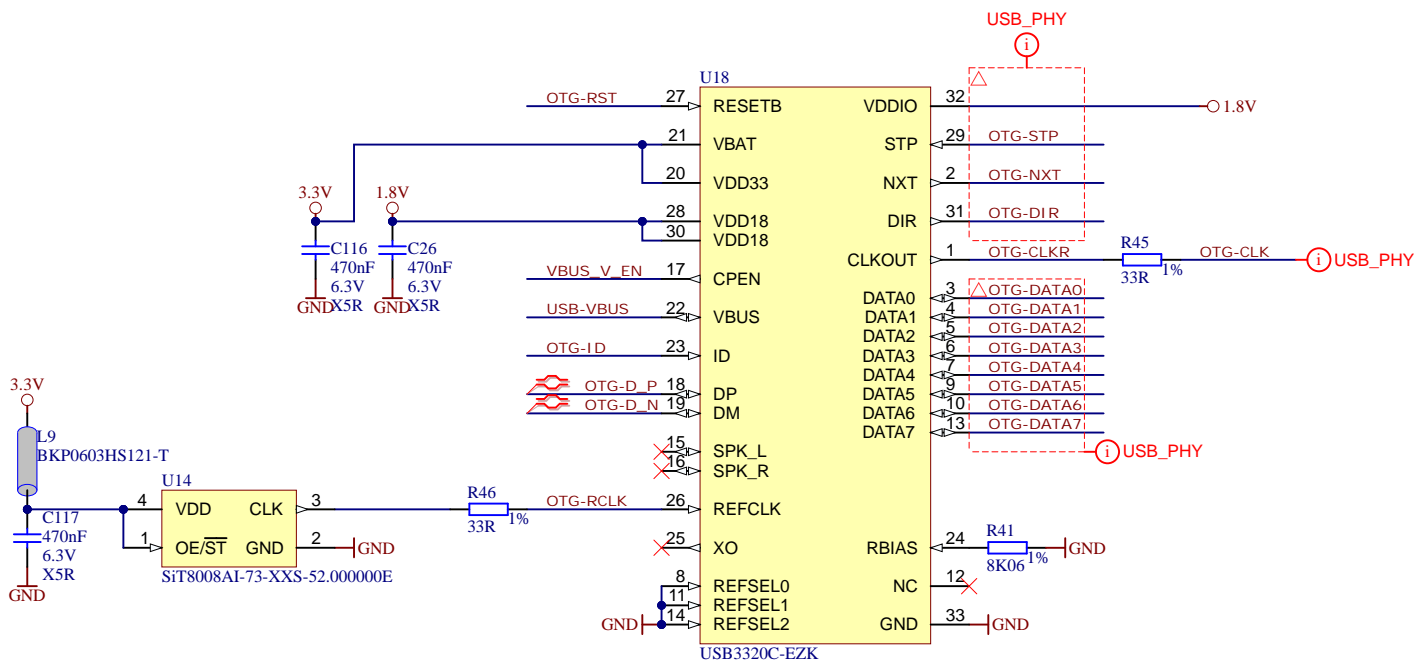
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Filename: DDR4-RAM_2.SchDoc		





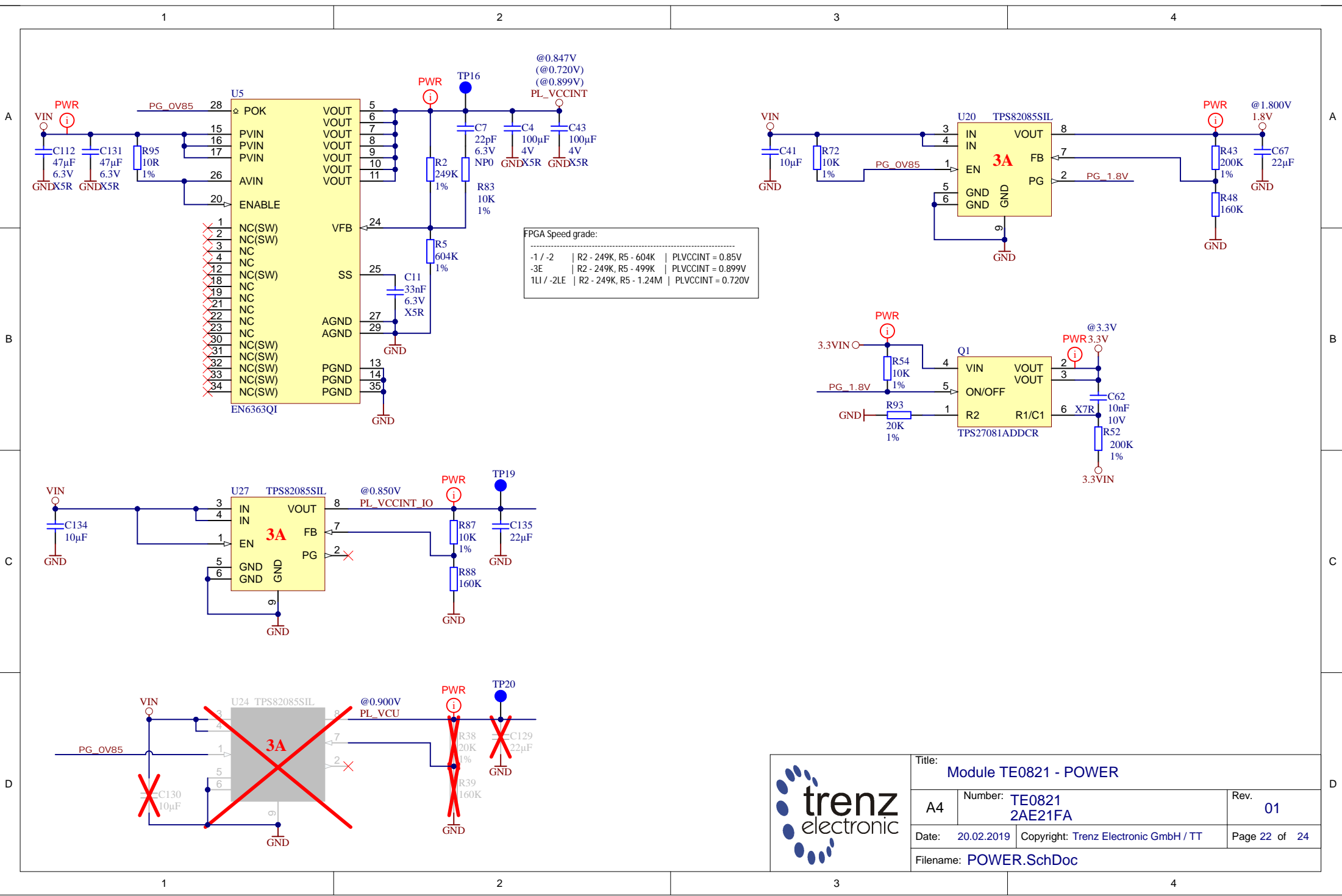

Title: Module TE0821 - eMMC		
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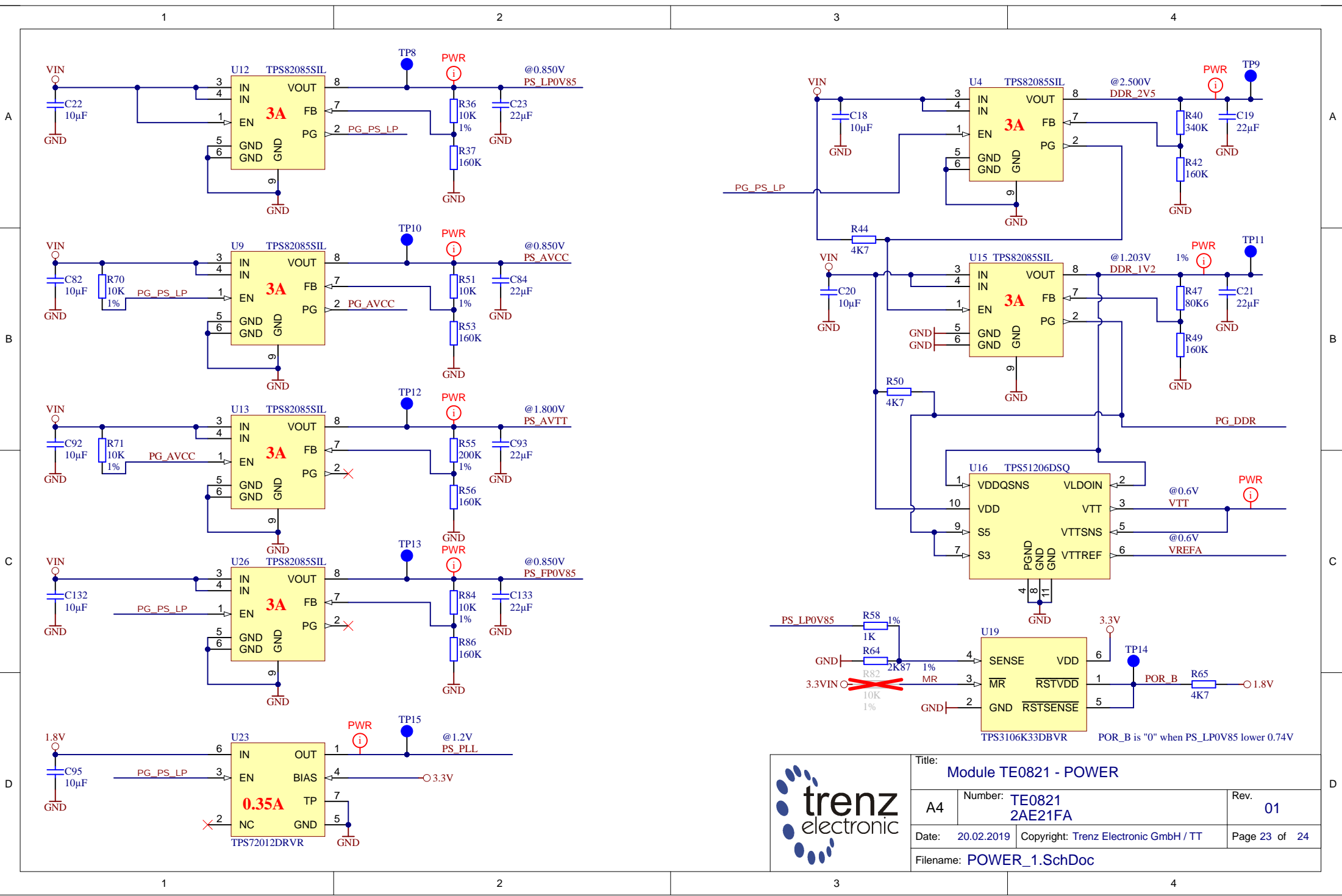
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Title: Module TE0821 - POWER		
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POR_B is "0" when PS_LP0V85 lower 0.74V

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Revision 01a (01.07.2020):

1. VY: R38 value was changed to 20K (was: 40K2) to set VCU 0.9V

Revision 01b (29.10.2020):

1. VY: Updated Block diagram

(07.02.2024):
2. OT: R82 set to not fitted

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B


B

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D

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