


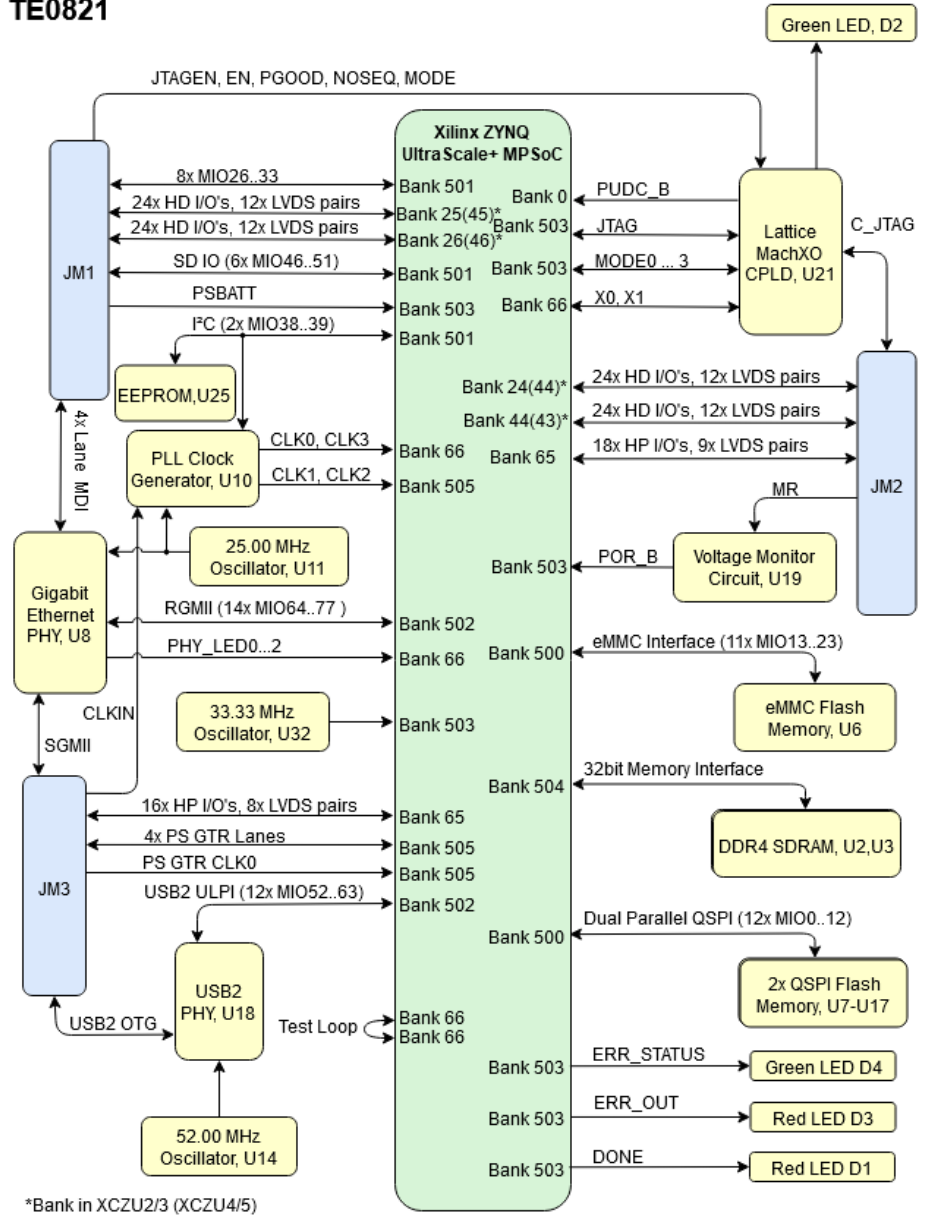
Regarding the usage of our schematics and alike documentation for Trenz module TE0821.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0821 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.


Schematics and other handouts serve for informational purposes only!

| | | | |
|---|---|--|----------------------------|
|  | Title: Module TE0821 | | |
| | A4 | Number: TE0821 3AE31PA | Rev. 01 |
| | Date: 14.08.2020 | Copyright: Trenz Electronic GmbH / TT | Page 1 of 24 |
| | Filename: Legal Notices Modules.SchDoc | | |

TE0821

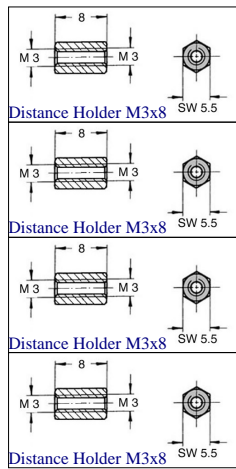
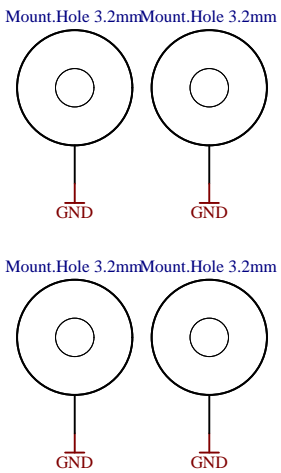
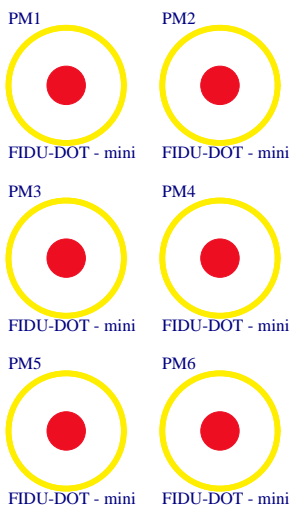
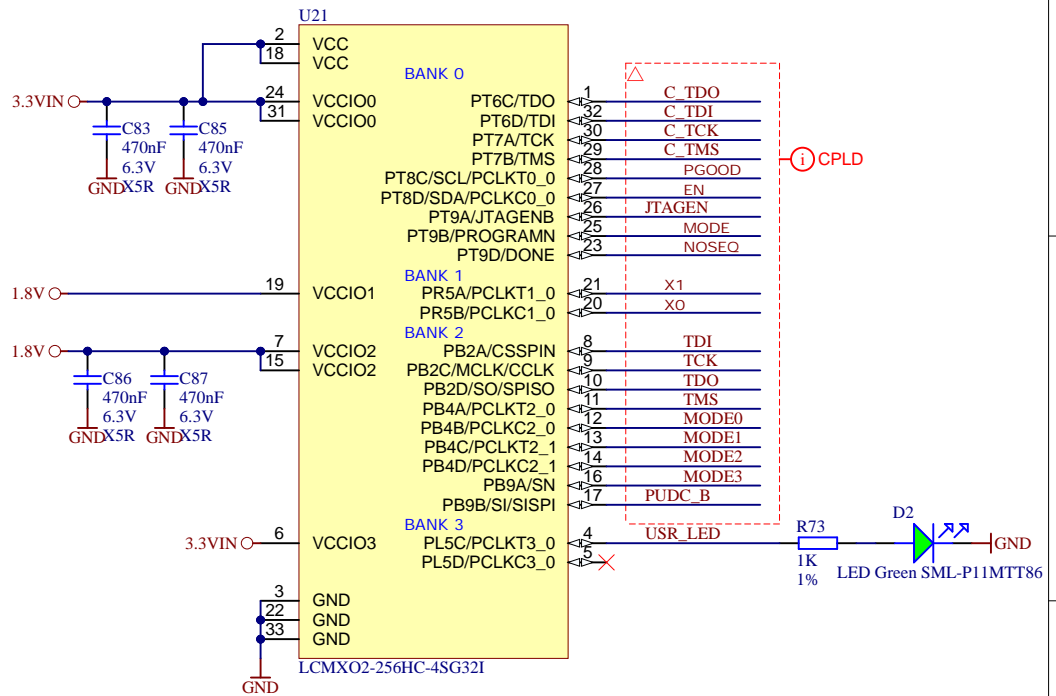


*Bank in XCZU2/3 (XCZU4/5)

| | | | |
|---|--|---|-----------------------------------|
|  | | Title: Module TE0821 - System Overview | |
| | | A4 | Number: TE0821 3AE31PA |
| Date: 18.01.2022 | | Copyright: 2015 Trenz Electronic GmbH | |
| Filename: TE0821-Overview.SchDoc | | Page 2 of 24 | |

| |
|--------------------------------------|
| U_USB-PHY USB-PHY.SchDoc |
| U_ETH-PHY ETH-PHY.SchDoc |
| U_B_HD B_HD.SchDoc |
| U_B64 B64.SchDoc |
| U_B65 B65.SchDoc |
| U_B66 B66.SchDoc |
| U_CONFIG CONFIG.SchDoc |
| U_B_MIO B_MIO.SchDoc |
| U_B_PS_GT B_PS_GT.SchDoc |
| U_CLK CLK.SchDoc |
| U_Overview TE0821-Overview.SchDoc |
| U_LN Legal Notices Modules.SchDoc |

| |
|---|
| U_B2B-Connectors B2B-Connectors.SchDoc |
| U_B2B-Connectors_2 B2B-Connectors_2.SchDoc |
| U_eMMC eMMC.SchDoc |
| U_PS_DDR PS_DDR.SchDoc |
| U_ZU_POWER ZU_POWER.SchDoc |
| U_ZU_PS_POWER ZU_PS_POWER.SchDoc |
| U_DDR4-RAM_2 DDR4-RAM_2.SchDoc |
| U_DDR4-RAM DDR4-RAM.SchDoc |
| U_POWER POWER.SchDoc |
| U_POWER_1 POWER_1.SchDoc |
| U_Revision_changes Revision Changes.SchDoc |

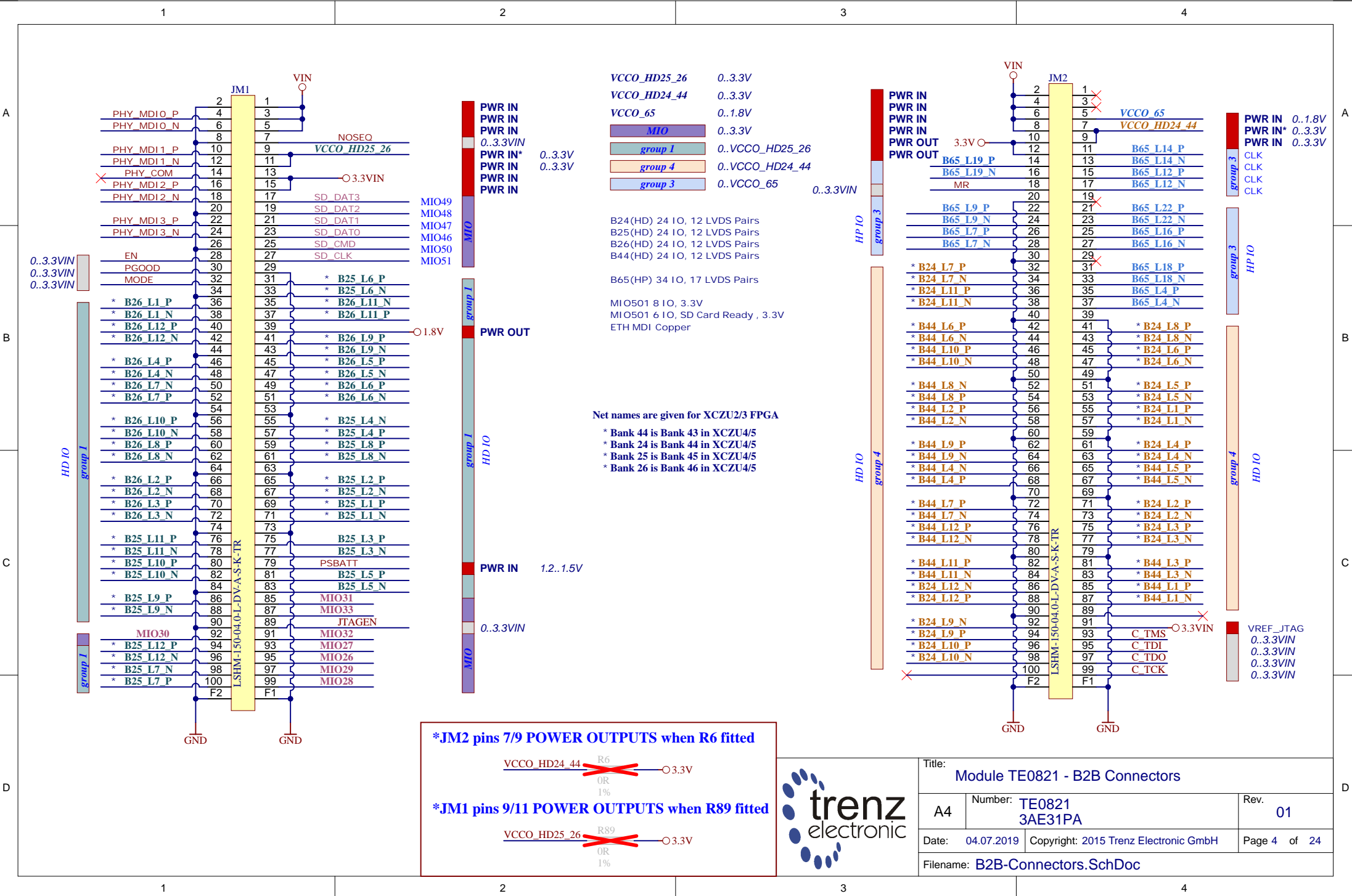


Special notes:

Component RC0201FR-0710KL removed



| | | |
|--------------------------------|--|----------------------------|
| Title: Module TE0821 | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: 2015 Trenz Electronic GmbH | Page 3 of 24 |
| Filename: TE0821.SchDoc | | |



| | |
|--------------|-----------------|
| VCCO_HD25_26 | 0..3.3V |
| VCCO_HD24_44 | 0..3.3V |
| VCCO_65 | 0..1.8V |
| MIO | 0..3.3V |
| group 1 | 0..VCCO_HD25_26 |
| group 4 | 0..VCCO_HD24_44 |
| group 3 | 0..VCCO_65 |

B24(HD) 24 IO, 12 LVDS Pairs
 B25(HD) 24 IO, 12 LVDS Pairs
 B26(HD) 24 IO, 12 LVDS Pairs
 B44(HD) 24 IO, 12 LVDS Pairs
 B65(HP) 34 IO, 17 LVDS Pairs

MIO501 8 IO, 3.3V
 MIO501 6 IO, SD Card Ready, 3.3V
 ETH MDI Copper

Net names are given for XCZU2/3 FPGA

- * Bank 44 is Bank 43 in XCZU4/5
- * Bank 24 is Bank 44 in XCZU4/5
- * Bank 25 is Bank 45 in XCZU4/5
- * Bank 26 is Bank 46 in XCZU4/5

***JM2 pins 7/9 POWER OUTPUTS when R6 fitted**

VCCO_HD24_44 ~~R6~~ 0.3.3V
OR 1%

***JM1 pins 9/11 POWER OUTPUTS when R89 fitted**

VCCO_HD25_26 ~~R89~~ 0.3.3V
OR 1%



| | | |
|---------------------------------------|---------------------------------------|--------------|
| Title: Module TE0821 - B2B Connectors | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 04.07.2019 | Copyright: 2015 Trenz Electronic GmbH | Page 4 of 24 |
| Filename: B2B-Connectors.SchDoc | | |

1

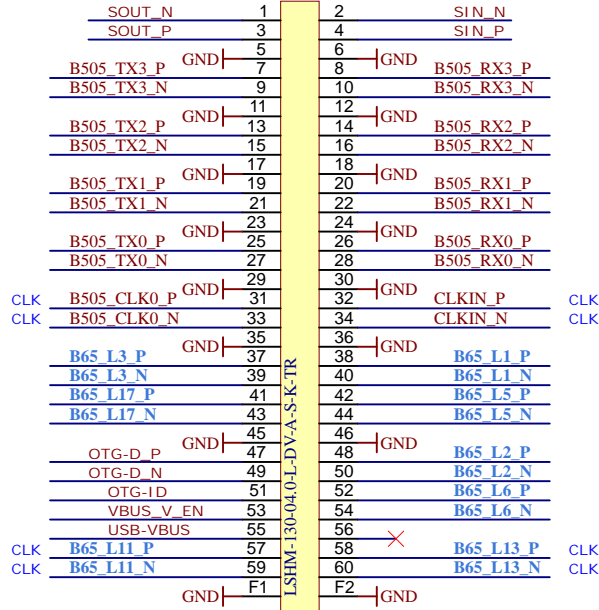
2

3

4

USB OTG
 ETH SGMII
 PS_GTR 4 Lanes
 PS_GTR CLK IN
 PLL CLK IN

JM3



HP IO
 group 3
 USB
 HP IO

group 3
 group 3
 group 3

X

X



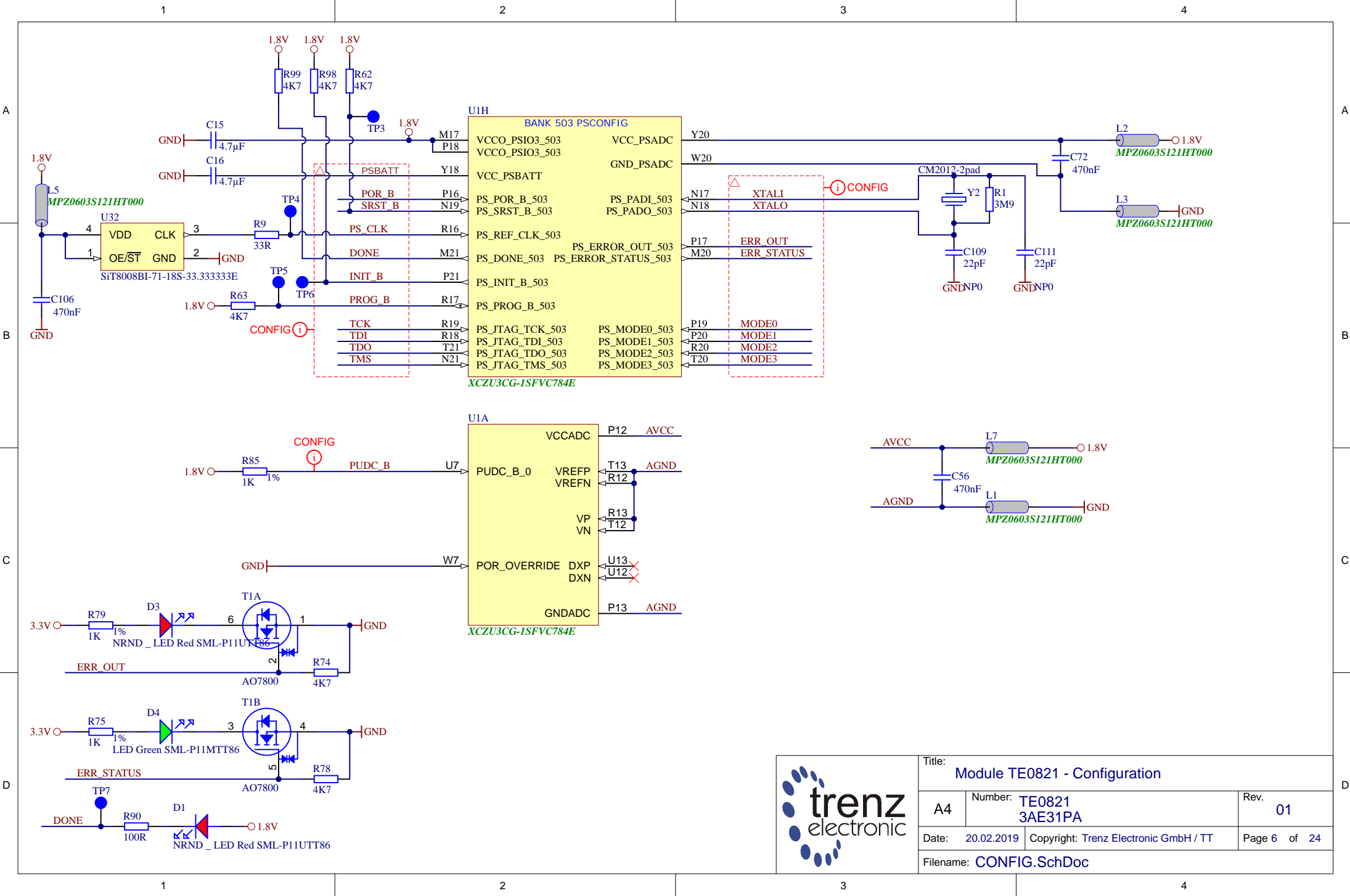
| | | |
|---------------------------------------|---------------------------------------|--------------|
| Title: Module TE0821 - B2B Connectors | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: 2015 Trenz Electronic GmbH | Page 5 of 24 |
| Filename: B2B-Connectors_2.SchDoc | | |

1

2

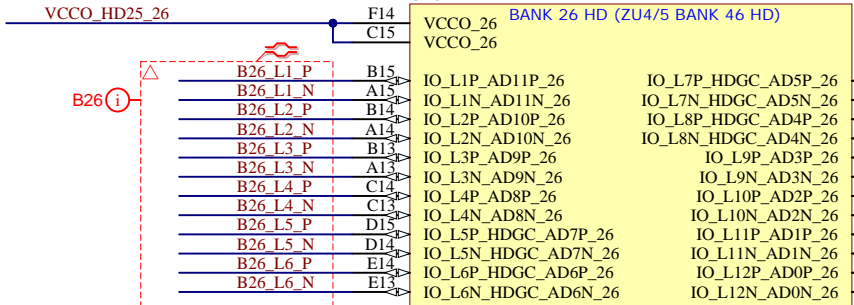
3

4

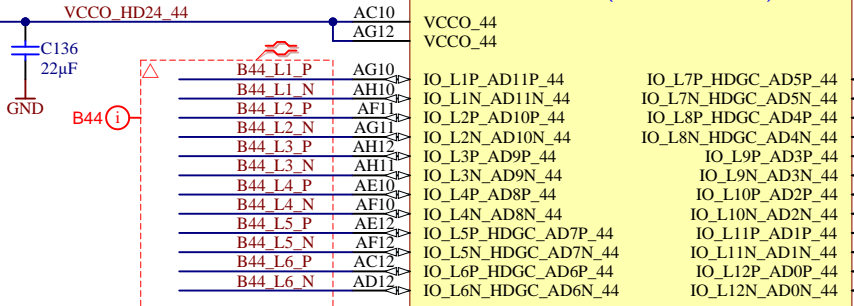


| | | |
|---|--|----------------------------|
| Title: Module TE0821 - Configuration | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 6 of 24 |
| Filename: CONFIG.SchDoc | | |

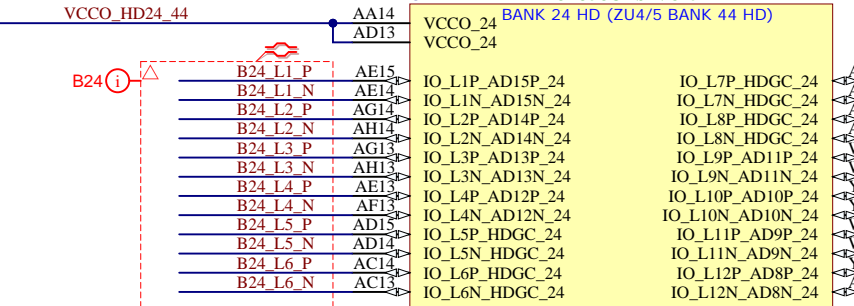
UIC



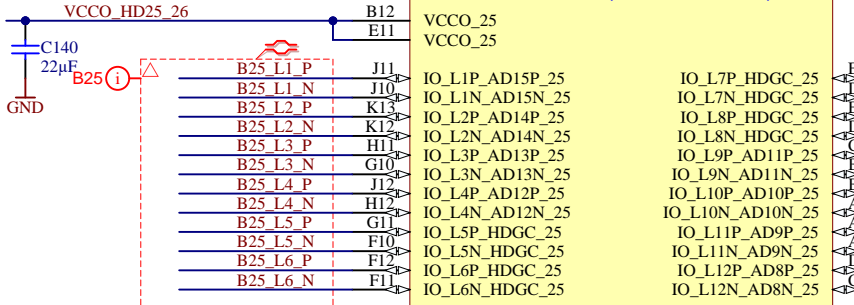
BANK 44 HD (ZU4/5 BANK 43 HD)



UIB **XCZU3CG-1SFVC784E**



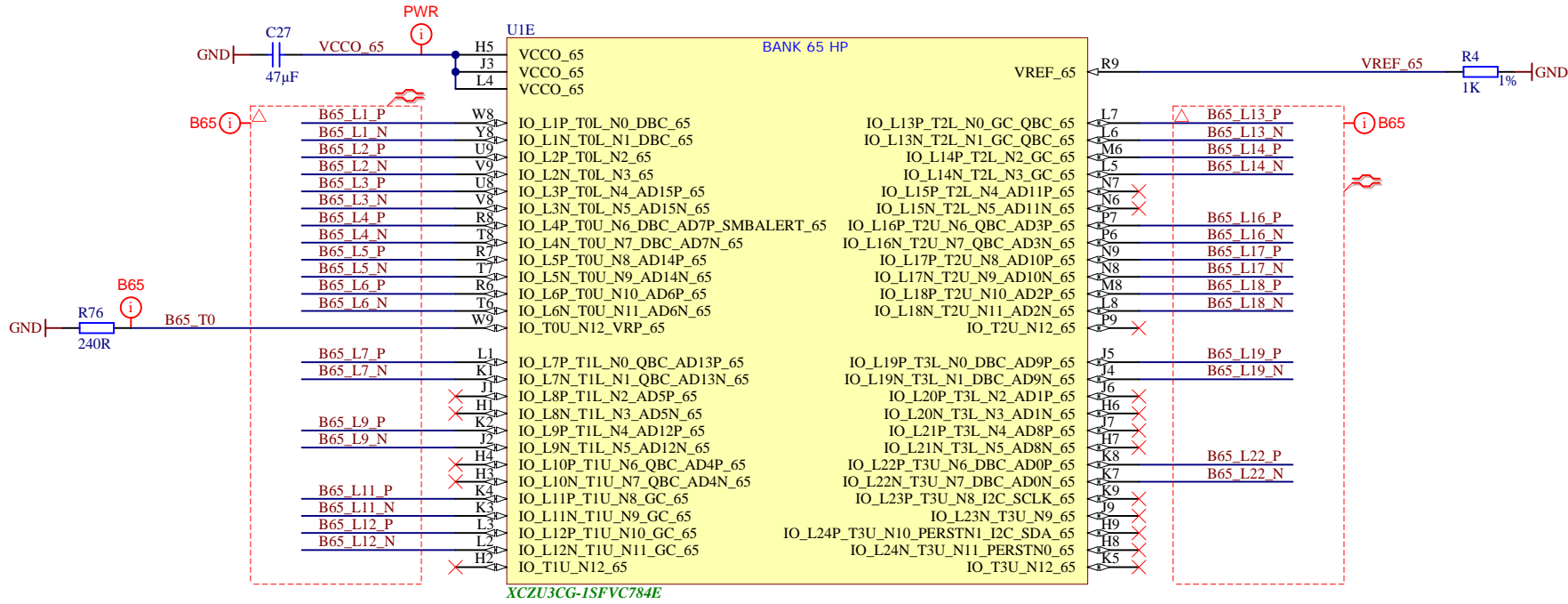
BANK 25 HD (ZU4/5 BANK 45 HD)



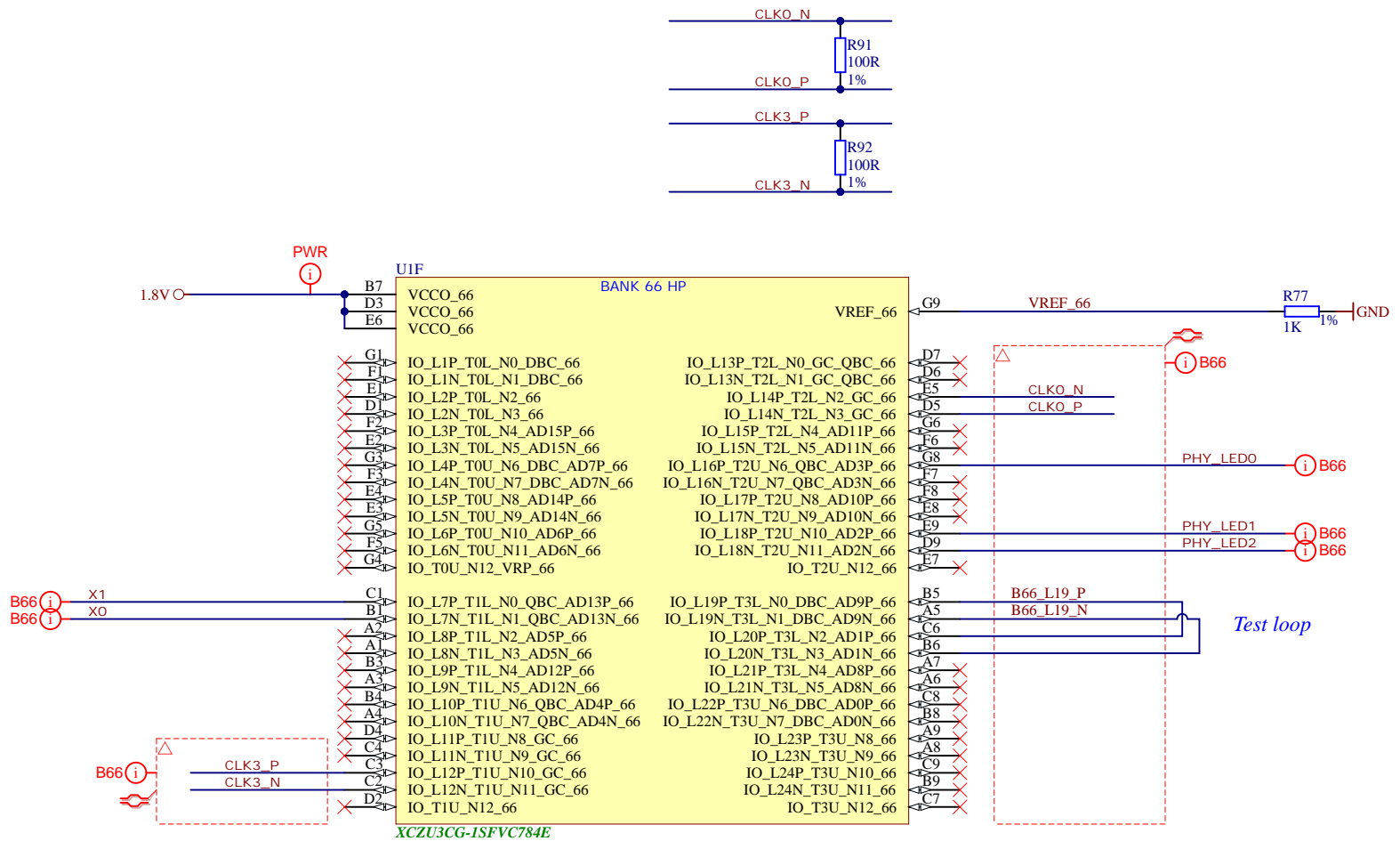
XCZU3CG-1SFVC784E



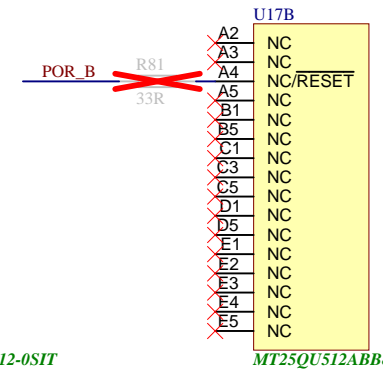
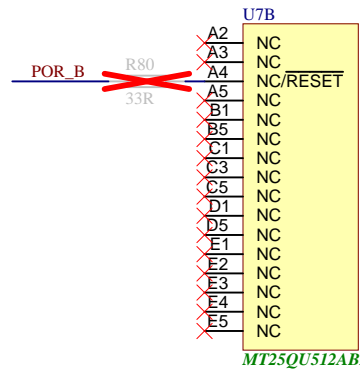
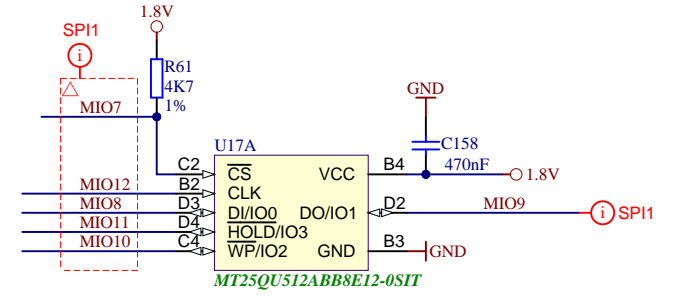
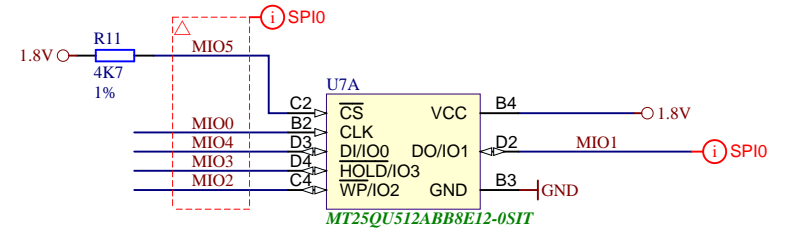
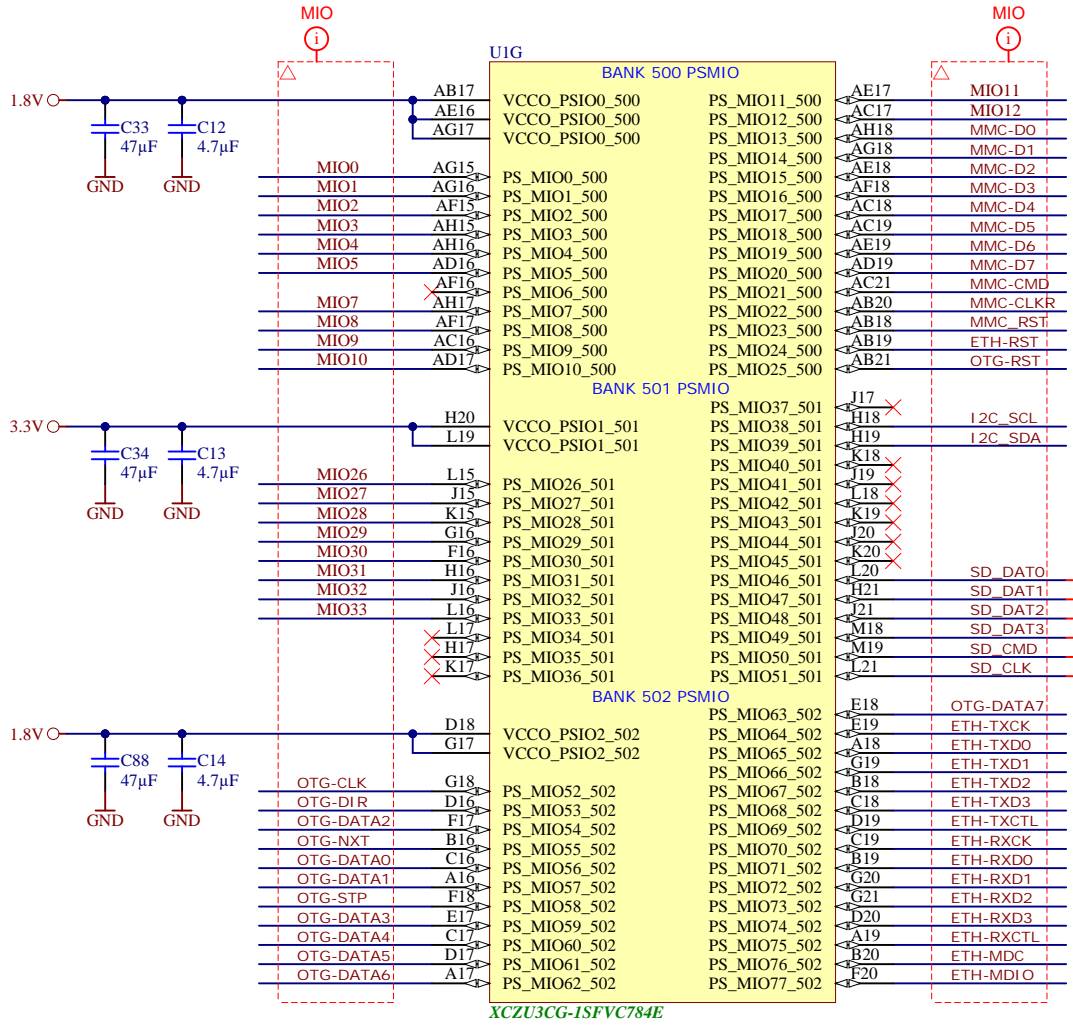
| | | |
|--|--|----------------------------|
| Title: Module TE0821 - HD Banks | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 7 of 24 |
| Filename: B_HD.SchDoc | | |



| | | |
|-----------------------------------|--|----------------------------|
| Title: Module TE0821 - B65 | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 9 of 24 |
| Filename: B65.SchDoc | | |



| | | |
|-----------------------------------|--|-----------------------------|
| Title: Module TE0821 - B66 | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 10 of 24 |
| Filename: B66.SchDoc | | |



| | | | |
|--|--|---|---|
| | | Title: Module TE0821 - MIO Banks | |
| | | A4 | Number: TE0821 3AE31PA Date: 20.02.2019 Copyright: Trenz Electronic GmbH / TT Filename: B_MIO.SchDoc |

A

B

C

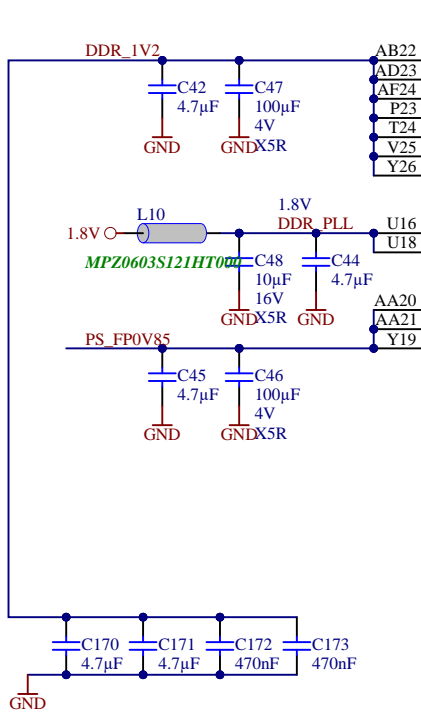
D

A

B

C

D



U11

BANK 504 PSDDR

| | | | | |
|----------------------|------------------|------|-------------|------|
| VCCO_PSDDR_504 | PS_DDR_CK0_504 | W25 | DDR4-CLK0 P | |
| VCCO_PSDDR_504 | PS_DDR_CK_N0_504 | W26 | DDR4-CLK0 N | |
| VCCO_PSDDR_504 | PS_DDR_CKE0_504 | V28 | DDR4-CKE0 | |
| VCCO_PSDDR_504 | PS_DDR_CK1_504 | Y24 | | × |
| VCCO_PSDDR_504 | PS_DDR_CK_N1_504 | Y25 | | × |
| VCCO_PSDDR_504 | PS_DDR_CKE1_504 | V27 | | × |
| VCC_PSDDR_PLL | PS_DDR_A0_504 | W28 | DDR4-A0 | |
| VCC_PSDDR_PLL | PS_DDR_A1_504 | Y28 | DDR4-A1 | |
| VCC_PSDDR_PLL | PS_DDR_A2_504 | AB28 | DDR4-A2 | |
| VCC_PSDDR_PLL | PS_DDR_A3_504 | AA28 | DDR4-A3 | |
| VCC_PSDDR_PLL | PS_DDR_A4_504 | Y27 | DDR4-A4 | |
| VCC_PSINTFP_DDR | PS_DDR_A5_504 | AA27 | DDR4-A5 | |
| VCC_PSINTFP_DDR | PS_DDR_A6_504 | Y22 | DDR4-A6 | |
| VCC_PSINTFP_DDR | PS_DDR_A7_504 | AA23 | DDR4-A7 | |
| VCC_PSINTFP_DDR | PS_DDR_A8_504 | AA22 | DDR4-A8 | |
| VCC_PSINTFP_DDR | PS_DDR_A9_504 | AB23 | DDR4-A9 | |
| VCC_PSINTFP_DDR | PS_DDR_A10_504 | AA25 | DDR4-A10 | |
| VCC_PSINTFP_DDR | PS_DDR_A11_504 | AA26 | DDR4-A11 | |
| VCC_PSINTFP_DDR | PS_DDR_A12_504 | AB25 | DDR4-A12 | |
| VCC_PSINTFP_DDR | PS_DDR_A13_504 | AB26 | DDR4-A13 | |
| VCC_PSINTFP_DDR | PS_DDR_A14_504 | AB24 | DDR4-A14 | |
| VCC_PSINTFP_DDR | PS_DDR_A15_504 | AC24 | DDR4-A15 | |
| VCC_PSINTFP_DDR | PS_DDR_A16_504 | AC23 | DDR4-A16 | |
| VCC_PSINTFP_DDR | PS_DDR_A17_504 | AC22 | DDR4-A17 | |
| PS_DDR_CS_N0_504 | | W27 | DDR4-CS | |
| PS_DDR_CS_N1_504 | | V26 | | × |
| PS_DDR_BA0_504 | | V23 | DDR4-BA0 | |
| PS_DDR_BA1_504 | | W22 | DDR4-BA1 | |
| PS_DDR_BG0_504 | | W24 | DDR4-BG0 | |
| PS_DDR_BG1_504 | | V22 | DDR4-BG1 | |
| PS_DDR_PARITY_504 | | V24 | DDR4-PAR | |
| PS_DDR_RAM_RST_N_504 | | U23 | DDR4-RESET | |
| PS_DDR_ACT_N_504 | | Y23 | DDR4-ACT | |
| PS_DDR_ALERT_N_504 | | U25 | DDR4-ALERT | |
| PS_DDR_ZQ_504 | | U24 | | 240R |
| PS_DDR_ODT0_504 | | U28 | DDR4-ODT0 | |
| PS_DDR_ODT1_504 | | U26 | | × |

XCZU3CG-1SFVC784E

U1J

BANK 504 PSDDR

| | | | | | |
|-------------|------|-------------------|-----------------|------|----------|
| DQ0 | AD21 | PS_DDR_DQ0_504 | PS_DDR_DQ32_504 | T22 | |
| DQ1 | AE20 | PS_DDR_DQ1_504 | PS_DDR_DQ33_504 | R22 | × |
| DQ2 | AD20 | PS_DDR_DQ2_504 | PS_DDR_DQ34_504 | P22 | × |
| DQ3 | AF20 | PS_DDR_DQ3_504 | PS_DDR_DQ35_504 | N22 | × |
| DQ4 | AH21 | PS_DDR_DQ4_504 | PS_DDR_DQ36_504 | T23 | × |
| DQ5 | AH20 | PS_DDR_DQ5_504 | PS_DDR_DQ37_504 | P24 | × |
| DQ6 | AH19 | PS_DDR_DQ6_504 | PS_DDR_DQ38_504 | R24 | × |
| DQ7 | AG19 | PS_DDR_DQ7_504 | PS_DDR_DQ39_504 | N24 | × |
| DQ8 | AF22 | PS_DDR_DQ8_504 | PS_DDR_DQ40_504 | H24 | × |
| DQ9 | AH22 | PS_DDR_DQ9_504 | PS_DDR_DQ41_504 | J24 | × |
| DQ10 | AE22 | PS_DDR_DQ10_504 | PS_DDR_DQ42_504 | M24 | × |
| DQ11 | AD23 | PS_DDR_DQ11_504 | PS_DDR_DQ43_504 | K24 | × |
| DQ12 | AH23 | PS_DDR_DQ12_504 | PS_DDR_DQ44_504 | J22 | × |
| DQ13 | AH24 | PS_DDR_DQ13_504 | PS_DDR_DQ45_504 | H22 | × |
| DQ14 | AE24 | PS_DDR_DQ14_504 | PS_DDR_DQ46_504 | K22 | × |
| DQ15 | AG24 | PS_DDR_DQ15_504 | PS_DDR_DQ47_504 | J22 | × |
| DQ16 | AC26 | PS_DDR_DQ16_504 | PS_DDR_DQ48_504 | M25 | × |
| DQ17 | AD26 | PS_DDR_DQ17_504 | PS_DDR_DQ49_504 | M26 | × |
| DQ18 | AD25 | PS_DDR_DQ18_504 | PS_DDR_DQ50_504 | L25 | × |
| DQ19 | AD24 | PS_DDR_DQ19_504 | PS_DDR_DQ51_504 | L26 | × |
| DQ20 | AG26 | PS_DDR_DQ20_504 | PS_DDR_DQ52_504 | K28 | × |
| DQ21 | AH25 | PS_DDR_DQ21_504 | PS_DDR_DQ53_504 | L28 | × |
| DQ22 | AH26 | PS_DDR_DQ22_504 | PS_DDR_DQ54_504 | M28 | × |
| DQ23 | AG25 | PS_DDR_DQ23_504 | PS_DDR_DQ55_504 | N28 | × |
| DQ24 | AH27 | PS_DDR_DQ24_504 | PS_DDR_DQ56_504 | J28 | × |
| DQ25 | AH28 | PS_DDR_DQ25_504 | PS_DDR_DQ57_504 | K27 | × |
| DQ26 | AF28 | PS_DDR_DQ26_504 | PS_DDR_DQ58_504 | H28 | × |
| DQ27 | AG28 | PS_DDR_DQ27_504 | PS_DDR_DQ59_504 | H27 | × |
| DQ28 | AC27 | PS_DDR_DQ28_504 | PS_DDR_DQ60_504 | G26 | × |
| DQ29 | AD27 | PS_DDR_DQ29_504 | PS_DDR_DQ61_504 | G25 | × |
| DQ30 | AD28 | PS_DDR_DQ30_504 | PS_DDR_DQ62_504 | K25 | × |
| DQ31 | AC28 | PS_DDR_DQ31_504 | PS_DDR_DQ63_504 | J25 | × |
| | | PS_DDR_DQ64_504 | PS_DDR_DQ64_504 | T28 | × |
| | | PS_DDR_DQ65_504 | PS_DDR_DQ65_504 | R28 | × |
| DDR4-DQS0 P | AF21 | PS_DDR_DQS_P0_504 | PS_DDR_DQ66_504 | P28 | × |
| DDR4-DQS0 N | AG21 | PS_DDR_DQS_N0_504 | PS_DDR_DQ67_504 | P27 | × |
| DDR4-DQS1 P | AF23 | PS_DDR_DQS_P1_504 | PS_DDR_DQ68_504 | P26 | × |
| DDR4-DQS1 N | AG23 | PS_DDR_DQS_N1_504 | PS_DDR_DQ69_504 | R25 | × |
| DDR4-DQS2 P | AF25 | PS_DDR_DQS_P2_504 | PS_DDR_DQ70_504 | P25 | × |
| DDR4-DQS2 N | AF26 | PS_DDR_DQS_N2_504 | PS_DDR_DQ71_504 | J25 | × |
| DDR4-DQS3 P | AE27 | PS_DDR_DQS_P3_504 | | | |
| DDR4-DQS3 N | AE27 | PS_DDR_DQS_N3_504 | | | |
| | N23 | PS_DDR_DQS_P4_504 | | | |
| | M23 | PS_DDR_DQS_N4_504 | PS_DDR_DM0_504 | AG20 | DDR4-DM0 |
| | L23 | PS_DDR_DQS_P5_504 | PS_DDR_DM1_504 | AE23 | DDR4-DM1 |
| | K23 | PS_DDR_DQS_N5_504 | PS_DDR_DM2_504 | AE25 | DDR4-DM2 |
| | N26 | PS_DDR_DQS_P6_504 | PS_DDR_DM3_504 | AE28 | DDR4-DM3 |
| | N27 | PS_DDR_DQS_N6_504 | PS_DDR_DM4_504 | R23 | |
| | J26 | PS_DDR_DQS_P7_504 | PS_DDR_DM5_504 | H23 | |
| | J27 | PS_DDR_DQS_N7_504 | PS_DDR_DM6_504 | L27 | |
| | R27 | PS_DDR_DQS_P8_504 | PS_DDR_DM7_504 | H26 | |
| | T27 | PS_DDR_DQS_N8_504 | PS_DDR_DM8_504 | T26 | |

XCZU3CG-1SFVC784E



| | | |
|--------------------------------------|--|-----------------------------|
| Title: Module TE0821 - PS DDR | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 12 of 24 |
| Filename: PS_DDR.SchDoc | | |

1

2

3

4

A

A

B

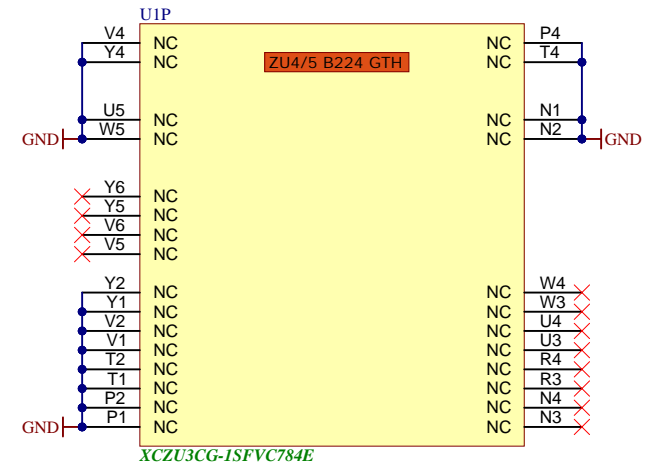
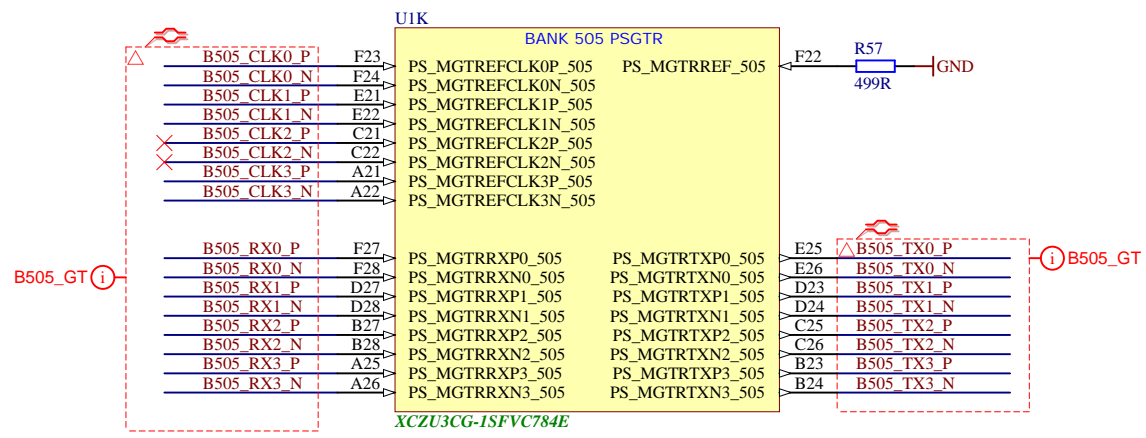
B

C

C

D

D



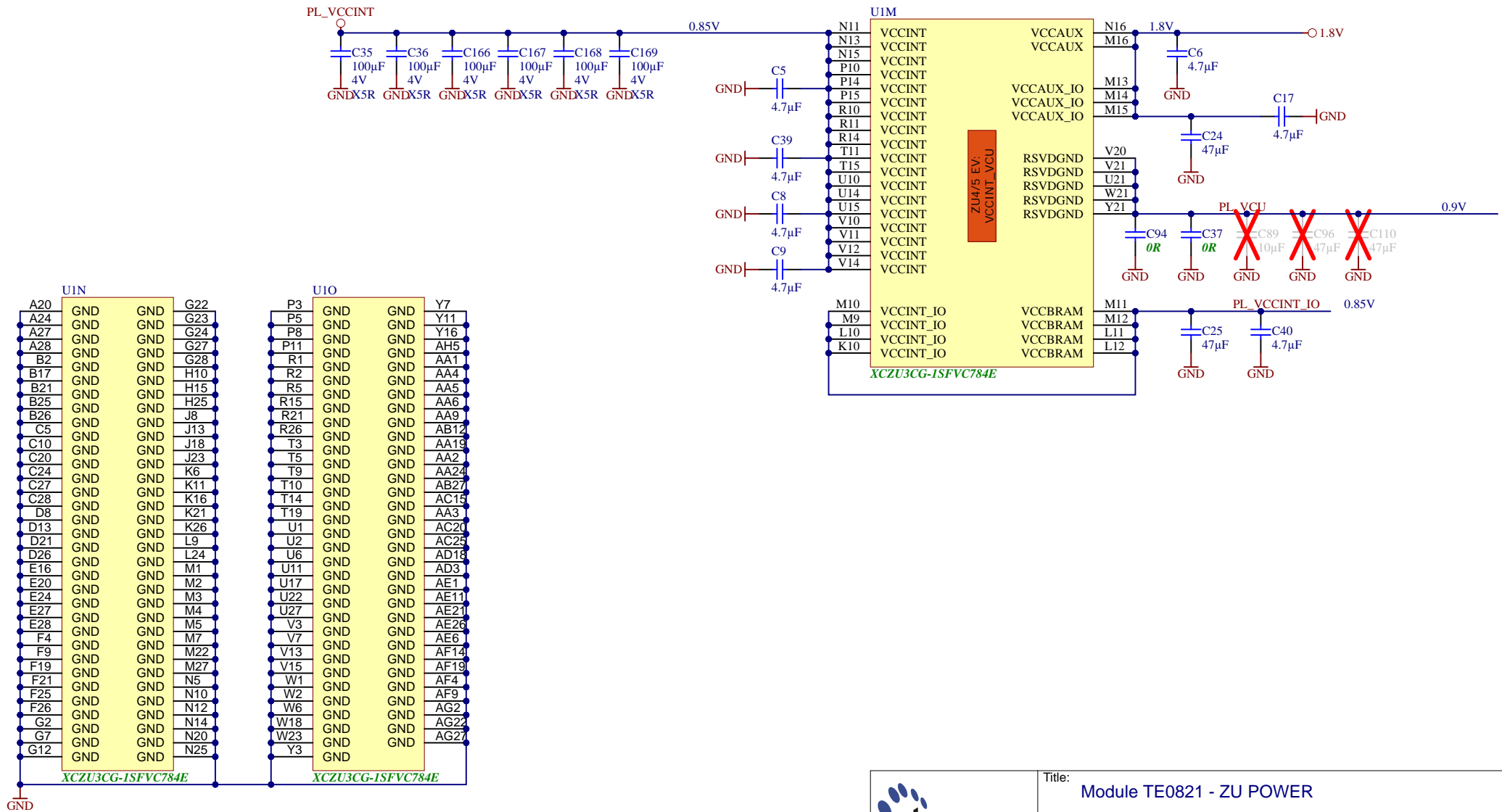
| | | |
|--------------------------------------|--|-----------------------------|
| Title: Module TE0821 - PS MGT | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 13 of 24 |
| Filename: B_PS_GT.SchDoc | | |

1

2

3

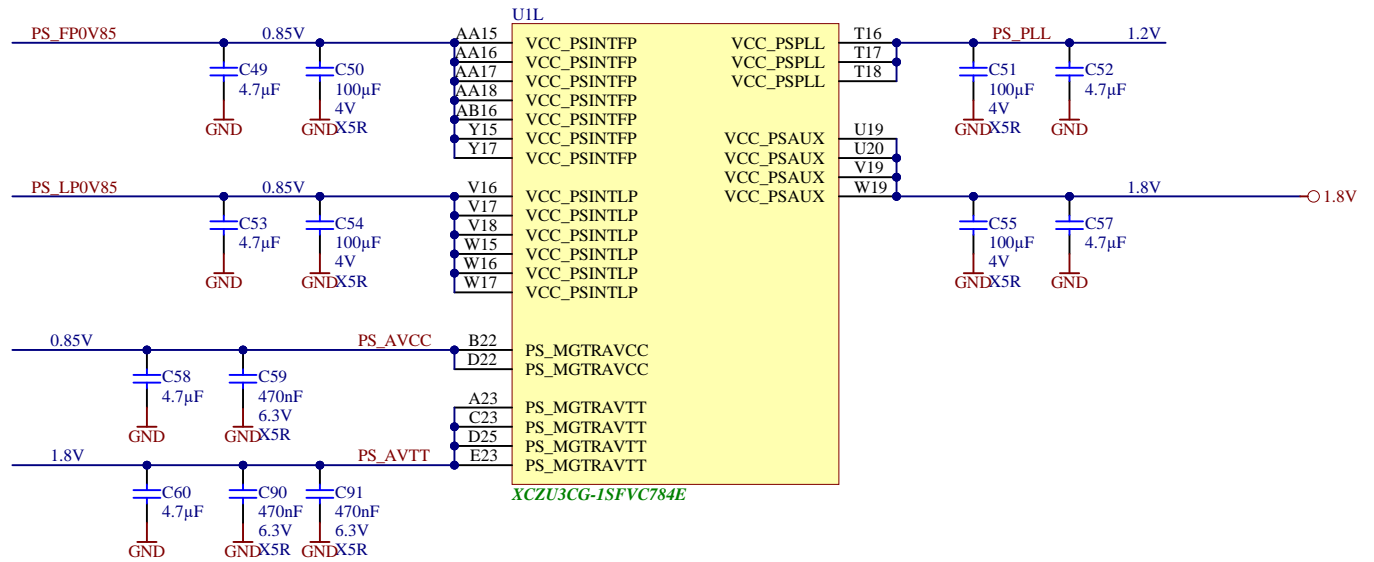
4




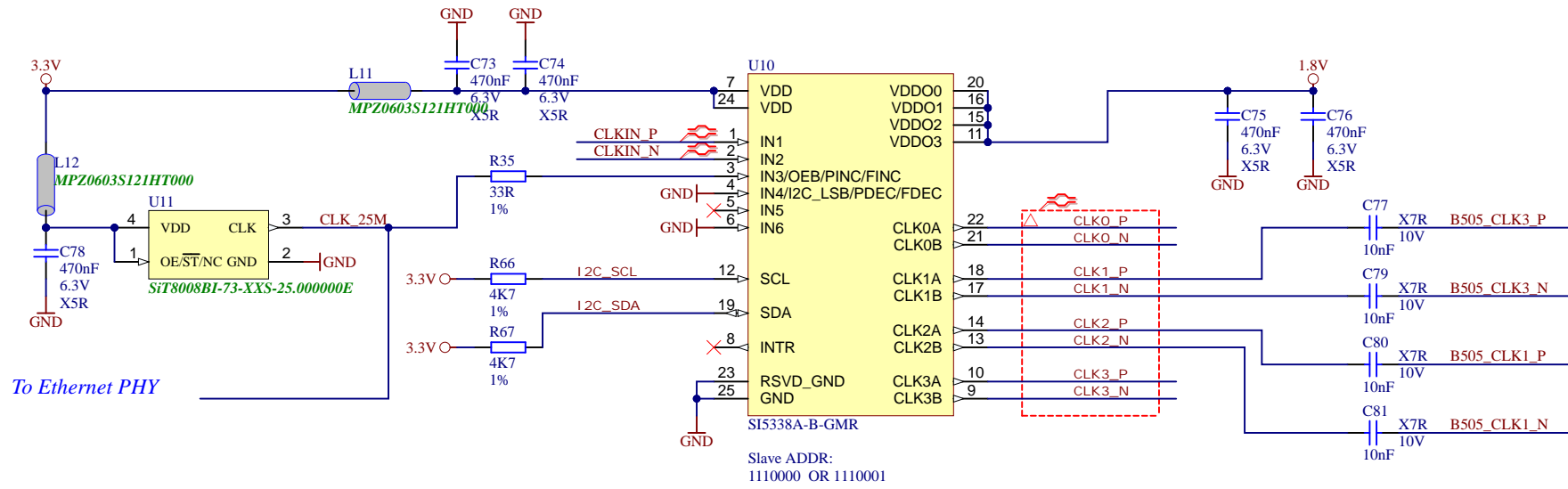
| U1N | | | | U1O | | | | Y7 | | | |
|-----|-----|-----|-----|-----|-----|-----|------|----|--|--|--|
| A20 | GND | GND | G22 | P3 | GND | GND | Y11 | | | | |
| A24 | GND | GND | G23 | P5 | GND | GND | Y16 | | | | |
| A27 | GND | GND | G24 | P8 | GND | GND | Y16 | | | | |
| A28 | GND | GND | G27 | P11 | GND | GND | AA5 | | | | |
| B2 | GND | GND | G28 | R1 | GND | GND | AA1 | | | | |
| B17 | GND | GND | H10 | R2 | GND | GND | AA4 | | | | |
| B21 | GND | GND | H15 | R5 | GND | GND | AA5 | | | | |
| B25 | GND | GND | H25 | R15 | GND | GND | AA6 | | | | |
| B26 | GND | GND | J8 | R21 | GND | GND | AA9 | | | | |
| C5 | GND | GND | J13 | R26 | GND | GND | AB12 | | | | |
| C10 | GND | GND | J18 | T3 | GND | GND | AA19 | | | | |
| C20 | GND | GND | J23 | T5 | GND | GND | AA2 | | | | |
| C24 | GND | GND | K6 | T9 | GND | GND | AA24 | | | | |
| C27 | GND | GND | K11 | T10 | GND | GND | AB27 | | | | |
| C28 | GND | GND | K16 | T14 | GND | GND | AC15 | | | | |
| D8 | GND | GND | K21 | T19 | GND | GND | AA3 | | | | |
| D13 | GND | GND | K26 | U1 | GND | GND | AC20 | | | | |
| D21 | GND | GND | L9 | U2 | GND | GND | AC25 | | | | |
| D26 | GND | GND | L24 | U6 | GND | GND | AD18 | | | | |
| E16 | GND | GND | M1 | U11 | GND | GND | AD3 | | | | |
| E20 | GND | GND | M2 | U17 | GND | GND | AE1 | | | | |
| E24 | GND | GND | M3 | U22 | GND | GND | AE11 | | | | |
| E27 | GND | GND | M4 | U27 | GND | GND | AE21 | | | | |
| E28 | GND | GND | M5 | V3 | GND | GND | AE26 | | | | |
| F4 | GND | GND | M7 | V7 | GND | GND | AE6 | | | | |
| F9 | GND | GND | M22 | V13 | GND | GND | AF14 | | | | |
| F19 | GND | GND | M27 | V15 | GND | GND | AF19 | | | | |
| F21 | GND | GND | N5 | W1 | GND | GND | AF4 | | | | |
| F25 | GND | GND | N10 | W2 | GND | GND | AF9 | | | | |
| F26 | GND | GND | N12 | W6 | GND | GND | AG2 | | | | |
| G2 | GND | GND | N14 | W18 | GND | GND | AG22 | | | | |
| G7 | GND | GND | N20 | W23 | GND | GND | AG27 | | | | |
| G12 | GND | GND | N25 | Y3 | GND | GND | | | | | |




| | | |
|--|--|-----------------------------|
| Title: Module TE0821 - ZU POWER | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 14 of 24 |
| Filename: ZU_POWER.SchDoc | | |

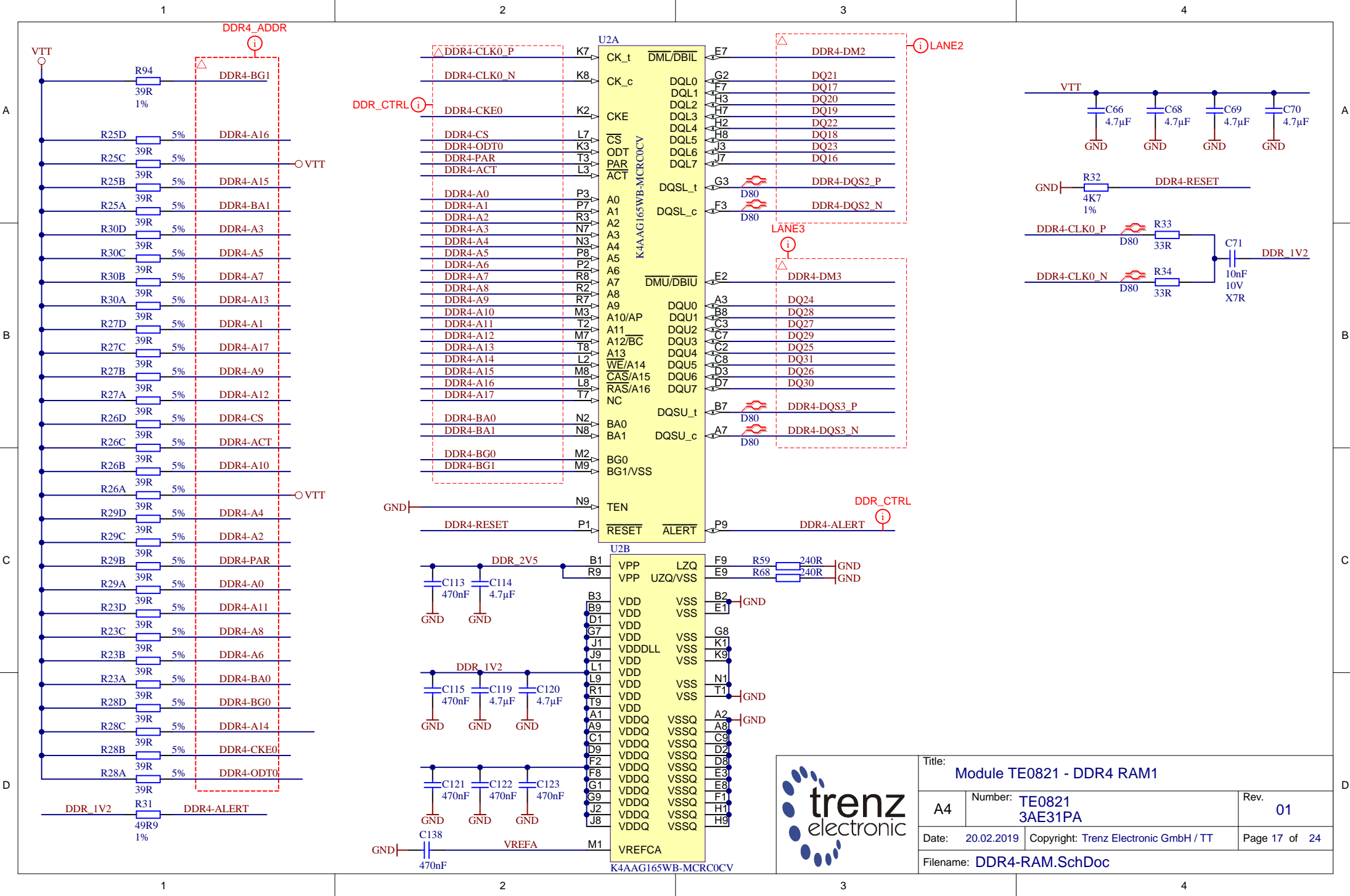


| | | | |
|---|---|--|-----------------------------|
|  | Title: Module TE0821 - ZU PS POWER | | |
| | A4 | Number: TE0821 3AE31PA | Rev. 01 |
| | Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 15 of 24 |
| | Filename: ZU_PS_POWER.SchDoc | | |



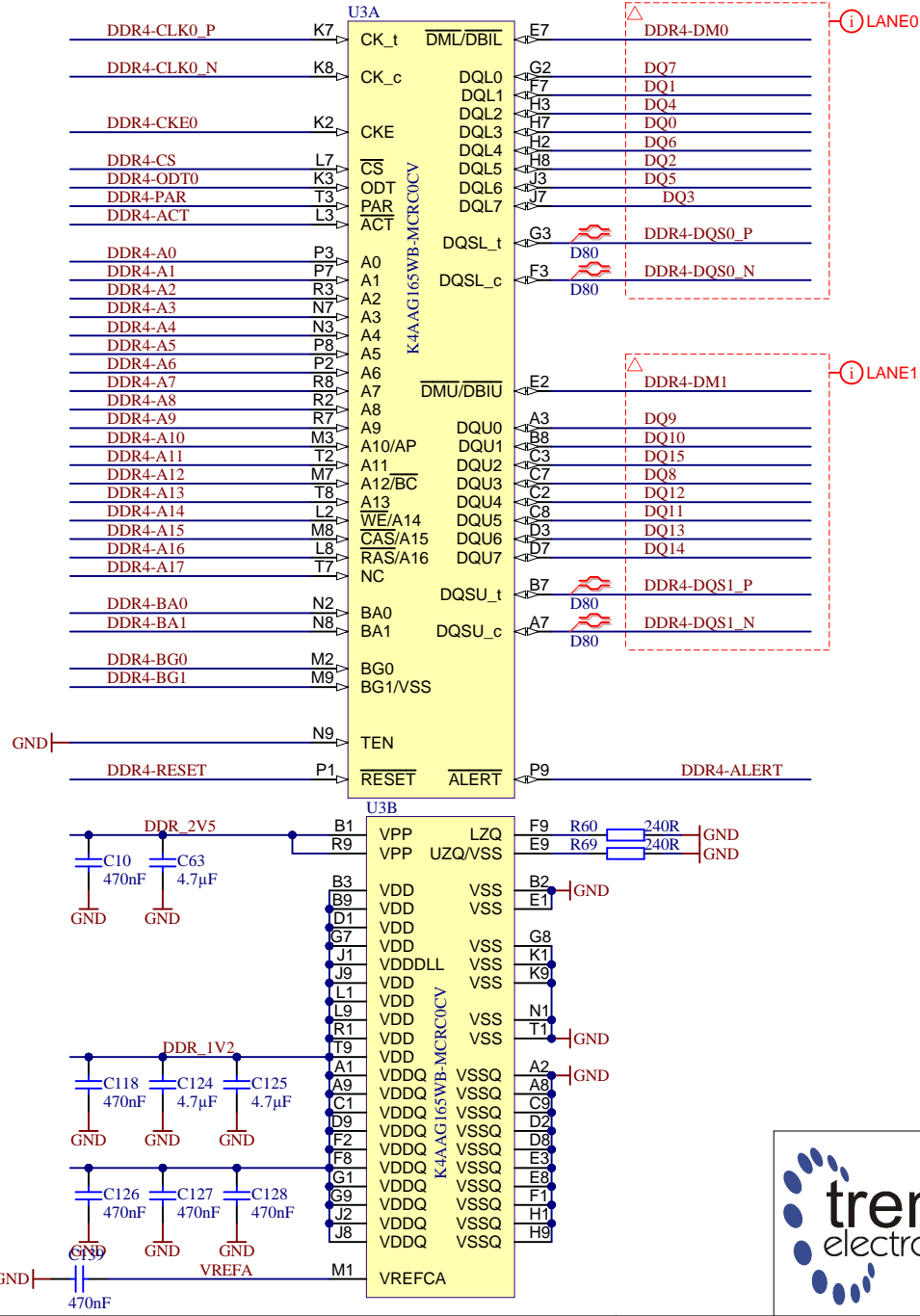
To Ethernet PHY

| | | | |
|---|--|---------------------------------------|---------------------------|
|  | | Title: Module TE0821 - CLK | |
| | | A4 | Number: TE0821 3AE31PA |
| Date: 20.02.2019 | | Copyright: 2015 Trenz Electronic GmbH | |
| Filename: CLK.SchDoc | | Page 16 of 24 | |

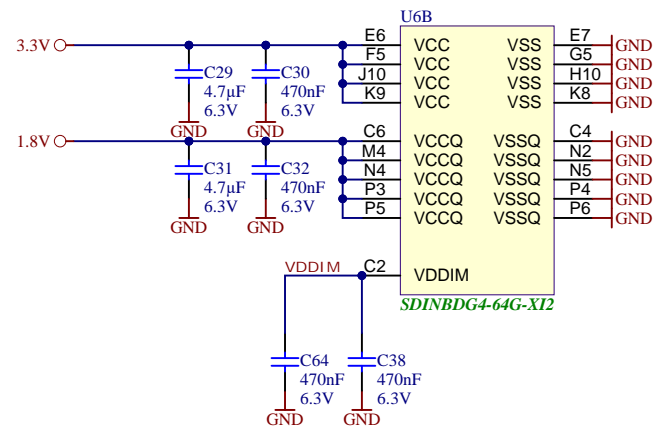
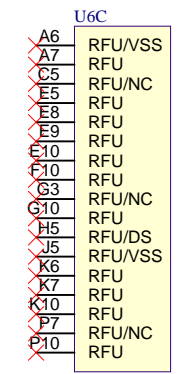
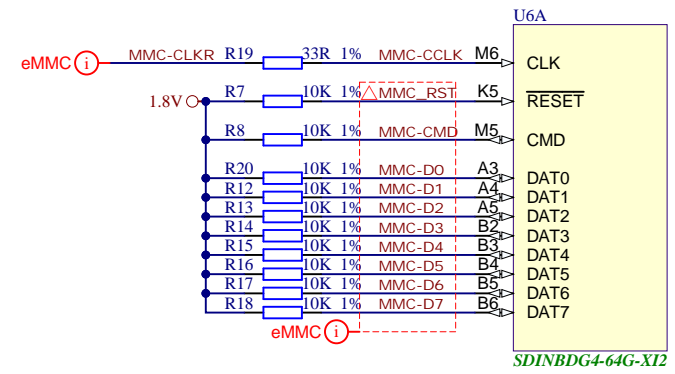
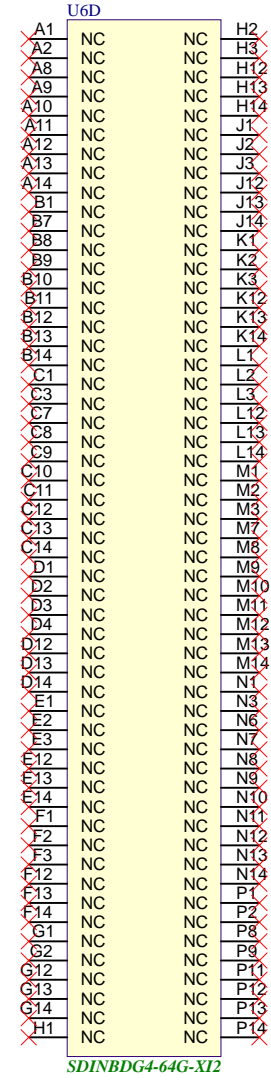


| | | |
|---|--|-----------------------------|
| Title: Module TE0821 - DDR4 RAM1 | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 17 of 24 |
| Filename: DDR4-RAM.SchDoc | | |

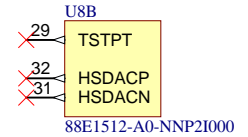
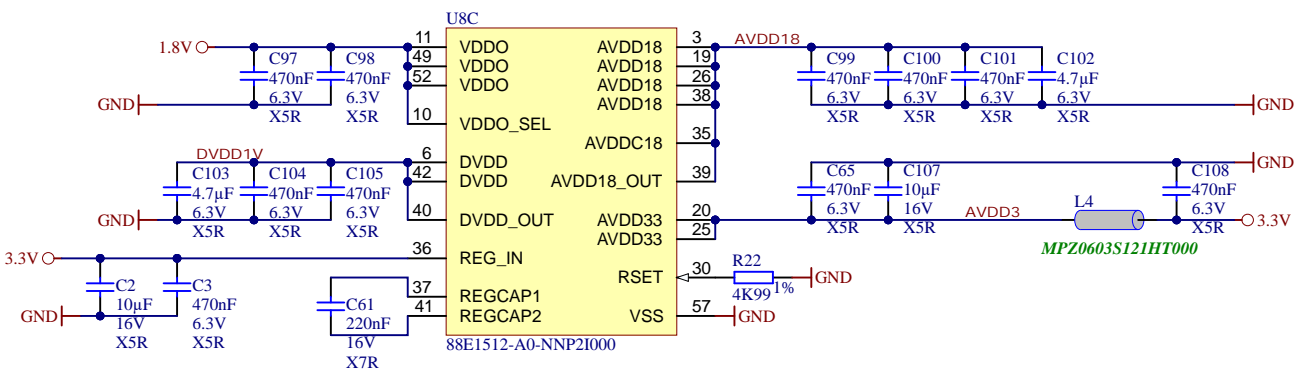
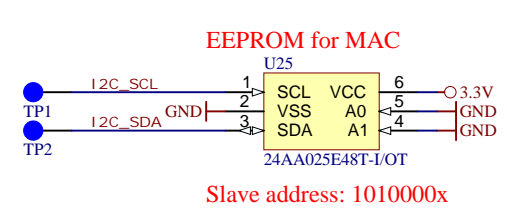
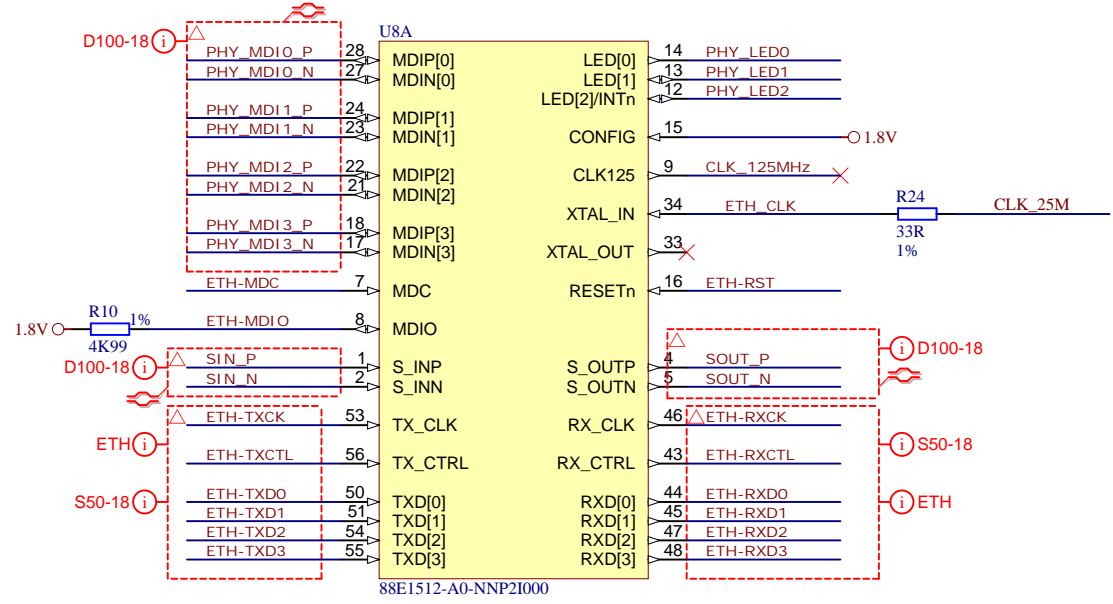




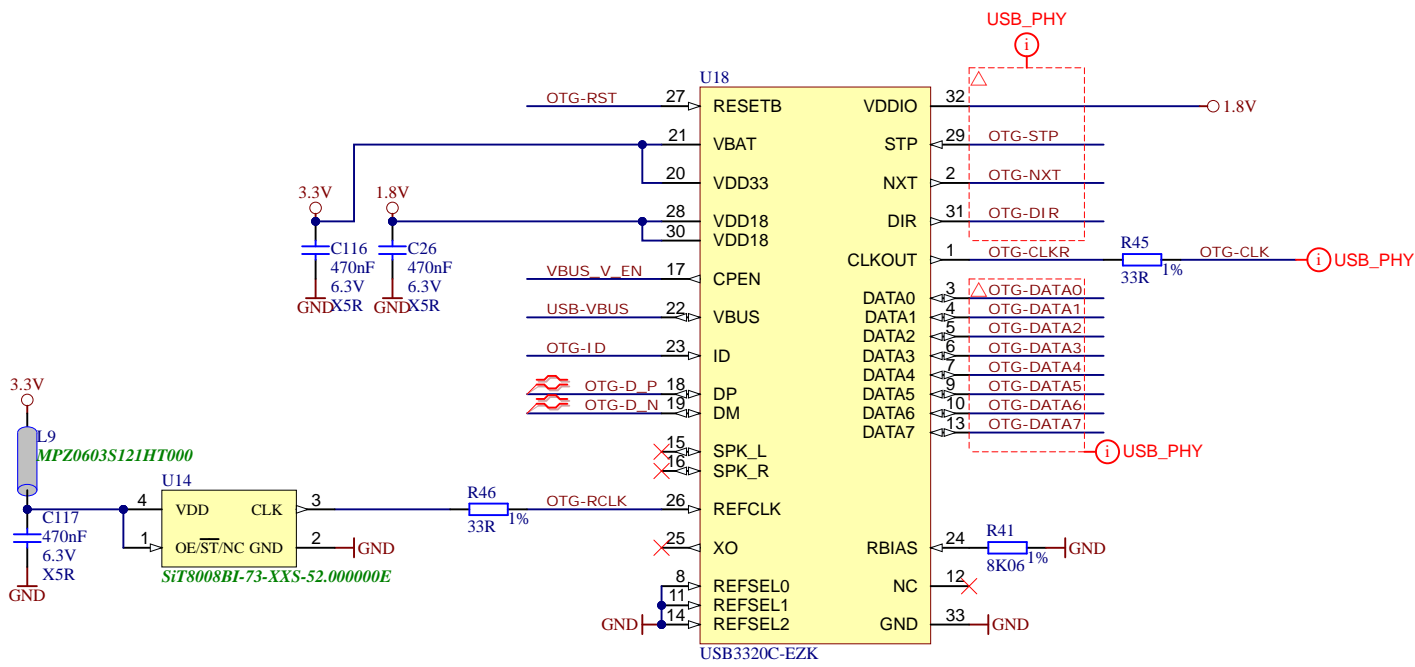
| | | |
|---|--|-----------------------------|
| Title: Module TE0821 - DDR4 RAM2 | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 18 of 24 |
| Filename: DDR4-RAM_2.SchDoc | | |



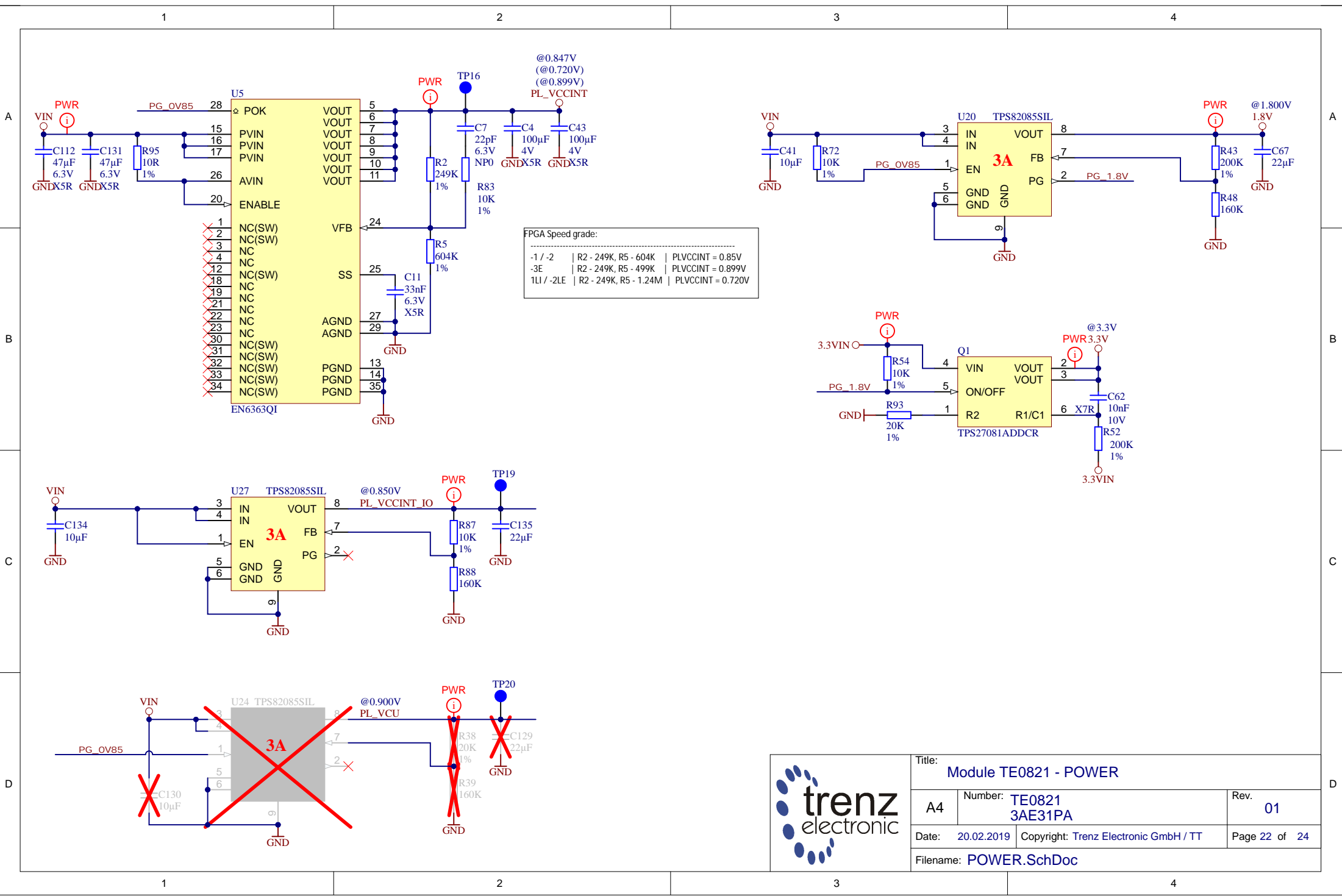
| | | |
|------------------------------------|--|-----------------------------|
| Title: Module TE0821 - eMMC | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 19 of 24 |
| Filename: eMMC.SchDoc | | |



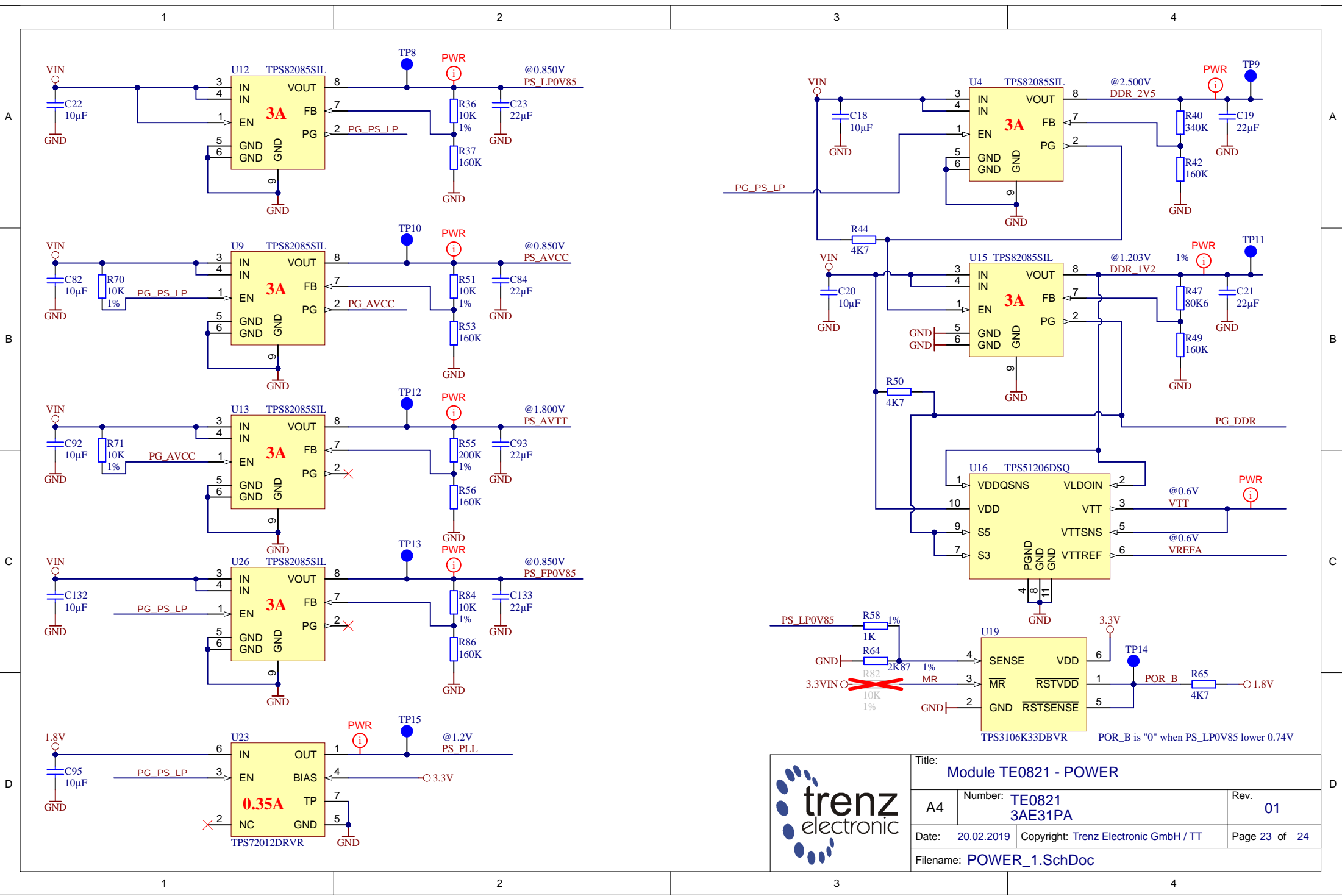
| | | |
|--|--|-----------------------------|
| Title: Module TE0821 - Ethernet PHY | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: 2015 Trenz Electronic GmbH | Page 20 of 24 |
| Filename: ETH-PHY.SchDoc | | |



| | | | |
|---------------------------------|---------------------------------------|---------------------------------------|----------------|
| | Title: Module TE0821 - USB PHY | | |
| | A4 | Number: TE0821 3AE31PA | Rev. 01 |
| | Date: 20.02.2019 | Copyright: 2015 Trenz Electronic GmbH | |
| | Page 21 of 24 | | |
| Filename: USB-PHY.SchDoc | | | |



| | | |
|-------------------------------------|--|-----------------------------|
| Title: Module TE0821 - POWER | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 22 of 24 |
| Filename: POWER.SchDoc | | |



| | | |
|-------------------------------------|--|-----------------------------|
| Title: Module TE0821 - POWER | | |
| A4 | Number: TE0821 3AE31PA | Rev. 01 |
| Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 23 of 24 |
| Filename: POWER_1.SchDoc | | |

POR_B is "0" when PS_LP0V85 lower 0.74V

1

2

3

4

Revision 01a (01.07.2020):

1. VY: R38 value was changed to 20K (was: 40K2) to set VCU 0.9V

Revision 01b (29.10.2020):

1. VY: Updated Block diagram

(07.02.2024):
2. OT: R82 set to not fitted

A

A

B


B

C

C

D

D

| | | | |
|---|--|--|-----------------------------|
|  | Title: Module TE0821 - Revision Changes | | |
| | A4 | Number: TE0821 3AE31PA | Rev. 01 |
| | Date: 20.02.2019 | Copyright: Trenz Electronic GmbH / TT | Page 24 of 24 |
| | Filename: Revision Changes.SchDoc | | |

1

2

3

4