


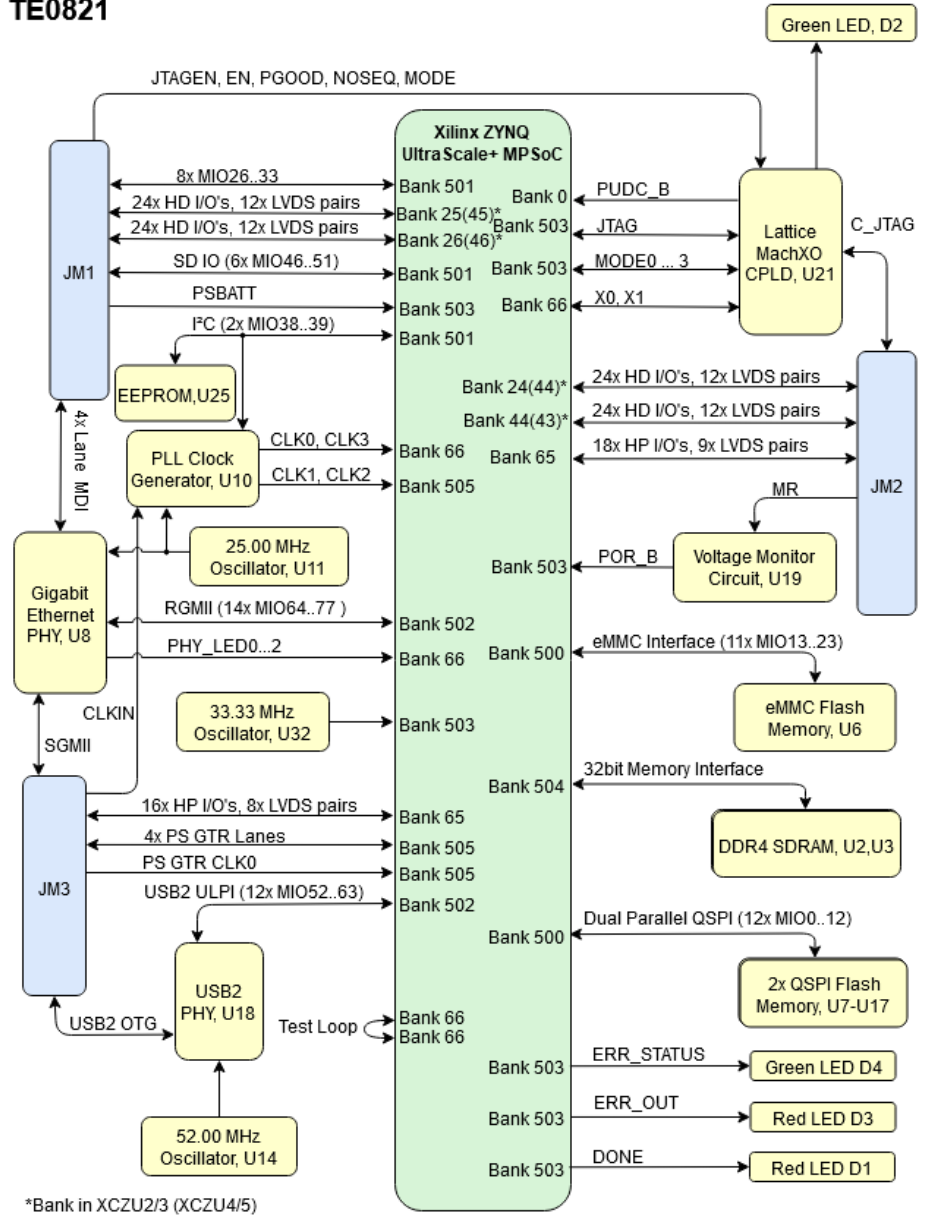
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Schematics and other handouts serve for informational purposes only!

	Title: <b>Module TE0821</b>		
	A4	Number: <b>TE0821 3BE21ML</b>	Rev. <b>01</b>
	Date: <b>14.08.2020</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>1</b> of <b>24</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		

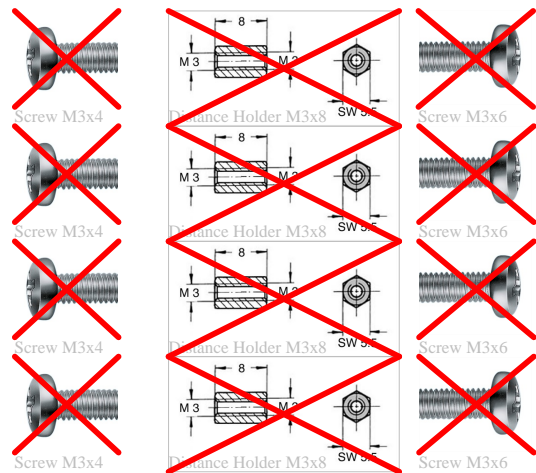
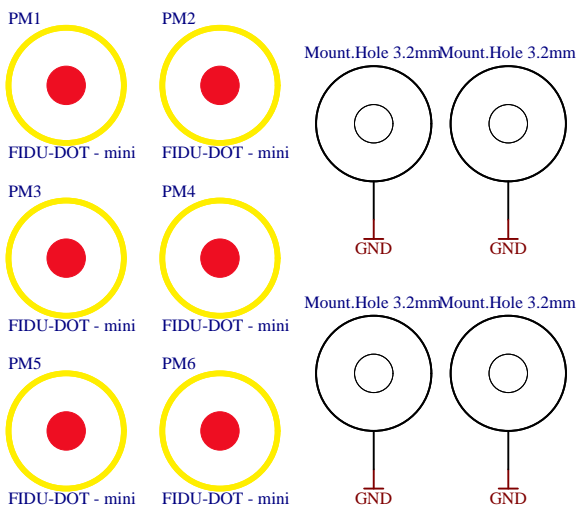
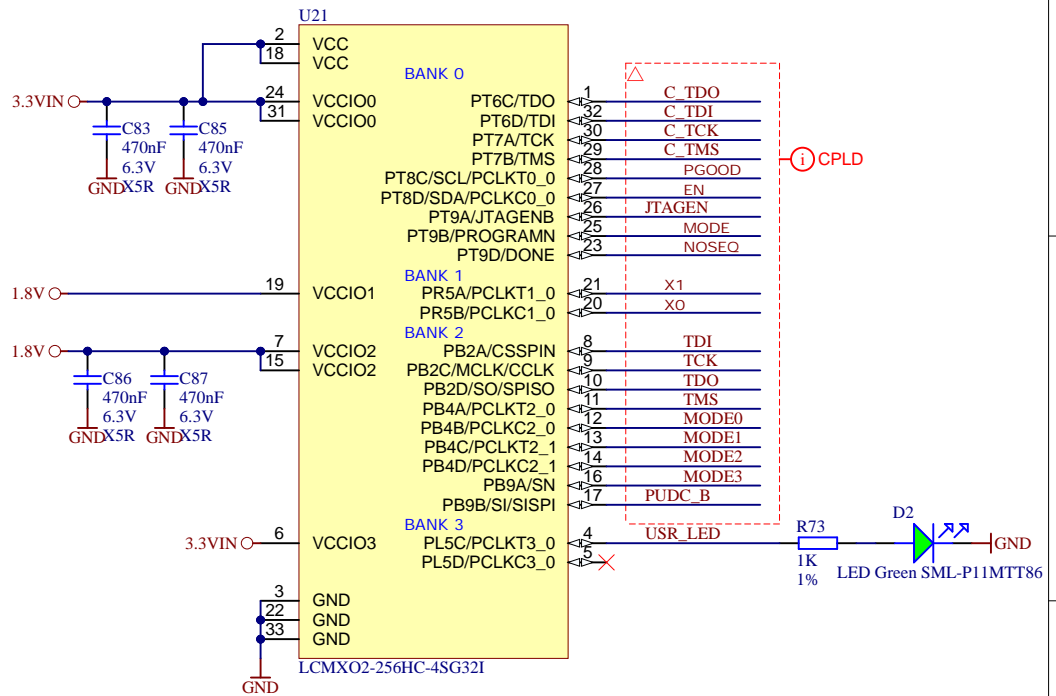
**TE0821**



	Title: <b>Module TE0821 - System Overview</b>	
	A4	Number: <b>TE0821 3BE21ML</b>
	Date: 18.01.2022	Rev. <b>01</b>
	Page 2 of 24	
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Filename: <b>TE0821-Overview.SchDoc</b>		

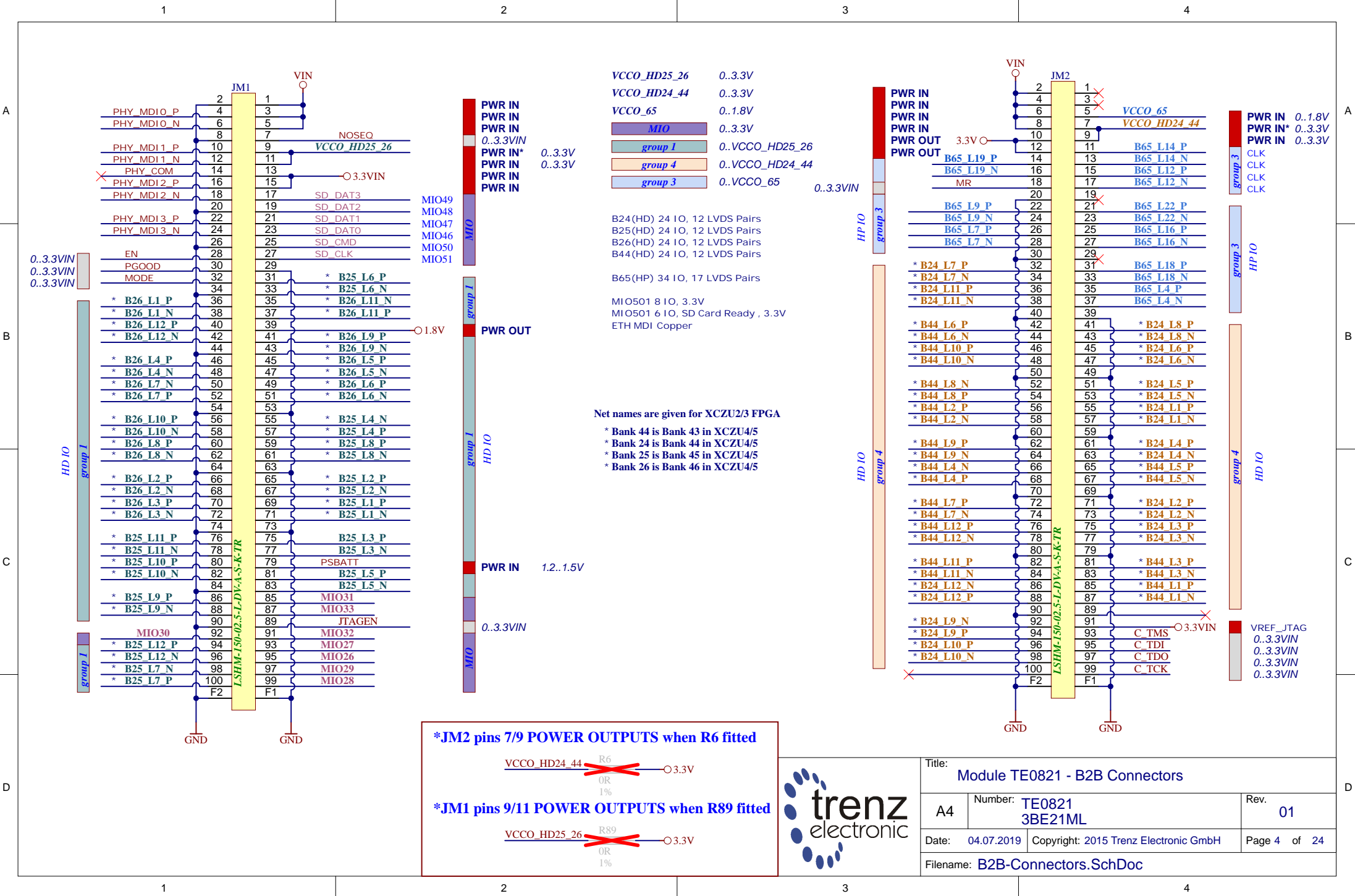
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U_ETH-PHY ETH-PHY.SchDoc
U_B_HD B_HD.SchDoc
U_B64 B64.SchDoc
U_B65 B65.SchDoc
U_B66 B66.SchDoc
U_CONFIG CONFIG.SchDoc
U_B_MIO B_MIO.SchDoc
U_B_PS_GT B_PS_GT.SchDoc
U_CLK CLK.SchDoc
U_Overview TE0821-Overview.SchDoc
U_LN Legal Notices Modules.SchDoc

U_B2B-Connectors B2B-Connectors.SchDoc
U_B2B-Connectors_2 B2B-Connectors_2.SchDoc
U_eMMC eMMC.SchDoc
U_PS_DDR PS_DDR.SchDoc
U_ZU_POWER ZU_POWER.SchDoc
U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_DDR4-RAM_2 DDR4-RAM_2.SchDoc
U_DDR4-RAM DDR4-RAM.SchDoc
U_POWER POWER.SchDoc
U_POWER_1 POWER_1.SchDoc
U_Revision_changes Revision Changes.SchDoc



Special notes:  
Component RC0201FR-0710KL removed

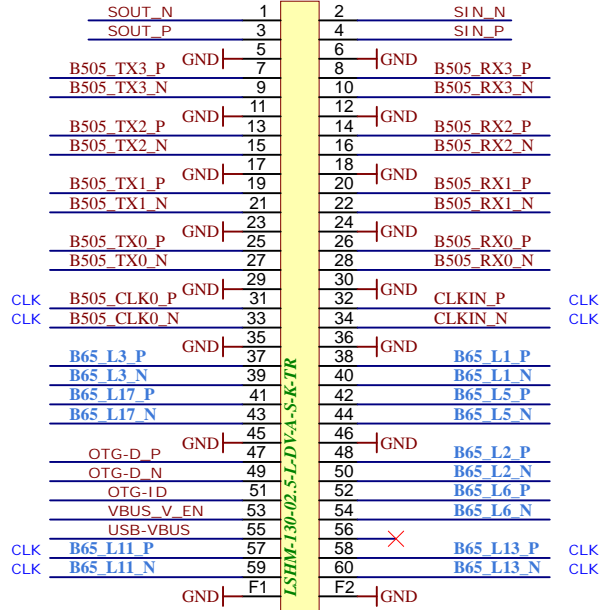
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	A4	Number: <b>TE0821 3BE21ML</b>	Rev. <b>01</b>
	Date: <b>20.02.2019</b>	Copyright: 2015 Trenz Electronic GmbH	Page <b>3</b> of <b>24</b>
	Filename: <b>TE0821.SchDoc</b>		



Title: Module TE0821 - B2B Connectors		
A4	Number: TE0821 3BE21ML	Rev. 01
Date: 04.07.2019	Copyright: 2015 Trenz Electronic GmbH	Page 4 of 24
Filename: B2B-Connectors.SchDoc		

USB OTG  
 ETH SGMII  
 PS\_GTR 4 Lanes  
 PS\_GTR CLK IN  
 PLL CLK IN

JM3



X

HP IO

group 3

HP IO

USB

CLK

CLK

CLK

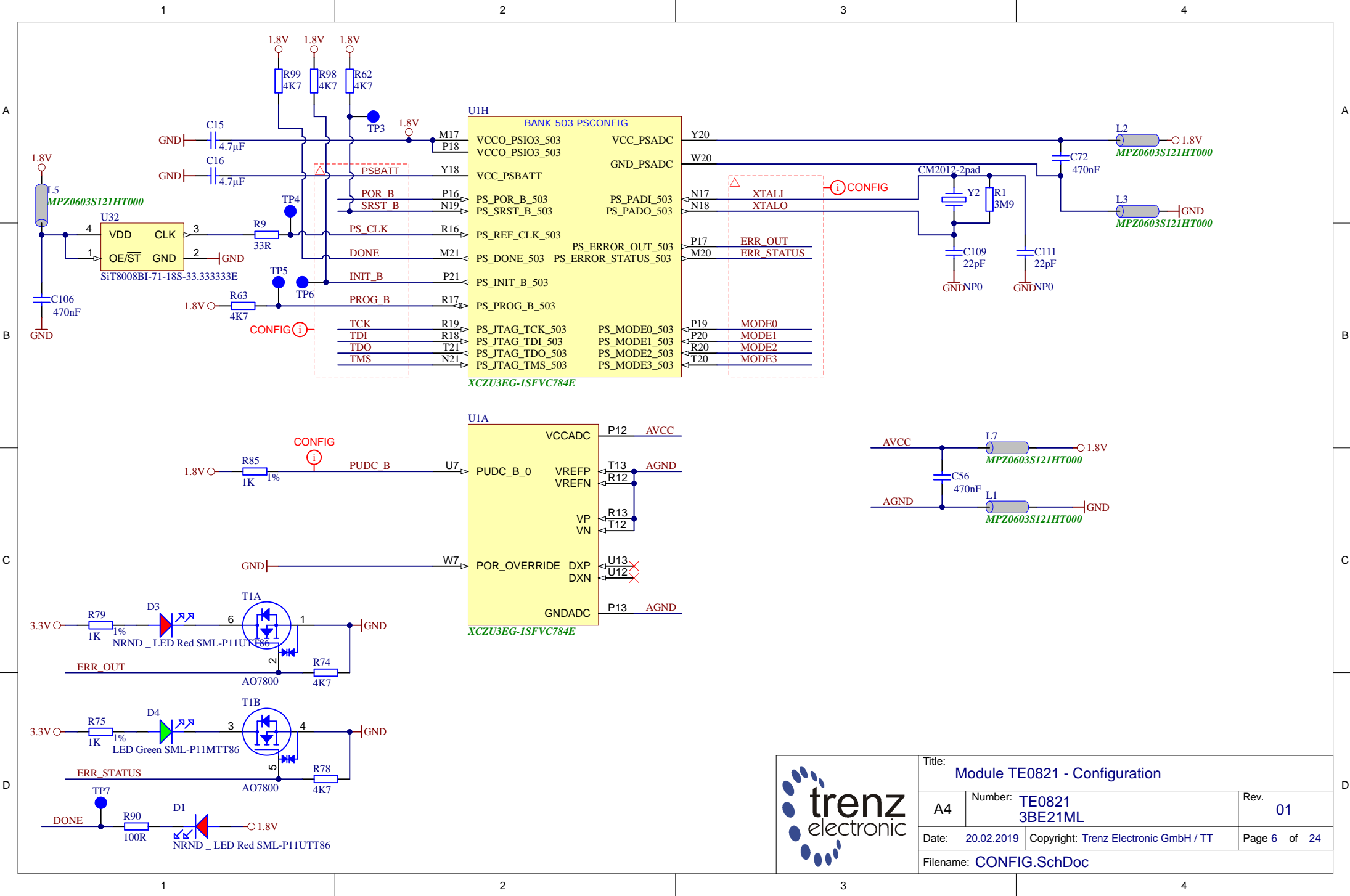
CLK

CLK

CLK

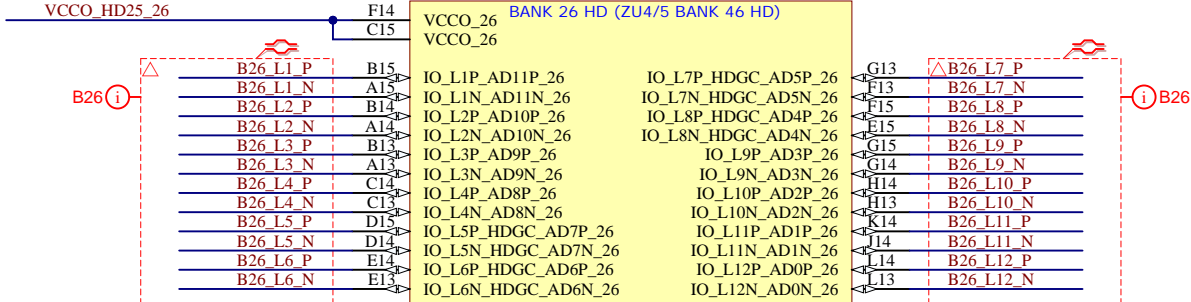


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Date: 20.02.2019	Copyright: 2015 Trenz Electronic GmbH	Page 5 of 24
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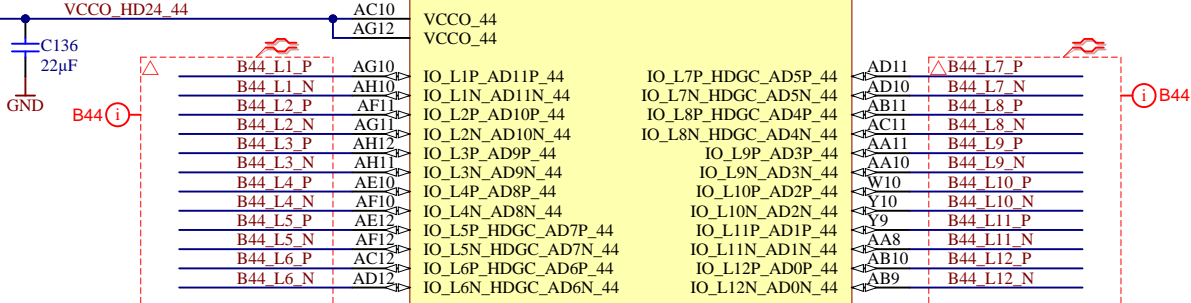


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Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>6</b> of <b>24</b>
Filename: <b>CONFIG.SchDoc</b>		

UIC

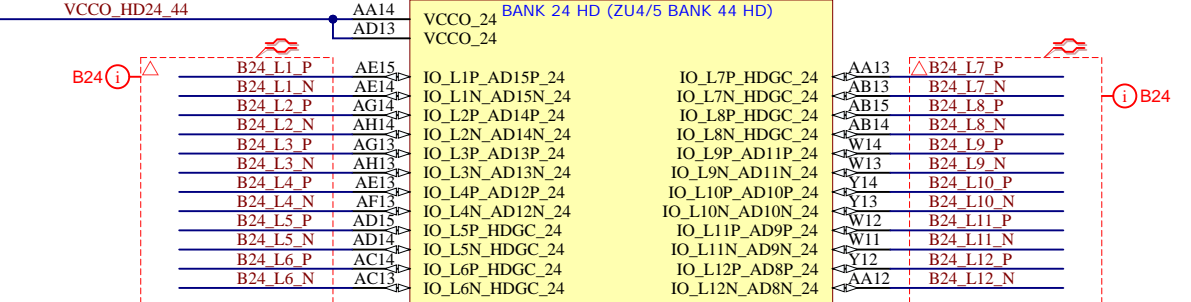


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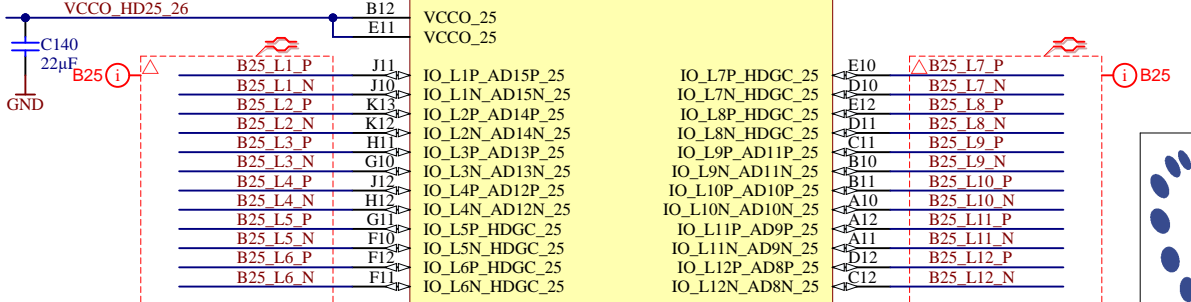


U1B XCZU3EG-1SFVC784E

BANK 24 HD (ZU4/5 BANK 44 HD)



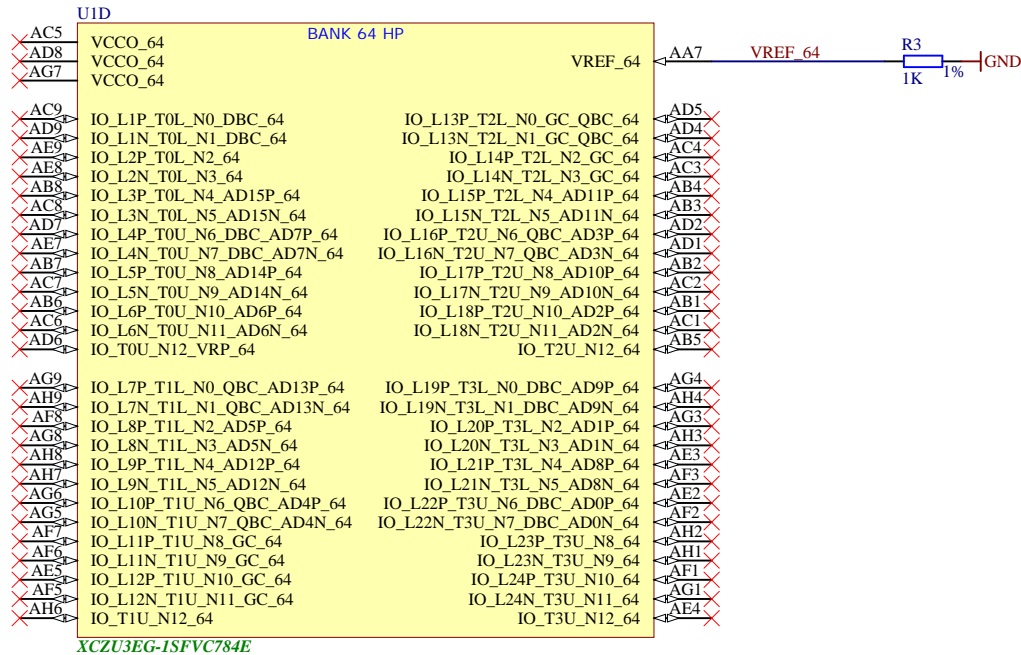

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XCZU3EG-1SFVC784E

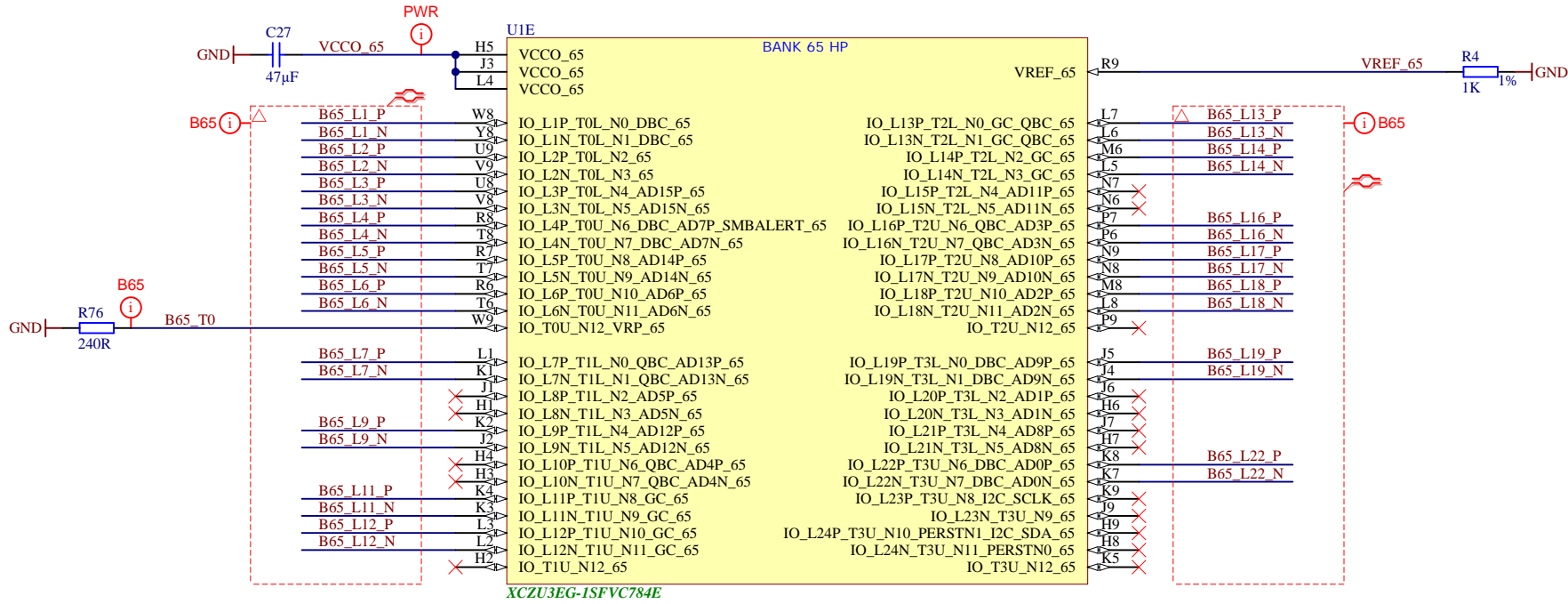


Title: <b>Module TE0821 - HD Banks</b>		
A4	Number: <b>TE0821 3BE21ML</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>7</b> of <b>24</b>
Filename: <b>B_HD.SchDoc</b>		

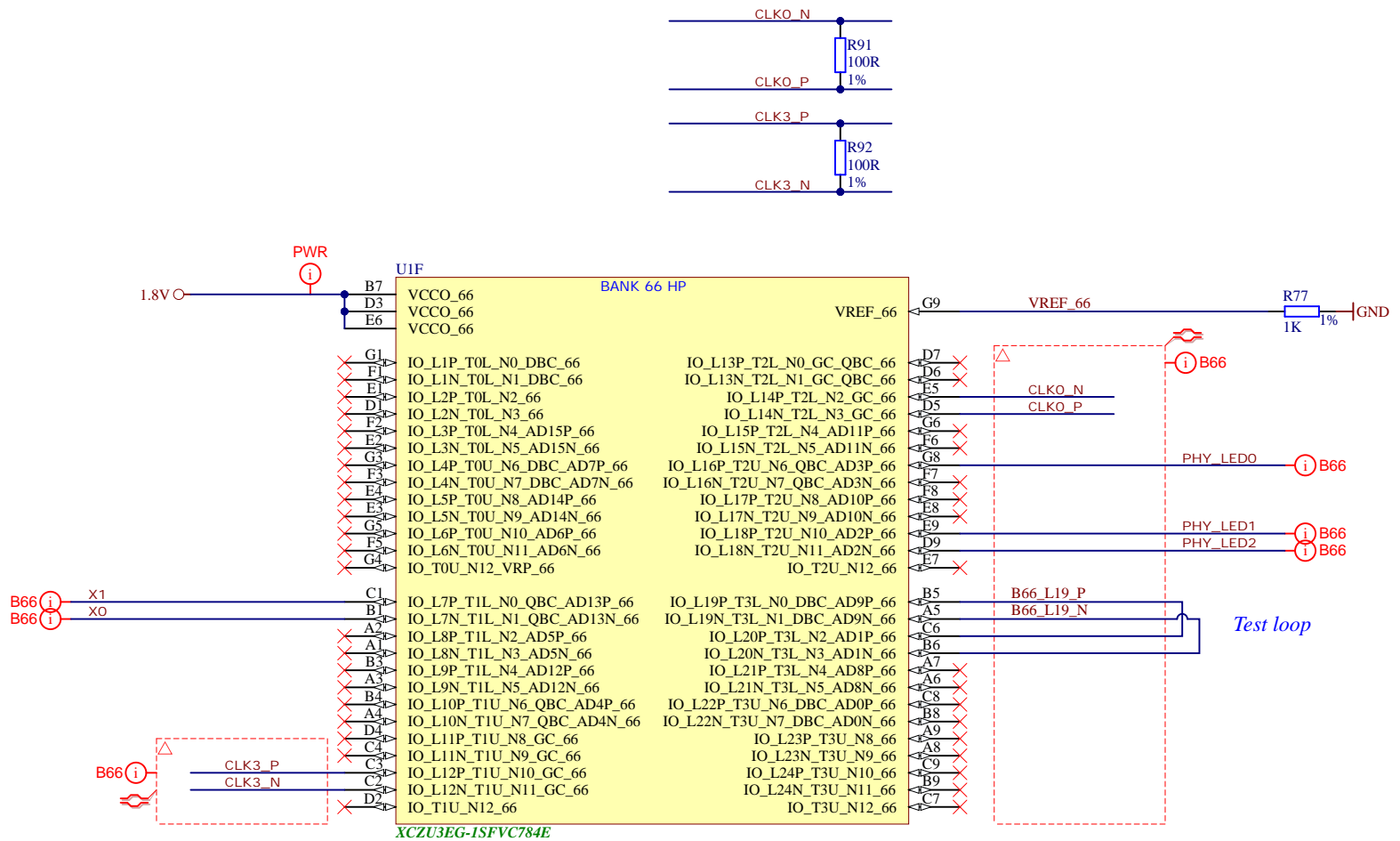



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A4	Number: <b>TE0821 3BE21ML</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>8</b> of <b>24</b>
Filename: <b>B64.SchDoc</b>		

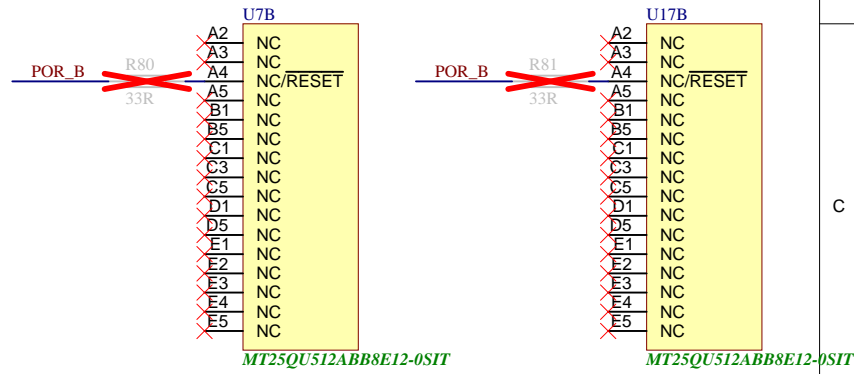
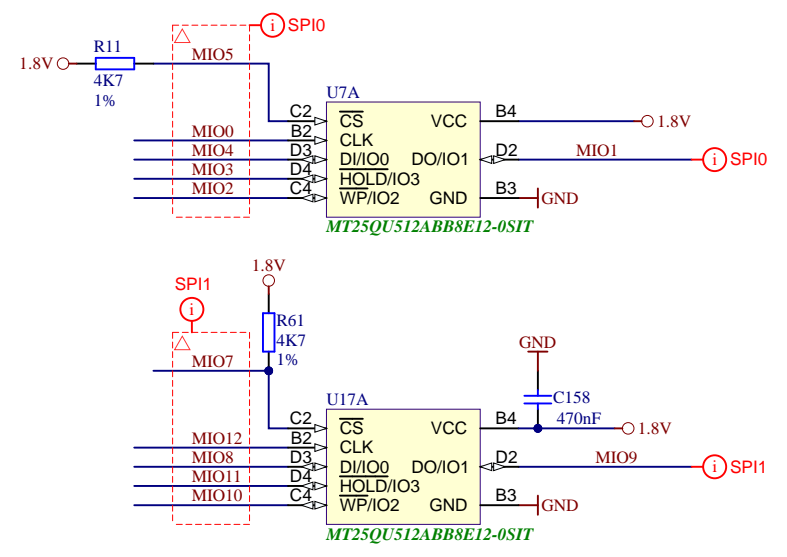
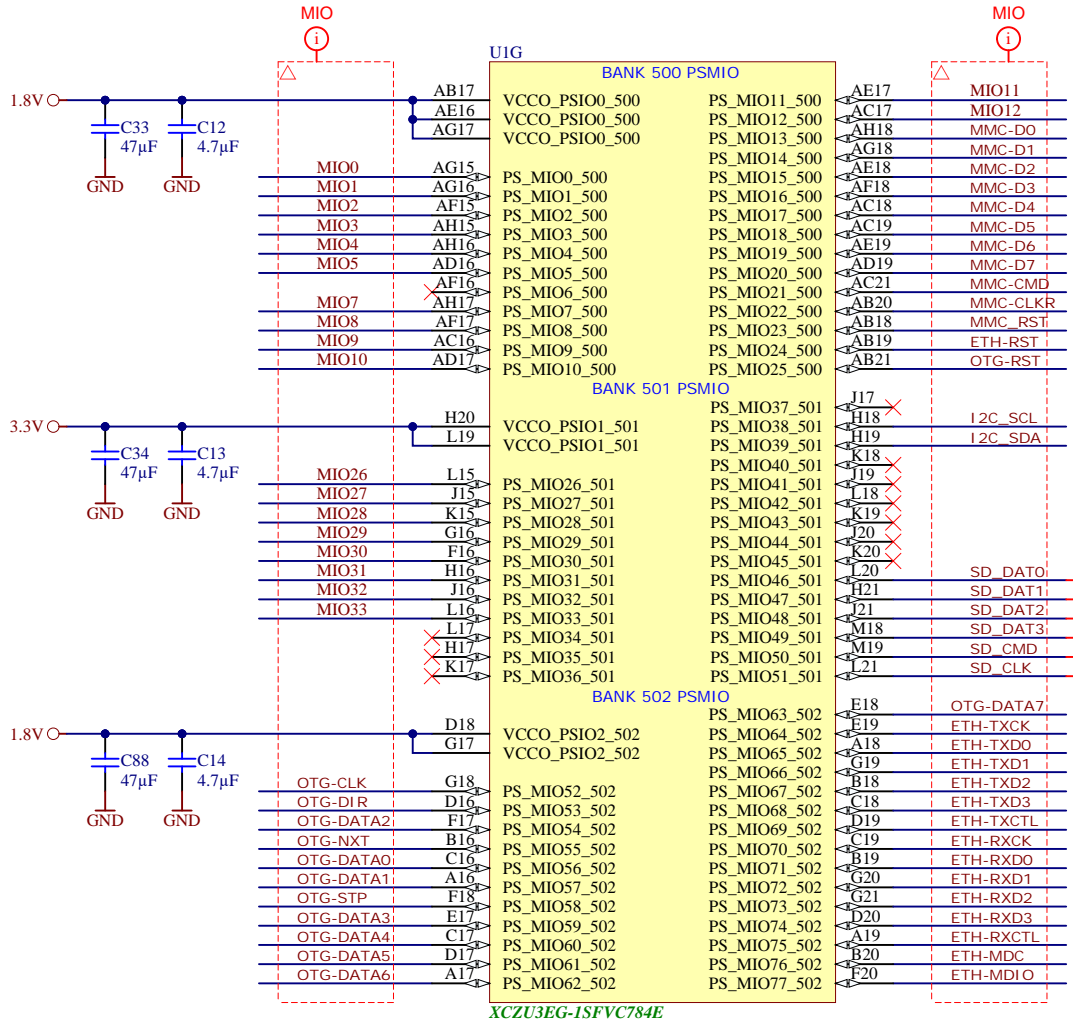





Title: <b>Module TE0821 - B65</b>		
A4	Number: <b>TE0821 3BE21ML</b>	Rev. <b>01</b>
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Filename: <b>B65.SchDoc</b>		



Title: <b>Module TE0821 - B66</b>		
A4	Number: <b>TE0821 3BE21ML</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>10</b> of <b>24</b>
Filename: <b>B66.SchDoc</b>		



				Title: <b>Module TE0821 - MIO Banks</b>	
				A4	Number: <b>TE0821 3BE21ML</b>
Date: 20.02.2019		Copyright: Trenz Electronic GmbH / TT		Page 11 of 24	
Filename: <b>B_MIO.SchDoc</b>					

A

B

C

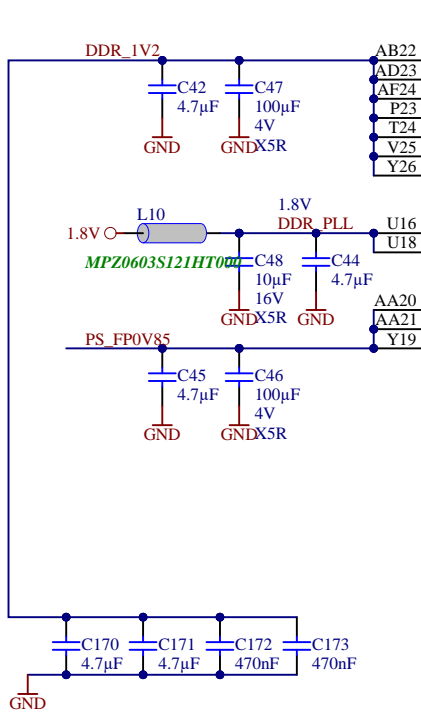
D

A

B

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U1I		BANK 504 PSDDR	
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0 P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0 N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
VCC_PSDDR_PLL	PS_DDR_A3_504	AA28	DDR4-A3
VCC_PSDDR_PLL	PS_DDR_A4_504	Y27	DDR4-A4
VCC_PSDDR_PLL	PS_DDR_A5_504	AA27	DDR4-A5
VCC_PSDDR_PLL	PS_DDR_A6_504	Y22	DDR4-A6
VCC_PSDDR_PLL	PS_DDR_A7_504	AA23	DDR4-A7
VCC_PSDDR_PLL	PS_DDR_A8_504	AA22	DDR4-A8
VCC_PSDDR_PLL	PS_DDR_A9_504	AB23	DDR4-A9
VCC_PSDDR_PLL	PS_DDR_A10_504	AA25	DDR4-A10
VCC_PSDDR_PLL	PS_DDR_A11_504	AA26	DDR4-A11
VCC_PSDDR_PLL	PS_DDR_A12_504	AB25	DDR4-A12
VCC_PSDDR_PLL	PS_DDR_A13_504	AB26	DDR4-A13
VCC_PSDDR_PLL	PS_DDR_A14_504	AB24	DDR4-A14
VCC_PSDDR_PLL	PS_DDR_A15_504	AC24	DDR4-A15
VCC_PSDDR_PLL	PS_DDR_A16_504	AC23	DDR4-A16
VCC_PSDDR_PLL	PS_DDR_A17_504	AC22	DDR4-A17
VCC_PSINTFP_DDR	PS_DDR_CS_N0_504	W27	DDR4-CS
VCC_PSINTFP_DDR	PS_DDR_CS_N1_504	V26	
VCC_PSINTFP_DDR	PS_DDR_BA0_504	V23	DDR4-BA0
VCC_PSINTFP_DDR	PS_DDR_BA1_504	W22	DDR4-BA1
VCC_PSINTFP_DDR	PS_DDR_BG0_504	W24	DDR4-BG0
VCC_PSINTFP_DDR	PS_DDR_BG1_504	V22	DDR4-BG1
VCC_PSINTFP_DDR	PS_DDR_PARITY_504	V24	DDR4-PAR
VCC_PSINTFP_DDR	PS_DDR_RAM_RST_N_504	U23	DDR4-RESET
VCC_PSINTFP_DDR	PS_DDR_ACT_N_504	Y23	DDR4-ACT
VCC_PSINTFP_DDR	PS_DDR_ALERT_N_504	U25	DDR4-ALERT
VCC_PSINTFP_DDR	PS_DDR_ZQ_504	U24	
VCC_PSINTFP_DDR	PS_DDR_ODT0_504	U28	DDR4-ODT0
VCC_PSINTFP_DDR	PS_DDR_ODT1_504	U26	

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U1J		BANK 504 PSDDR	
DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504
DQ11	AD23	PS_DDR_DQ11_504	PS_DDR_DQ43_504
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504
DDR4-DQS0 P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ64_504
DDR4-DQS0 N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ65_504
DDR4-DQS1 P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ66_504
DDR4-DQS1 N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ67_504
DDR4-DQS2 P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504
DDR4-DQS2 N	AF26	PS_DDR_DQS_N2_504	PS_DDR_DQ69_504
DDR4-DQS3 P	AE27	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504
DDR4-DQS3 N	AE27	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504
	N23	PS_DDR_DQS_P4_504	PS_DDR_DM0_504
	M23	PS_DDR_DQS_N4_504	PS_DDR_DM1_504
	L23	PS_DDR_DQS_P5_504	PS_DDR_DM2_504
	K23	PS_DDR_DQS_N5_504	PS_DDR_DM3_504
	N26	PS_DDR_DQS_P6_504	PS_DDR_DM4_504
	N27	PS_DDR_DQS_N6_504	PS_DDR_DM5_504
	J26	PS_DDR_DQS_P7_504	PS_DDR_DM6_504
	J27	PS_DDR_DQS_N7_504	PS_DDR_DM7_504
	R27	PS_DDR_DQS_P8_504	PS_DDR_DM8_504
	T27	PS_DDR_DQS_N8_504	

XCZU3EG-1SFVC784E



Title: <b>Module TE0821 - PS DDR</b>		
A4	Number: <b>TE0821 3BE21ML</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>12</b> of <b>24</b>
Filename: <b>PS_DDR.SchDoc</b>		

1

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A

A

B

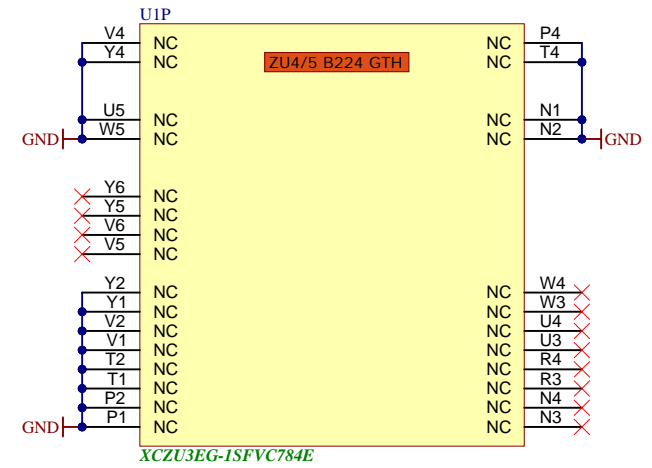
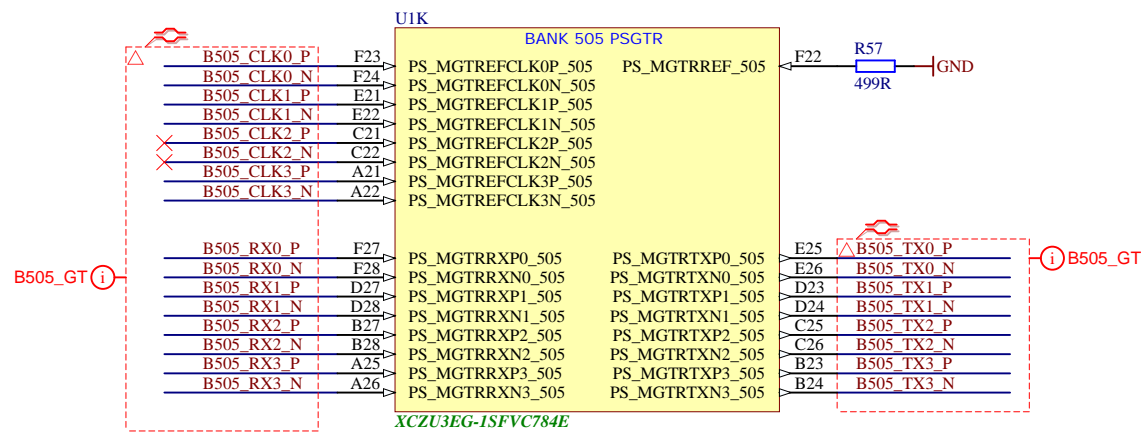
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C

C

D

D



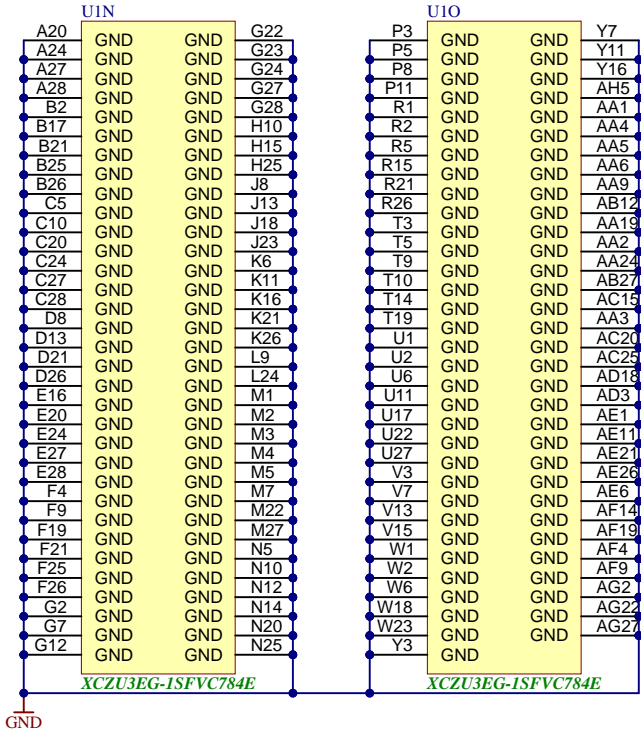
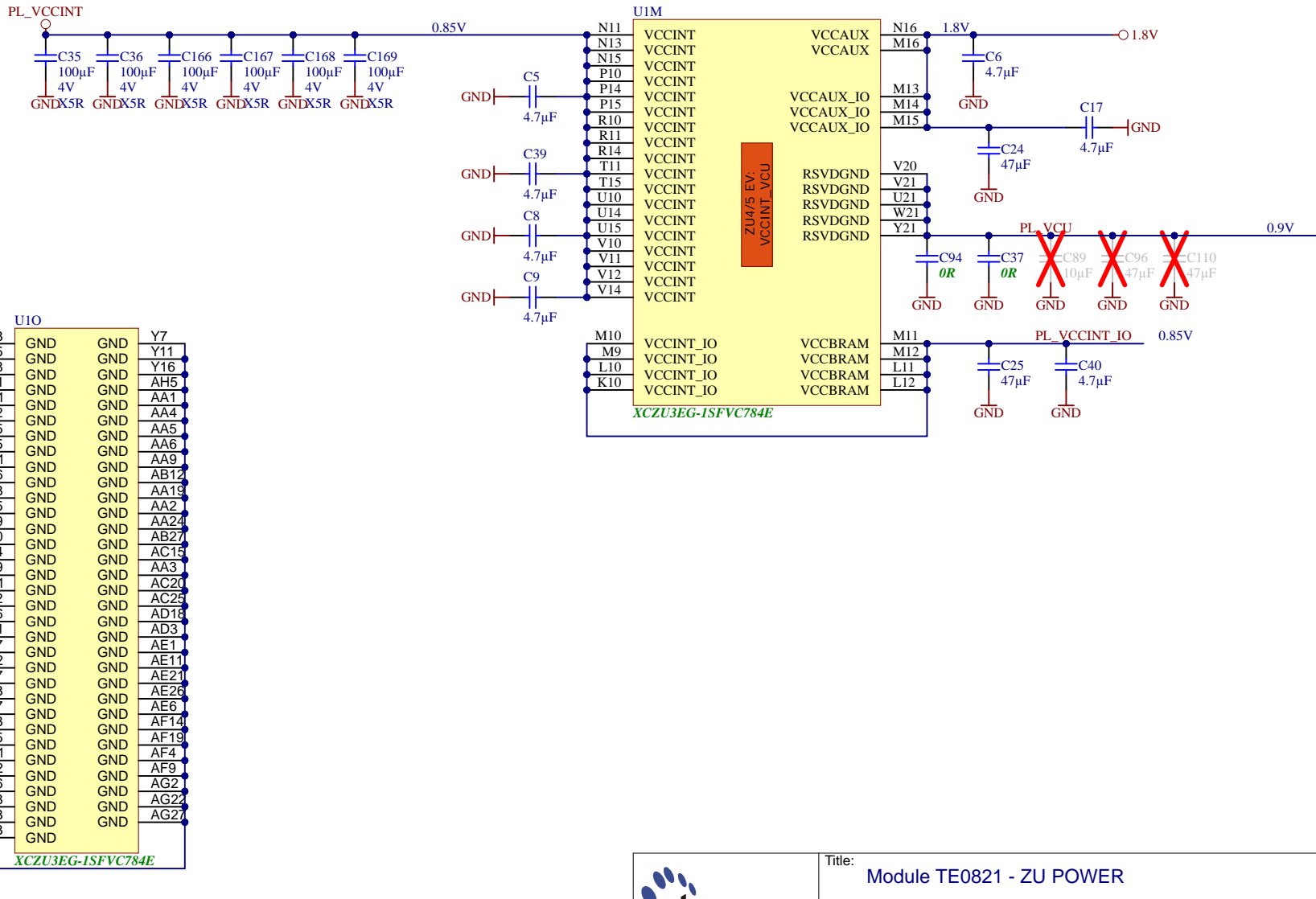
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	Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>13</b> of <b>24</b>
	Filename: <b>B_PS_GT.SchDoc</b>		


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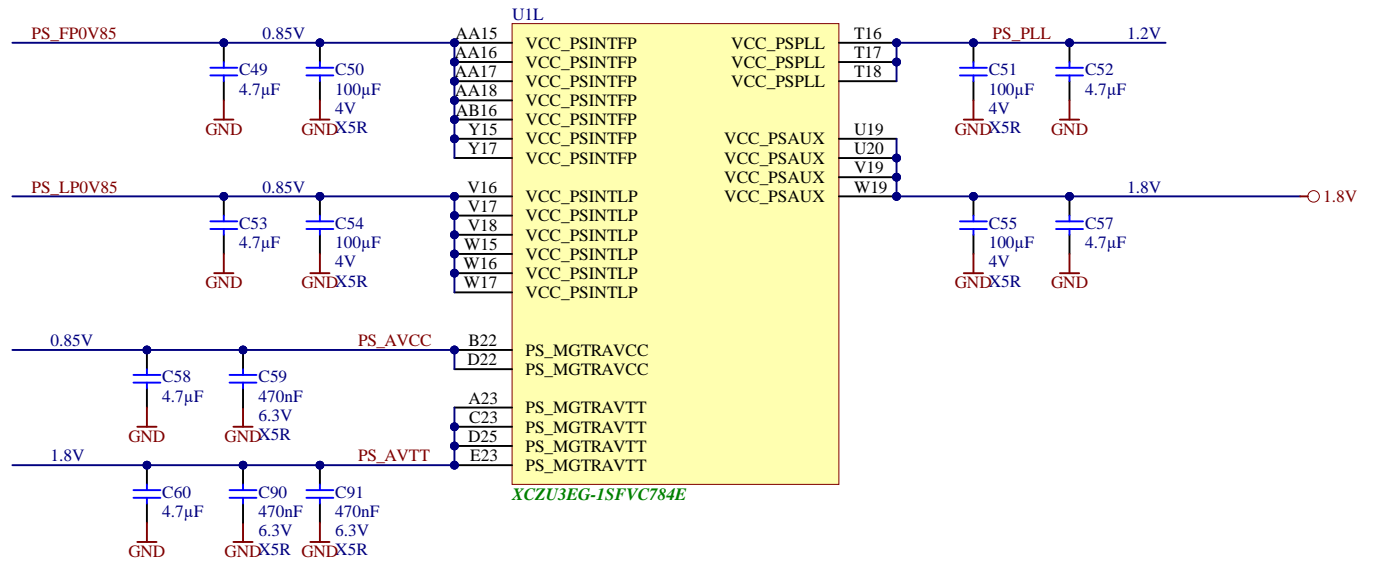
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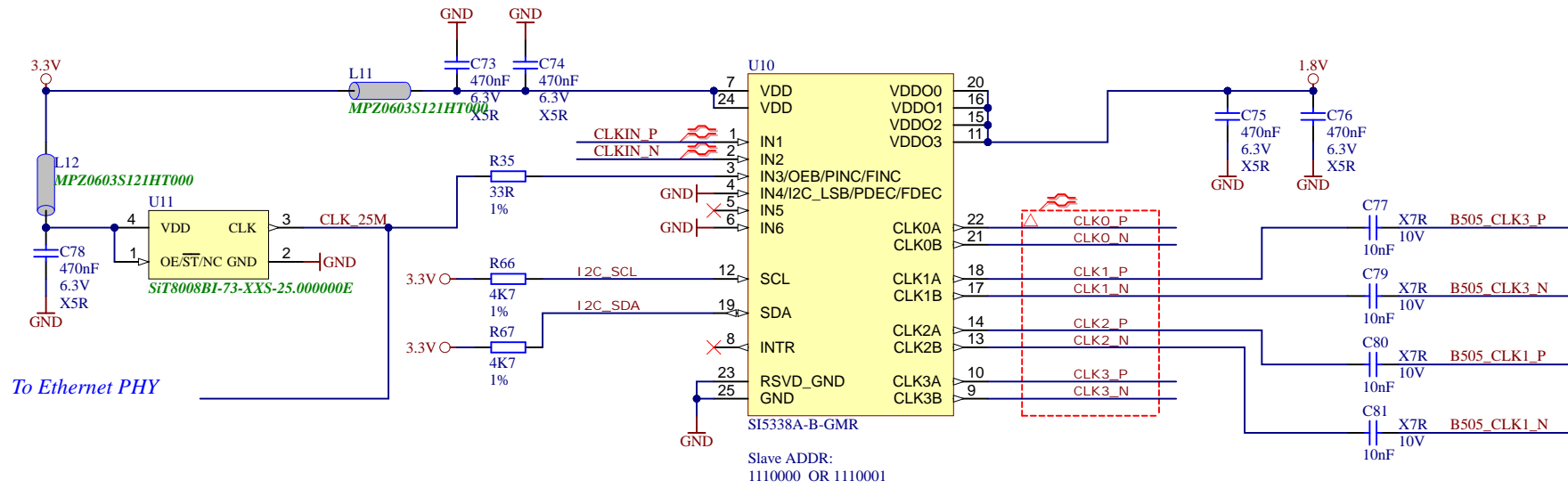
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		A4 Number: <b>TE0821 3BE21ML</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>		Copyright: <b>Trenz Electronic GmbH / TT</b>	
Filename: <b>ZU_POWER.SchDoc</b>			




	Title: <b>Module TE0821 - ZU PS POWER</b>		
	A4	Number: <b>TE0821 3BE21ML</b>	Rev. <b>01</b>
	Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>15</b> of <b>24</b>
	Filename: <b>ZU_PS_POWER.SchDoc</b>		

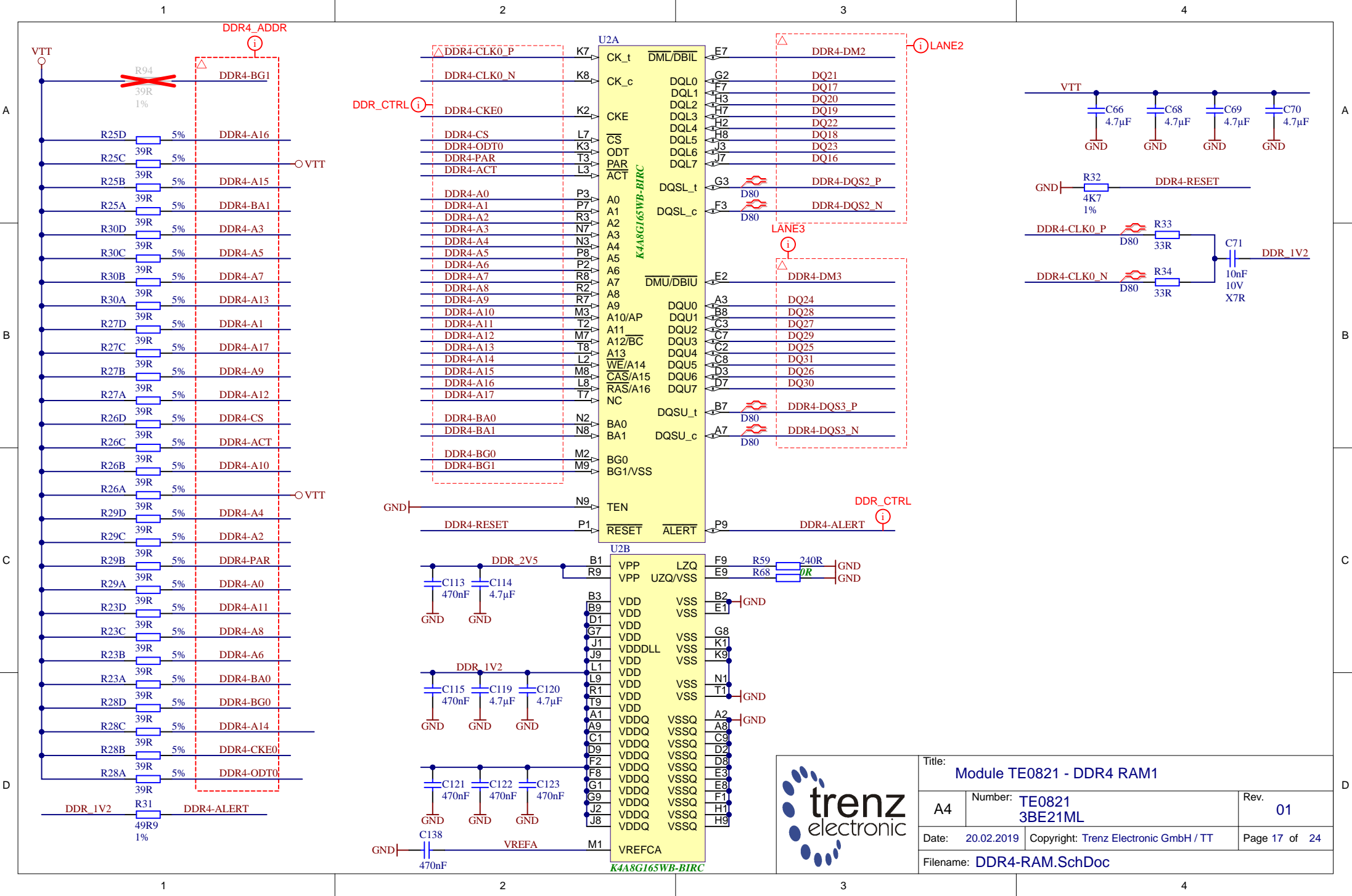


To Ethernet PHY

Slave ADDR:  
1110000 OR 1110001

		Title: Module TE0821 - CLK	
		A4	Number: TE0821 3BE21ML
Date: 20.02.2019		Copyright: 2015 Trenz Electronic GmbH	
Filename: CLK.SchDoc		Page 16 of 24	





Title: <b>Module TE0821 - DDR4 RAM1</b>		
A4	Number: <b>TE0821 3BE21ML</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>17</b> of <b>24</b>
Filename: <b>DDR4-RAM.SchDoc</b>		



A

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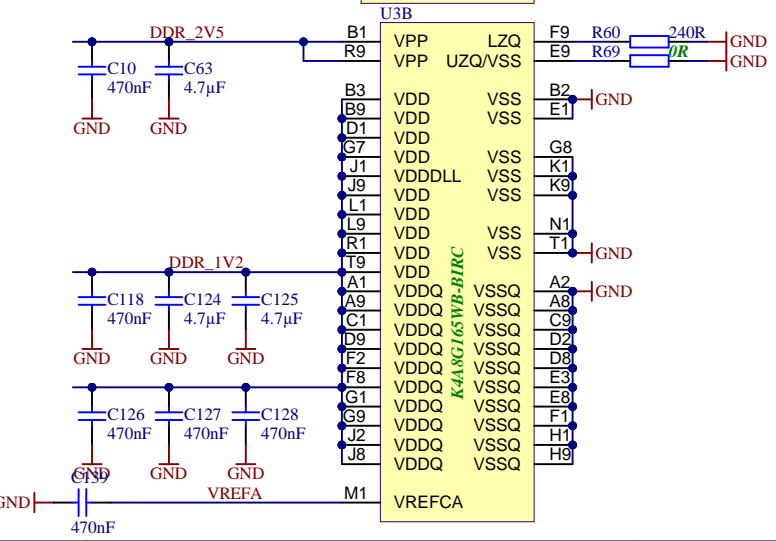
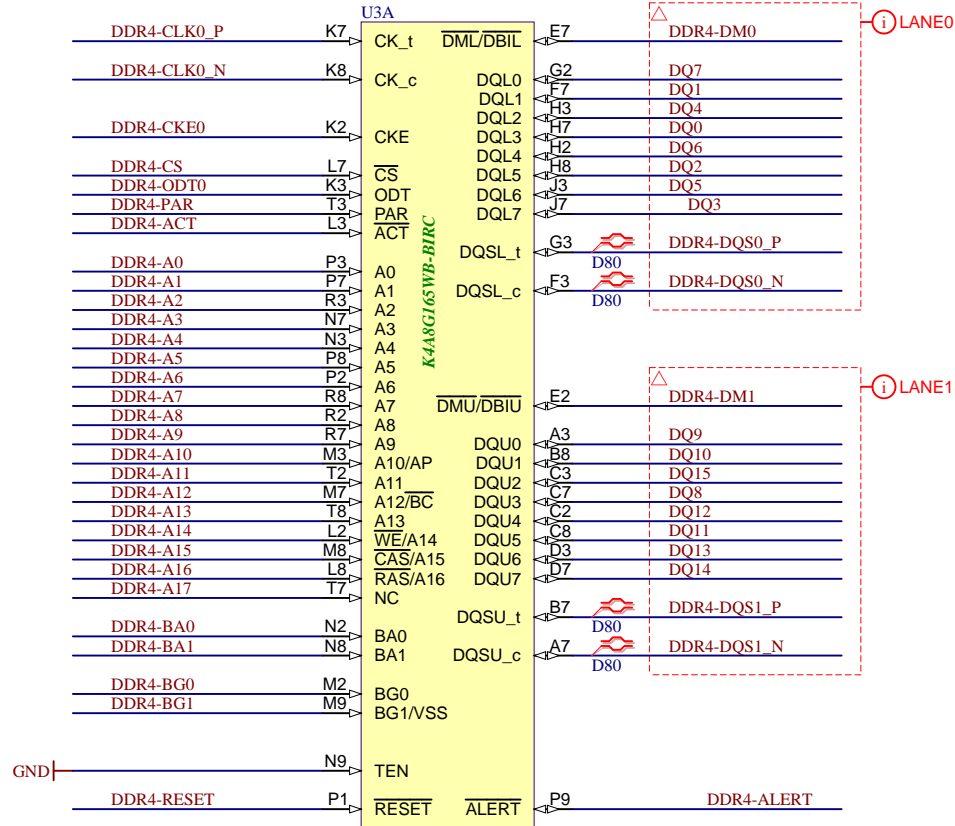
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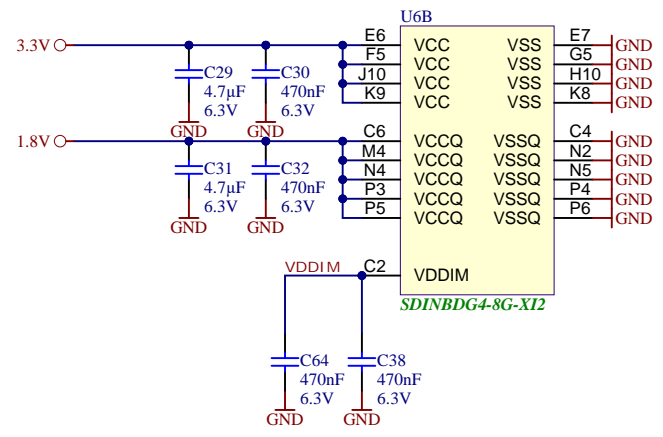
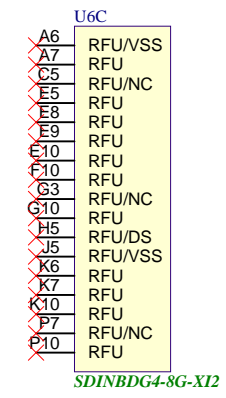
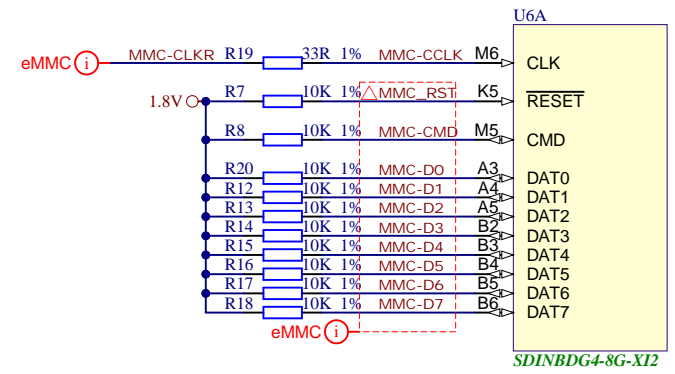
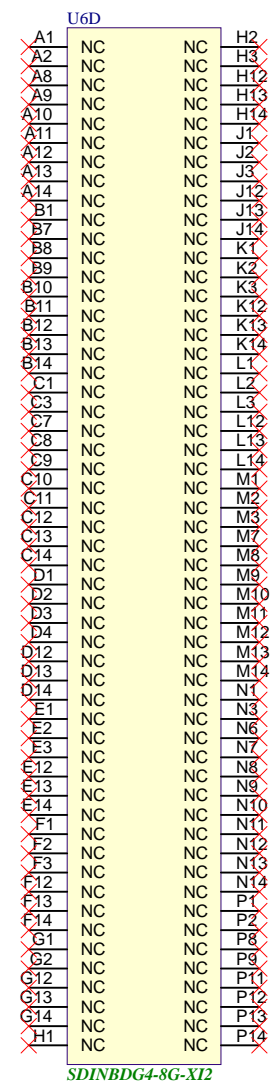

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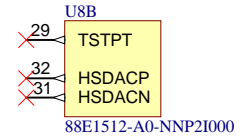
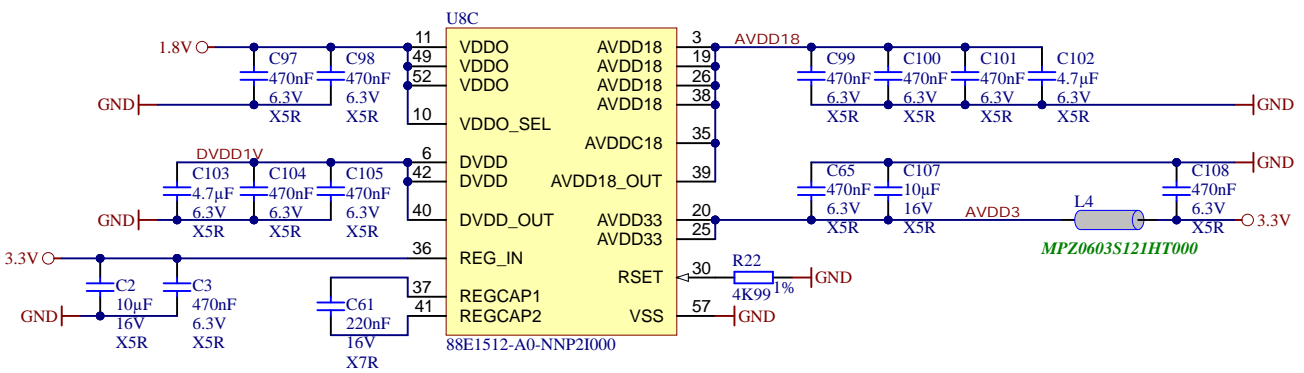
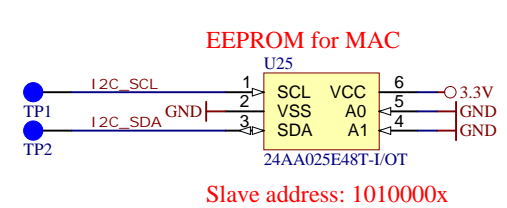
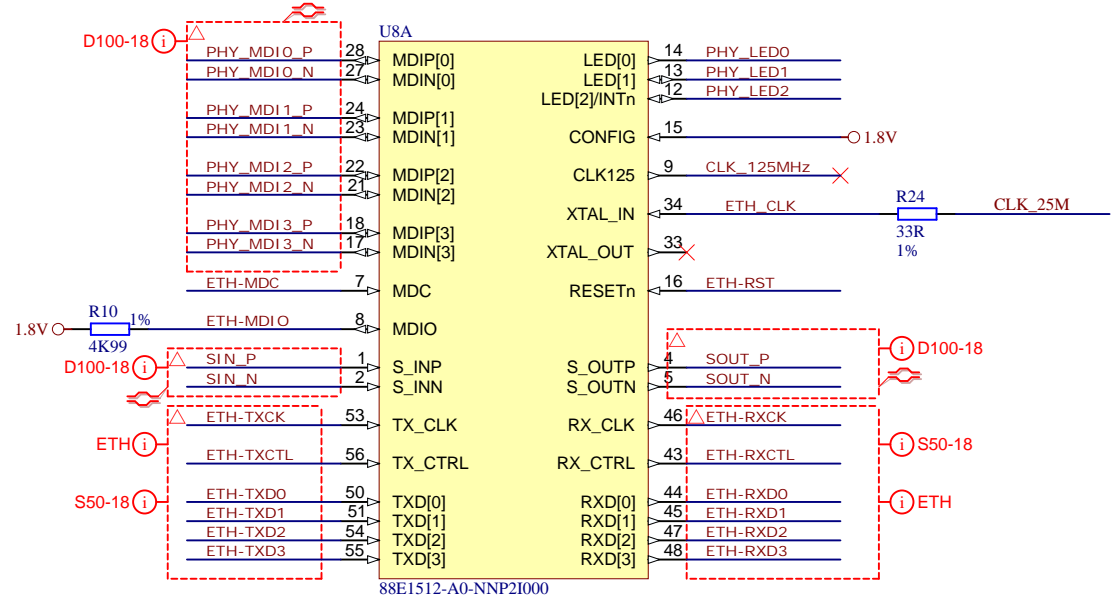
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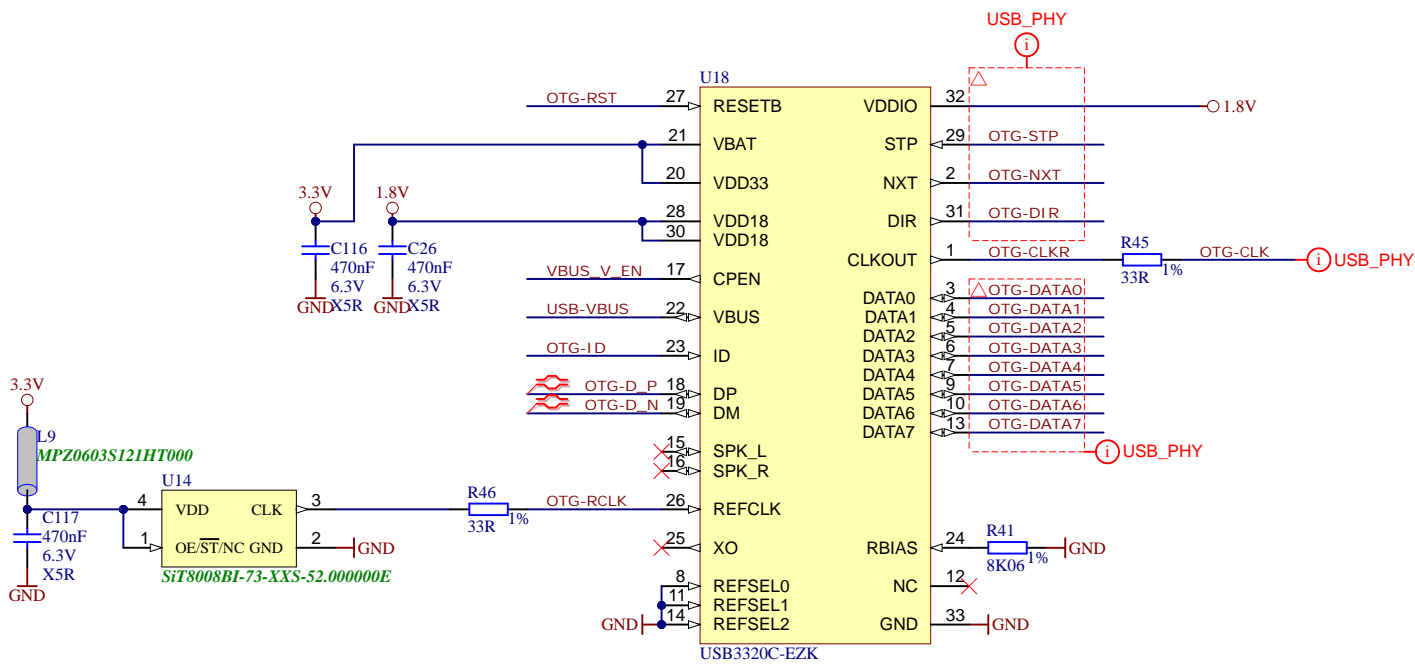
Title: Module TE0821 - DDR4 RAM2		
A4	Number: TE0821 3BE21ML	Rev. 01
Date: 20.02.2019	Copyright: Trenz Electronic GmbH / TT	Page 18 of 24
Filename: DDR4-RAM_2.SchDoc		





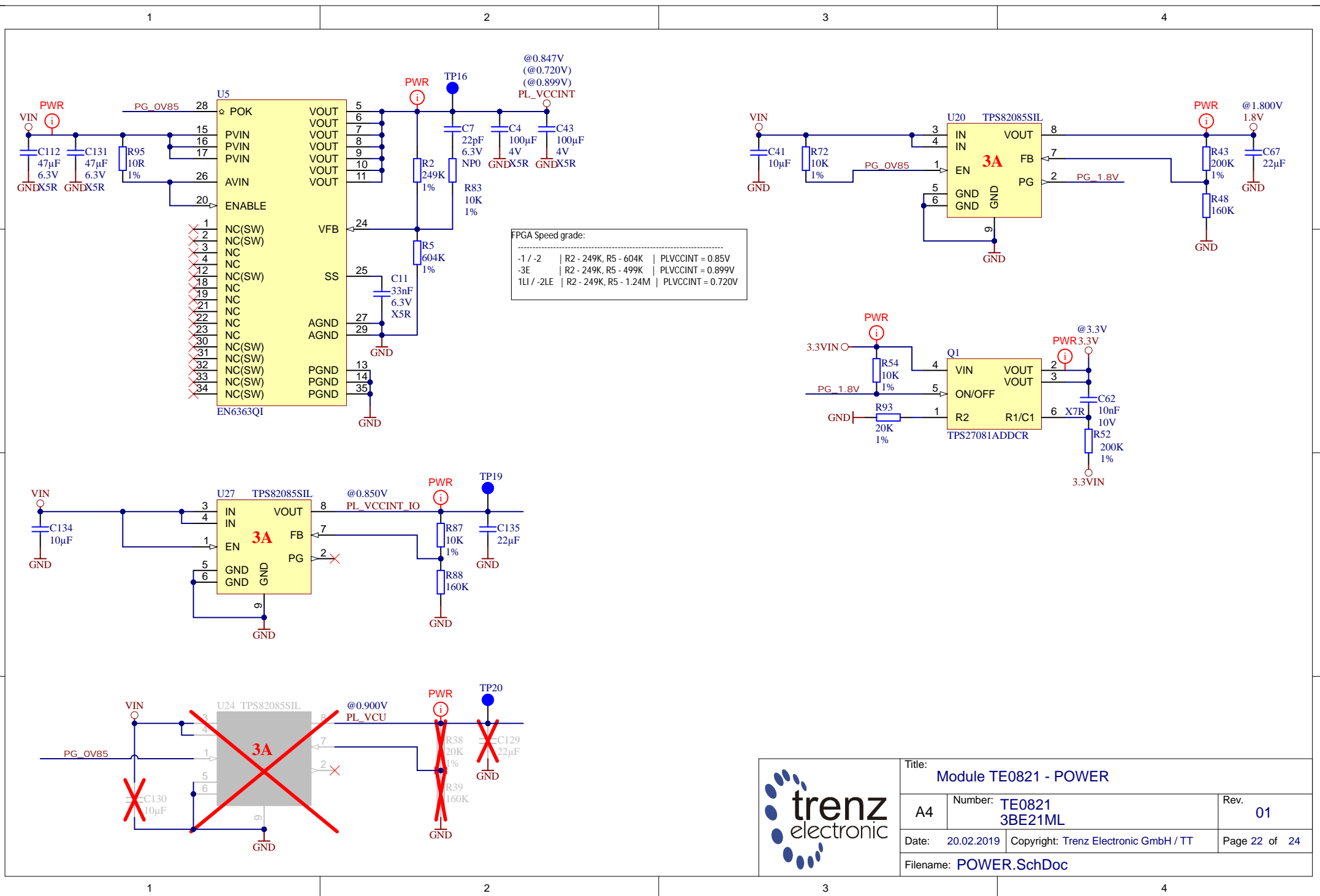

Title: <b>Module TE0821 - eMMC</b>		
A4	Number: <b>TE0821 3BE21ML</b>	Rev. <b>01</b>
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Filename: <b>eMMC.SchDoc</b>		



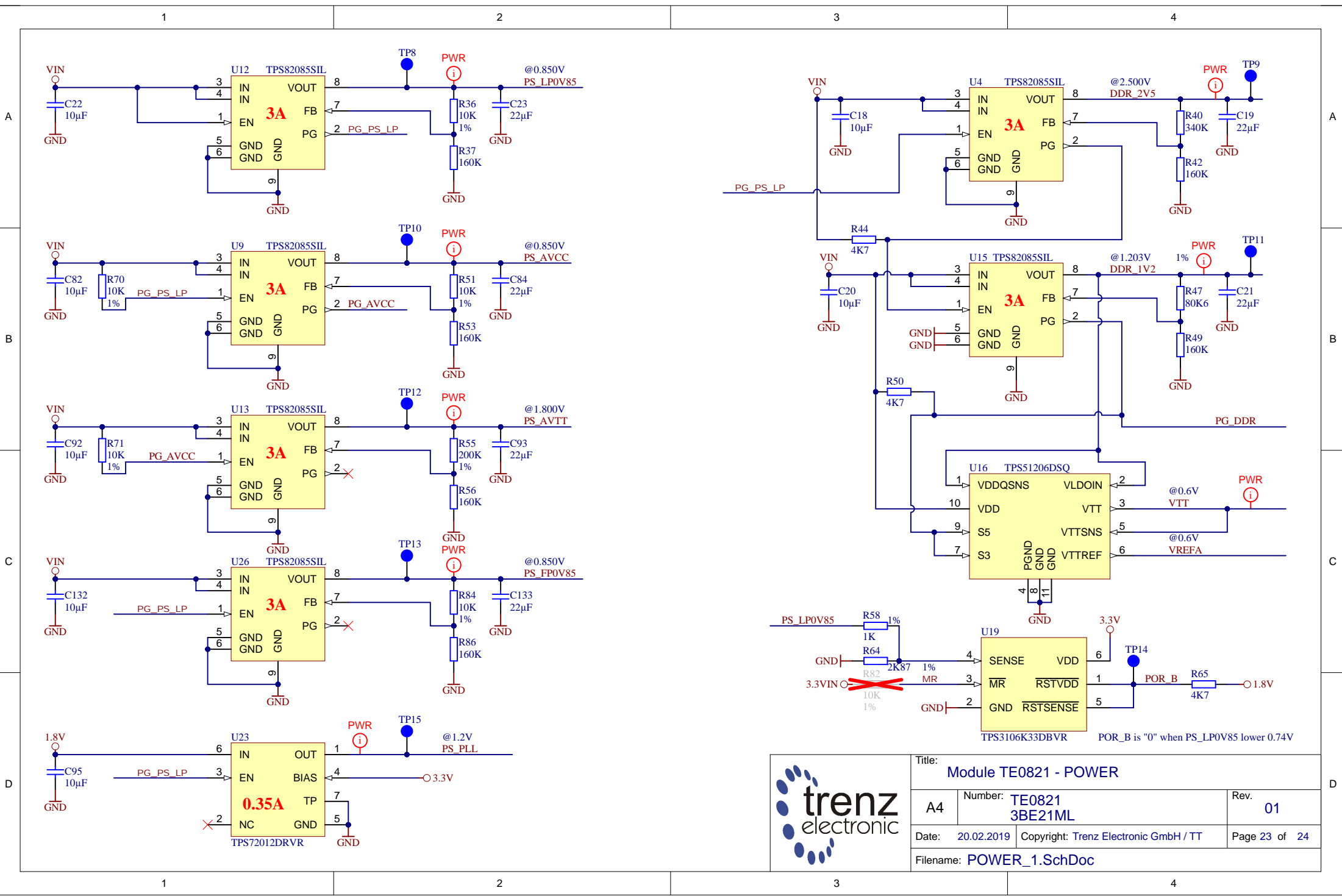
Title: <b>Module TE0821 - Ethernet PHY</b>		
A4	Number: <b>TE0821 3BE21ML</b>	Rev. <b>01</b>
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	Title: <b>Module TE0821 - USB PHY</b>		
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Title: <b>Module TE0821 - POWER</b>		
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Title: <b>Module TE0821 - POWER</b>		
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Revision 01a (01.07.2020):

1. VY: R38 value was changed to 20K (was: 40K2) to set VCU 0.9V

Revision 01b (29.10.2020):

1. VY: Updated Block diagram

(07.02.2024):  
2. OT: R82 set to not fitted

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A

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B

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C

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D

	Title: <b>Module TE0821 - Revision Changes</b>		
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	Filename: <b>Revision Changes.SchDoc</b>		

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