


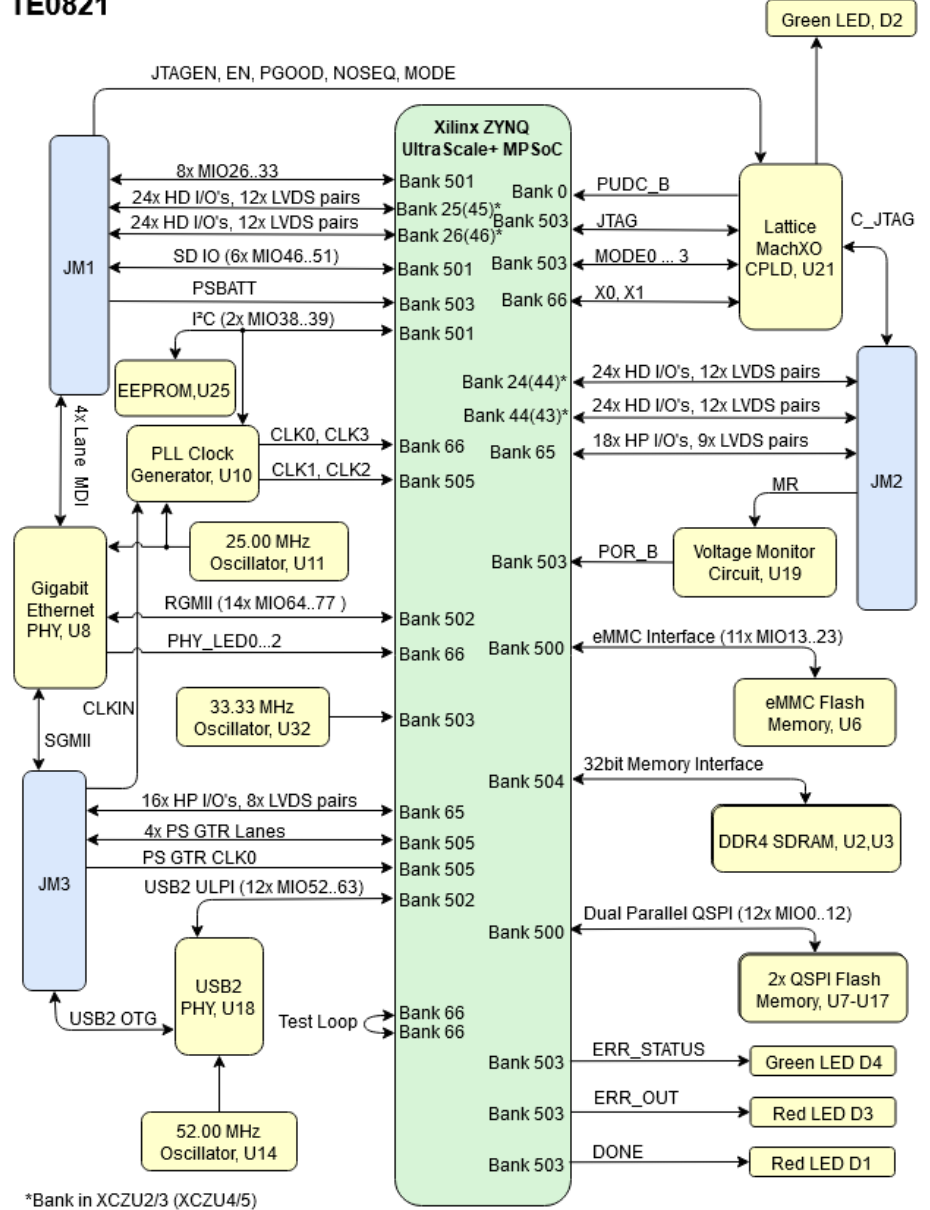
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Schematics and other handouts serve for informational purposes only!

	Title: <b>Module TE0821</b>		
	A4	Number: <b>TE0821 4DE31FL</b>	Rev. <b>01</b>
	Date: <b>14.08.2020</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>1</b> of <b>24</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		

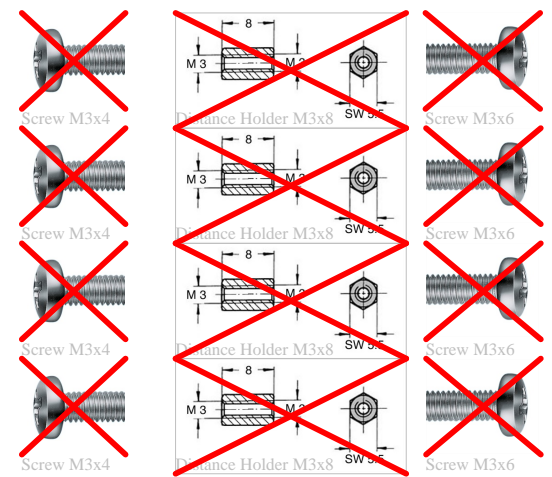
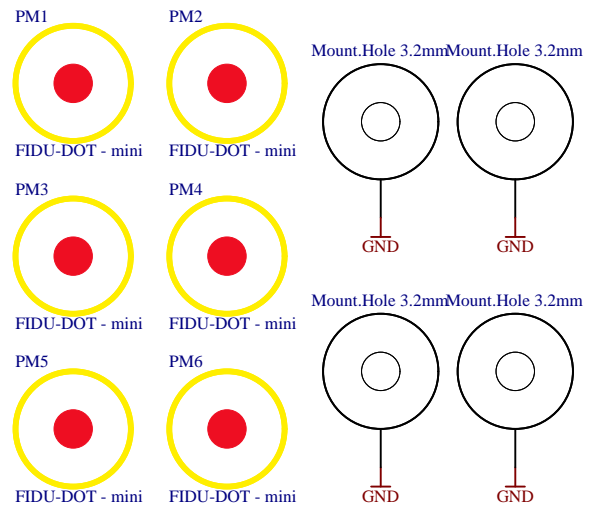
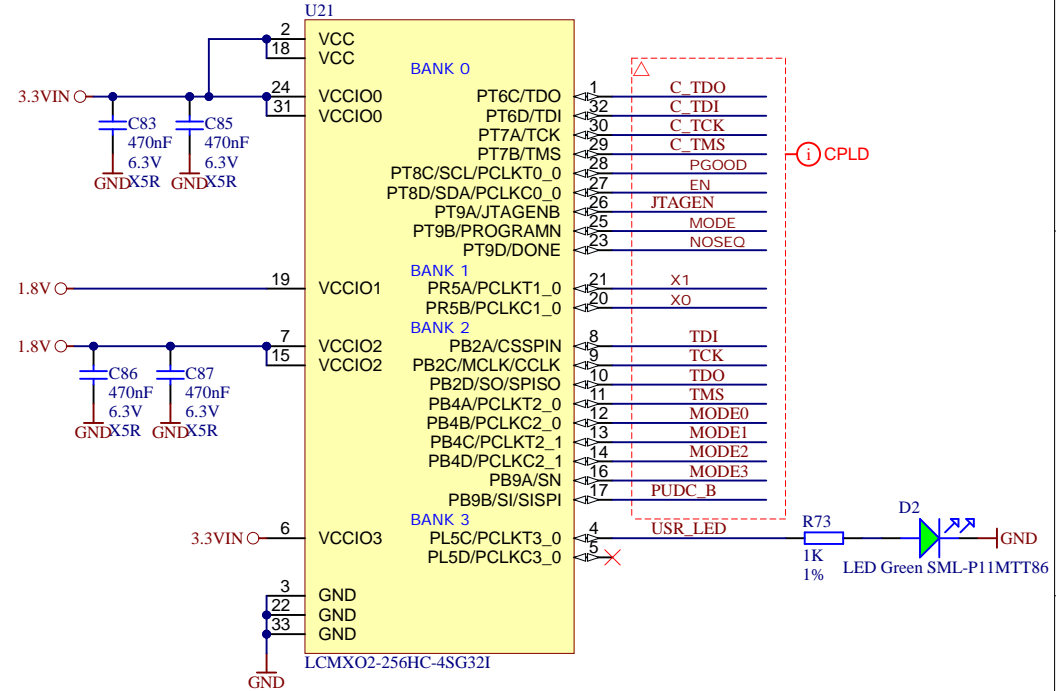
**TE0821**



		Title: <b>Module TE0821 - System Overview</b>	
		A4	Number: <b>TE0821 4DE31FL</b>
Date: 18.01.2022		Copyright: 2015 Trenz Electronic GmbH	
Filename: <b>TE0821-Overview.SchDoc</b>		Page 2 of 24	

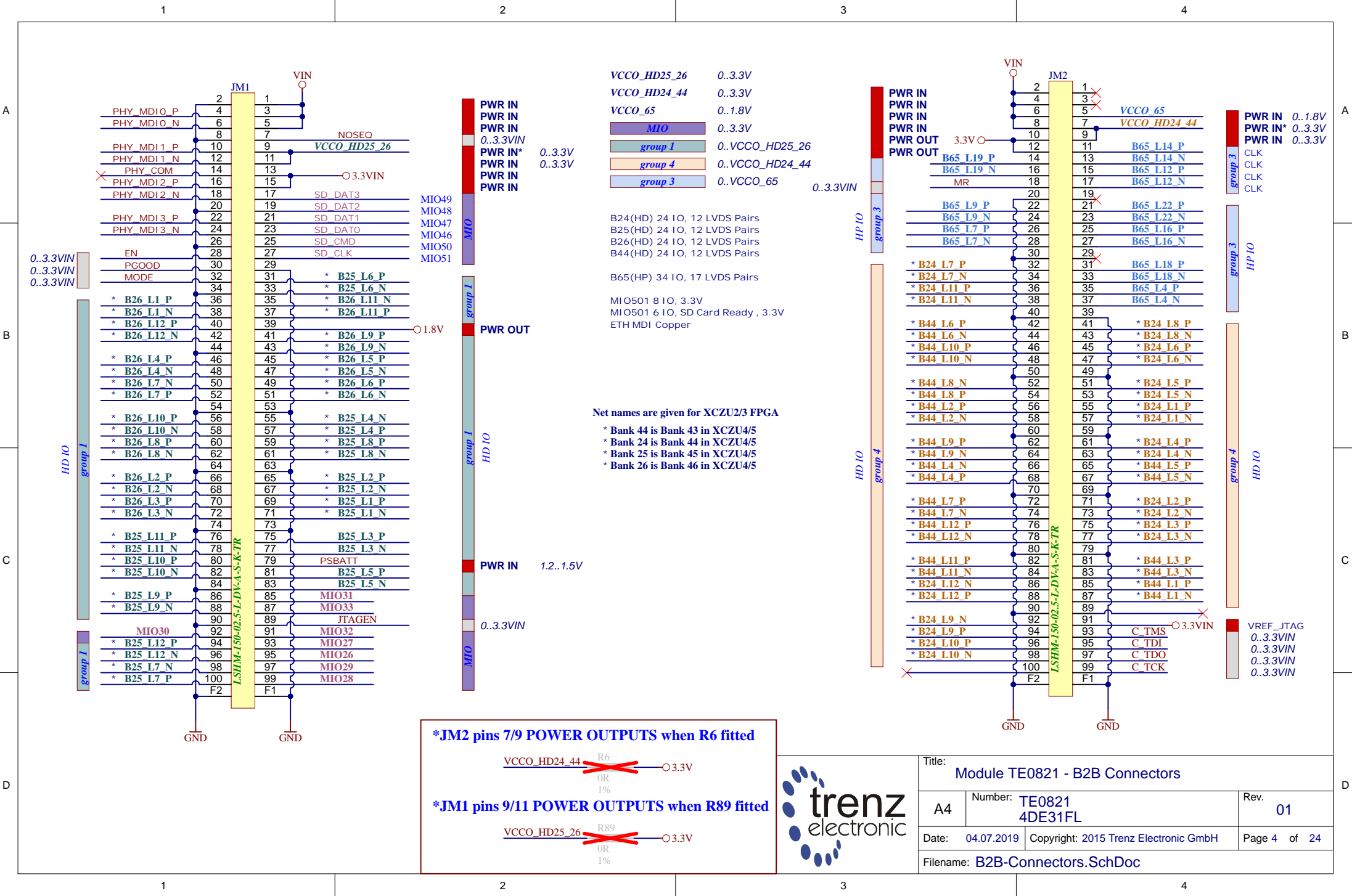
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U_ETH-PHY ETH-PHY.SchDoc
U_B_HD B_HD.SchDoc
U_B64 B64.SchDoc
U_B65 B65.SchDoc
U_B66 B66.SchDoc
U_CONFIG CONFIG.SchDoc
U_B_MIO B_MIO.SchDoc
U_B_PS_GT B_PS_GT.SchDoc
U_CLK CLK.SchDoc
U_Overview TE0821-Overview.SchDoc
U_LN Legal Notices Modules.SchDoc

U_B2B-Connectors B2B-Connectors.SchDoc
U_B2B-Connectors_2 B2B-Connectors_2.SchDoc
U_eMMC eMMC.SchDoc
U_PS_DDR PS_DDR.SchDoc
U_ZU_POWER ZU_POWER.SchDoc
U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_DDR4-RAM_2 DDR4-RAM_2.SchDoc
U_DDR4-RAM DDR4-RAM.SchDoc
U_POWER POWER.SchDoc
U_POWER_1 POWER_1.SchDoc
U_Revision_changes Revision Changes.SchDoc



Special notes:  
Component RC0201FR-0710KL removed

	Title: <b>Module TE0821</b>		
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**\*JM2 pins 7/9 POWER OUTPUTS when R6 fitted**

VCCO\_HD24\_44 ~~R6~~ 0.3.3V  
OR  
1%

**\*JM1 pins 9/11 POWER OUTPUTS when R89 fitted**

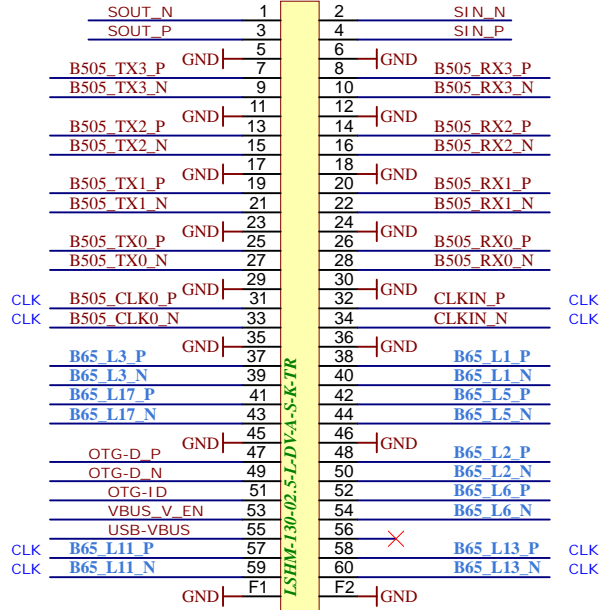
VCCO\_HD25\_26 ~~R89~~ 0.3.3V  
OR  
1%



Title: Module TE0821 - B2B Connectors			
A4	Number: TE0821 4DE31FL	Rev. 01	
Date: 04.07.2019	Copyright: 2015 Trenz Electronic GmbH	Page 4 of 24	
Filename: B2B-Connectors.SchDoc			

USB OTG  
 ETH SGMII  
 PS\_GTR 4 Lanes  
 PS\_GTR CLK IN  
 PLL CLK IN

JM3



X

HP IO

group 3

USB

HP IO

CLK

CLK

CLK

CLK

CLK

CLK

CLK

CLK

CLK

CLK

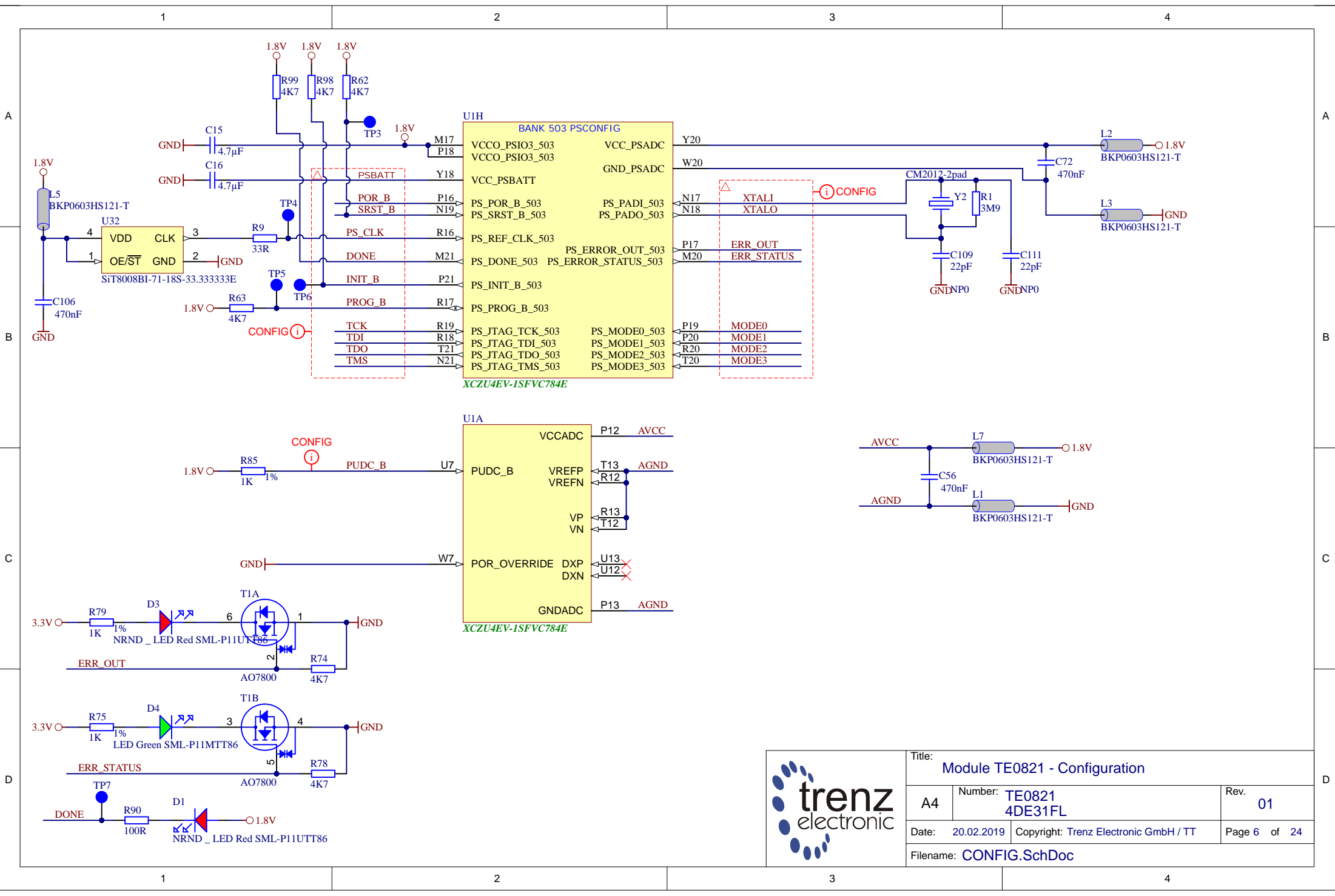
CLK

CLK

CLK

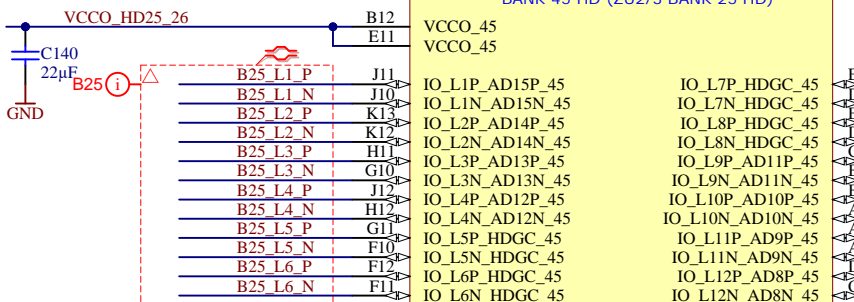
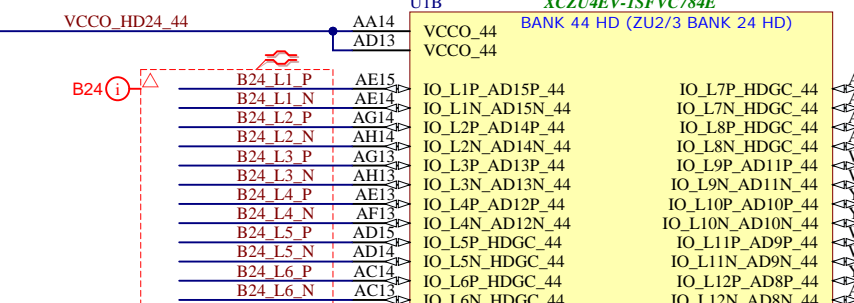
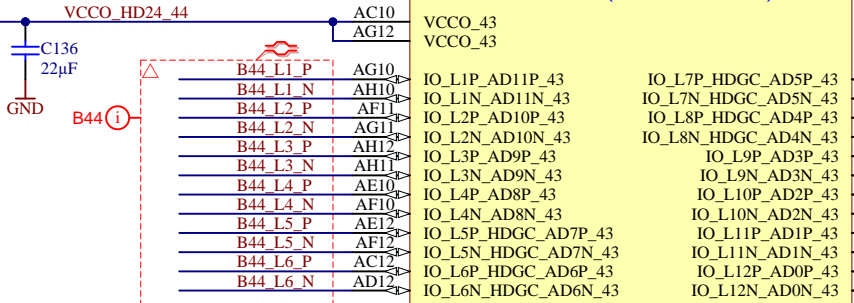
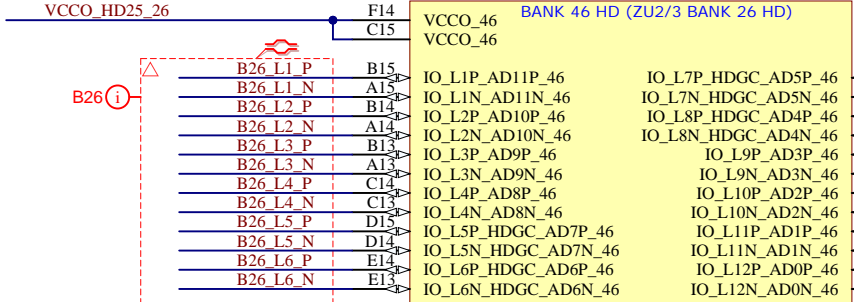
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	Title: Module TE0821 - B2B Connectors		
	A4	Number: TE0821 4DE31FL	Rev. 01
	Date: 20.02.2019	Copyright: 2015 Trenz Electronic GmbH	Page 5 of 24
	Filename: B2B-Connectors_2.SchDoc		



Title: Module TE0821 - Configuration		
A4	Number: TE0821 4DE31FL	Rev. 01
Date: 20.02.2019	Copyright: Trenz Electronic GmbH / TT	Page 6 of 24
Filename: CONFIG.SchDoc		

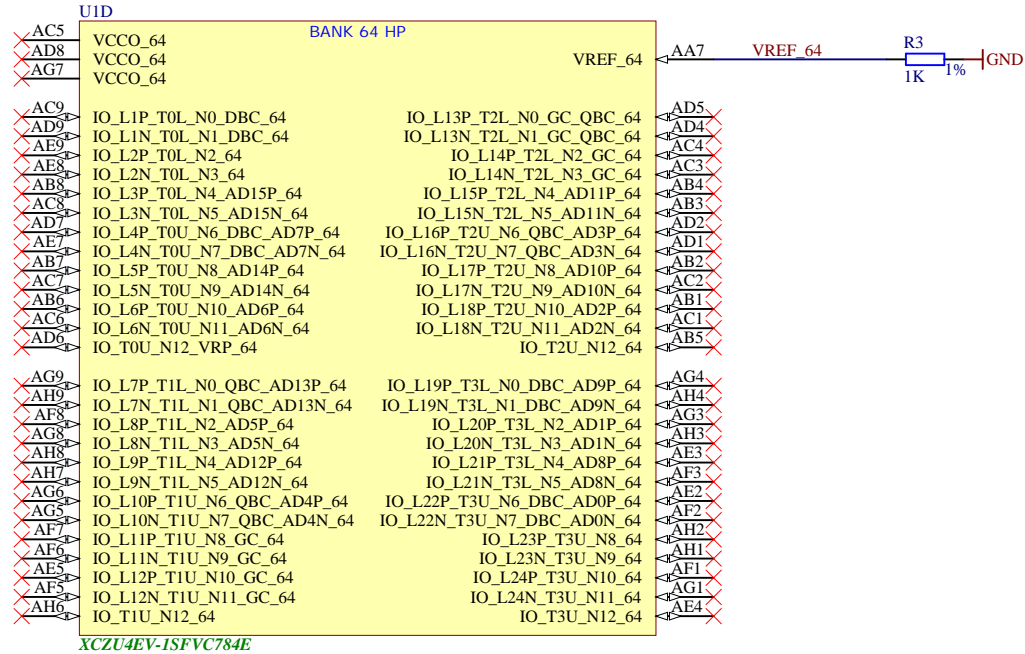

UIC



XCZU4EV-1SFVC784E

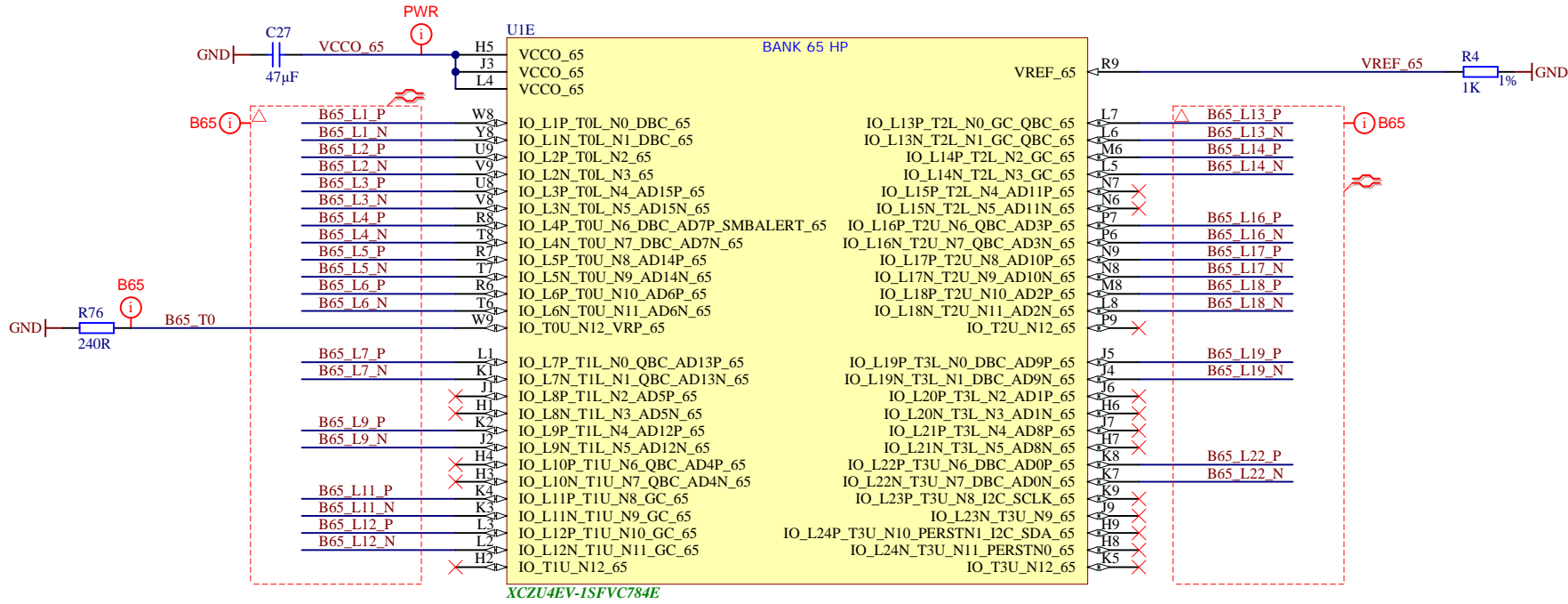


Title: <b>Module TE0821 - HD Banks</b>		
A4	Number: <b>TE0821 4DE31FL</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>7</b> of <b>24</b>
Filename: <b>B_HD.SchDoc</b>		

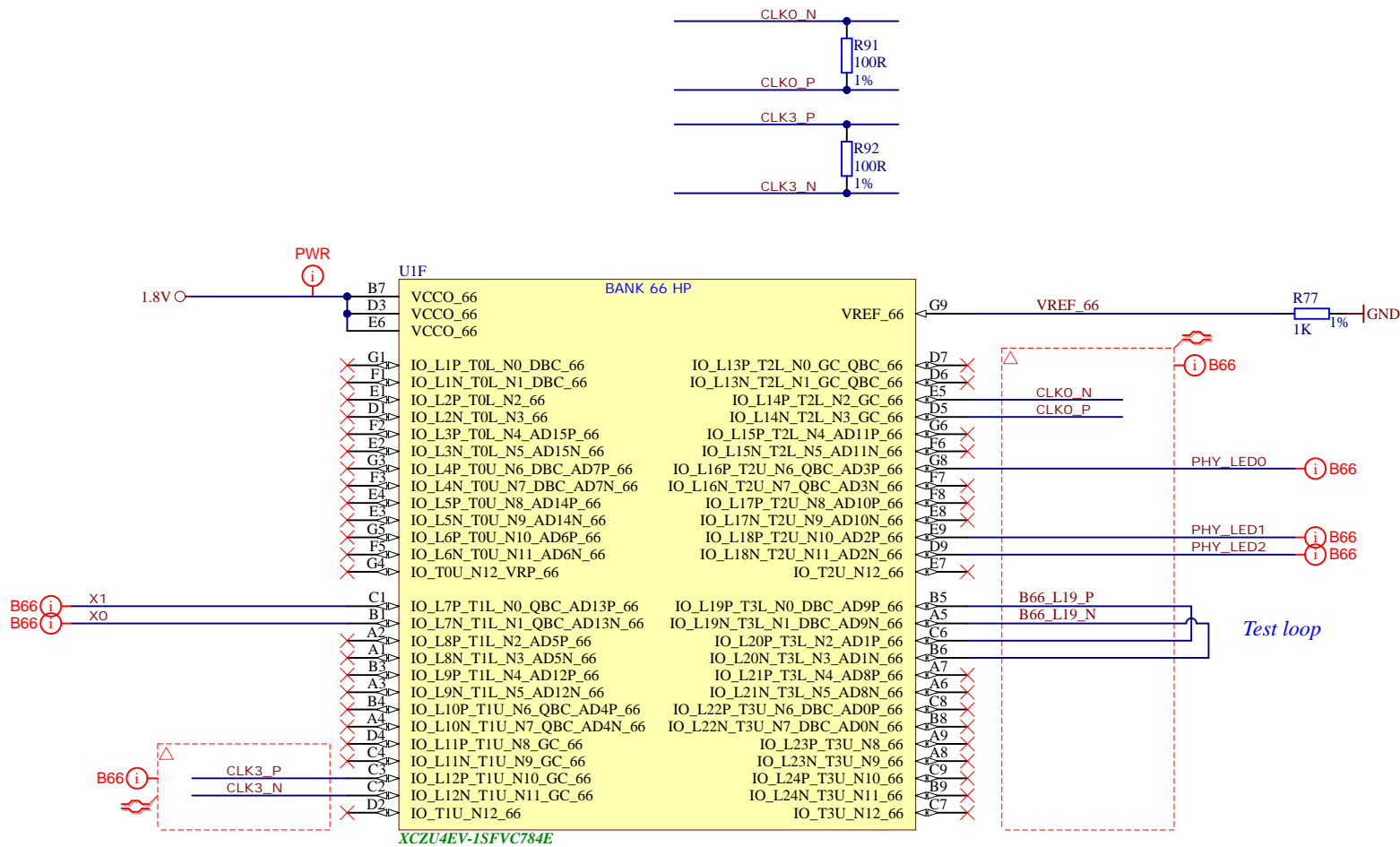



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A4	Number: <b>TE0821 4DE31FL</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>8</b> of <b>24</b>
Filename: <b>B64.SchDoc</b>		

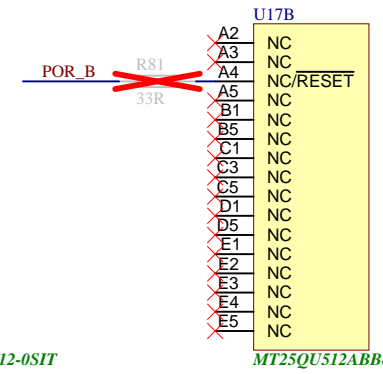
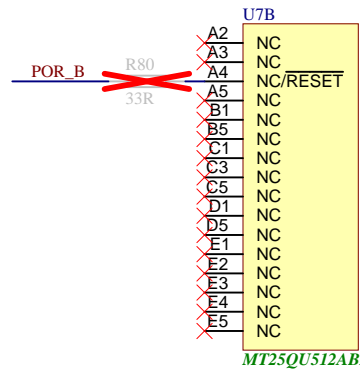
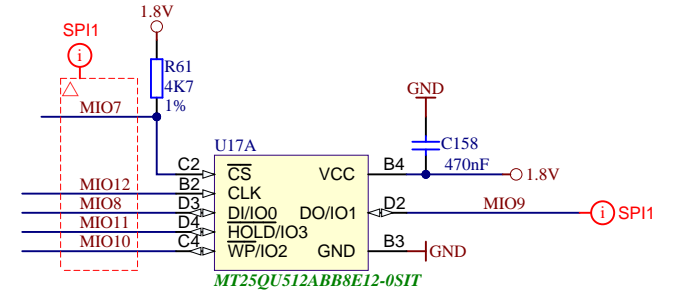
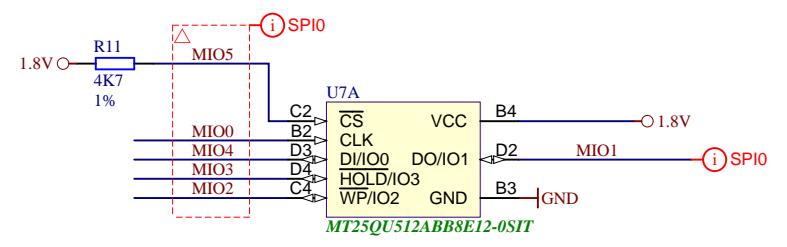
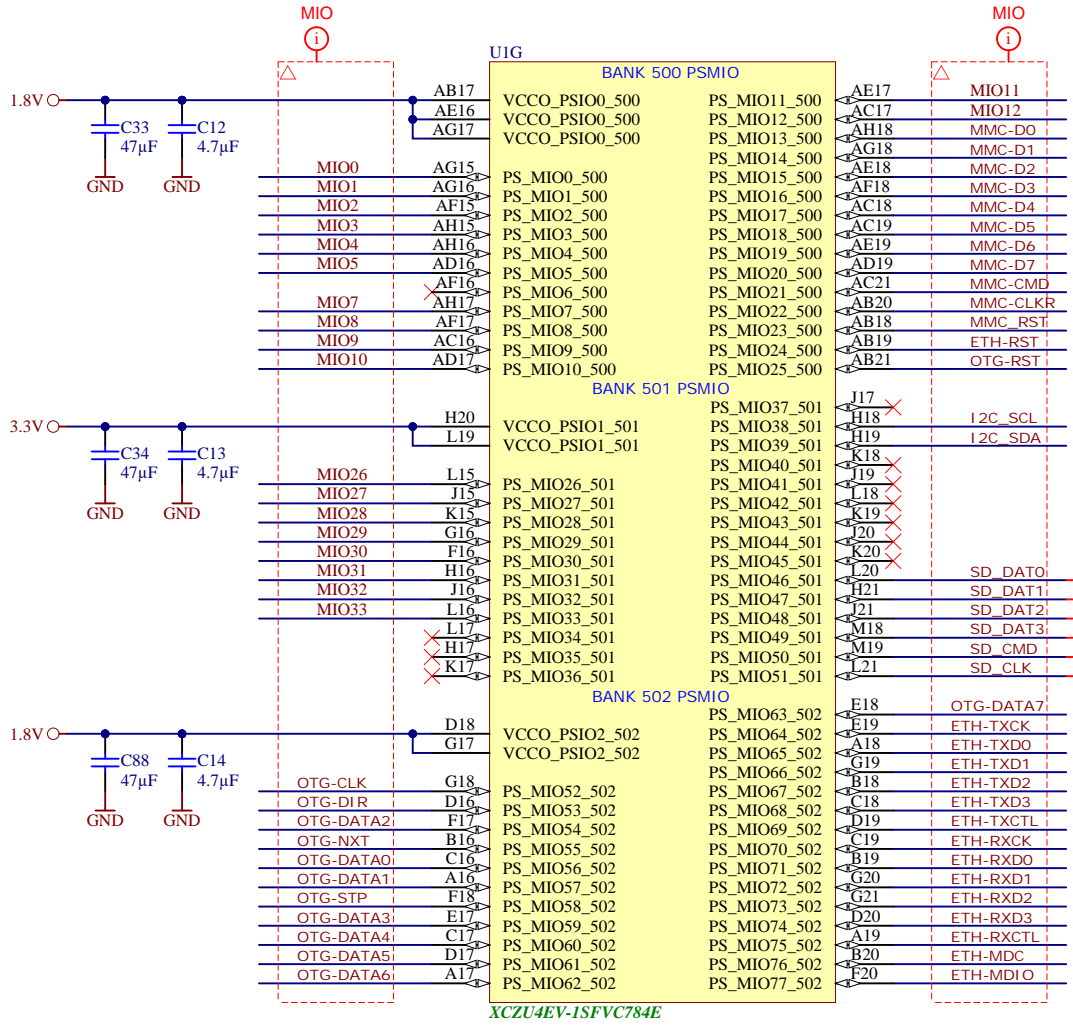




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Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>9</b> of <b>24</b>
Filename: <b>B65.SchDoc</b>		



Title: <b>Module TE0821 - B66</b>		
A4	Number: <b>TE0821 4DE31FL</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>10</b> of <b>24</b>
Filename: <b>B66.SchDoc</b>		



			Title: <b>Module TE0821 - MIO Banks</b>	
			A4	Number: <b>TE0821 4DE31FL</b>
Date: <b>20.02.2019</b>		Copyright: <b>Trenz Electronic GmbH / TT</b>		Page <b>11</b> of <b>24</b>
Filename: <b>B_MIO.SchDoc</b>				

A

B

C

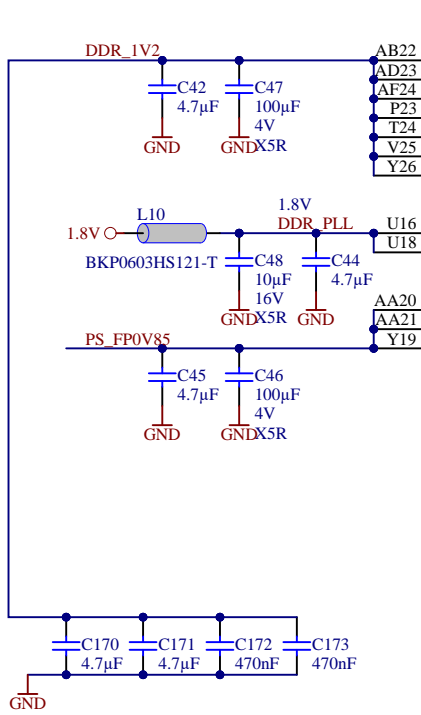
D

A

B

C

D



U11		BANK 504 PSDDR	
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0 P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0 N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
VCC_PSDDR_PLL	PS_DDR_A3_504	AA28	DDR4-A3
VCC_PSDDR_PLL	PS_DDR_A4_504	Y27	DDR4-A4
VCC_PSDDR_PLL	PS_DDR_A5_504	AA27	DDR4-A5
VCC_PSDDR_PLL	PS_DDR_A6_504	Y22	DDR4-A6
VCC_PSDDR_PLL	PS_DDR_A7_504	AA23	DDR4-A7
VCC_PSDDR_PLL	PS_DDR_A8_504	AA22	DDR4-A8
VCC_PSDDR_PLL	PS_DDR_A9_504	AB23	DDR4-A9
VCC_PSDDR_PLL	PS_DDR_A10_504	AA25	DDR4-A10
VCC_PSDDR_PLL	PS_DDR_A11_504	AA26	DDR4-A11
VCC_PSDDR_PLL	PS_DDR_A12_504	AB25	DDR4-A12
VCC_PSDDR_PLL	PS_DDR_A13_504	AB26	DDR4-A13
VCC_PSDDR_PLL	PS_DDR_A14_504	AB24	DDR4-A14
VCC_PSDDR_PLL	PS_DDR_A15_504	AC24	DDR4-A15
VCC_PSDDR_PLL	PS_DDR_A16_504	AC23	DDR4-A16
VCC_PSDDR_PLL	PS_DDR_A17_504	AC22	DDR4-A17
VCC_PSINTFP_DDR	PS_DDR_CS_N0_504	W27	DDR4-CS
VCC_PSINTFP_DDR	PS_DDR_CS_N1_504	V26	
VCC_PSINTFP_DDR	PS_DDR_BA0_504	V23	DDR4-BA0
VCC_PSINTFP_DDR	PS_DDR_BA1_504	W22	DDR4-BA1
VCC_PSINTFP_DDR	PS_DDR_BG0_504	W24	DDR4-BG0
VCC_PSINTFP_DDR	PS_DDR_BG1_504	V22	DDR4-BG1
VCC_PSINTFP_DDR	PS_DDR_PARITY_504	V24	DDR4-PAR
VCC_PSINTFP_DDR	PS_DDR_RAM_RST_N_504	U23	DDR4-RESET
VCC_PSINTFP_DDR	PS_DDR_ACT_N_504	Y23	DDR4-ACT
VCC_PSINTFP_DDR	PS_DDR_ALERT_N_504	U25	DDR4-ALERT
VCC_PSINTFP_DDR	PS_DDR_ZQ_504	U24	
VCC_PSINTFP_DDR	PS_DDR_ODT0_504	U28	DDR4-ODT0
VCC_PSINTFP_DDR	PS_DDR_ODT1_504	U26	

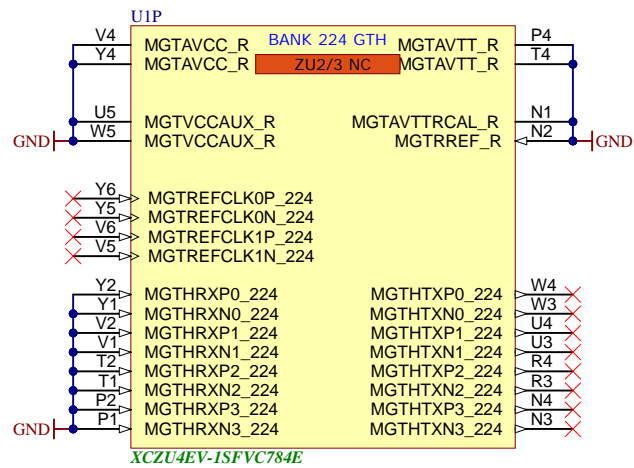
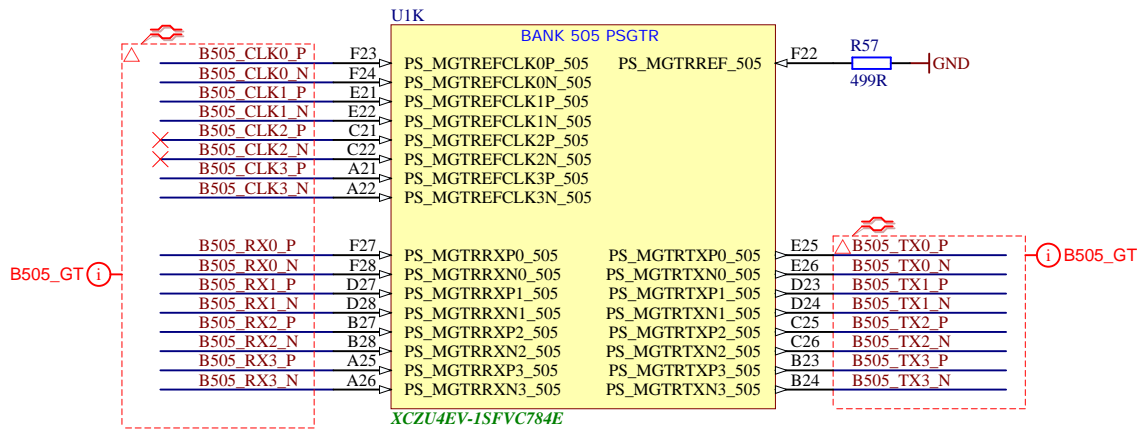
XCZU4EV-1SFVC784E

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DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504	R22	
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504	P22	
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504	N22	
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504	T23	
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504	P24	
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	R24	
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	N24	
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504	H24	
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504	J24	
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504	M24	
DQ11	AD23	PS_DDR_DQ11_504	PS_DDR_DQ43_504	K24	
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504	J22	
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504	H22	
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504	K22	
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504	J22	
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504	M25	
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504	M26	
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504	L25	
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504	L26	
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504	K28	
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504	L28	
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504	M28	
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504	N28	
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504	J28	
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504	K27	
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504	H28	
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504	H27	
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504	G26	
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504	G25	
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504	K25	
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504	J25	
DDR4-DQS0 P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ64_504	T28	
DDR4-DQS0 N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ65_504	R28	
DDR4-DQS1 P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ66_504	P28	
DDR4-DQS1 N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ67_504	P27	
DDR4-DQS2 P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504	P26	
DDR4-DQS2 N	AF26	PS_DDR_DQS_N2_504	PS_DDR_DQ69_504	R25	
DDR4-DQS3 P	AE27	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504	P25	
DDR4-DQS3 N	AE27	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504	T25	
	N23	PS_DDR_DQS_P4_504	PS_DDR_DM0_504	AG20	DDR4-DM0
	M23	PS_DDR_DQS_N4_504	PS_DDR_DM1_504	AE23	DDR4-DM1
	L23	PS_DDR_DQS_P5_504	PS_DDR_DM2_504	AE25	DDR4-DM2
	K23	PS_DDR_DQS_N5_504	PS_DDR_DM3_504	AE28	DDR4-DM3
	N26	PS_DDR_DQS_P6_504	PS_DDR_DM4_504	R23	
	N27	PS_DDR_DQS_N6_504	PS_DDR_DM5_504	H23	
	J26	PS_DDR_DQS_P7_504	PS_DDR_DM6_504	L27	
	J27	PS_DDR_DQS_N7_504	PS_DDR_DM7_504	H26	
	R27	PS_DDR_DQS_P8_504	PS_DDR_DM8_504	T26	
	T27	PS_DDR_DQS_N8_504			

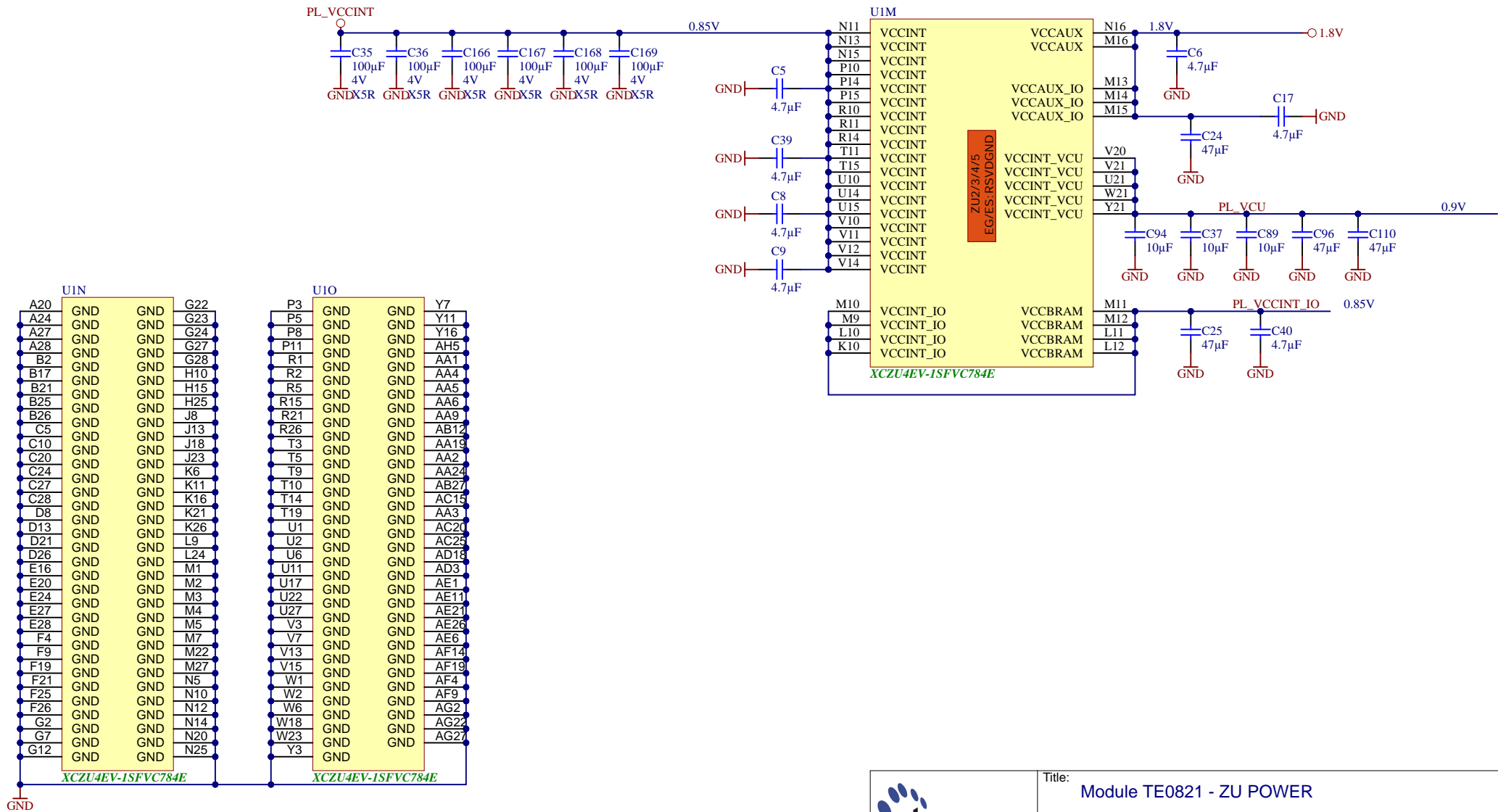
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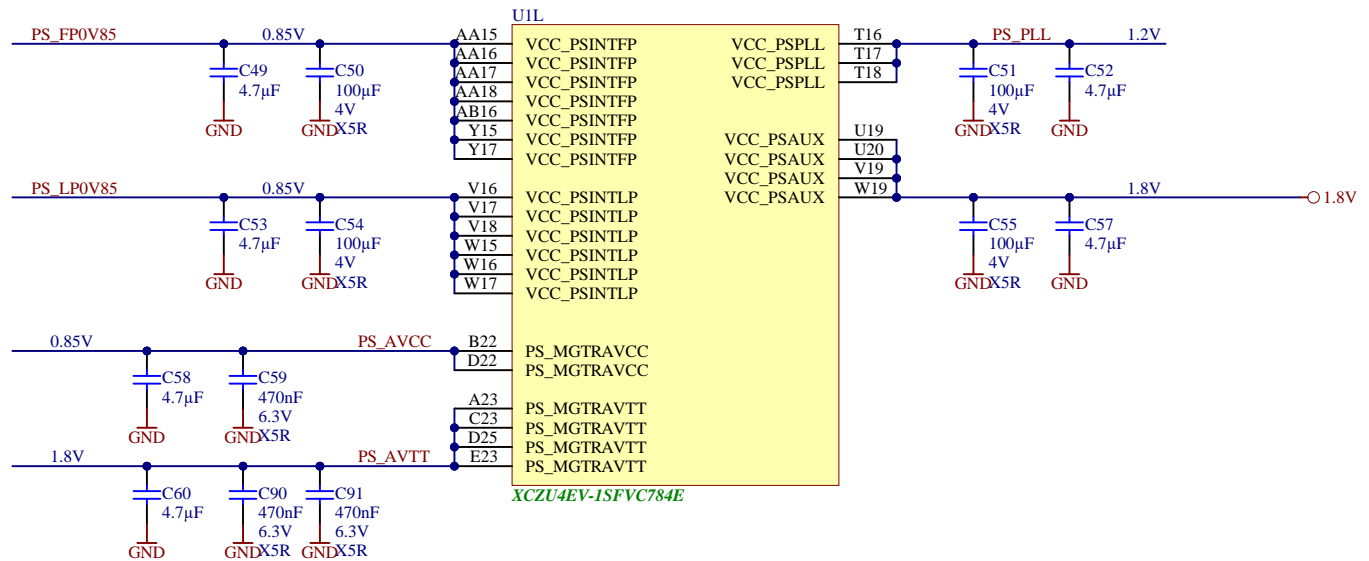
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A4	Number: <b>TE0821 4DE31FL</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>12</b> of <b>24</b>
Filename: <b>PS_DDR.SchDoc</b>		



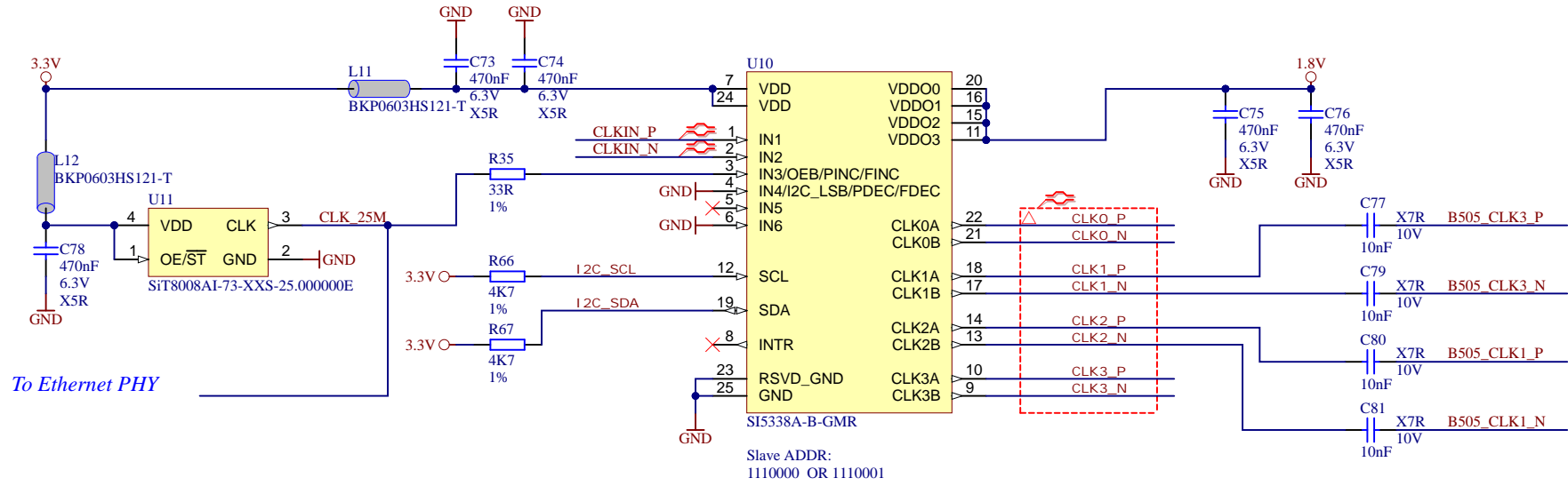
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	Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>13</b> of <b>24</b>
	Filename: <b>B_PS_GT.SchDoc</b>		




Title: <b>Module TE0821 - ZU POWER</b>		
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Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>14</b> of <b>24</b>
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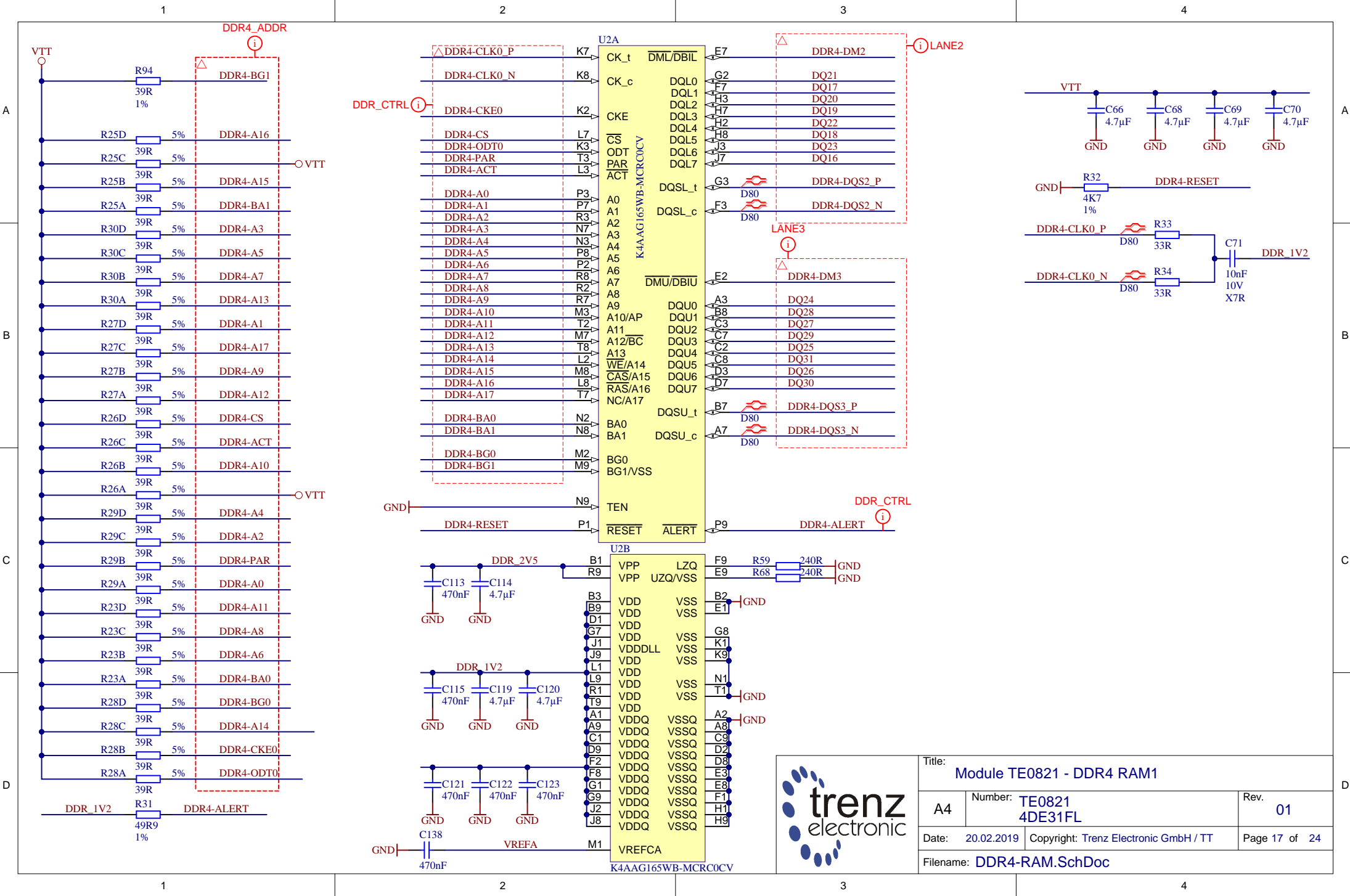
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A4	Number: TE0821 4DE31FL	Rev. 01
Date: 20.02.2019	Copyright: Trenz Electronic GmbH / TT	Page 15 of 24
Filename: ZU_PS_POWER.SchDoc		



To Ethernet PHY

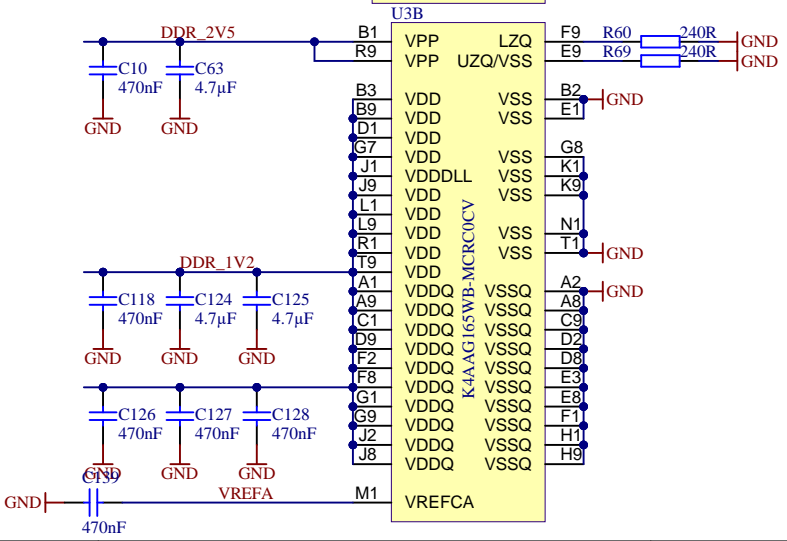
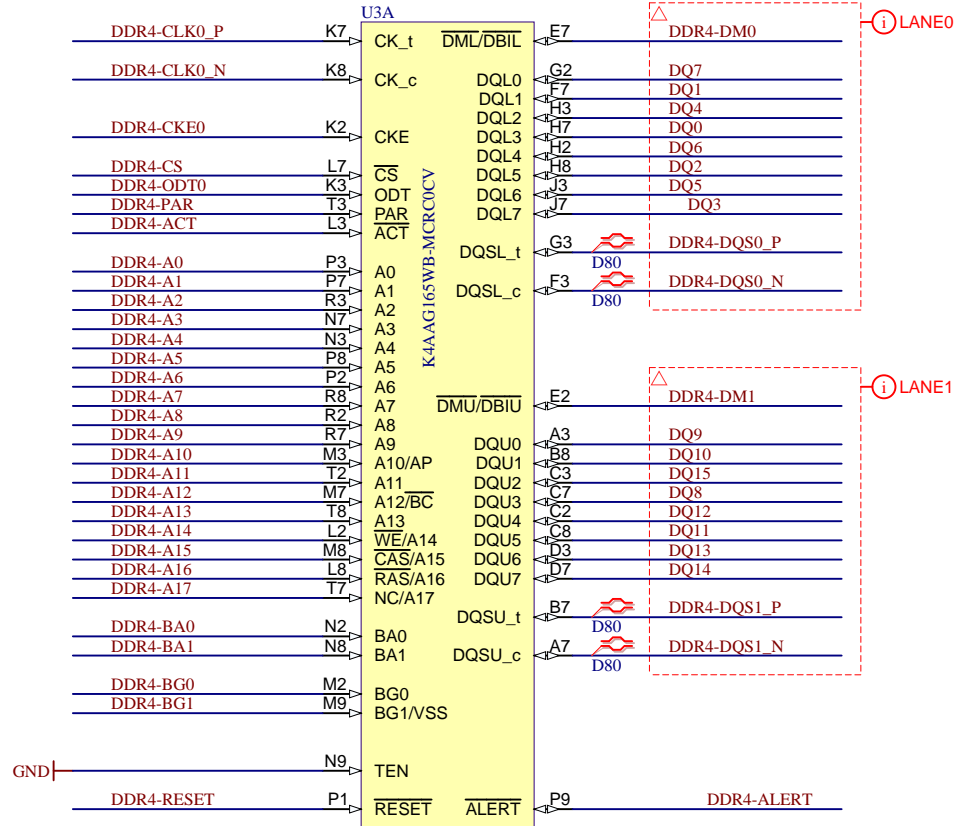
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		A4	Number: <b>TE0821 4DE31FL</b> Date: 20.02.2019 Filename: <b>CLK.SchDoc</b>



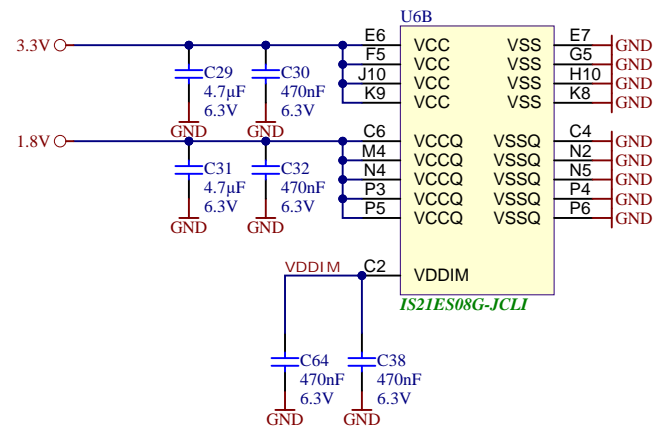
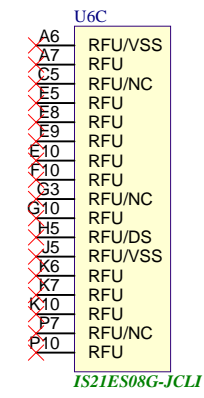
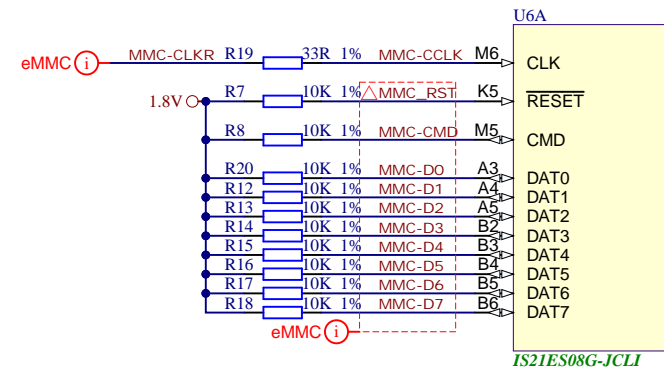
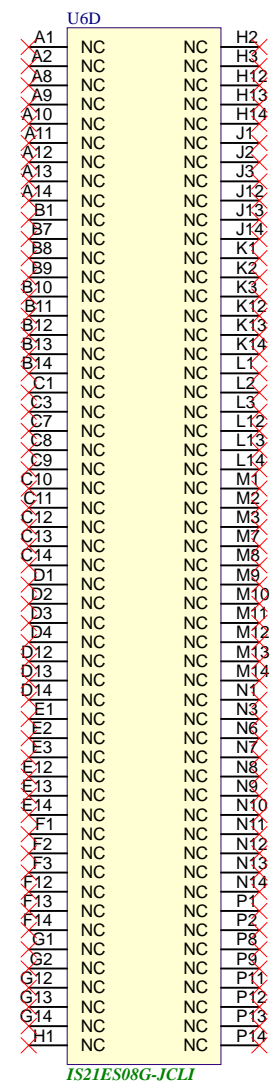


Title: <b>Module TE0821 - DDR4 RAM1</b>		
A4	Number: <b>TE0821 4DE31FL</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>17</b> of <b>24</b>
Filename: <b>DDR4-RAM.SchDoc</b>		

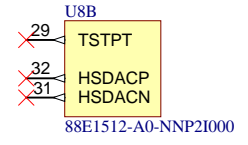
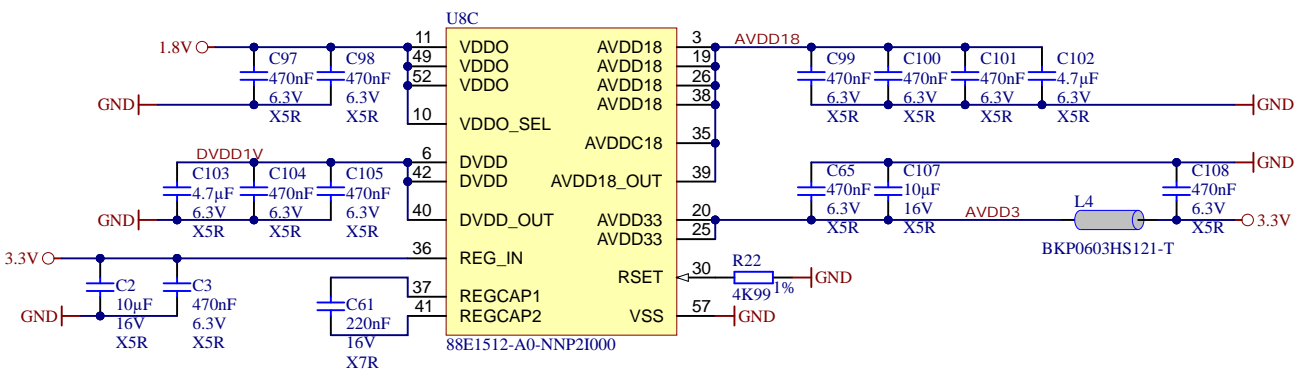
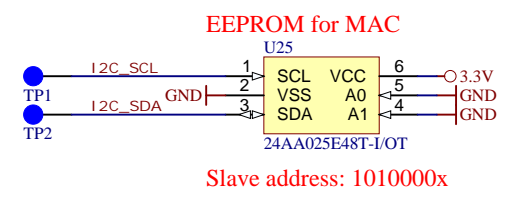
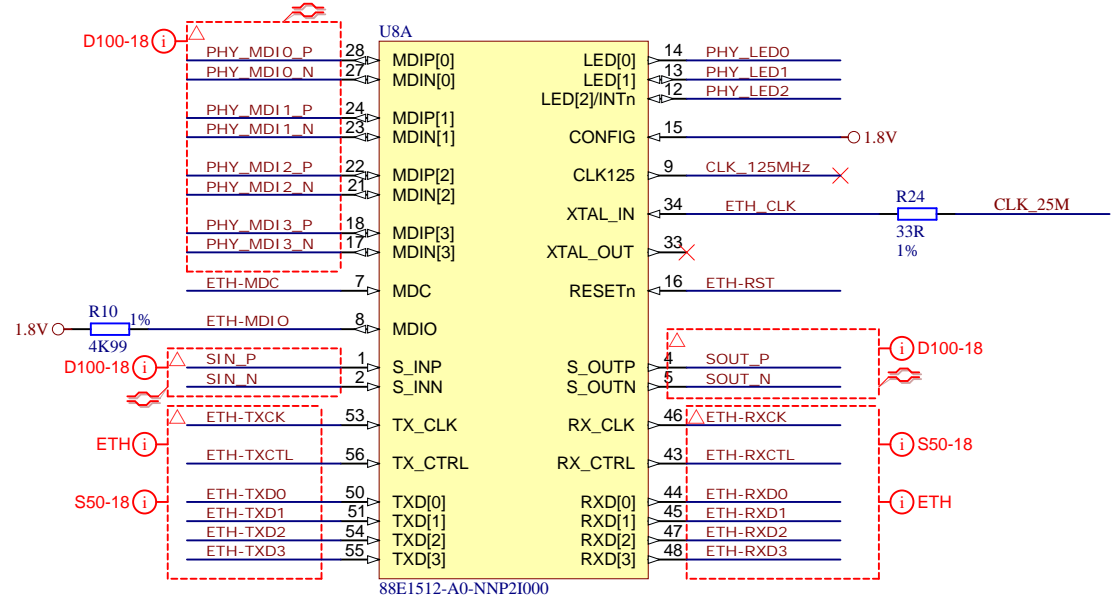




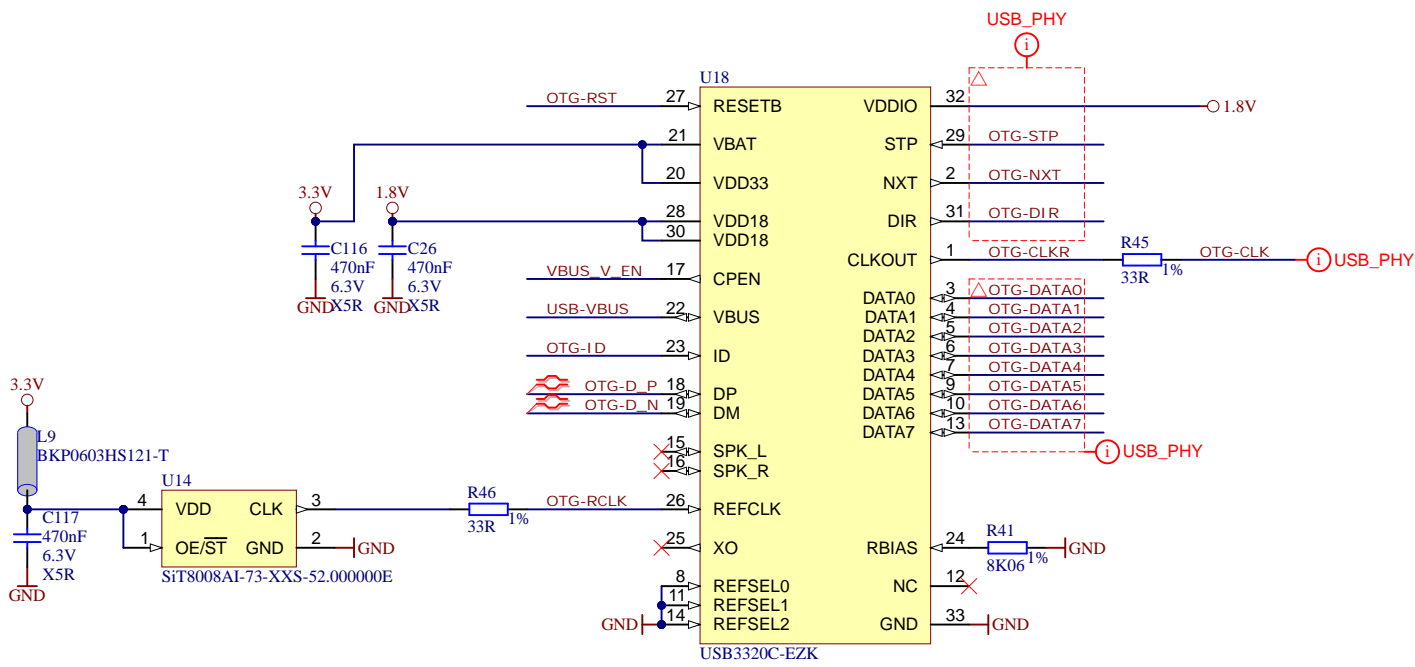
Title: <b>Module TE0821 - DDR4 RAM2</b>		
A4	Number: <b>TE0821 4DE31FL</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>18</b> of <b>24</b>
Filename: <b>DDR4-RAM_2.SchDoc</b>		



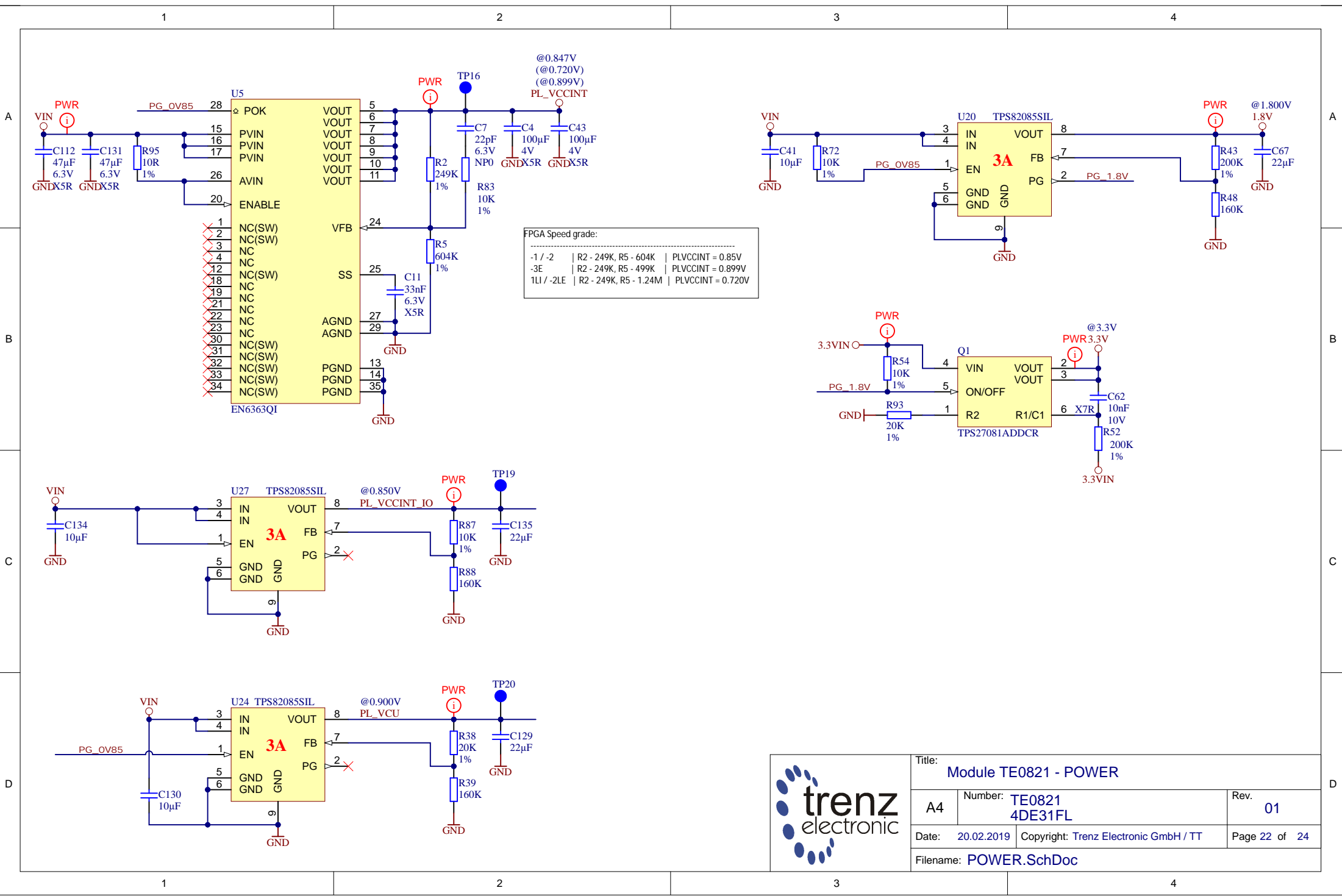
	Title: <b>Module TE0821 - eMMC</b>		
	A4	Number: <b>TE0821 4DE31FL</b>	Rev. <b>01</b>
	Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>19</b> of <b>24</b>
	Filename: <b>eMMC.SchDoc</b>		



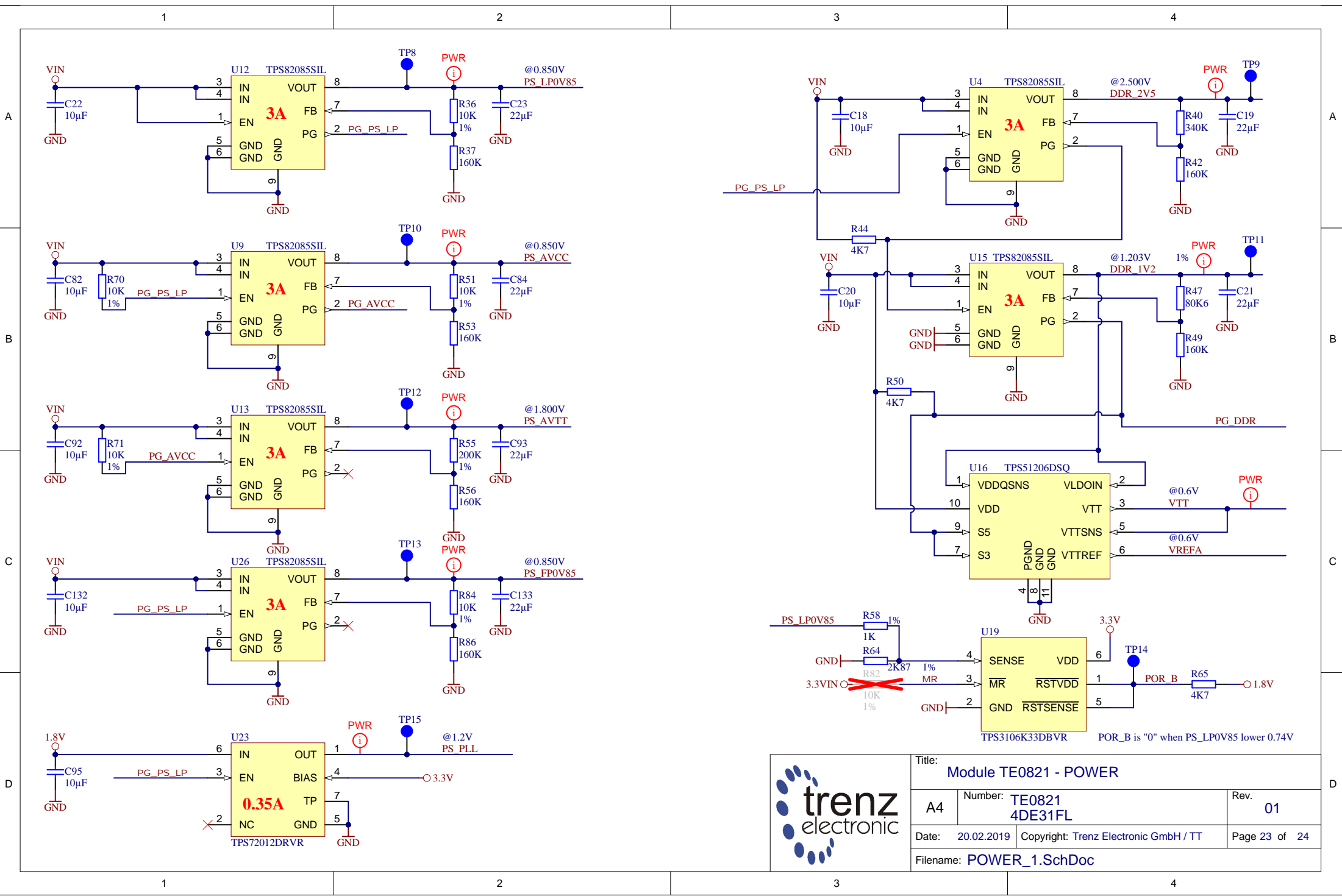
Title: <b>Module TE0821 - Ethernet PHY</b>		
A4	Number: <b>TE0821 4DE31FL</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>2015 Trenz Electronic GmbH</b>	Page <b>20</b> of <b>24</b>
Filename: <b>ETH-PHY.SchDoc</b>		



	Title: <b>Module TE0821 - USB PHY</b>	
	A4	Number: <b>TE0821 4DE31FL</b>
	Date: 20.02.2019	Rev. <b>01</b>
	Copyright: 2015 Trenz Electronic GmbH	
Page 21 of 24		
Filename: <b>USB-PHY.SchDoc</b>		



Title: <b>Module TE0821 - POWER</b>		
A4	Number: <b>TE0821 4DE31FL</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>22</b> of <b>24</b>
Filename: <b>POWER.SchDoc</b>		



Title: <b>Module TE0821 - POWER</b>		
A4	Number: <b>TE0821 4DE31FL</b>	Rev. <b>01</b>
Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>23</b> of <b>24</b>
Filename: <b>POWER_1.SchDoc</b>		

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Revision 01a (01.07.2020):

1. VY: R38 value was changed to 20K (was: 40K2) to set VCU 0.9V

Revision 01b (29.10.2020):

1. VY: Updated Block diagram

(07.02.2024):  
2. OT: R82 set to not fitted

A

A

B


B

C

C

D

D

	Title: <b>Module TE0821 - Revision Changes</b>		
	A4	Number: <b>TE0821 4DE31FL</b>	Rev. <b>01</b>
	Date: <b>20.02.2019</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>24</b> of <b>24</b>
	Filename: <b>Revision Changes.SchDoc</b>		

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