

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-MISC
FPGA-MISC.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_FPGA-B44
FPGA-B44.SchDoc

U_FPGA-B45
FPGA-B45.SchDoc

U_FPGA-B46
FPGA-B46.SchDoc

U_FPGA-B47
FPGA-B47.SchDoc

U_FPGA-B64
FPGA-B64.SchDoc

U_FPGA-B65
FPGA-B65.SchDoc

U_FPGA-B66
FPGA-B66.SchDoc

U_FPGA-B67
FPGA-B67.SchDoc

U_FPGA-B68
FPGA-B68.SchDoc

U_DDR4-RAM
DDR4-RAM.SchDoc

U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

U_B2B-Connectors
B2B-Connectors.SchDoc

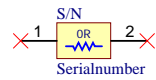
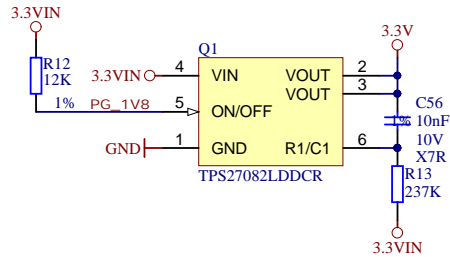
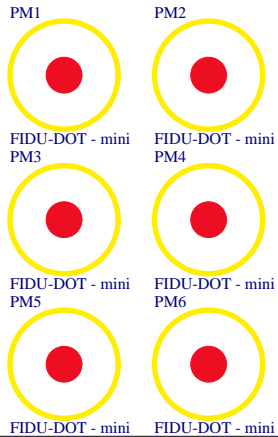
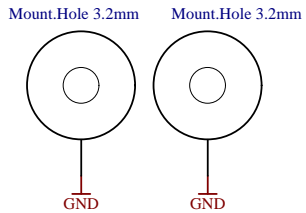
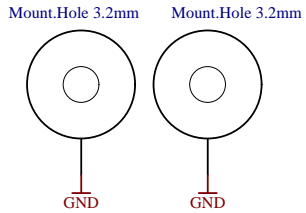
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CPLD.SchDoc

U_Clock
Clock.SchDoc

U_PWR1
PWR1.SchDoc

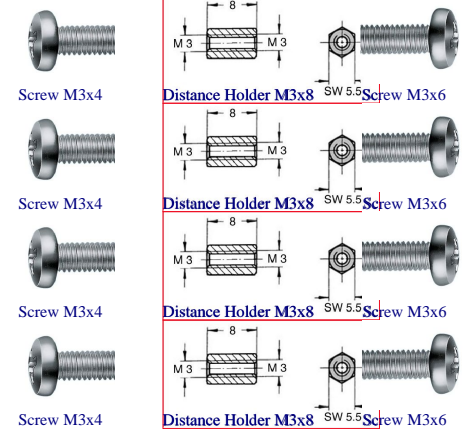
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PWR2.SchDoc


U_POWER_2
POWER_2.SchDoc

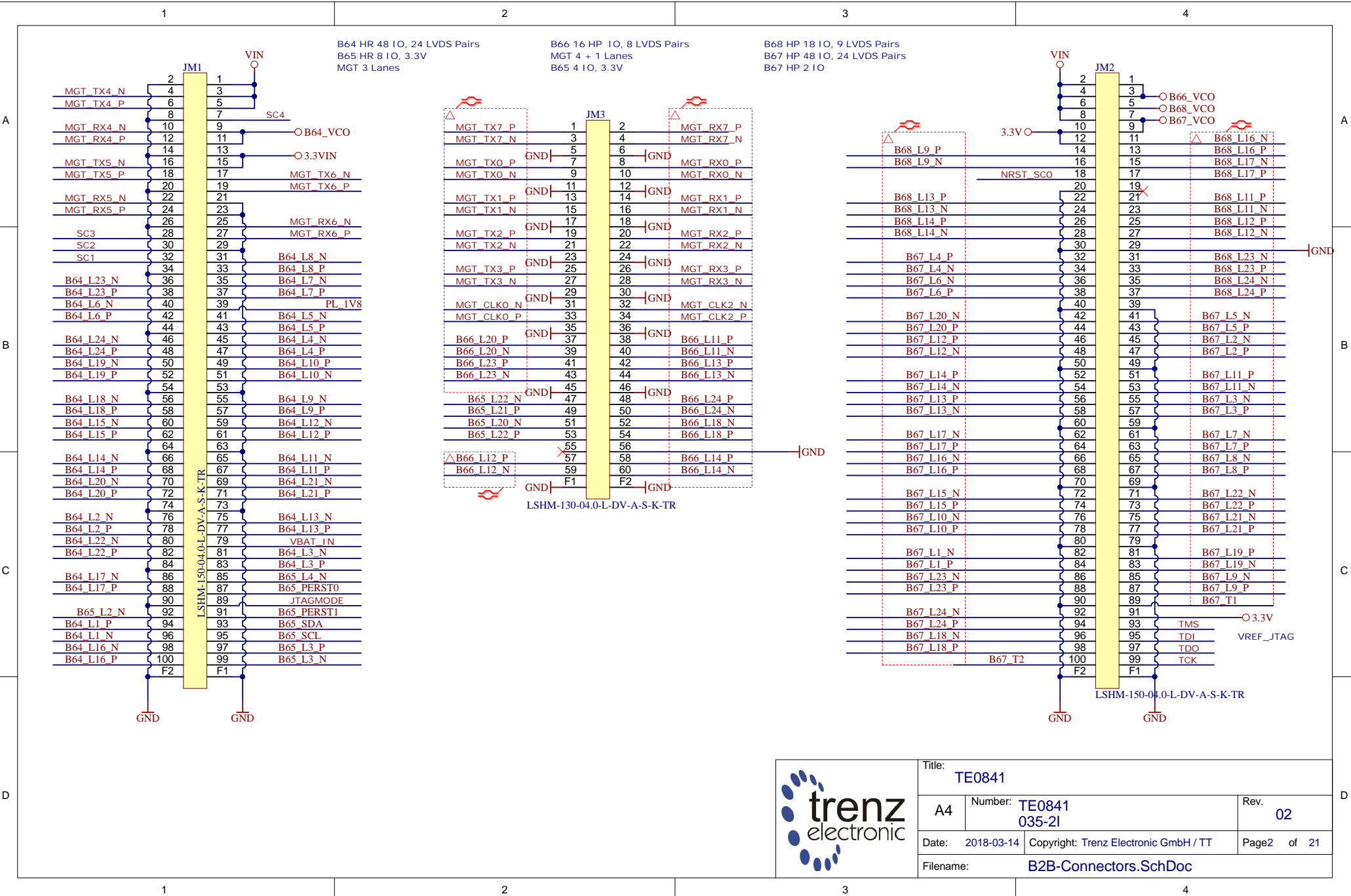


Serial
Serial
Serialnumber 6,3 x 6.3mm

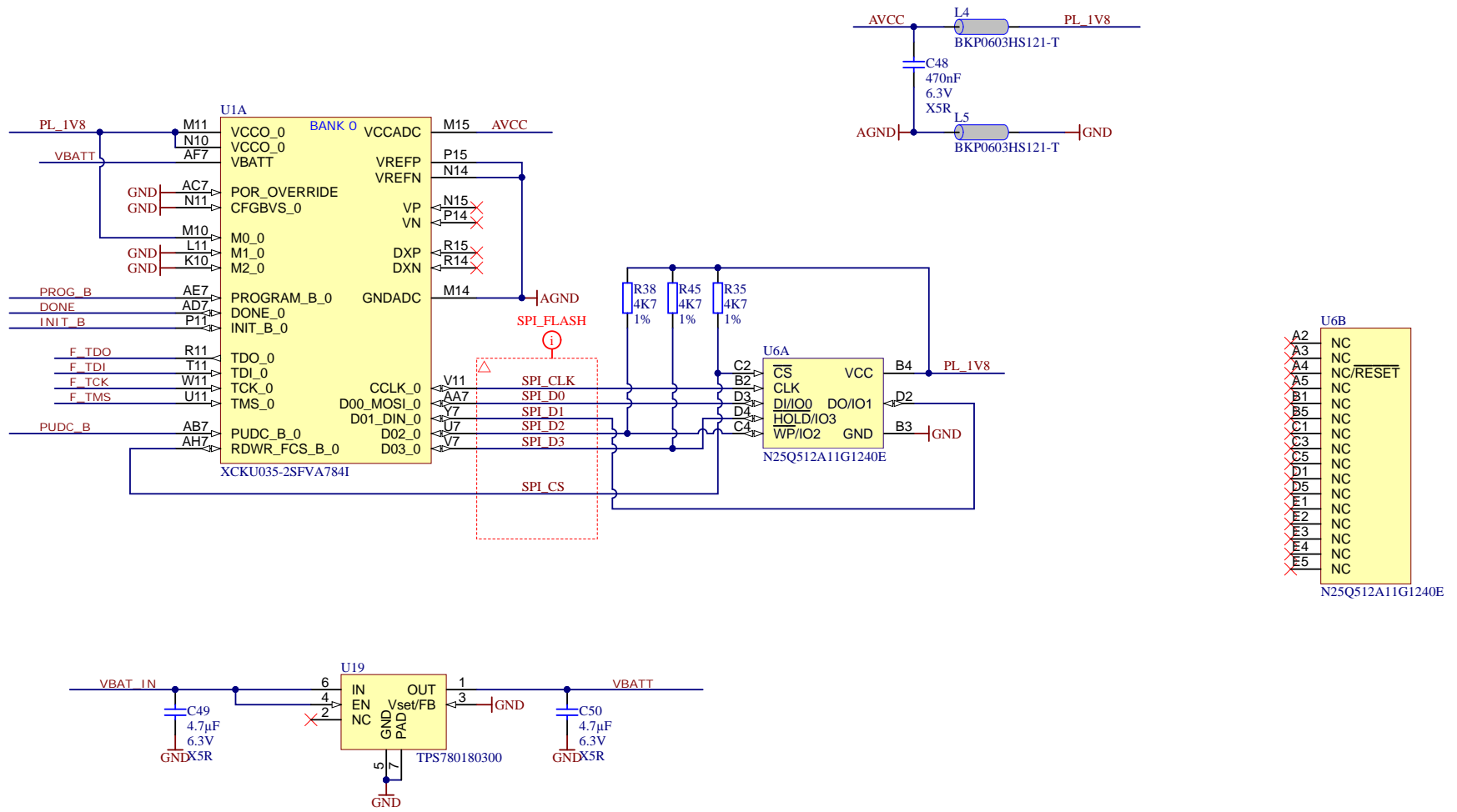
Top of Board




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Filename: B2B-Connectors.SchDoc		



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1 2 3 4

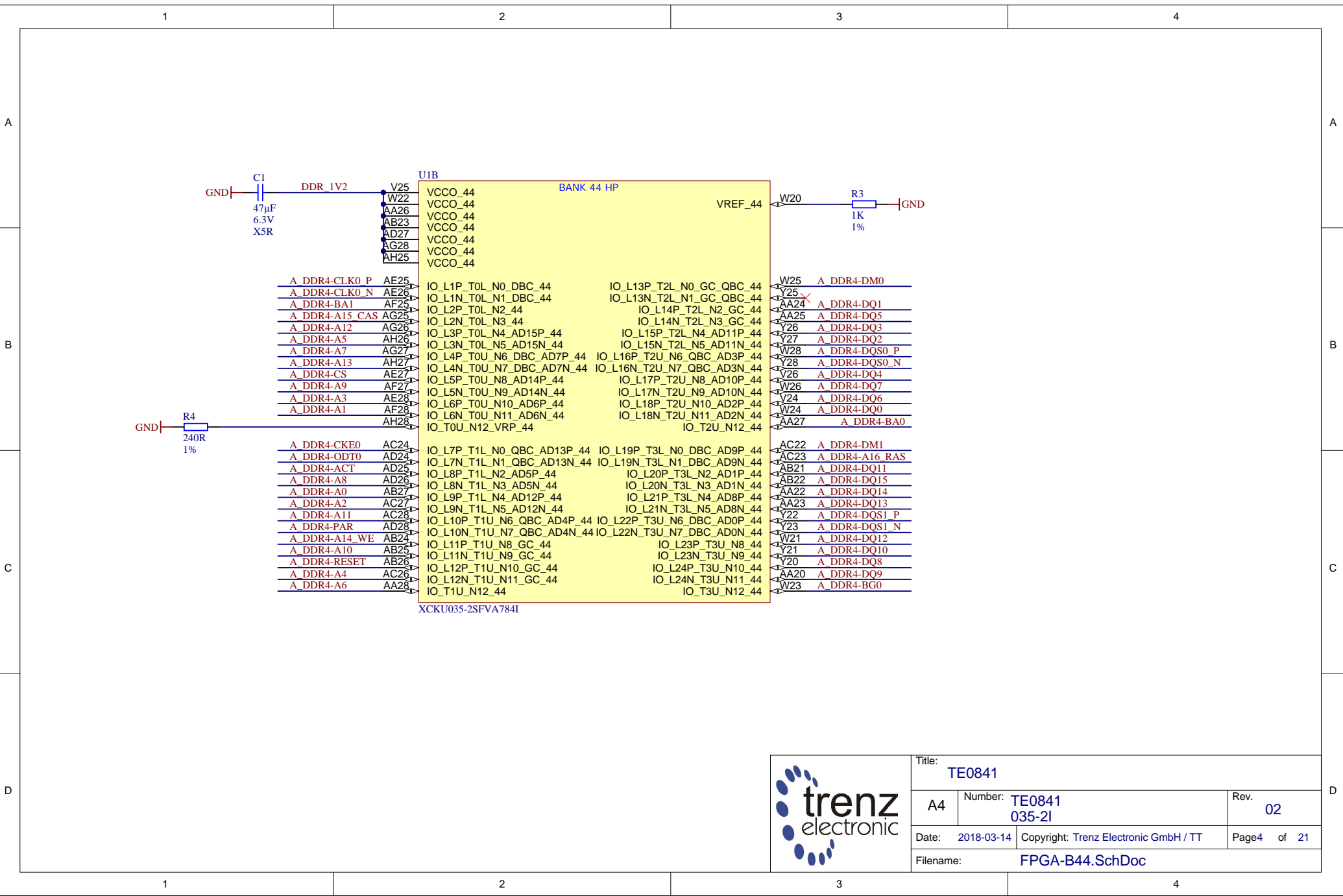
A

B

C

D

1 2 3 4



	Title: TE0841	
	A4	Number: TE0841 035-2I
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Filename: FPGA-B44.SchDoc		

1

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A

A

B

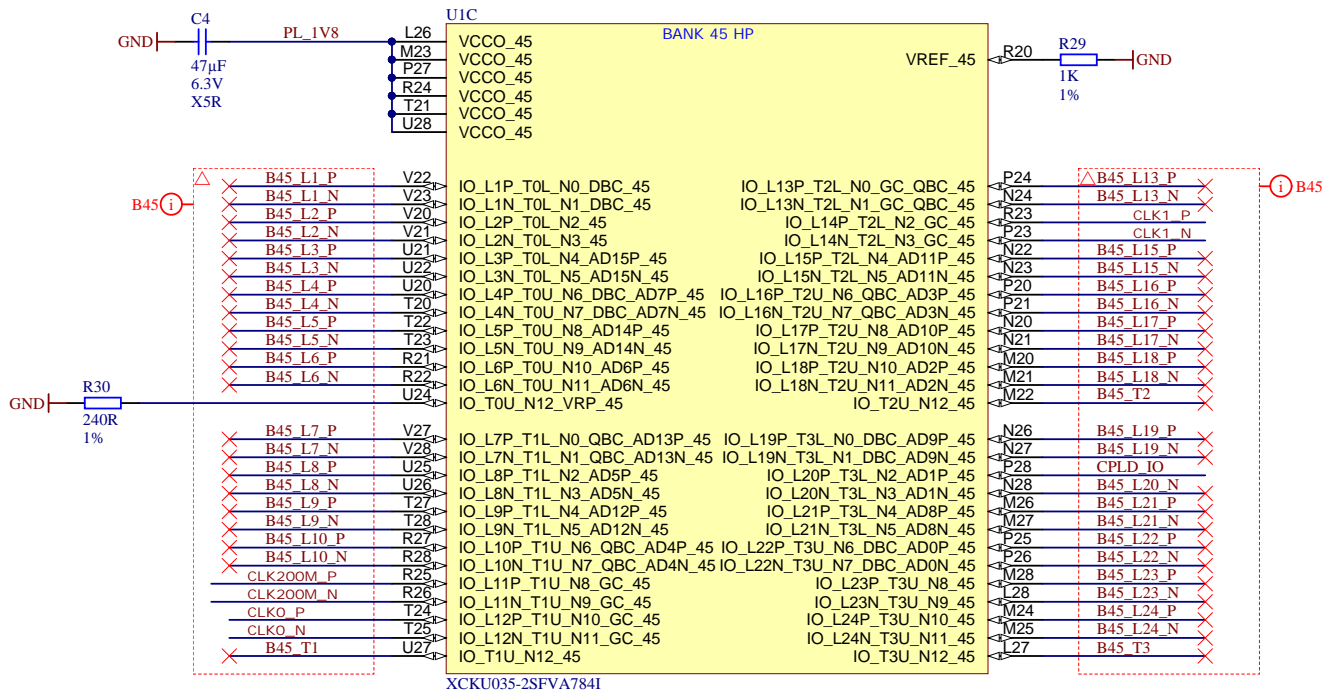
B

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D



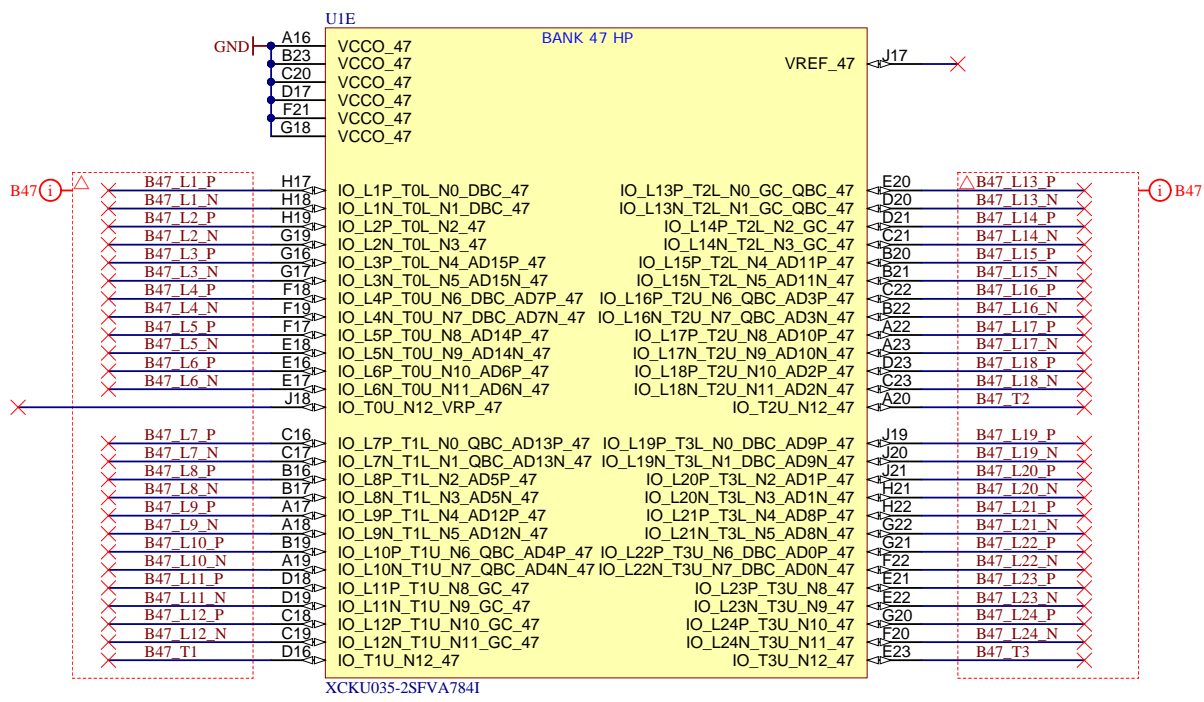

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Filename: FPGA-B47.SchDoc		

1

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A

A

B

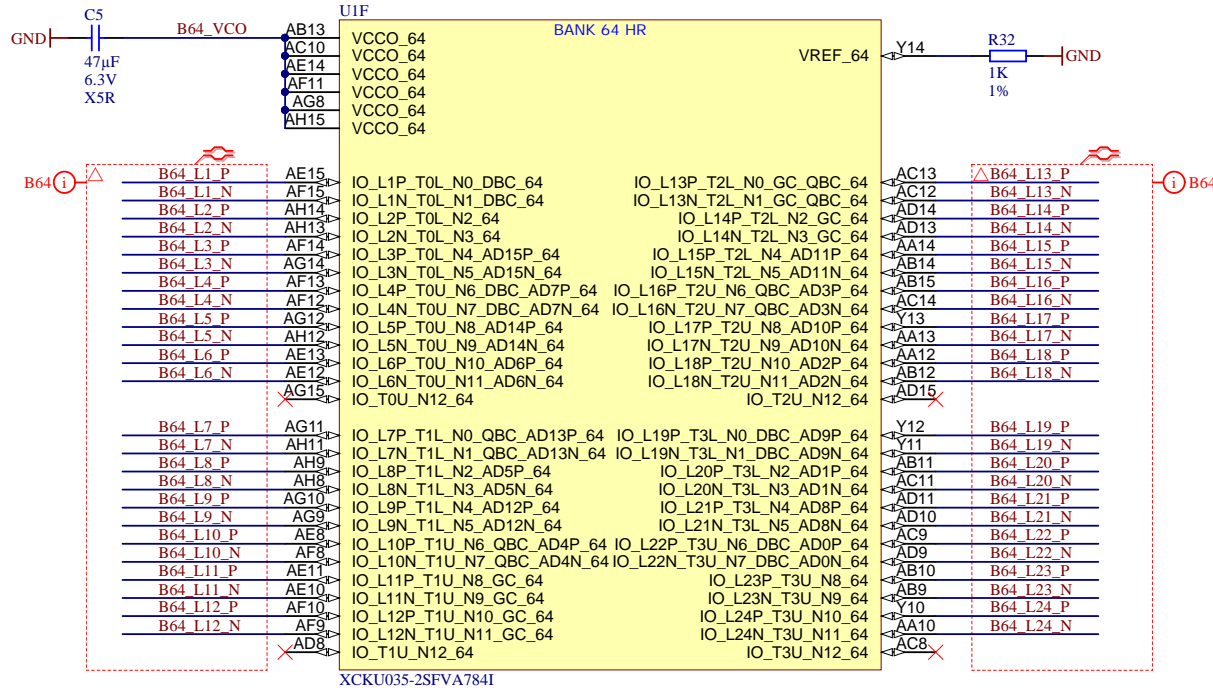
B

C

C

D

D



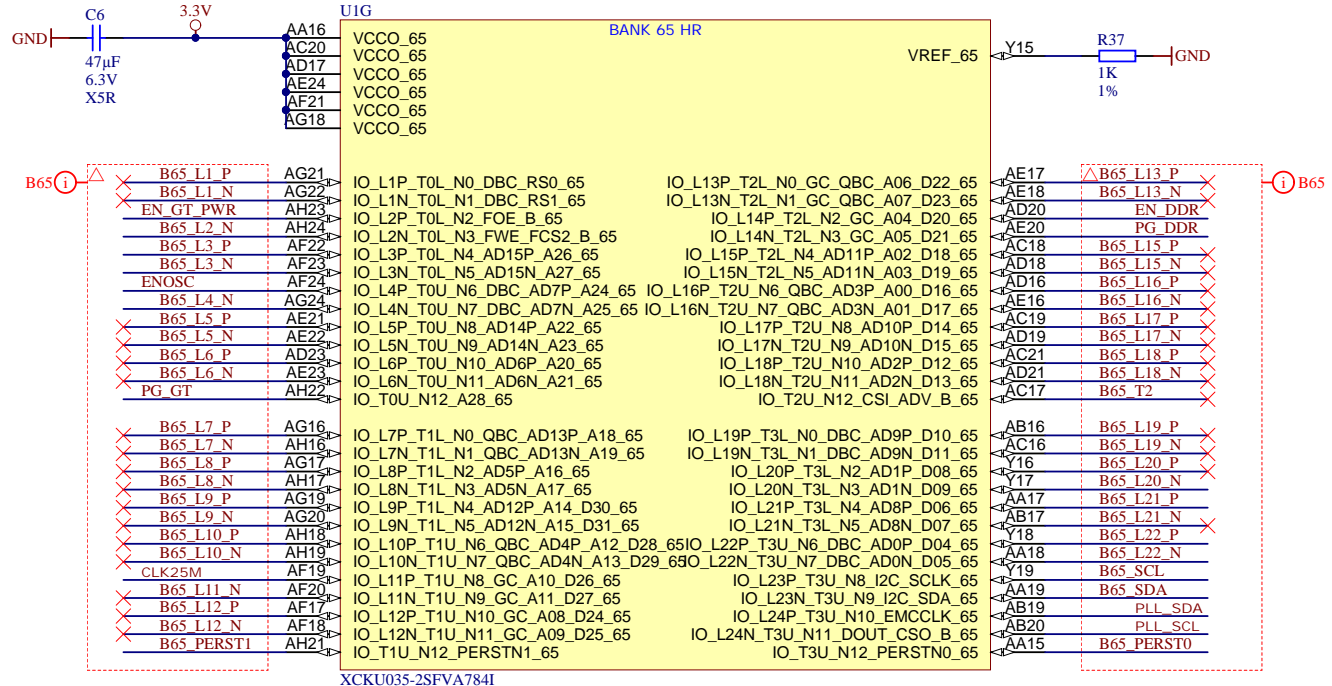
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Filename: FPGA-B64.SchDoc		

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Title: TE0841		
A4	Number: TE0841 035-2I	Rev. 02
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Filename: FPGA-B65.SchDoc		

1

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A

A

B

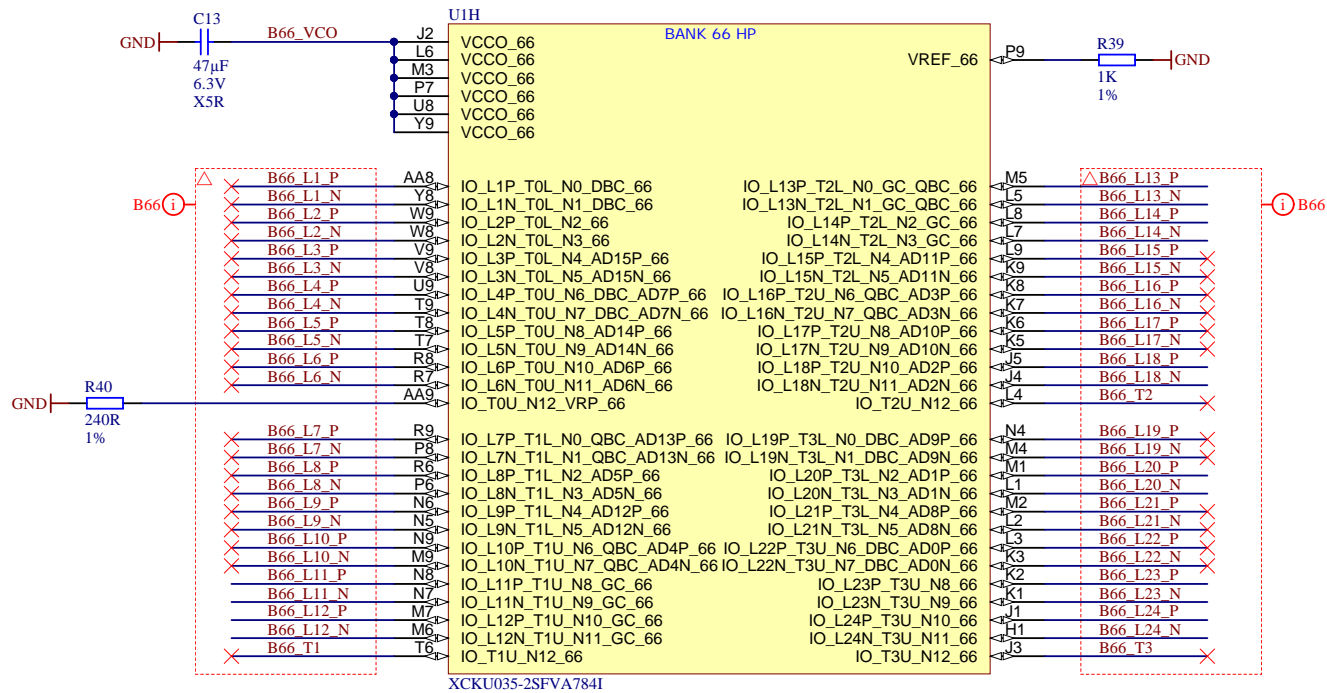
B

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C

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D



Title: TE0841		
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A

A

B

B

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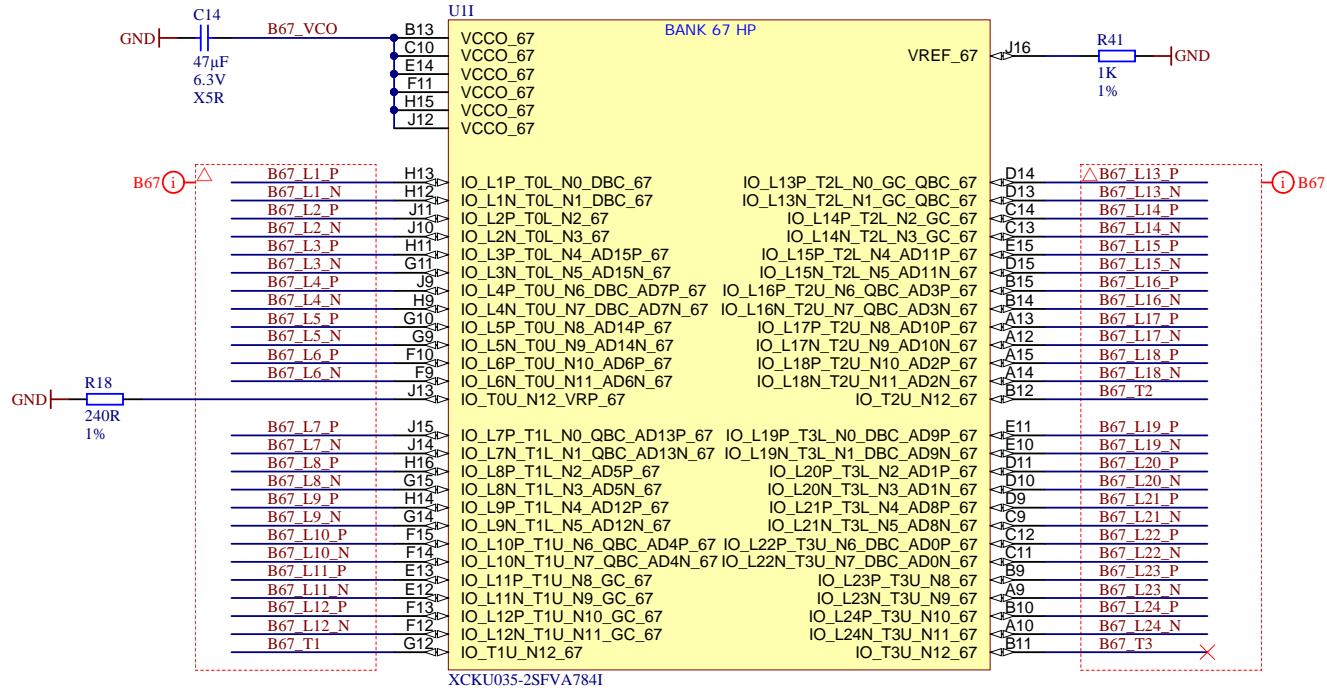
D

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Title: TE0841		
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1

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A

A

B

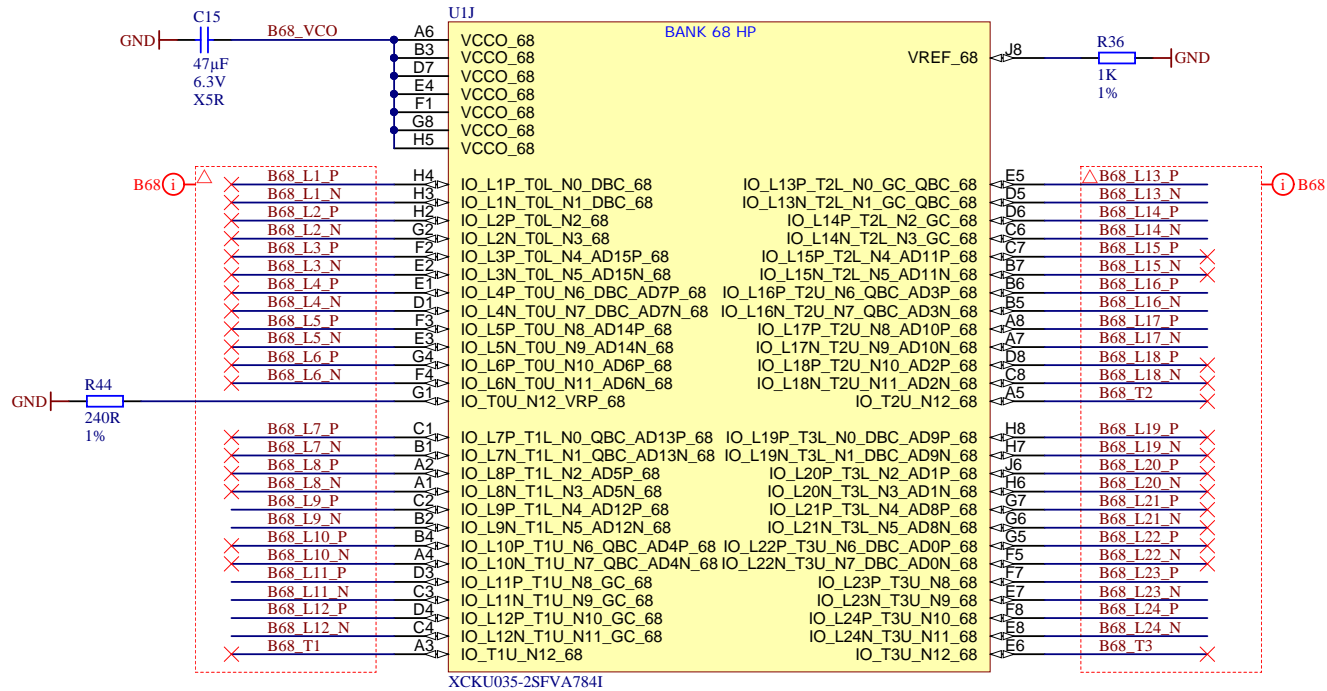
B


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C

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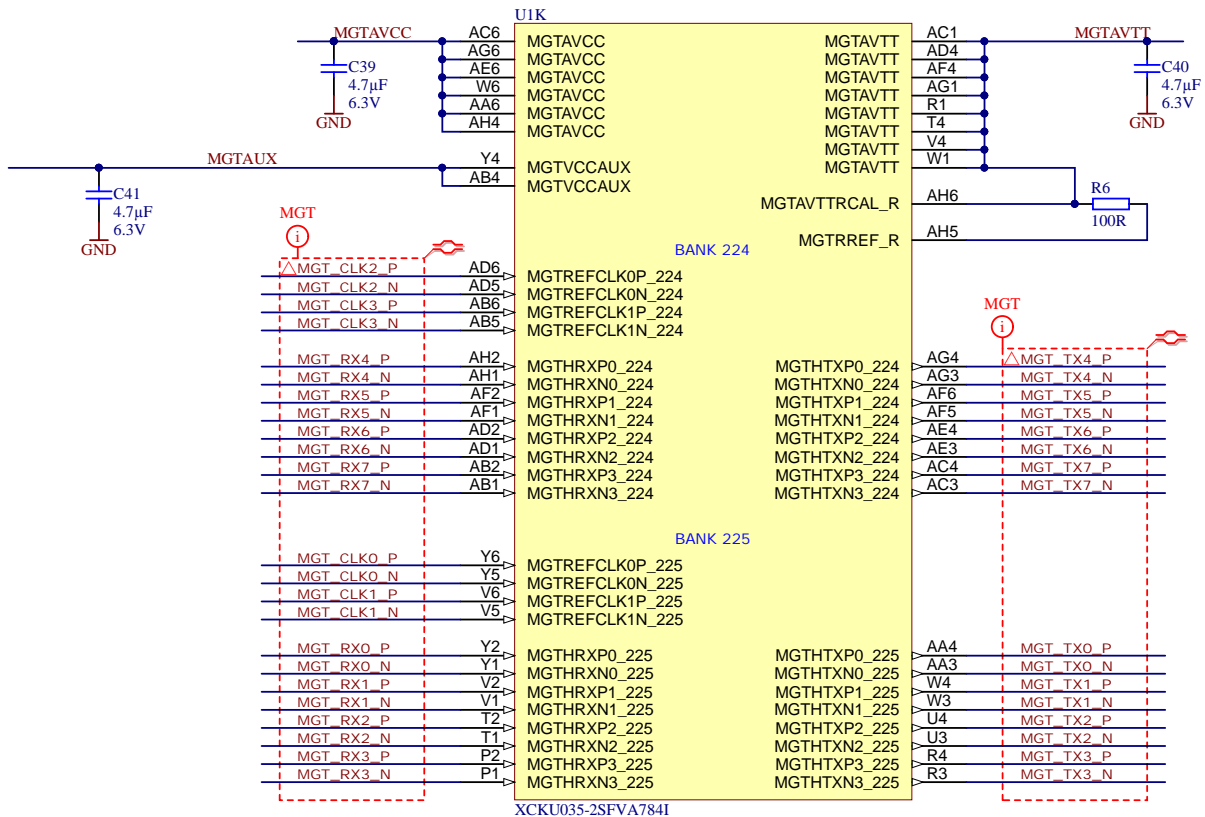
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	Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT	
	Filename: FPGA-B68.SchDoc		Page 12 of 21


1

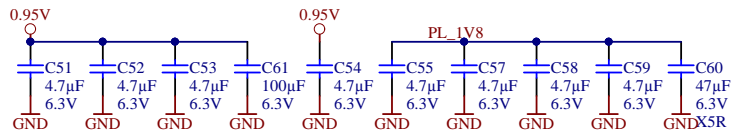
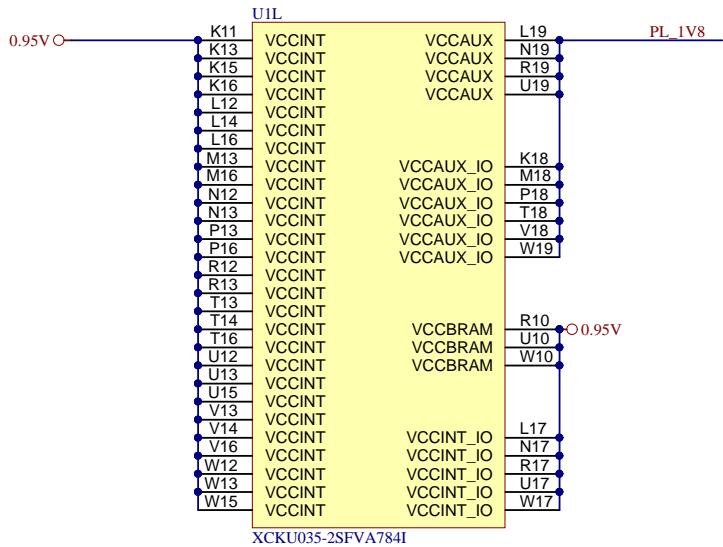
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3

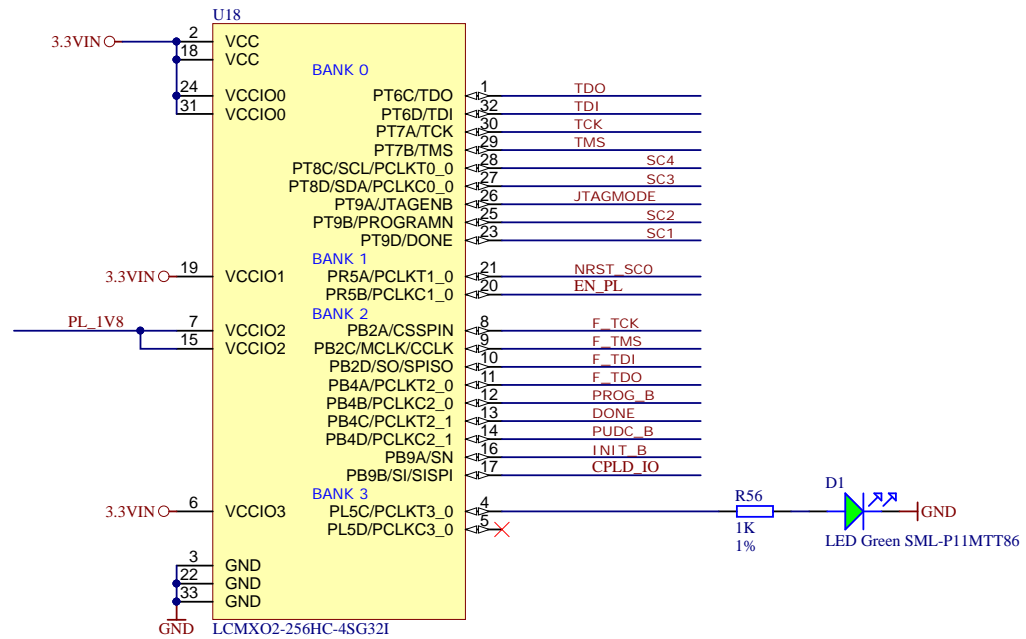
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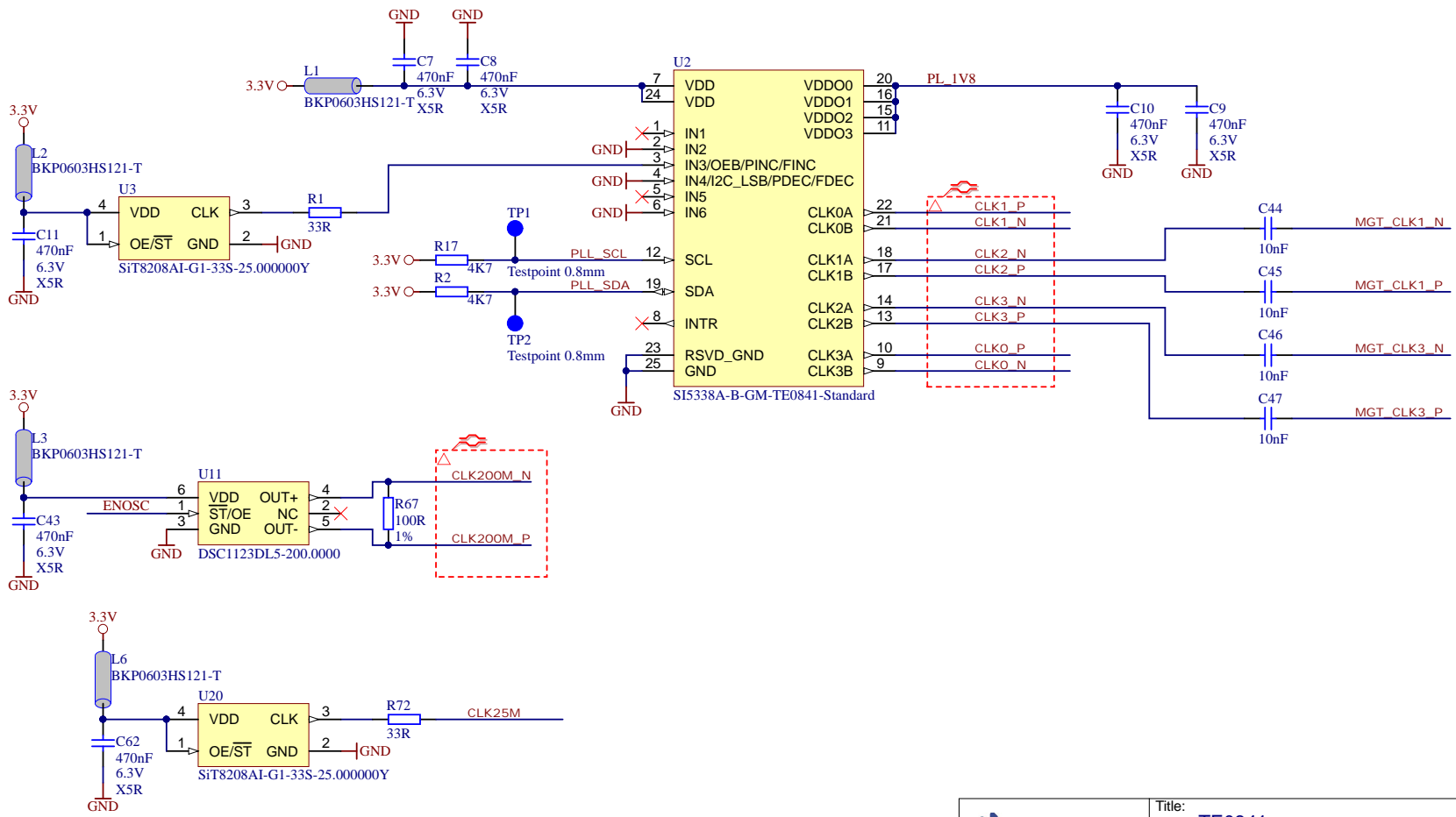
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	Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT	
	Filename: FPGA-MGT.SchDoc		Page13 of 21




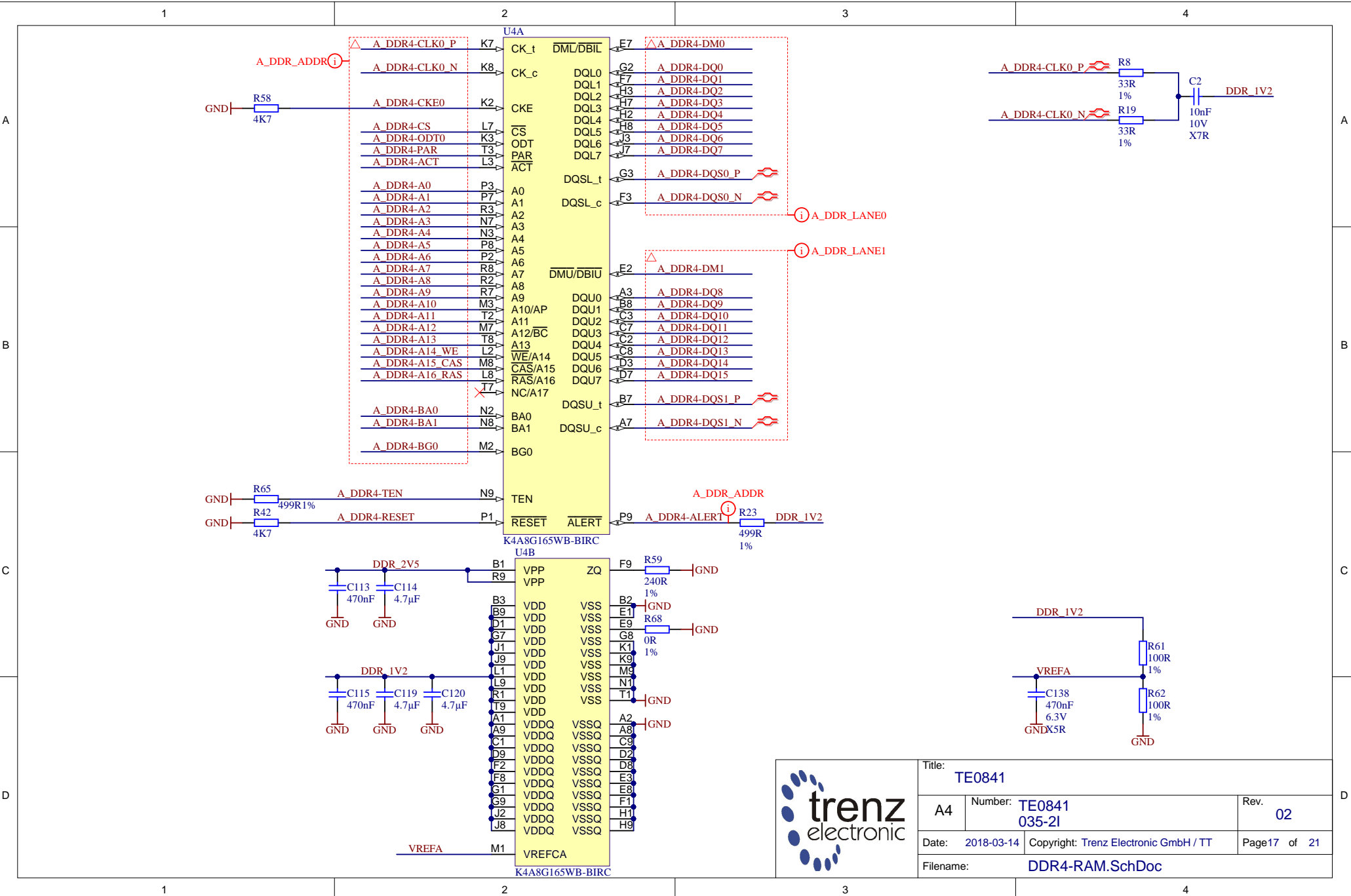
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Filename: FPGA-PWR.SchDoc		



	Title: TE0841		
	A4	Number: TE0841 035-2I	Rev. 02
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	Filename: CPLD.SchDoc		



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		A4	Number: TE0841 035-21
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Title: TE0841		
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Filename: DDR4-RAM.SchDoc		

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A

A

B

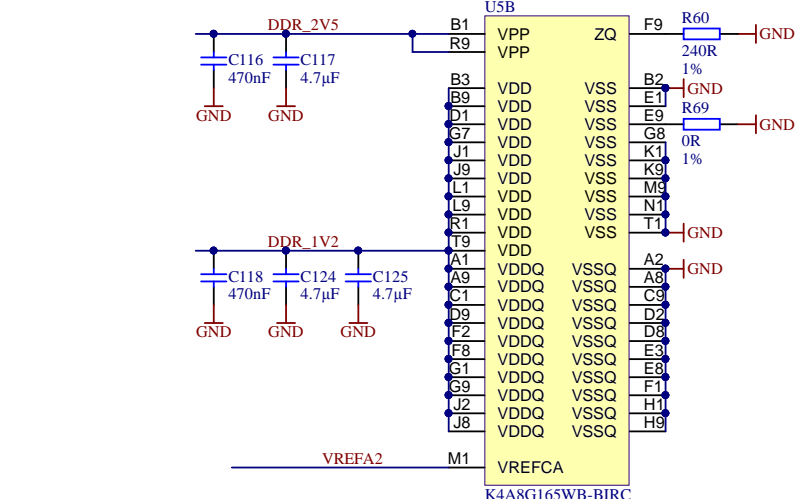
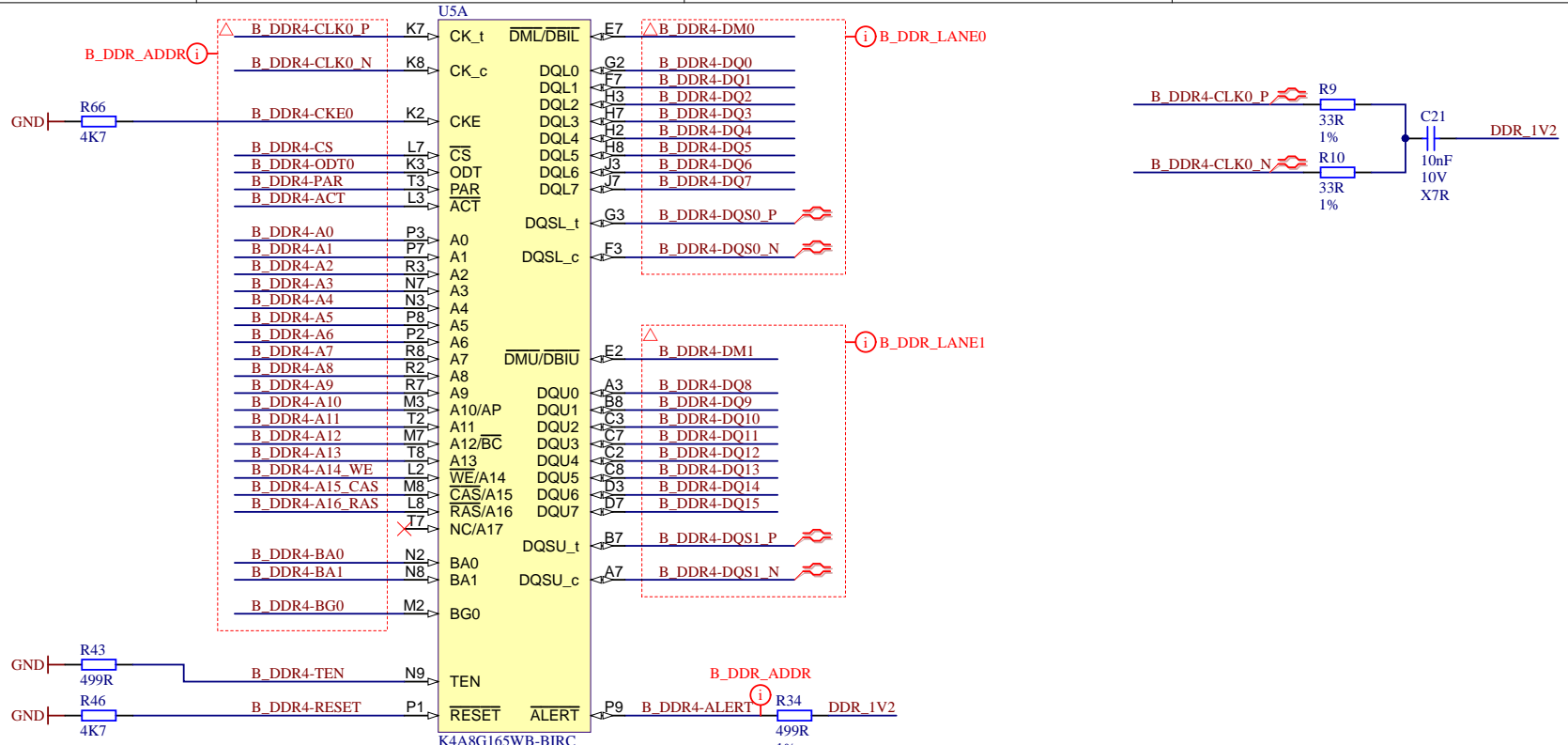
B

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C

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D



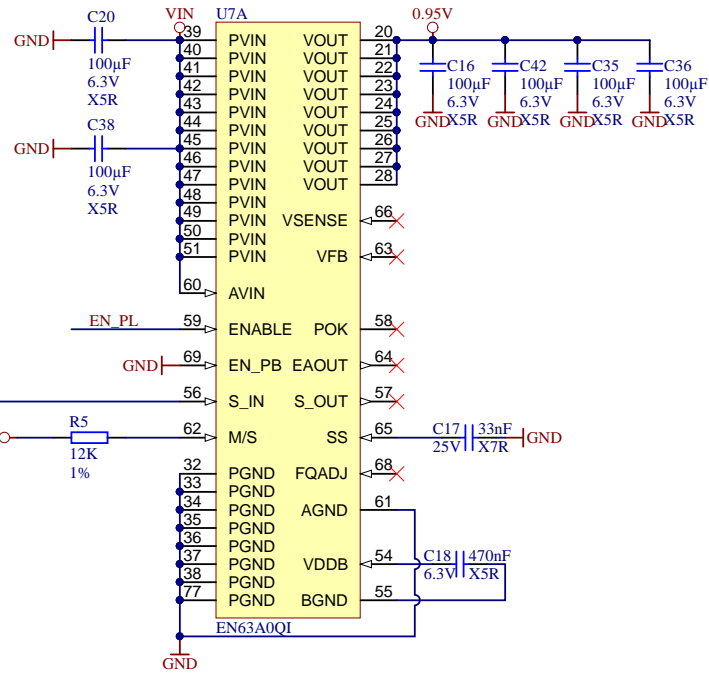
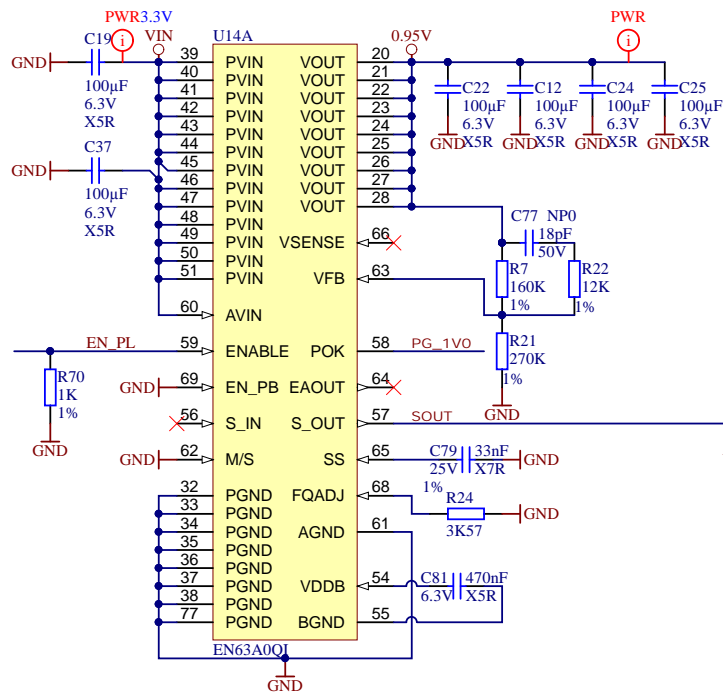
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A4	Number: TE0841 035-21	Rev. 02
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Filename: DDR4-RAM_2.SchDoc		

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U14B EN63A0QI Pin Connections:

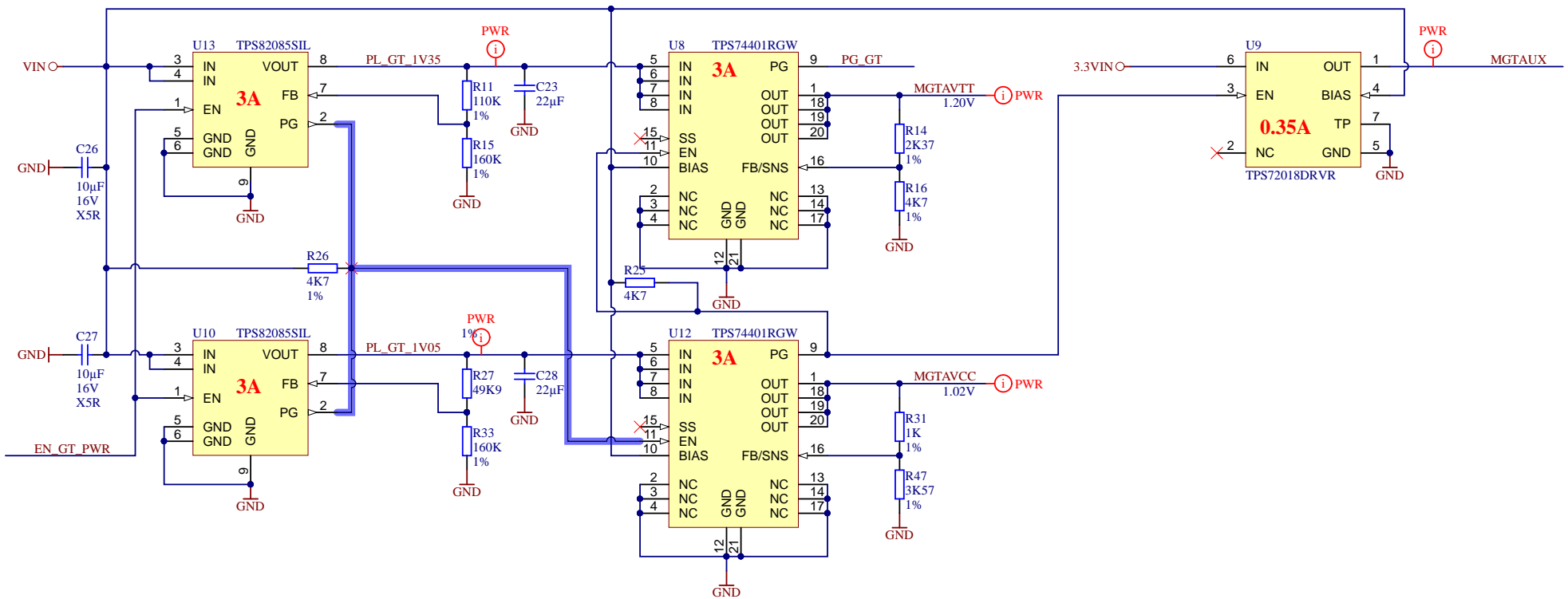
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2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76

U7B EN63A0QI Pin Connections:

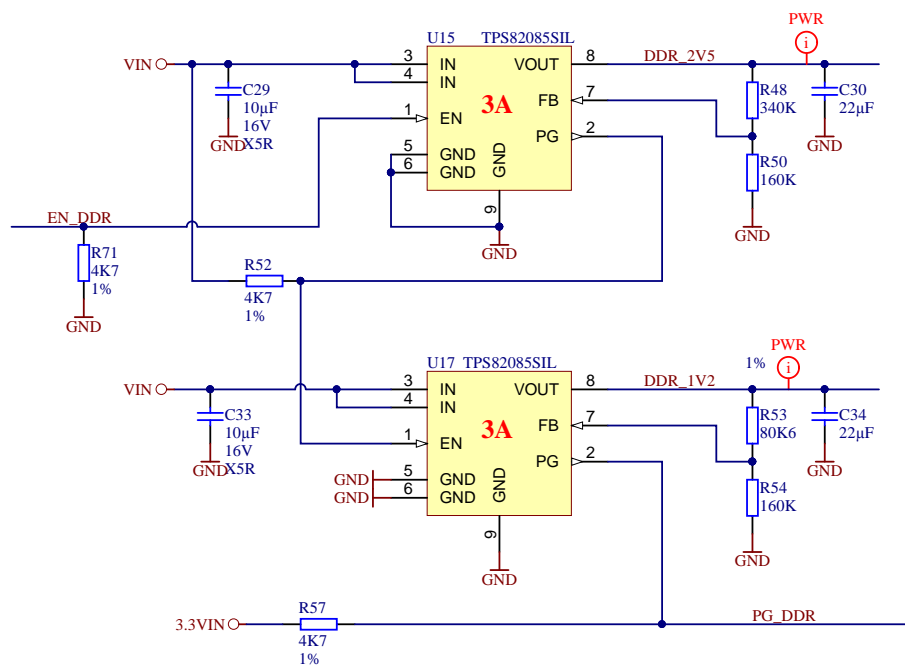
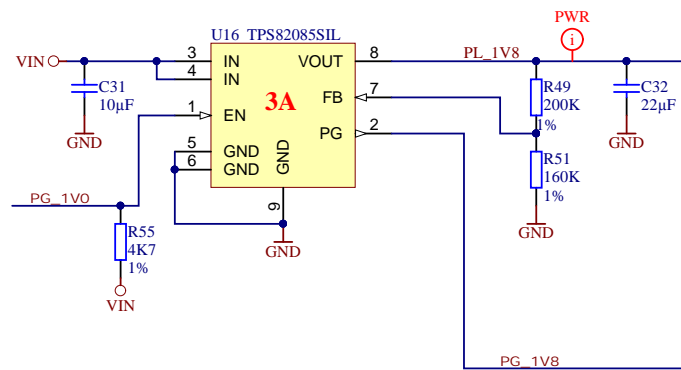
1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76



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Filename: PWR2.SchDoc		



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Filename: POWER_2.SchDoc		

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CHANGES REV01 TO REV01A (08.16.2017):

- 1) U1: changed schematic symbol. Next pins swapped to mach same polarity order:
- AE13 (IO_L6P_T0U_N10_AD6P_64)/AE12 (IO_L6N_T0U_N11_AD6N_64)
- J5 (IO_L18P_T2U_N10_AD2P_66)/J4 (IO_L18N_T2U_N11_AD2N_66)

2) Net names changed (no electrical changes):

- JM1: swapped signals B64_L6:
- B64_L6_N - pin 40 (was pin 42)
- B64_L6_P - pin 42 (was pin 40)
- JM3: swapped signals B64_L6:
- B66_L18_N - pin 52 (was pin 54)
- B66_L18_P - pin 54 (was pin 52)

CHANGES REV01A TO REV02 (03.2018):

- 1) U4 / U5: changed DDR4 chip: NT5AD256M16B2-GN -> K4A4G165WE-BCRC (K4A8G165WB-BIRC)
- 2) Fixed sense connection on DCDC
- 3) U6: changed SPI flash chip: N25Q256A11E1240E-> N25Q512A11G1240E
- 4) Full update LIB
- 5) Added additional resistors for support 16GBit DDR chips
- 6) Added strong pull-down to EN_PL
- 7) Added additional testpoints for I2C bus
- 8) Added additional MEMS oscillator (25MHz)
- 9) Changed pull-up power supply VIN -> 3.3VIN on the PG_DDR net
- 10) Added pull-down on the EN_DDR

A

A

B

B

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C

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D

1

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Title: TE0841 - Changes list		
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