

U\_FPGA-MGT  
FPGA-MGT.SchDoc

U\_FPGA-MISC  
FPGA-MISC.SchDoc

U\_FPGA-PWR  
FPGA-PWR.SchDoc

U\_FPGA-B44  
FPGA-B44.SchDoc

U\_FPGA-B45  
FPGA-B45.SchDoc

U\_FPGA-B46  
FPGA-B46.SchDoc

U\_FPGA-B47  
FPGA-B47.SchDoc

U\_FPGA-B64  
FPGA-B64.SchDoc

U\_FPGA-B65  
FPGA-B65.SchDoc

U\_FPGA-B66  
FPGA-B66.SchDoc

U\_FPGA-B67  
FPGA-B67.SchDoc

U\_FPGA-B68  
FPGA-B68.SchDoc

U\_DDR4-RAM  
DDR4-RAM.SchDoc

U\_DDR4-RAM\_2  
DDR4-RAM\_2.SchDoc

U\_B2B-Connectors  
B2B-Connectors.SchDoc

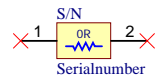
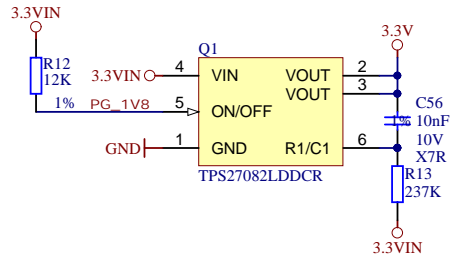
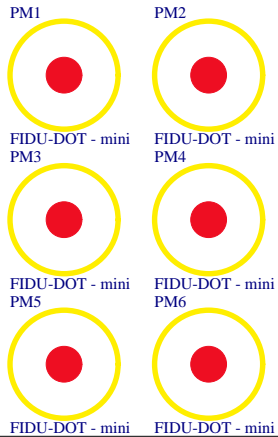
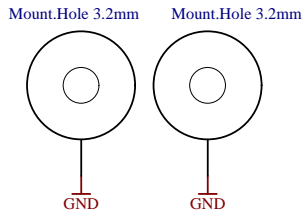
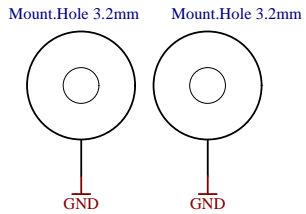
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CPLD.SchDoc

U\_Clock  
Clock.SchDoc

U\_PWR1  
PWR1.SchDoc

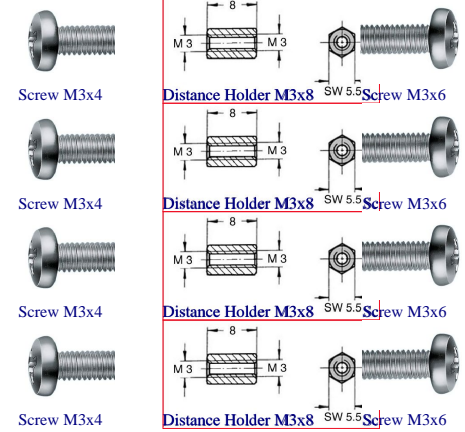
U\_PWR2  
PWR2.SchDoc

U\_POWER\_2  
POWER\_2.SchDoc

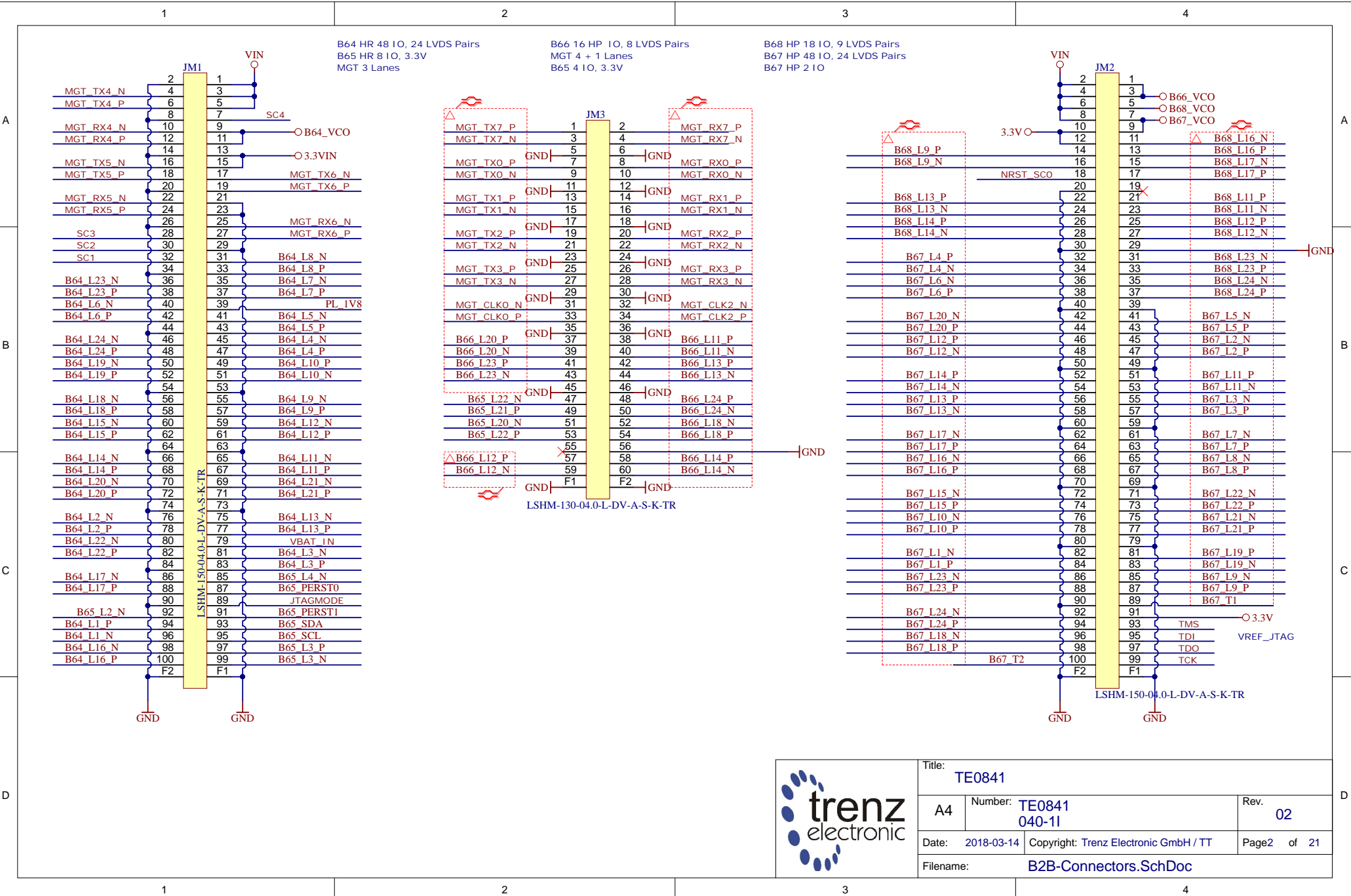


Serial  
Serial  
Serialnumber 6,3 x 6.3mm

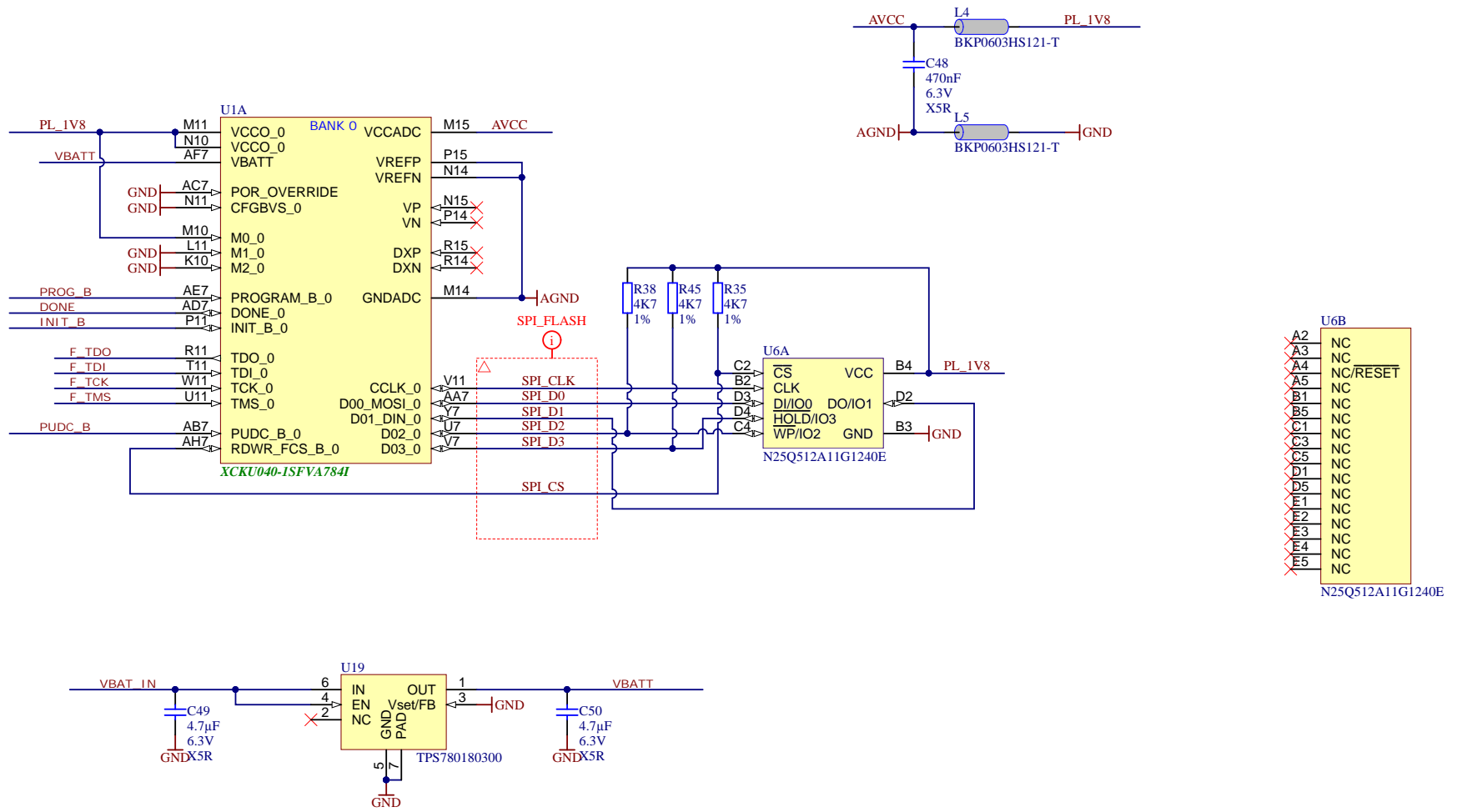
Top of Board



Title: TE0841		
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Filename: TE0841.SchDoc		



Title: TE0841		
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Filename: B2B-Connectors.SchDoc		

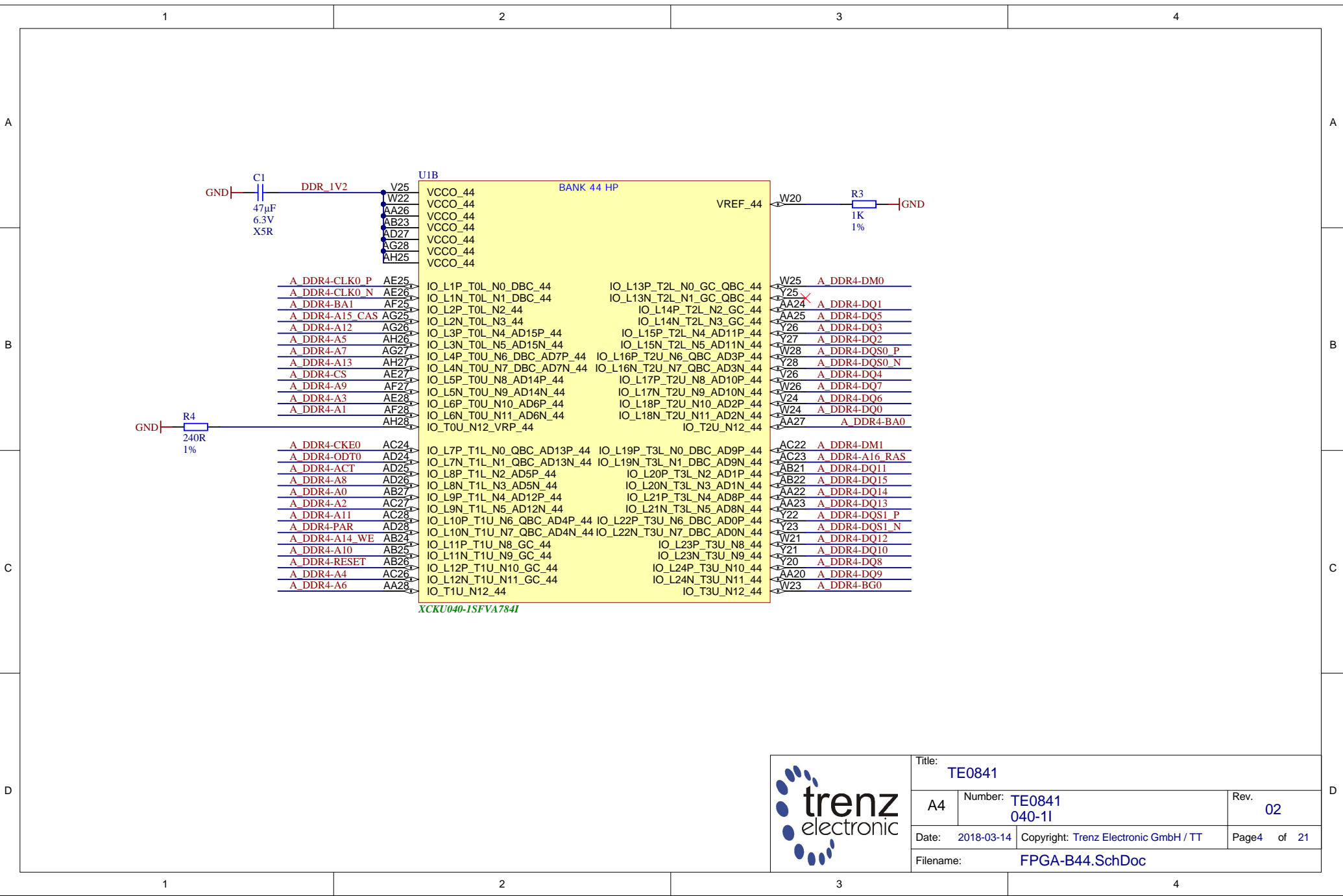


U6B

A2	NC
A3	NC
A4	NC/RESET
A5	NC
B1	NC
B5	NC
C1	NC
C3	NC
C5	NC
D1	NC
D5	NC
E1	NC
E2	NC
E3	NC
E4	NC
E5	NC

N25Q512A11G1240E

	Title: TE0841		
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XCKU040-1SFVA7841

	Title: TE0841	
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Filename: FPGA-B44.SchDoc		

1

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A

A

B

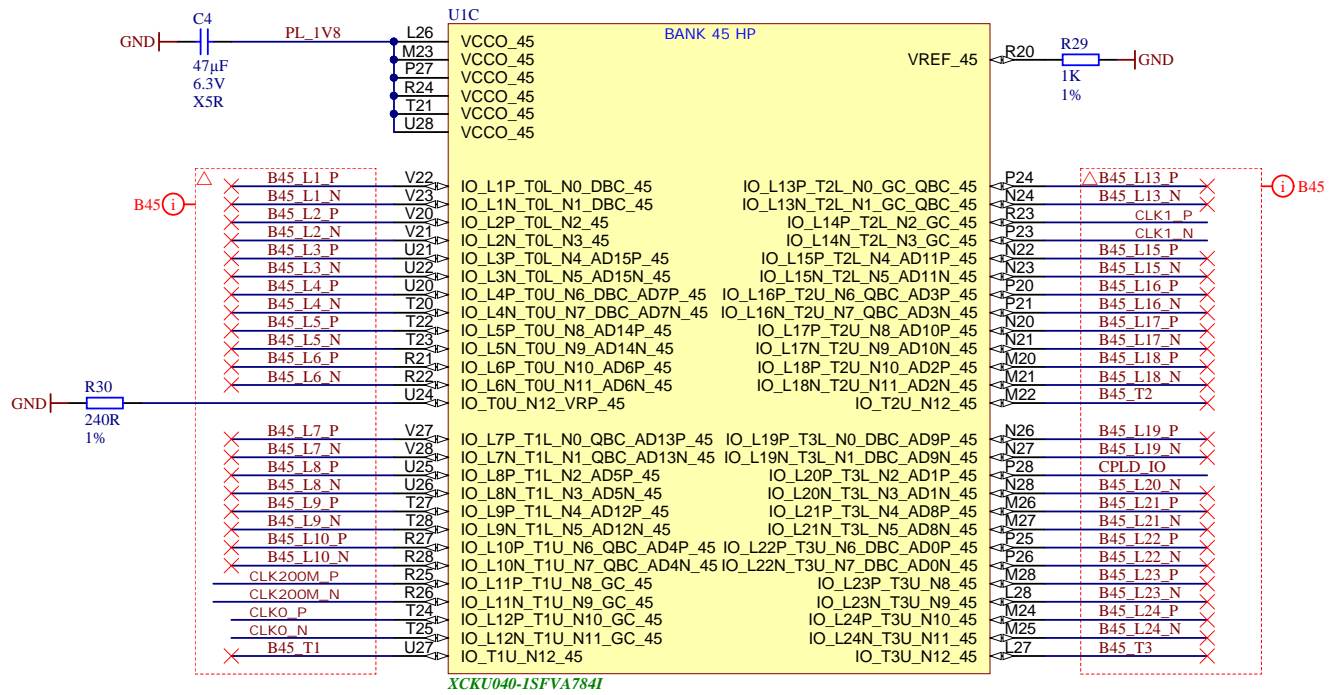
B

C

C

D

D



Title: TE0841		
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Filename: FPGA-B45.SchDoc		

1

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1

2

3

4

A

A

B

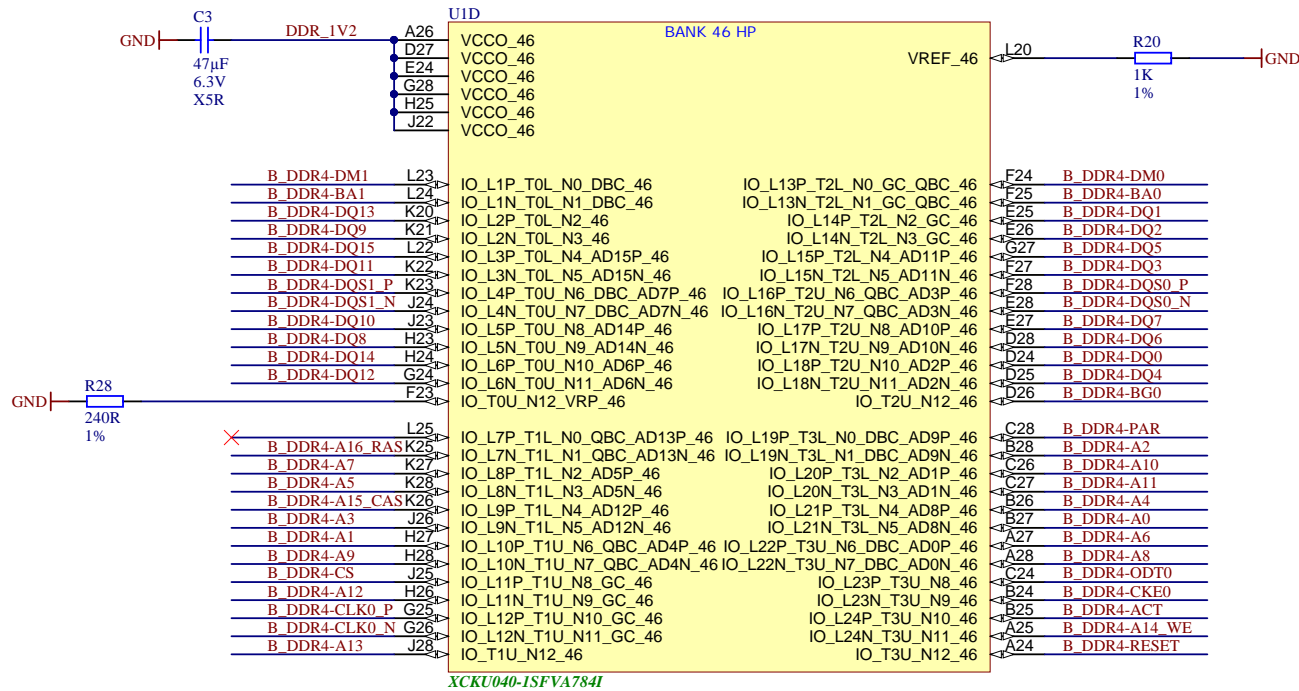
B

C

C

D

D



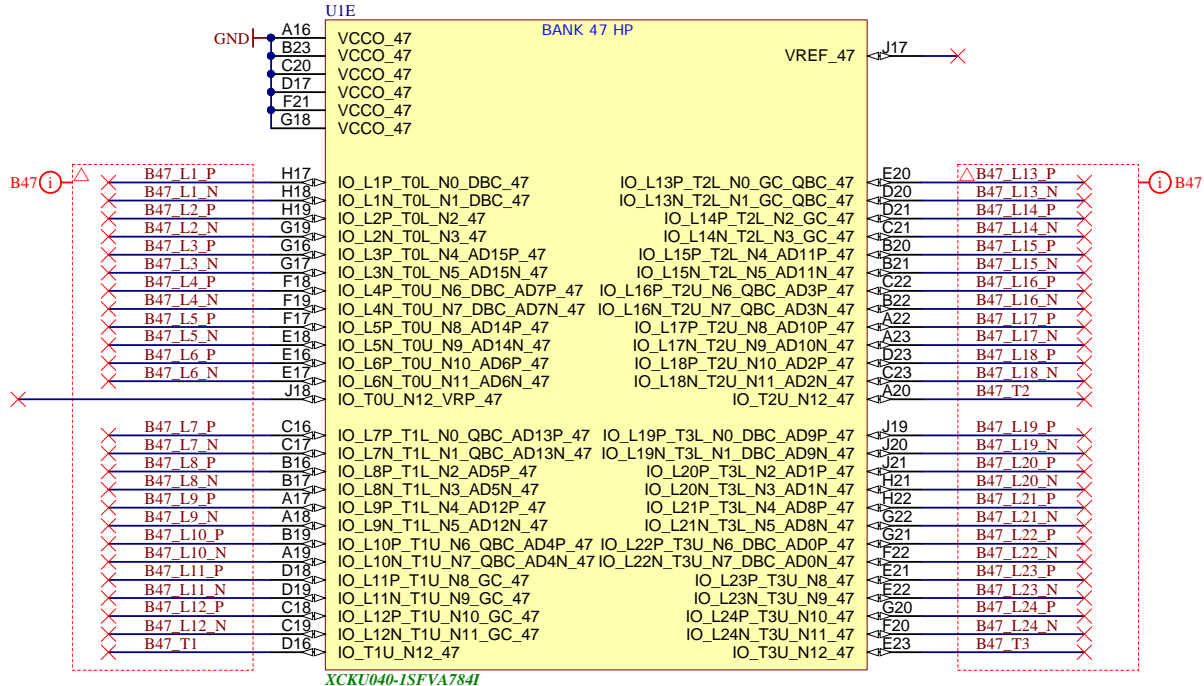

Title: <b>TE0841</b>		
A4	Number: <b>TE0841 040-11</b>	Rev. <b>02</b>
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Filename: <b>FPGA-B46.SchDoc</b>		

1

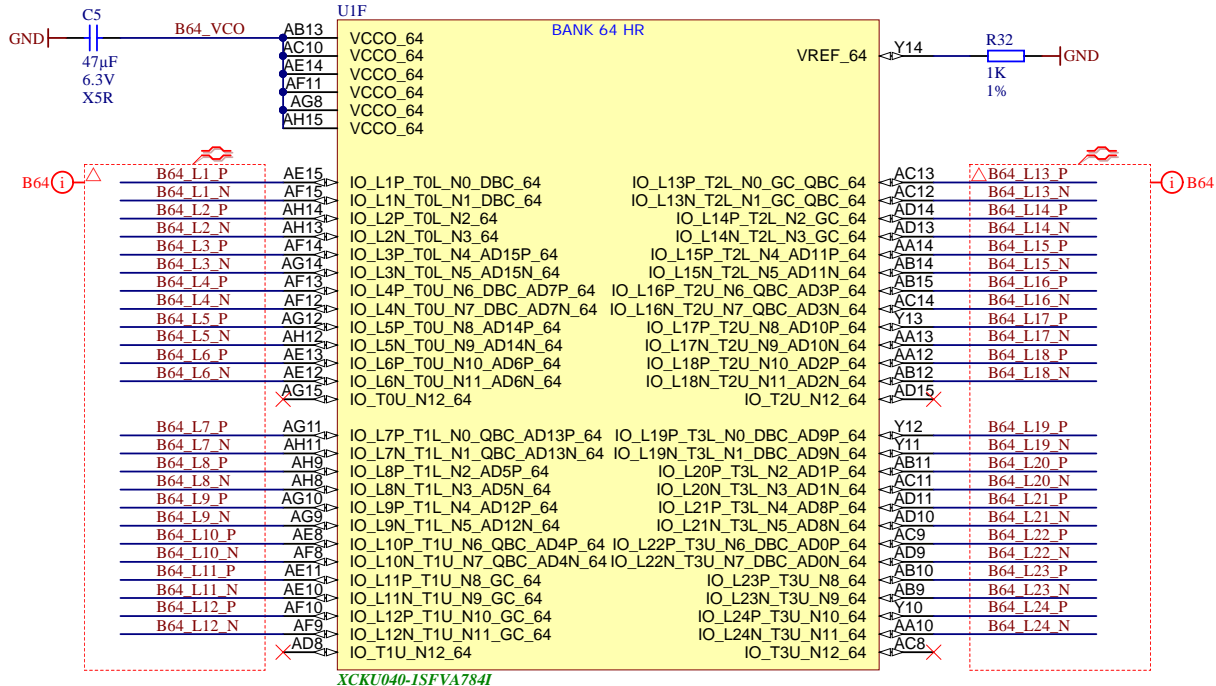
2

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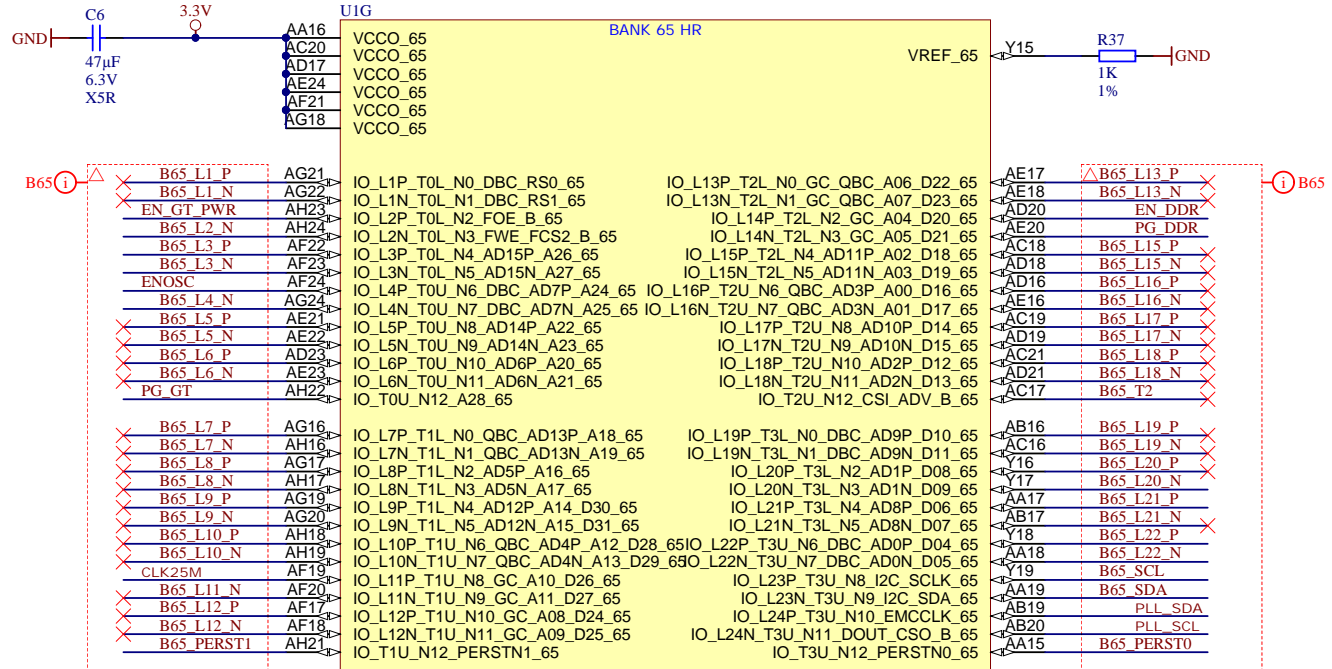



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A4	Number: <b>TE0841 040-11</b>	Rev. <b>02</b>
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Filename: <b>FPGA-B47.SchDoc</b>		



	Title: TE0841	
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	Filename: FPGA-B64.SchDoc	Rev. 02
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XCKU040-ISFVA784I



Title: TE0841		
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Filename: FPGA-B65.SchDoc		

1

2

3

4

A

A

B

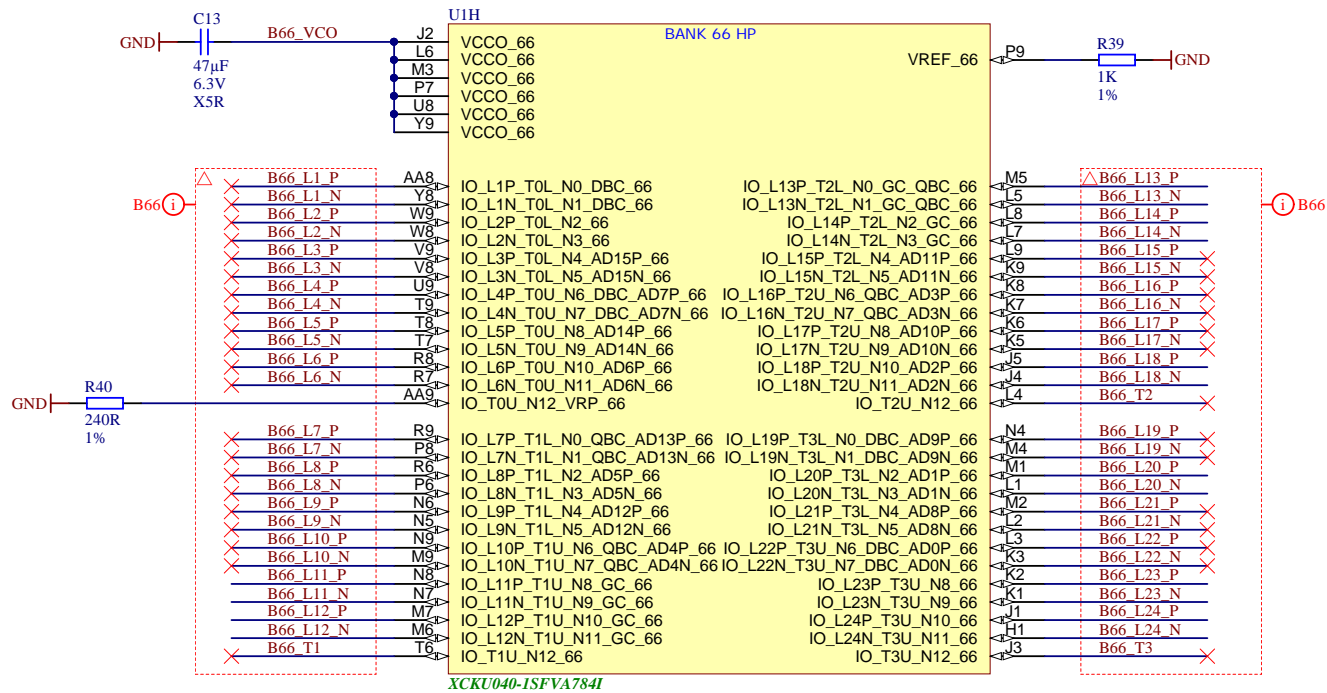

B

C

C

D

D

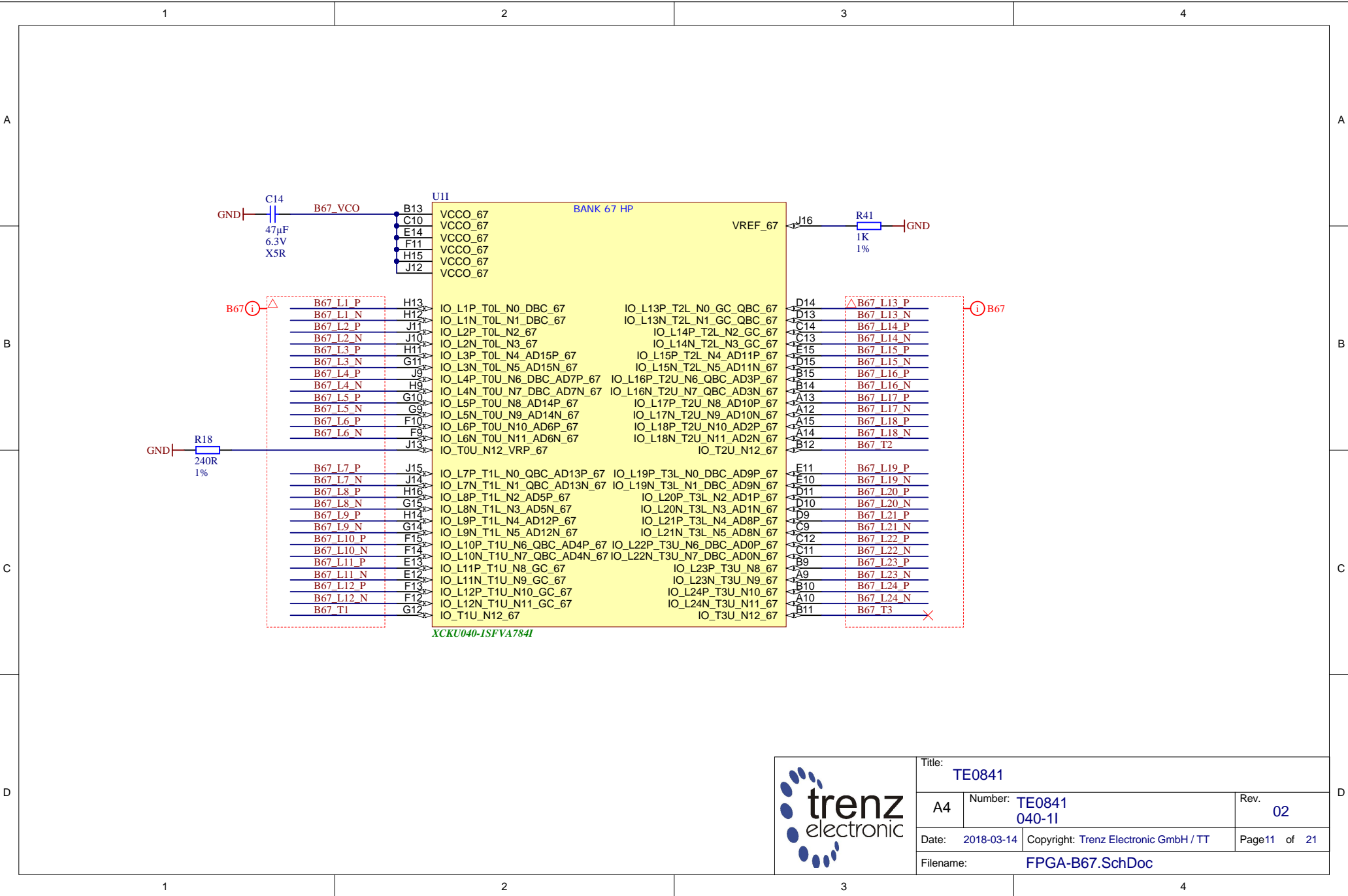
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A4	Number: TE0841 040-11	Rev. 02
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Filename: FPGA-B66.SchDoc		

1

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3

4



Title: TE0841		
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Filename: FPGA-B67.SchDoc		

1

2

3

4

A

A

B

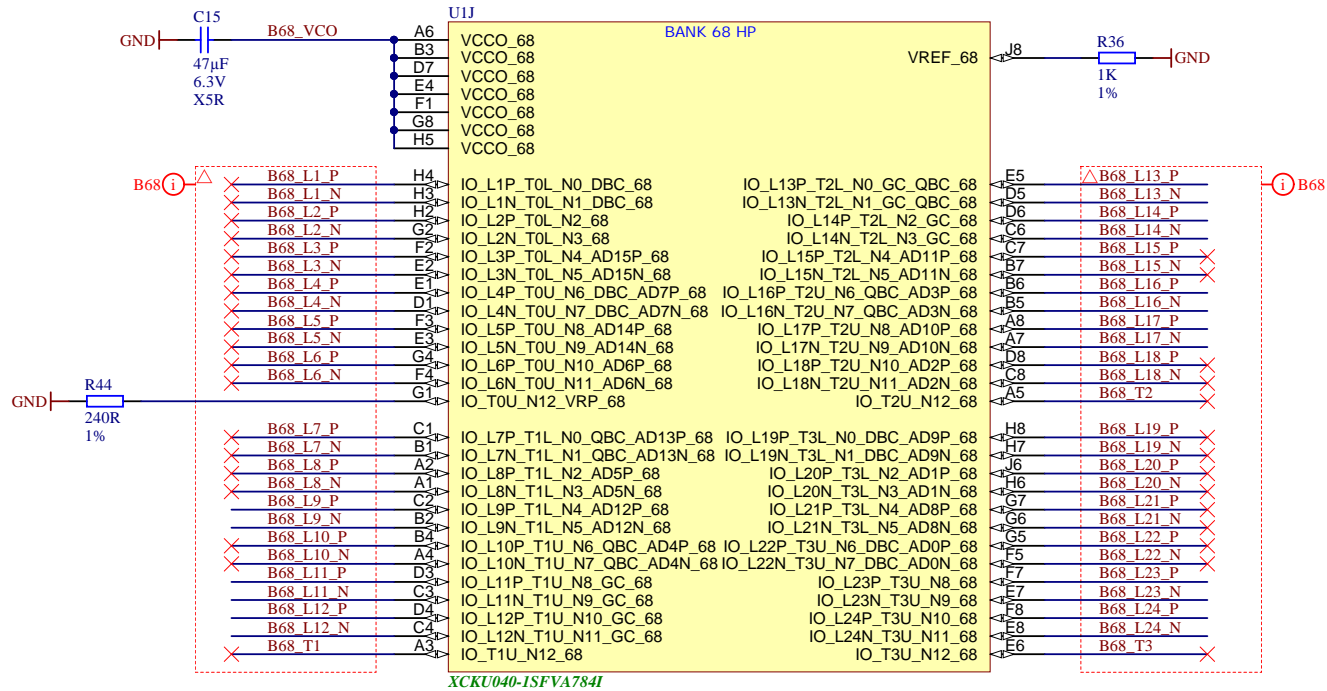
B

C

C

D

D



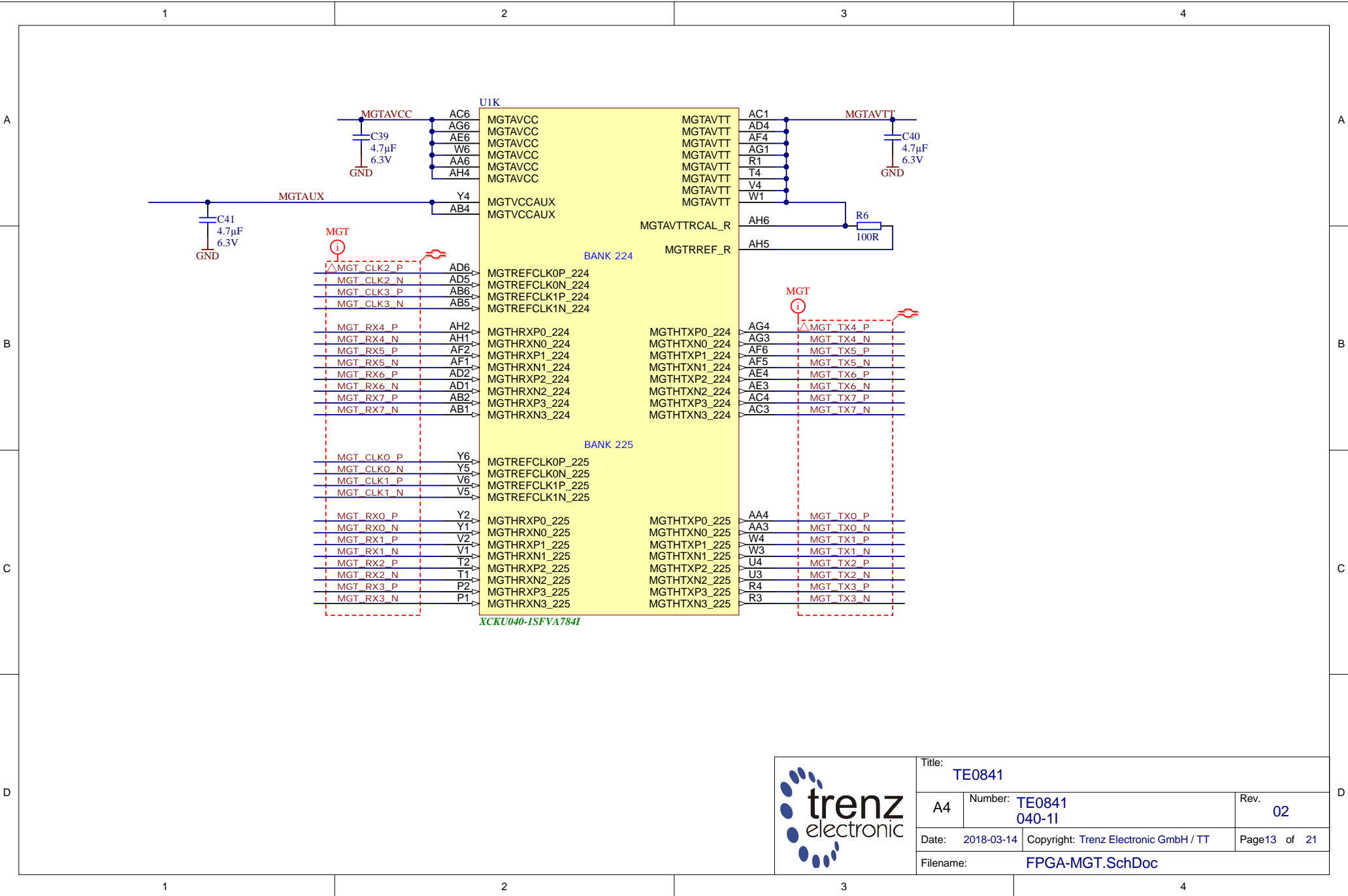
Title: TE0841		
A4	Number: TE0841 040-11	Rev. 02
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Filename: FPGA-B68.SchDoc		

1

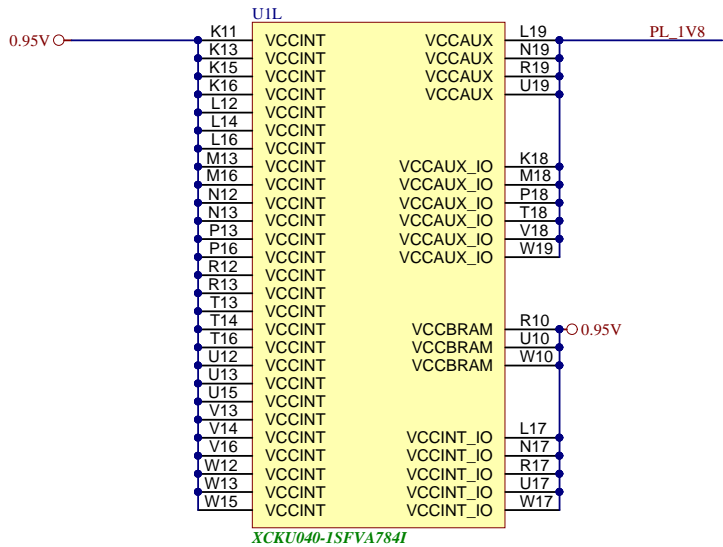
2

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Title: TE0841		
A4	Number: TE0841 040-11	Rev. 02
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Filename: FPGA-MGT.SchDoc		

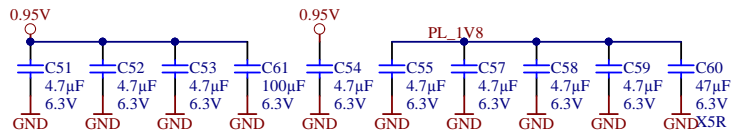


XCKU040-1SFVA784I

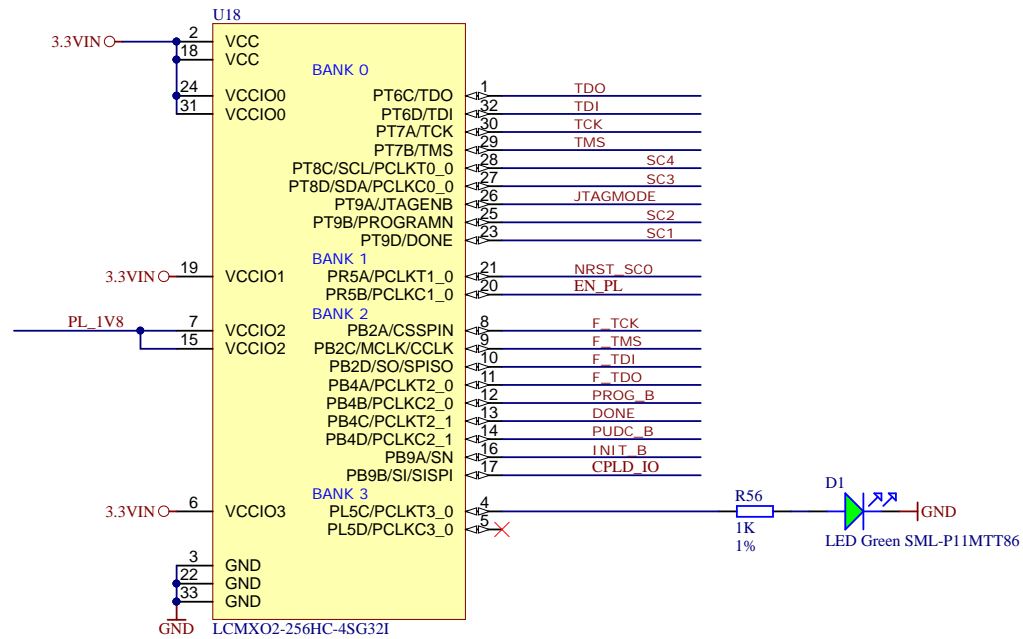



XCKU040-1SFVA784I

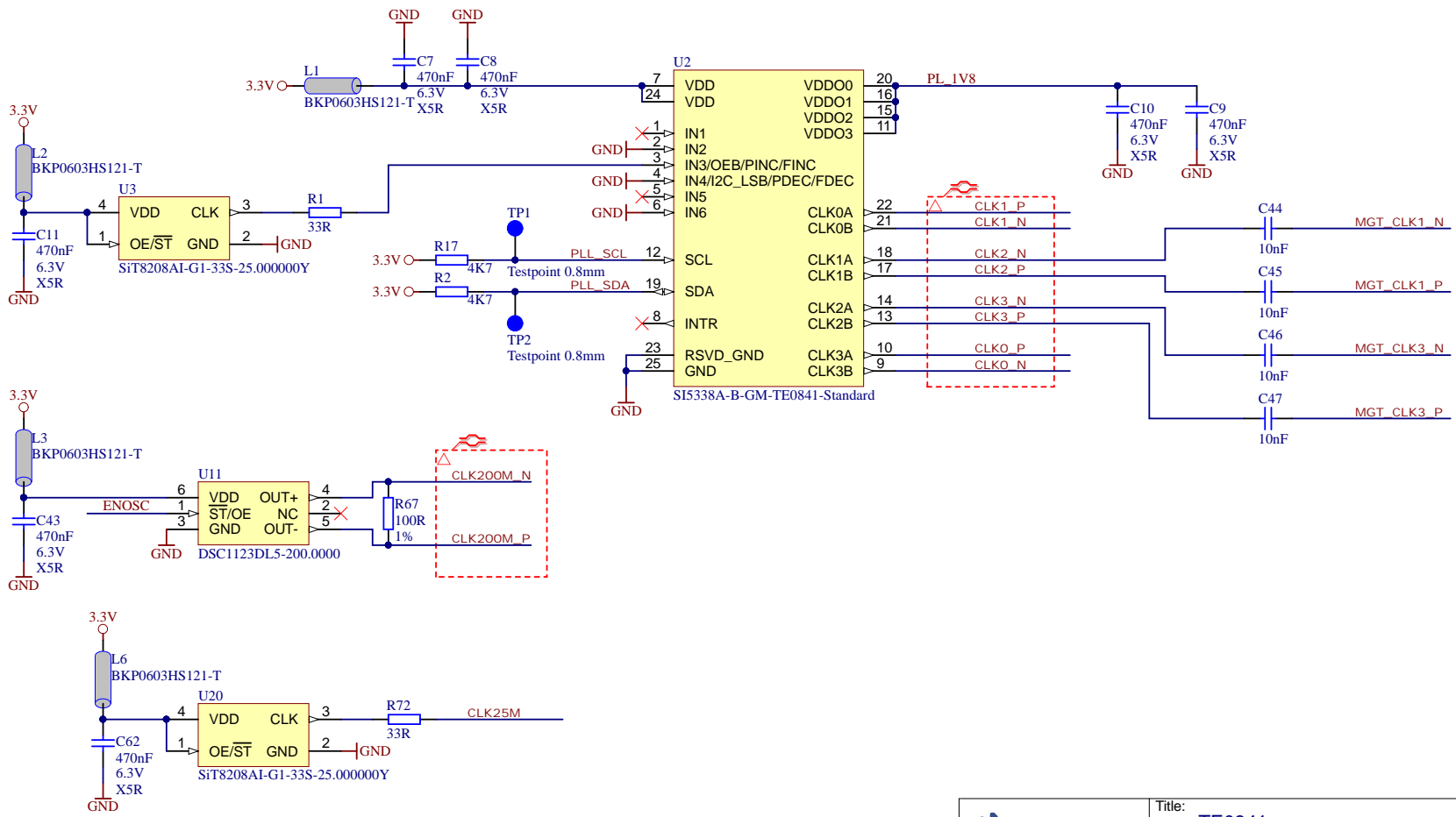
XCKU040-1SFVA784I




Title: TE0841		
A4	Number: TE0841 040-11	Rev. 02
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Filename: FPGA-PWR.SchDoc		

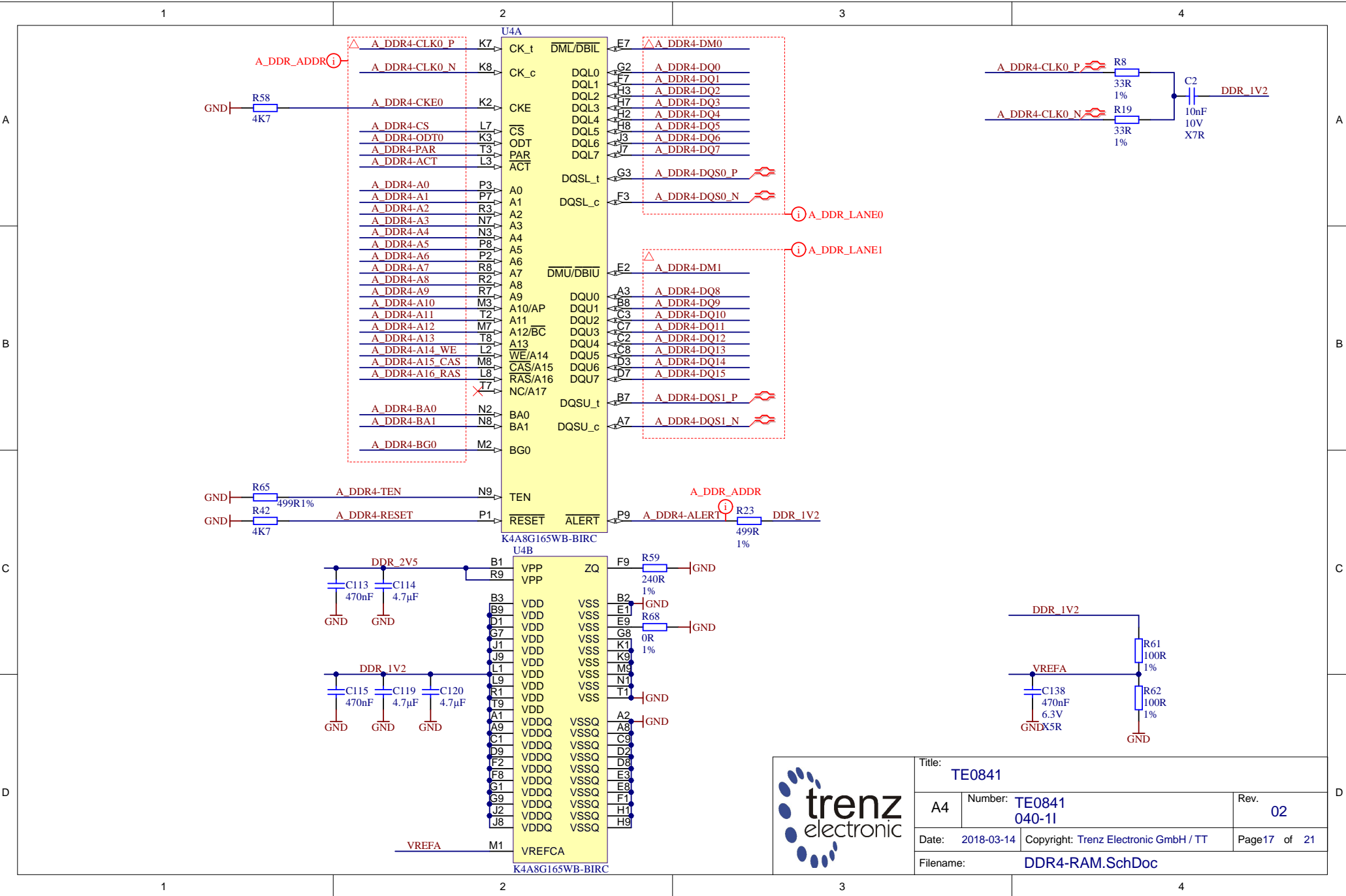


	Title: TE0841		
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	Filename: CPLD.SchDoc		



		Title: TE0841	
		A4	Number: TE0841 040-11
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Filename: Clock.SchDoc		Page 16 of 21	





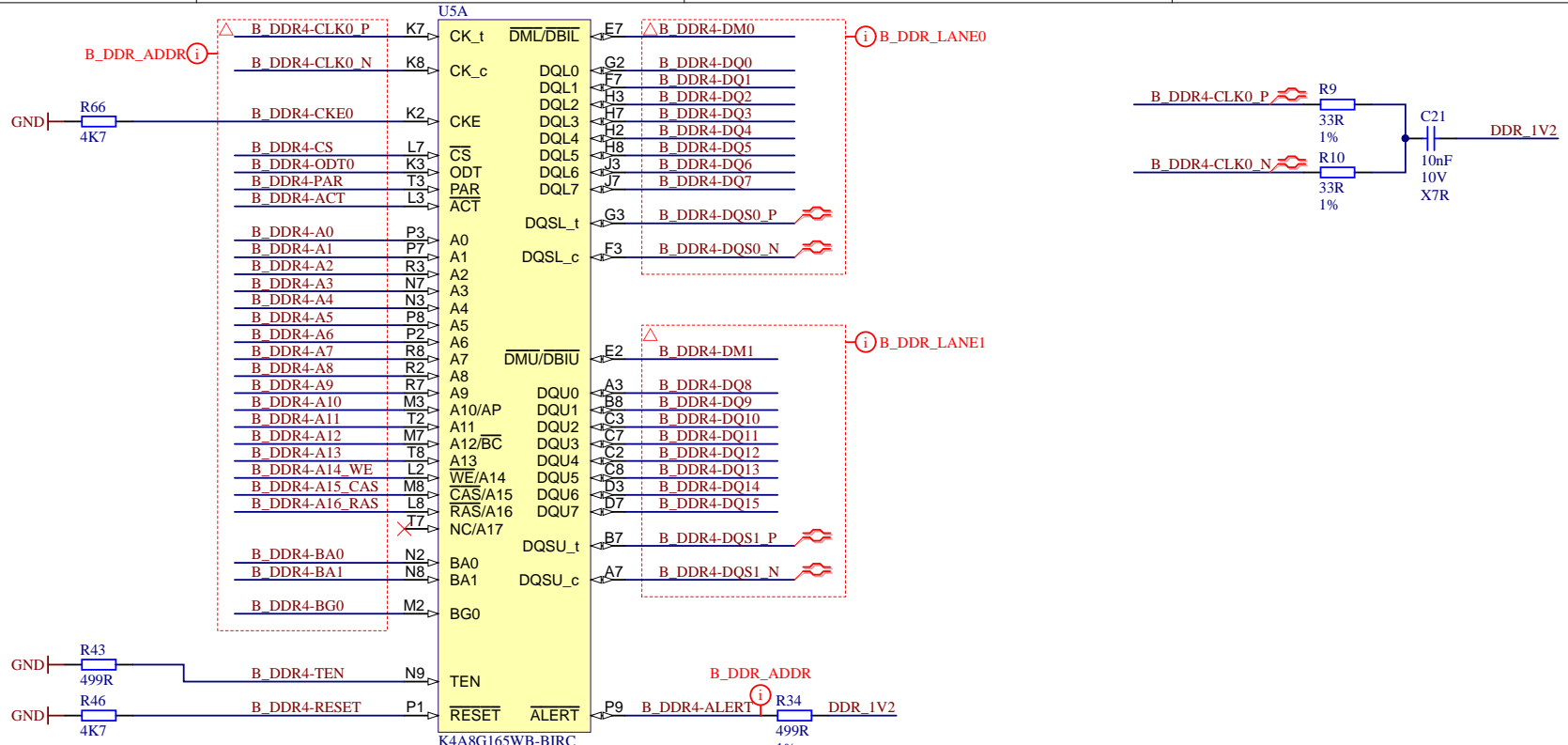
Title: TE0841		
A4	Number: TE0841 040-11	Rev. 02
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Filename: DDR4-RAM.SchDoc		

1

2

3

4



A

B

C

A

B

C

D

B

C

D

A

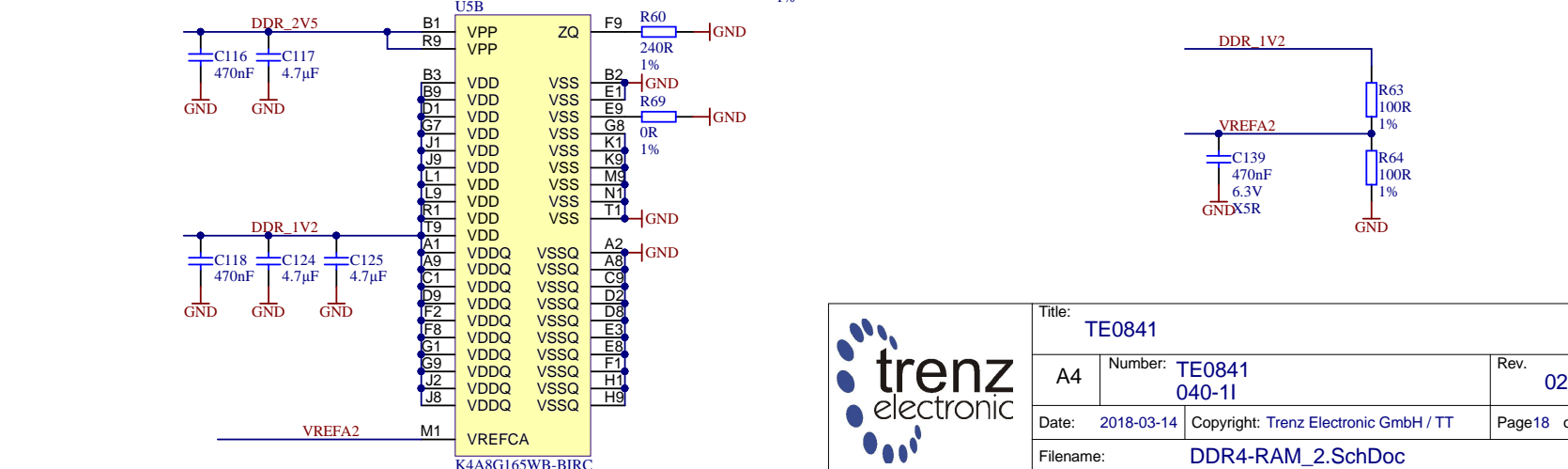
C

D

A

B

D



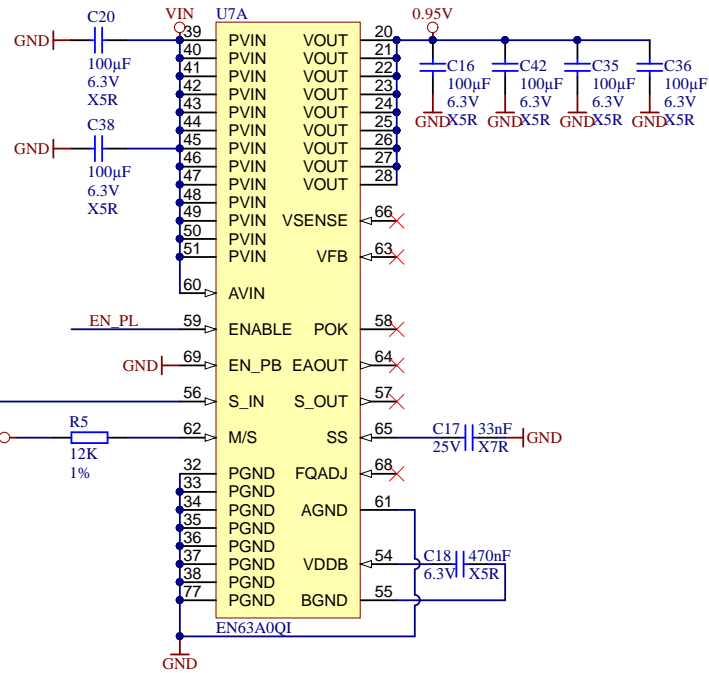
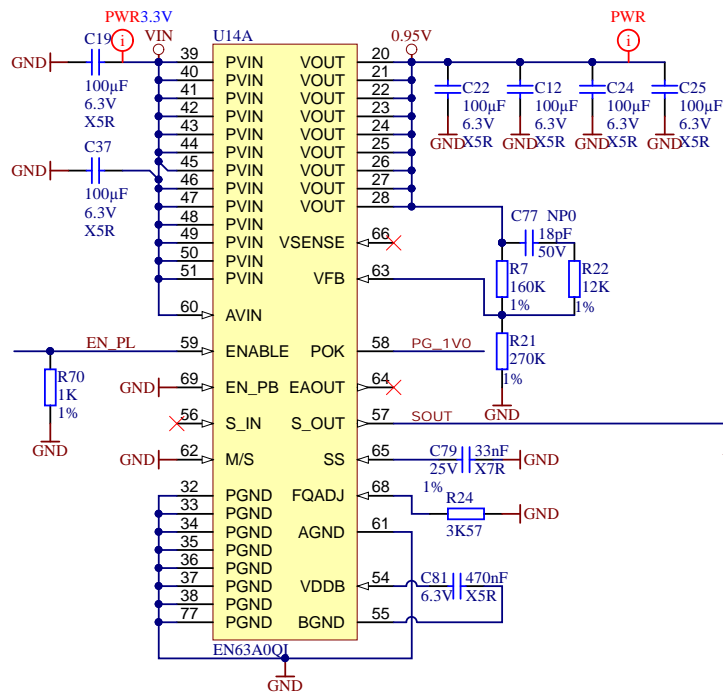
Title: TE0841		
A4	Number: TE0841 040-11	Rev. 02
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Filename: DDR4-RAM_2.SchDoc		

1

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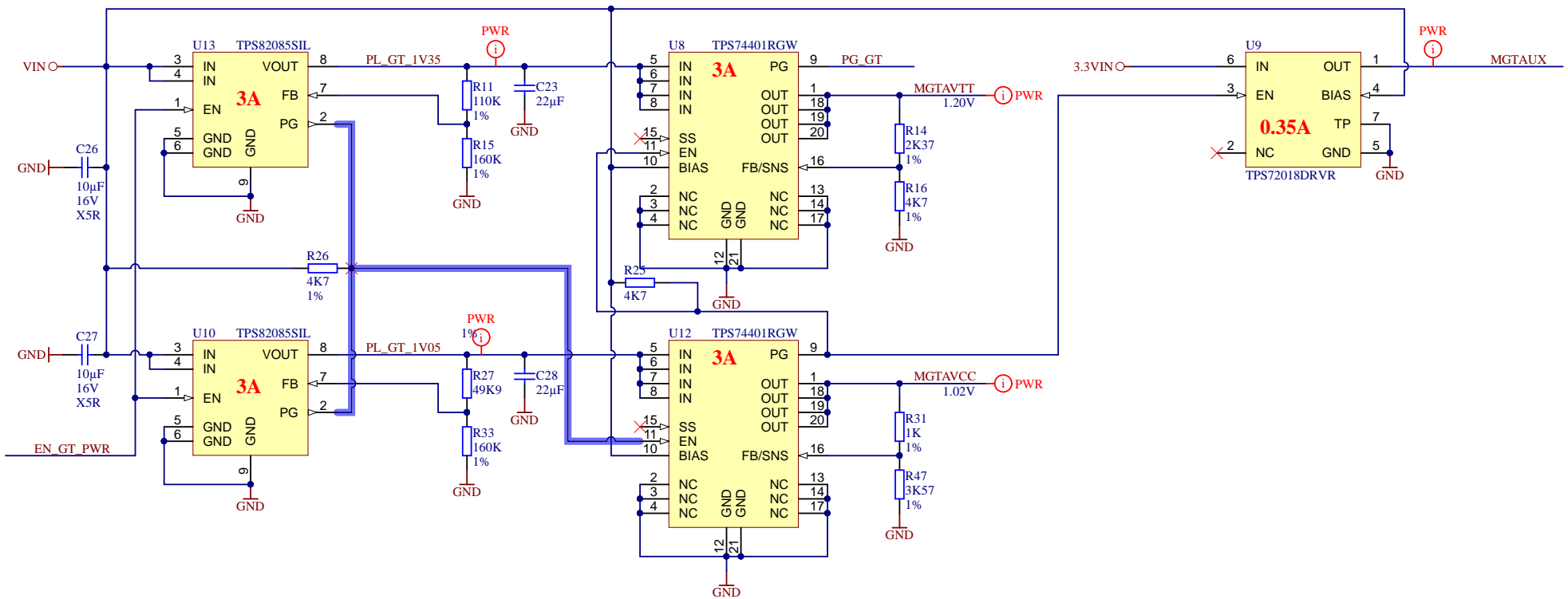
U14B			
1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76

EN63A0QI

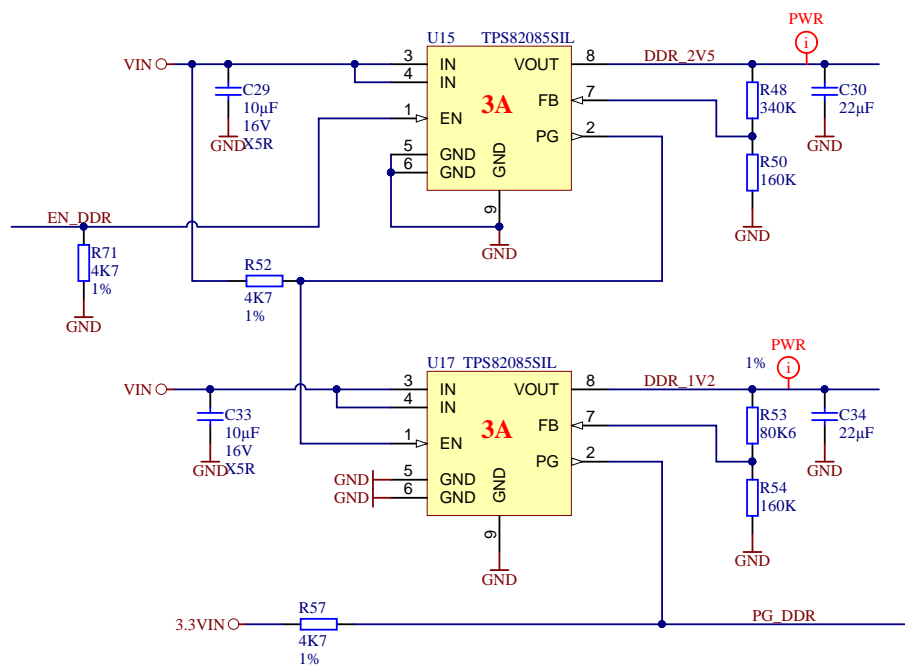
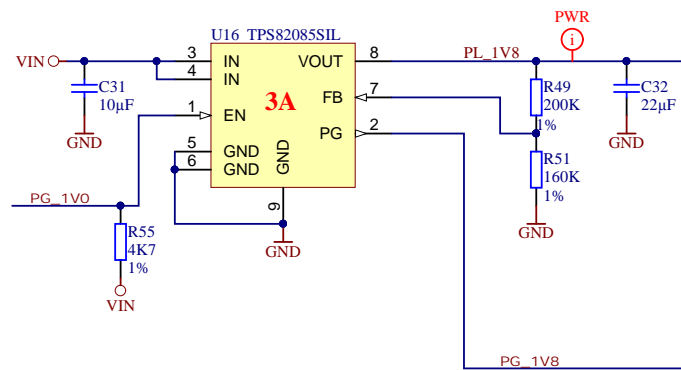
U7B			
1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76

EN63A0QI

	Title: TE0841		
	A4	Number: TE0841 040-11	Rev. 02
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	Filename: PWR1.SchDoc		



Title: TE0841		
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Filename: PWR2.SchDoc		



Title: TE0841		
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Filename: POWER_2.SchDoc		

1

2

3

4

CHANGES REV01 TO REV01A (08.16.2017):

- 1) U1: changed schematic symbol. Next pins swapped to mach same polarity order:
  - AE13 (IO\_L6P\_T0U\_N10\_AD6P\_64)/AE12 (IO\_L6N\_T0U\_N11\_AD6N\_64)
  - J5 (IO\_L18P\_T2U\_N10\_AD2P\_66)/J4 (IO\_L18N\_T2U\_N11\_AD2N\_66)

2) Net names changed (no electrical changes):

- JM1: swapped signals B64\_L6:
  - B64\_L6\_N - pin 40 (was pin 42)
  - B64\_L6\_P - pin 42 (was pin 40)
- JM3: swapped signals B64\_L6:
  - B66\_L18\_N - pin 52 (was pin 54)
  - B66\_L18\_P - pin 54 (was pin 52)

CHANGES REV01A TO REV02 ( 03.2018):

- 1) U4 / U5: changed DDR4 chip: NT5AD256M16B2-GN -> K4A4G165WE-BCRC (K4A8G165WB-BIRC)
- 2) Fixed sense connection on DCDC
- 3) U6: changed SPI flash chip: N25Q256A11E1240E-> N25Q512A11G1240E
- 4) Full update LIB
- 5) Added additional resistors for support 16GBit DDR chips
- 6) Added strong pull-down to EN\_PL
- 7) Added additional testpoints for I2C bus
- 8) Added additional MEMS oscillator (25MHz)
- 9) Changed pull-up power supply VIN -> 3.3VIN on the PG\_DDR net
- 10) Added pull-down on the EN\_DDR

A

A

B

B

C

C

D

D

1

2

3

4



Title: <b>TE0841 - Changes list</b>		
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Filename: <b>Revision_Changes.SchDoc</b>		