

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-MISC
FPGA-MISC.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_FPGA-B44
FPGA-B44.SchDoc

U_FPGA-B45
FPGA-B45.SchDoc

U_FPGA-B46
FPGA-B46.SchDoc

U_FPGA-B47
FPGA-B47.SchDoc

U_FPGA-B64
FPGA-B64.SchDoc

U_FPGA-B65
FPGA-B65.SchDoc

U_FPGA-B66
FPGA-B66.SchDoc

U_FPGA-B67
FPGA-B67.SchDoc

U_FPGA-B68
FPGA-B68.SchDoc

U_DDR4-RAM
DDR4-RAM.SchDoc

U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

U_B2B-Connectors
B2B-Connectors.SchDoc

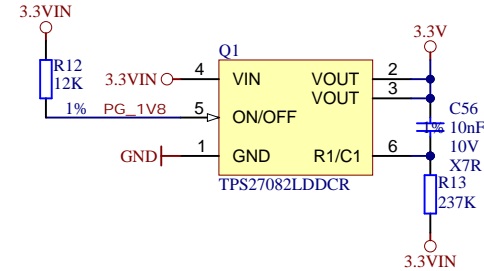
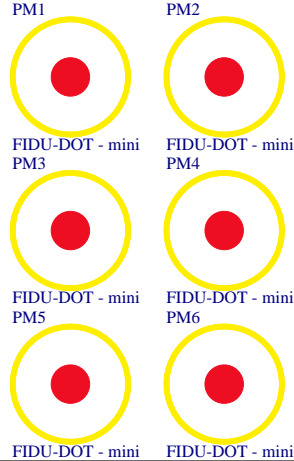
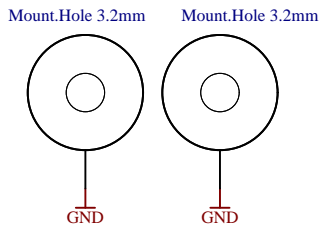
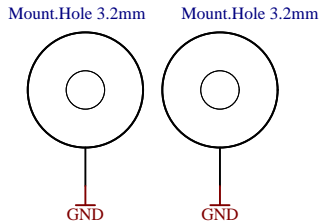
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CPLD.SchDoc

U_Clock
Clock.SchDoc

U_PWR1
PWR1.SchDoc

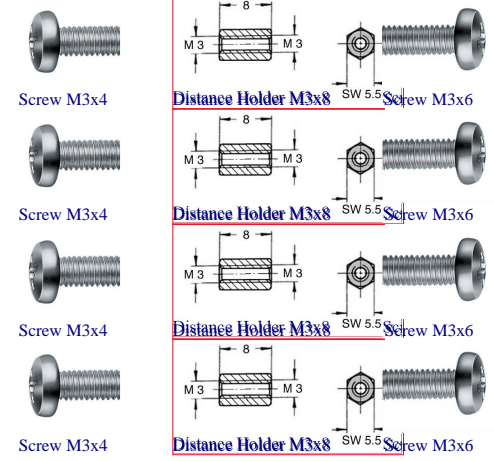
U_PWR2
PWR2.SchDoc

U_POWER_2
POWER_2.SchDoc



Serial
Serialnumber 6,3 x 6.3mm

Top of Board



Assembly variant	31C21-A
Created by	VY
Modified by	VY
Modified at	2019-07-10
SVN Revision	8580



Title: TE0841		
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1

2

3

4

B64 HR 48 IO, 24 LVDS Pairs
 B65 HR 8 IO, 3.3V
 MGT 3 Lanes

B66 16 HP IO, 8 LVDS Pairs
 MGT 4 + 1 Lanes
 B65 4 IO, 3.3V

B68 HP 18 IO, 9 LVDS Pairs
 B67 HP 48 IO, 24 LVDS Pairs
 B67 HP 2 IO

A

A

B

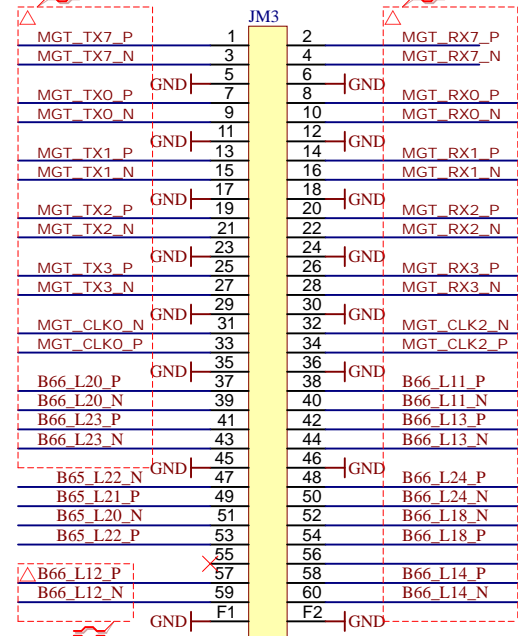
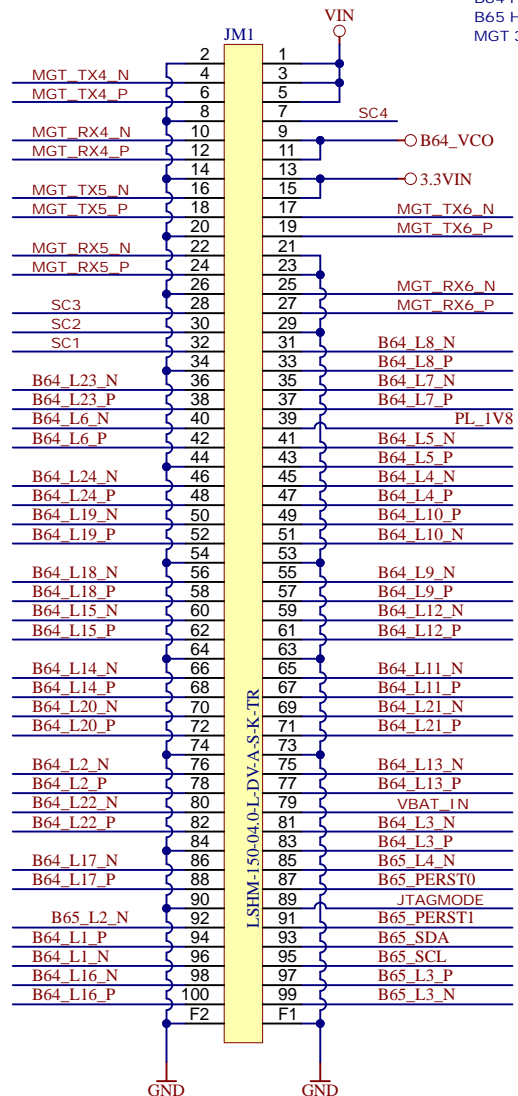
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C

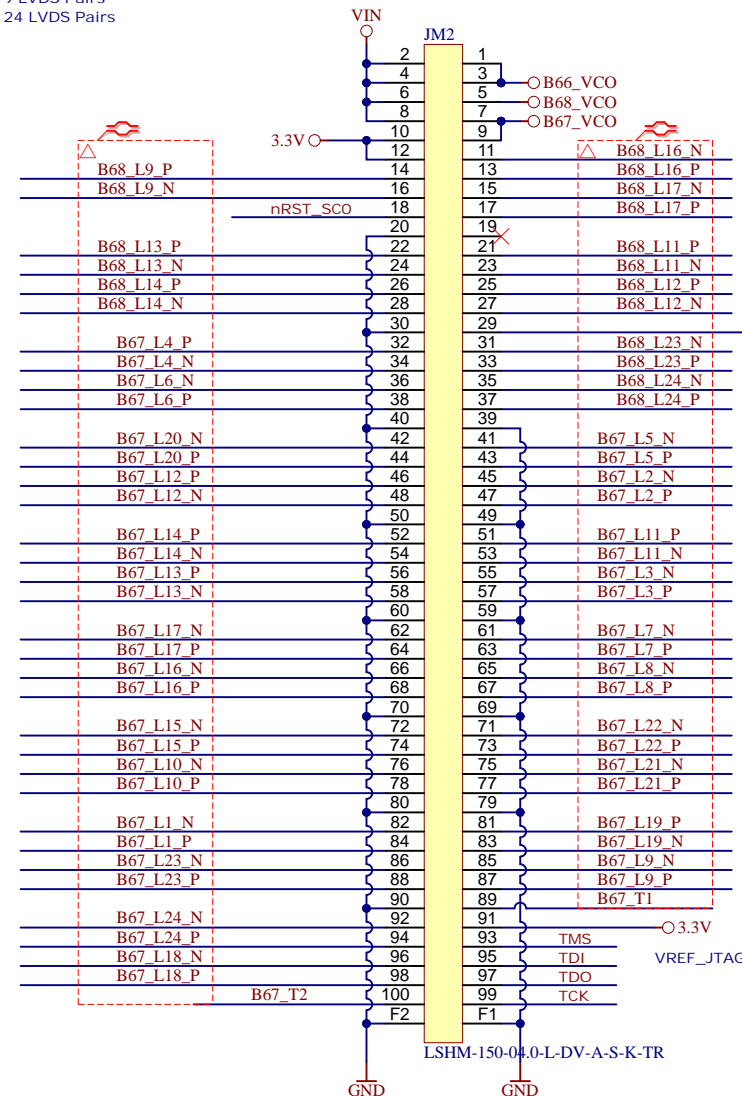
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D

D



LSHM-130-04-0-L-DV-A-S-K-TR



LSHM-150-04-0-L-DV-A-S-K-TR



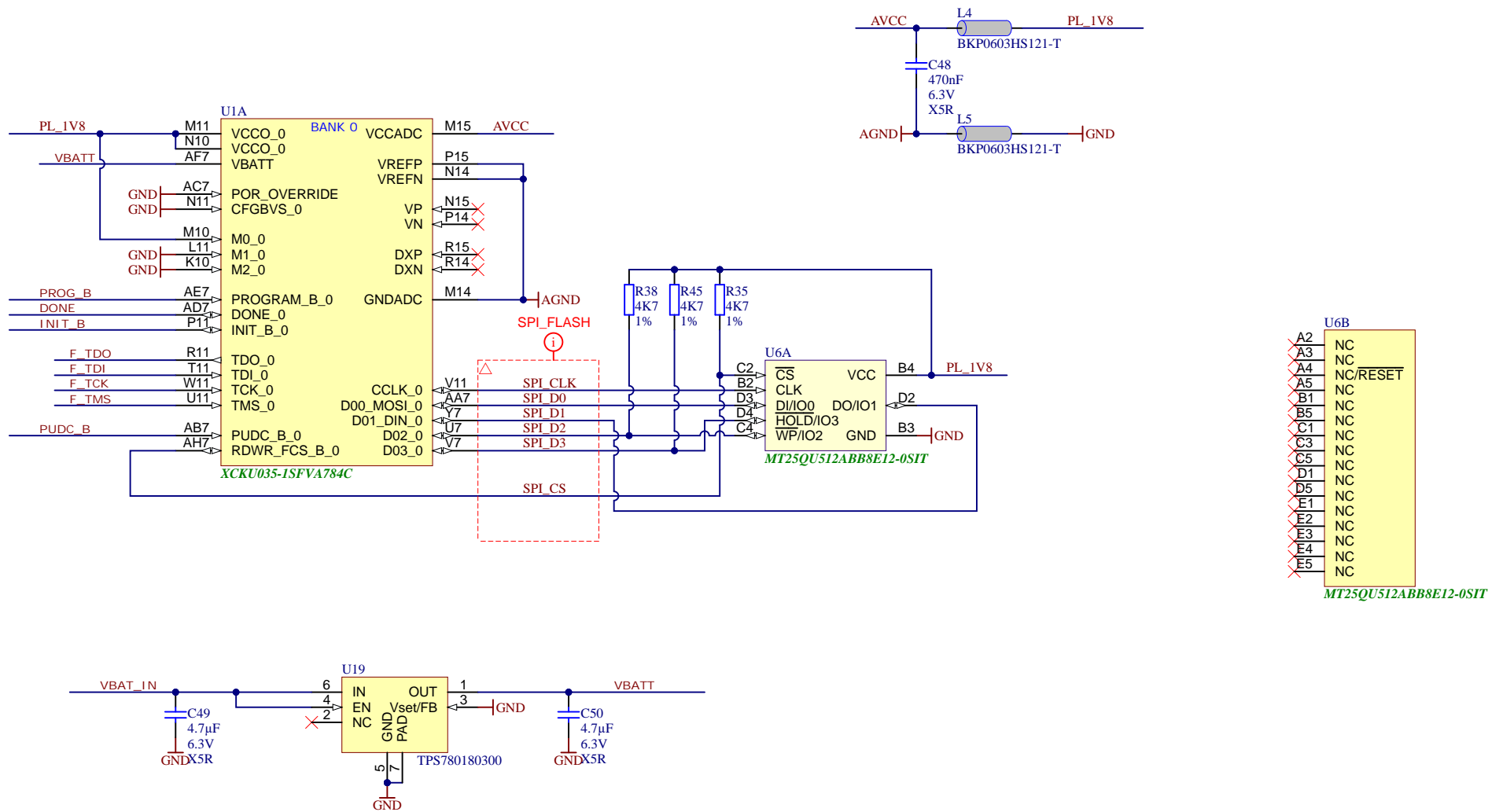
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Filename: B2B-Connectors.SchDoc		

1

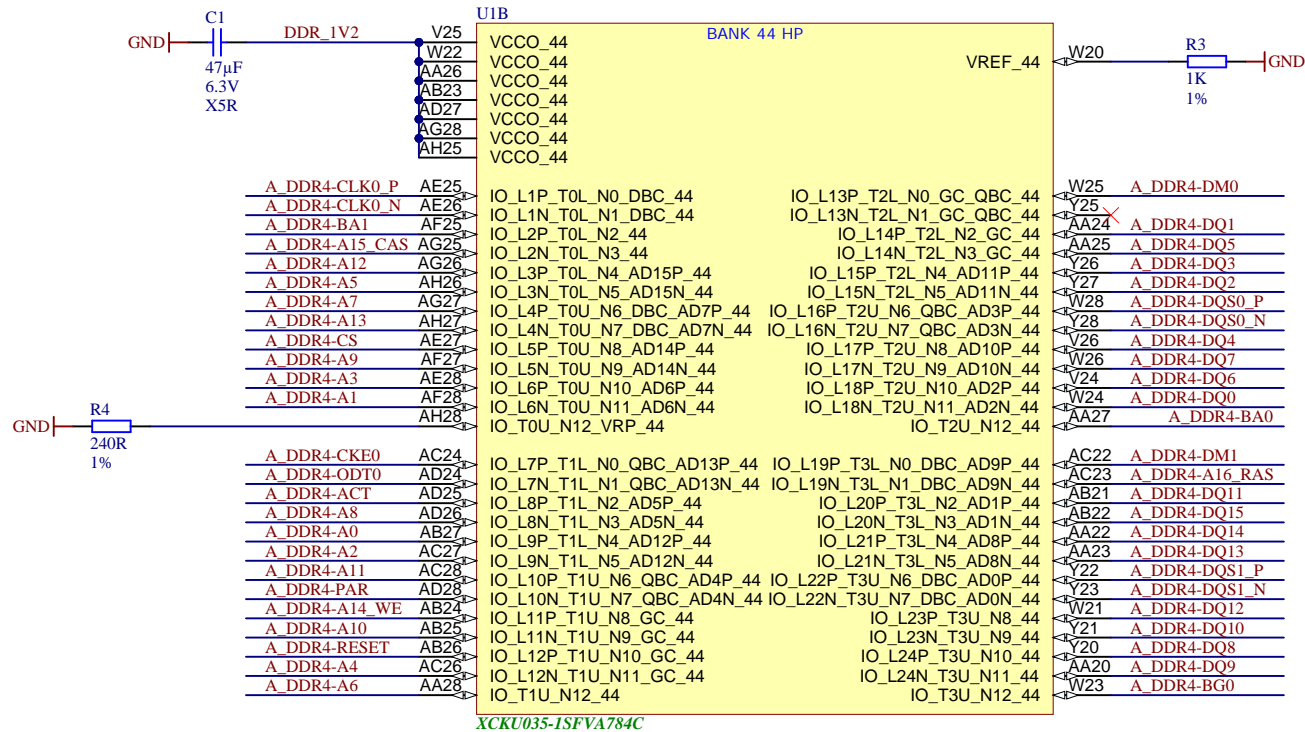
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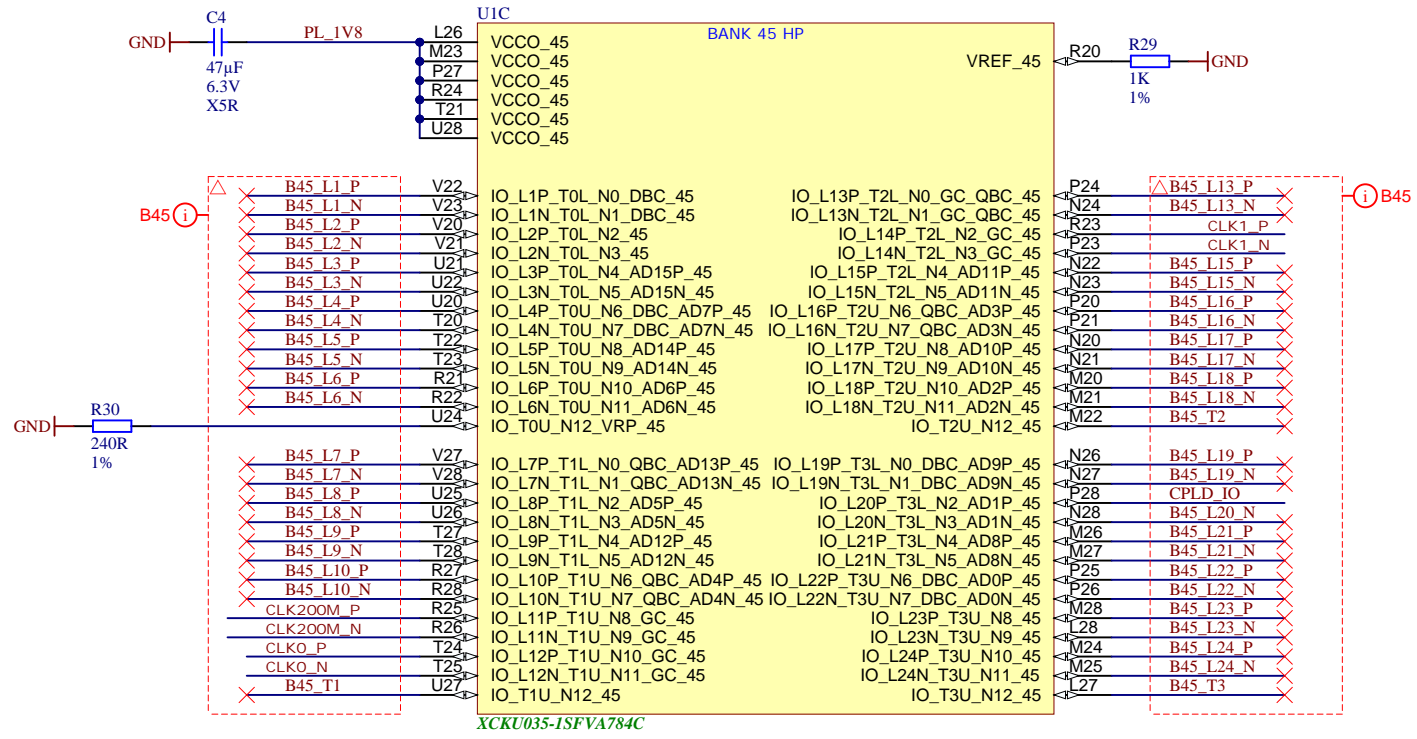
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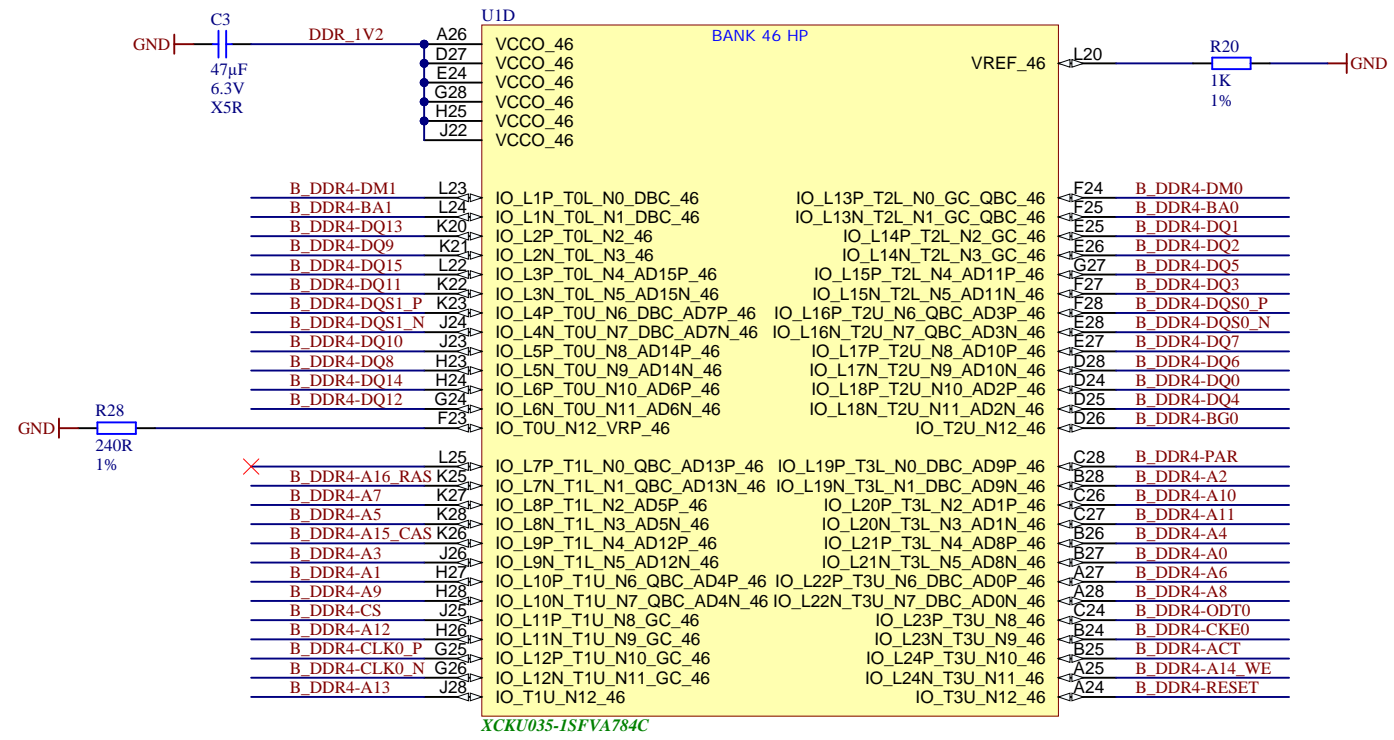

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	Filename: FPGA-MISC.SchDoc		



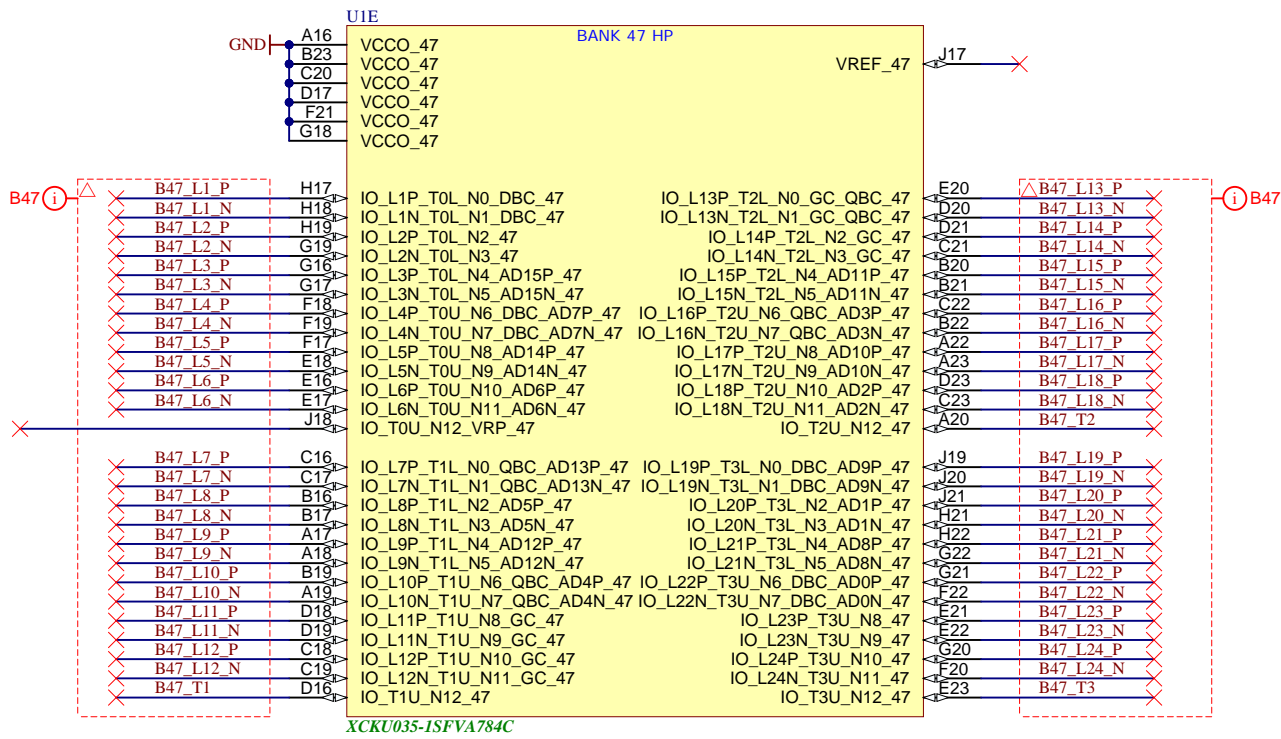
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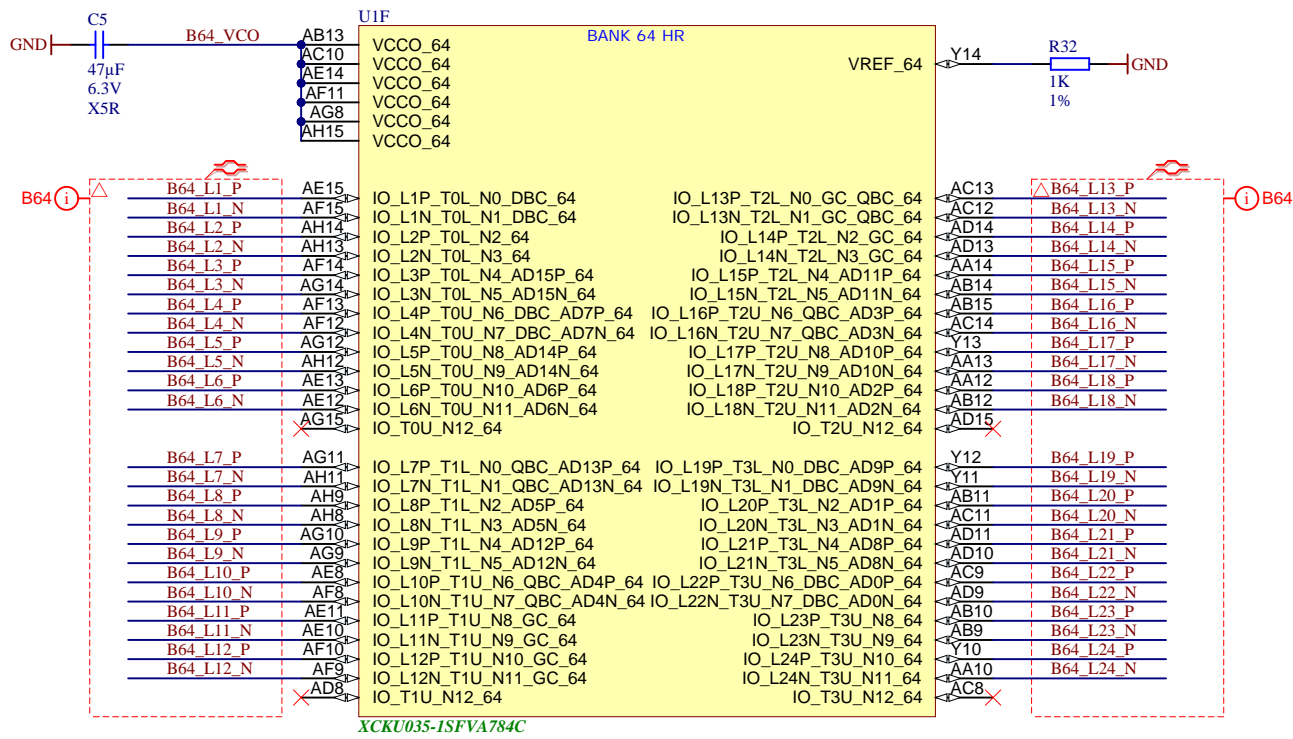
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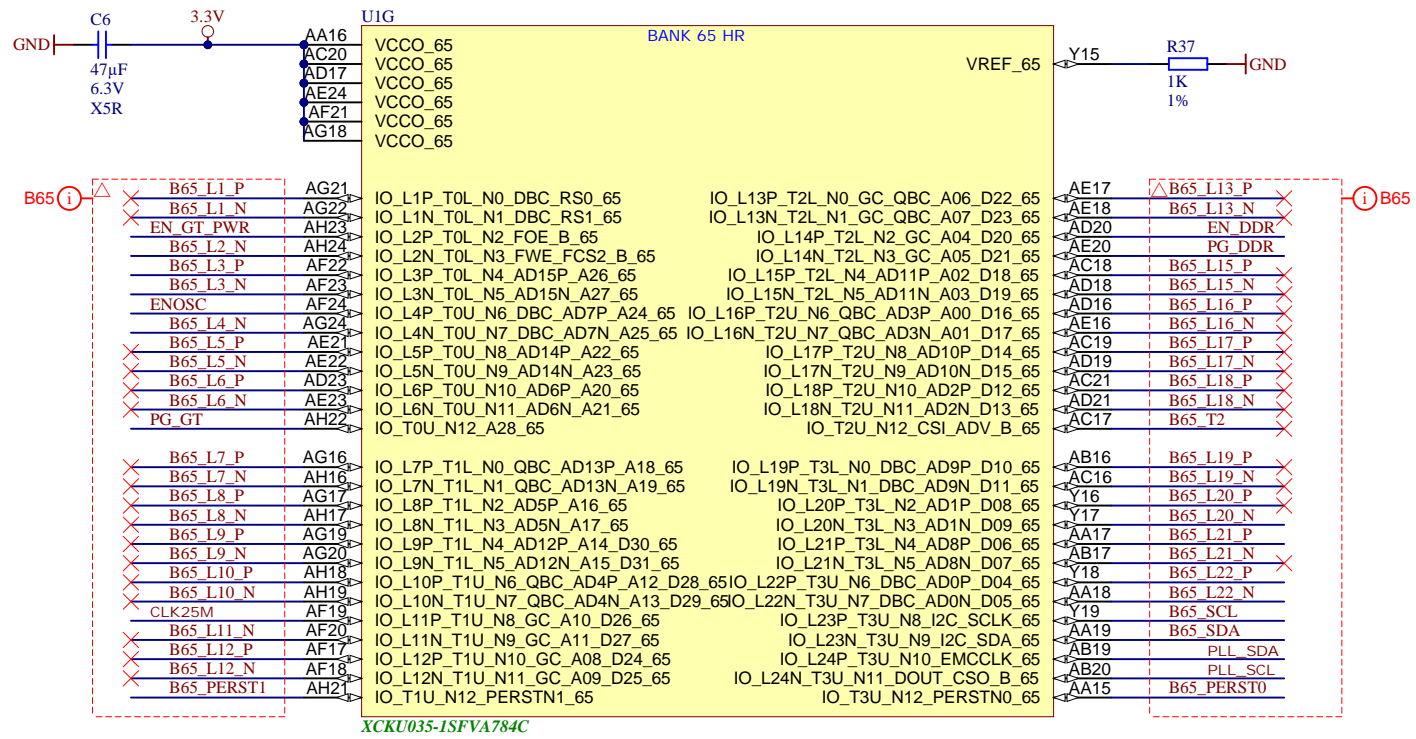
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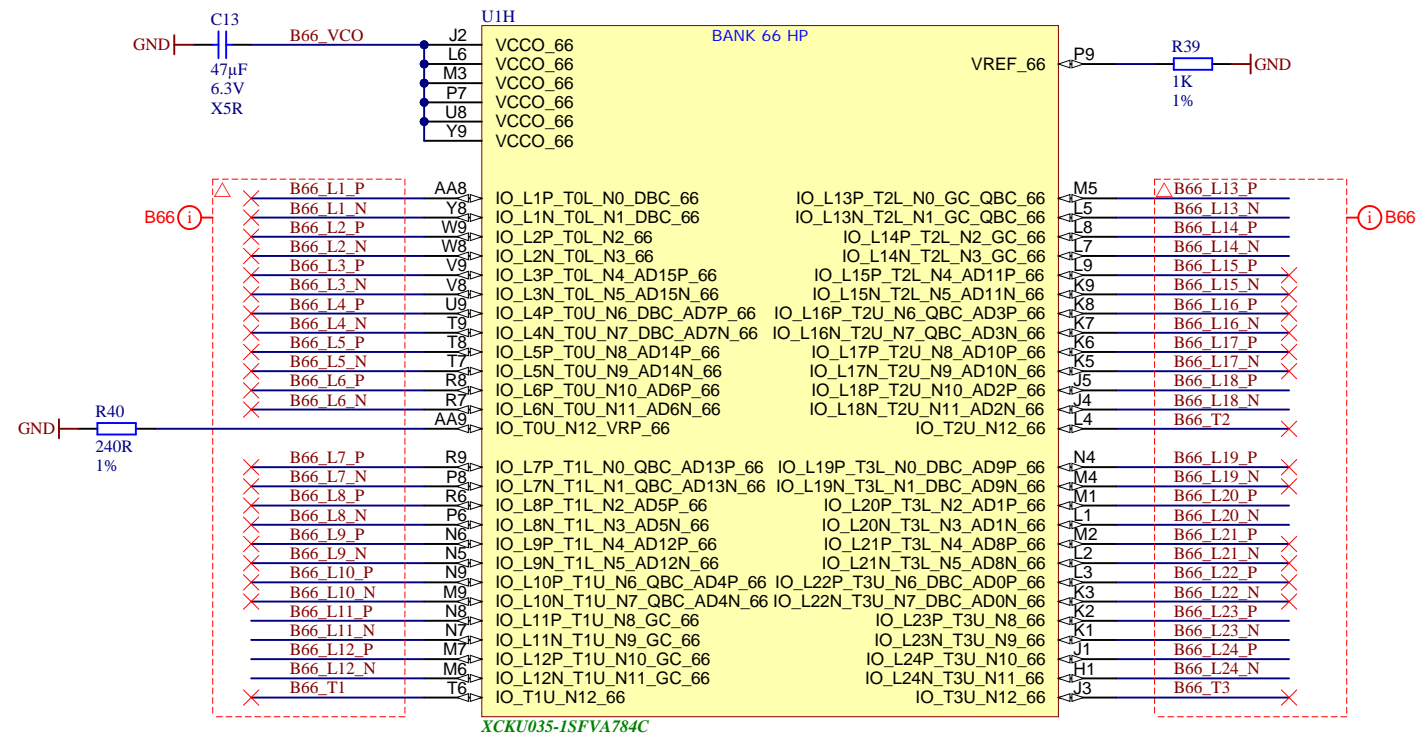
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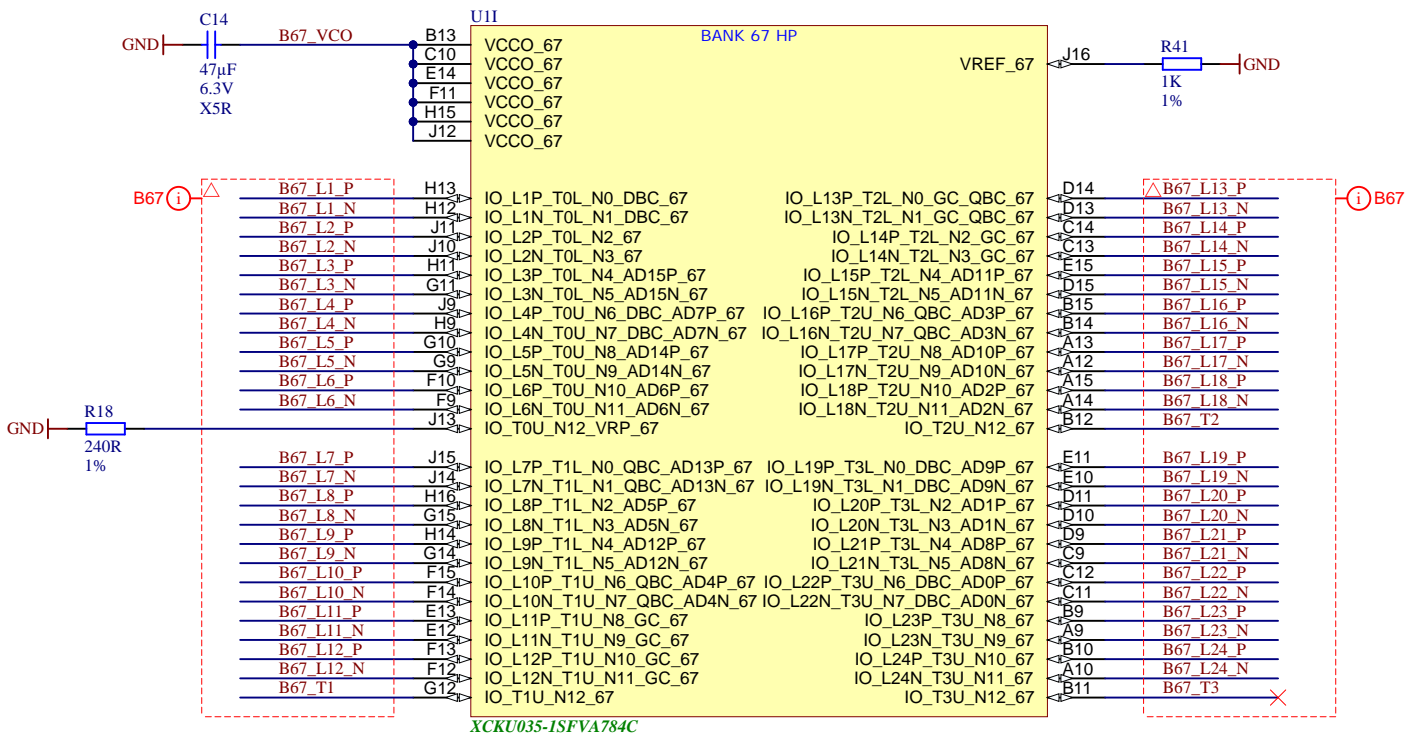
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Title: TE0841		
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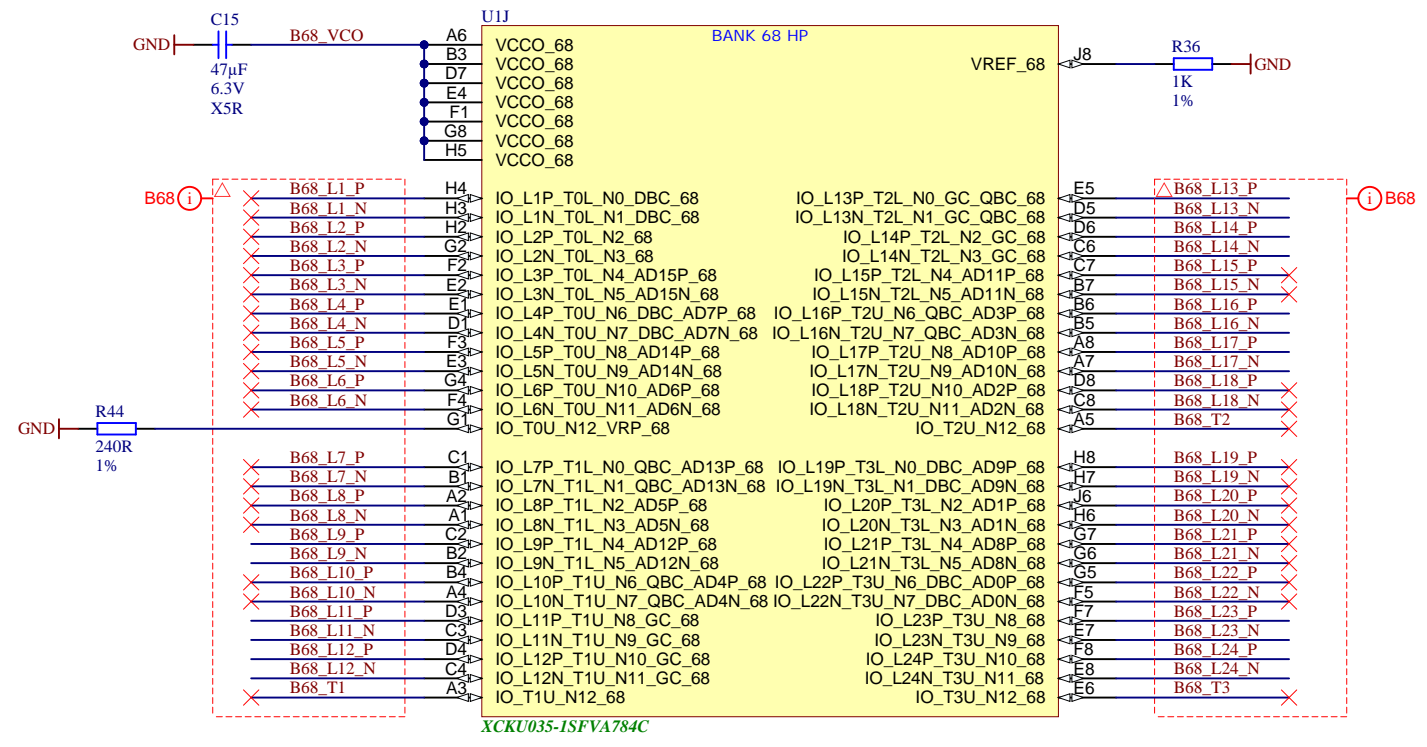
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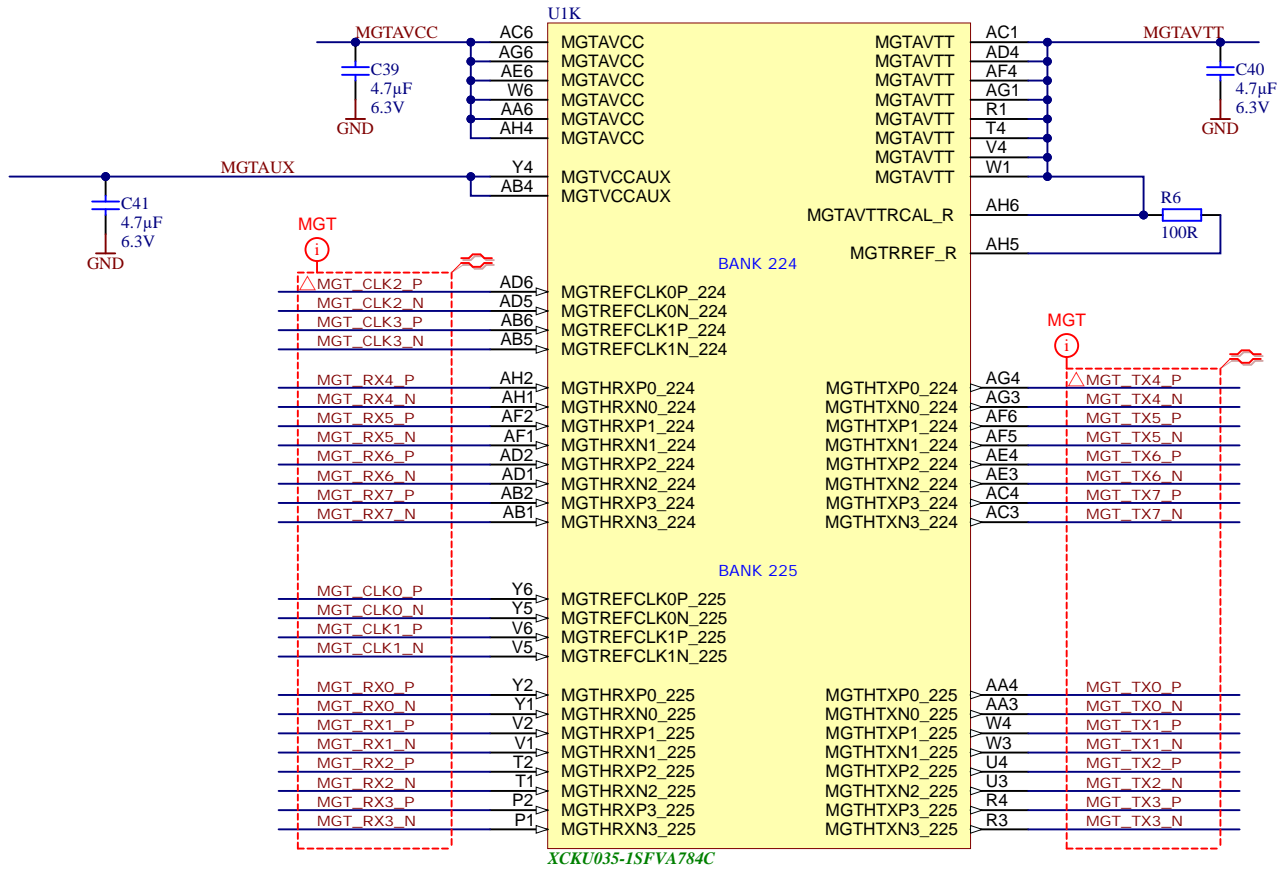
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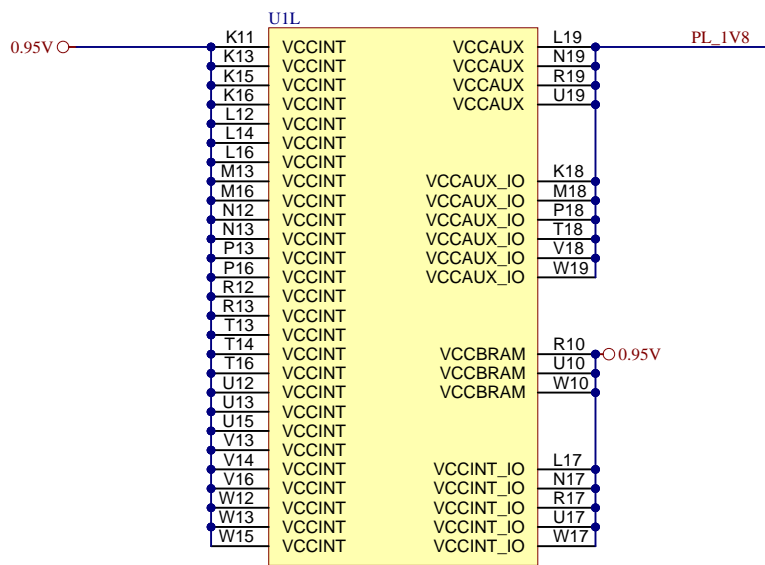
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Filename: FPGA-B67.SchDoc		



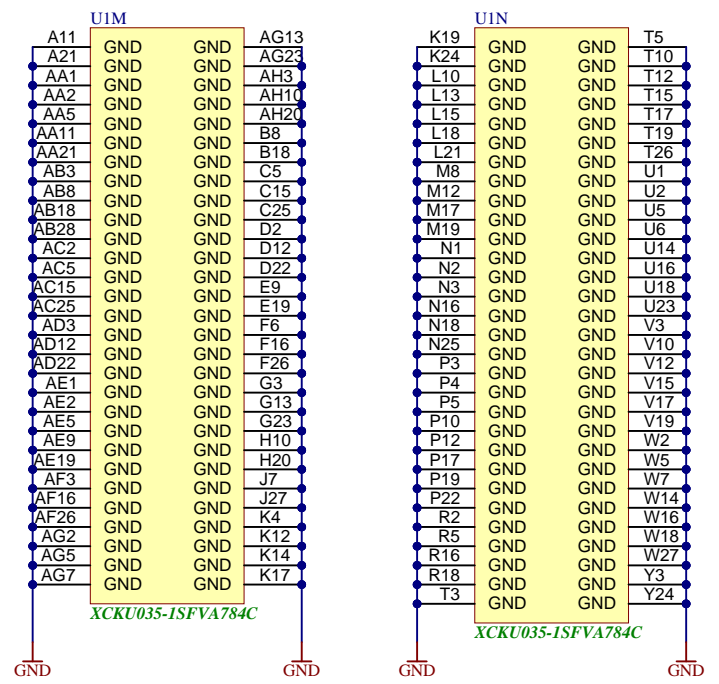
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Title: TE0841		
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Filename: FPGA-MGT.SchDoc		

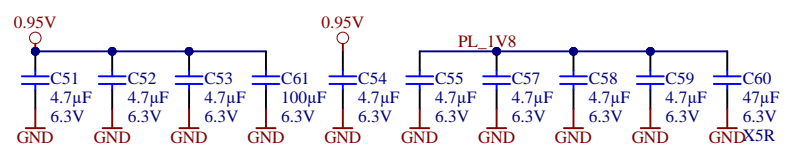


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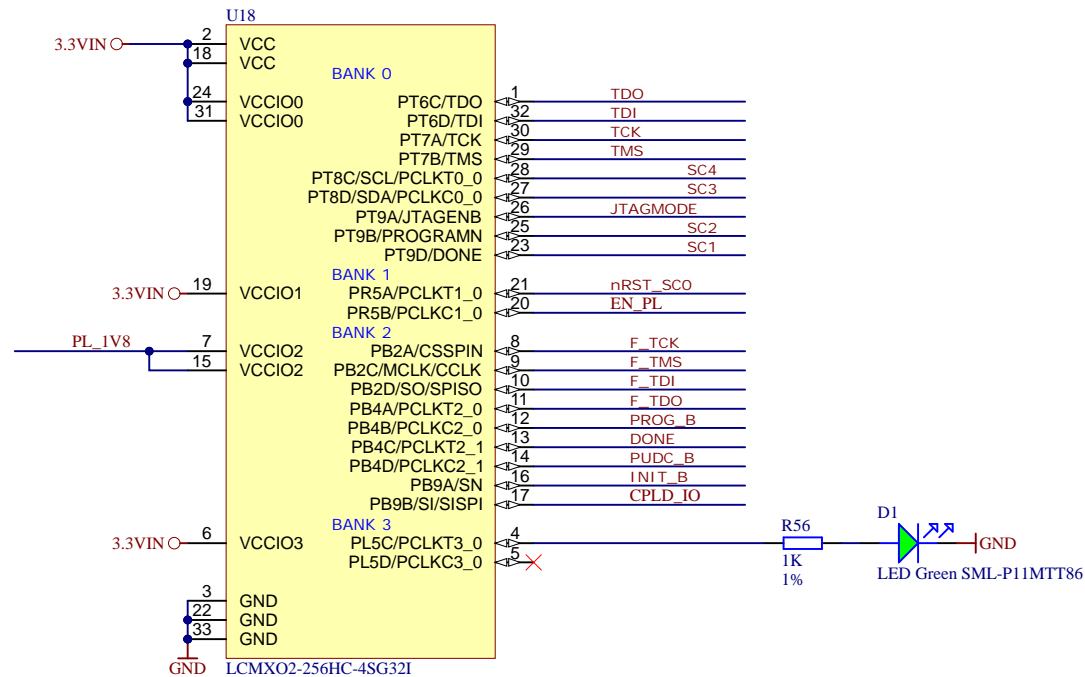


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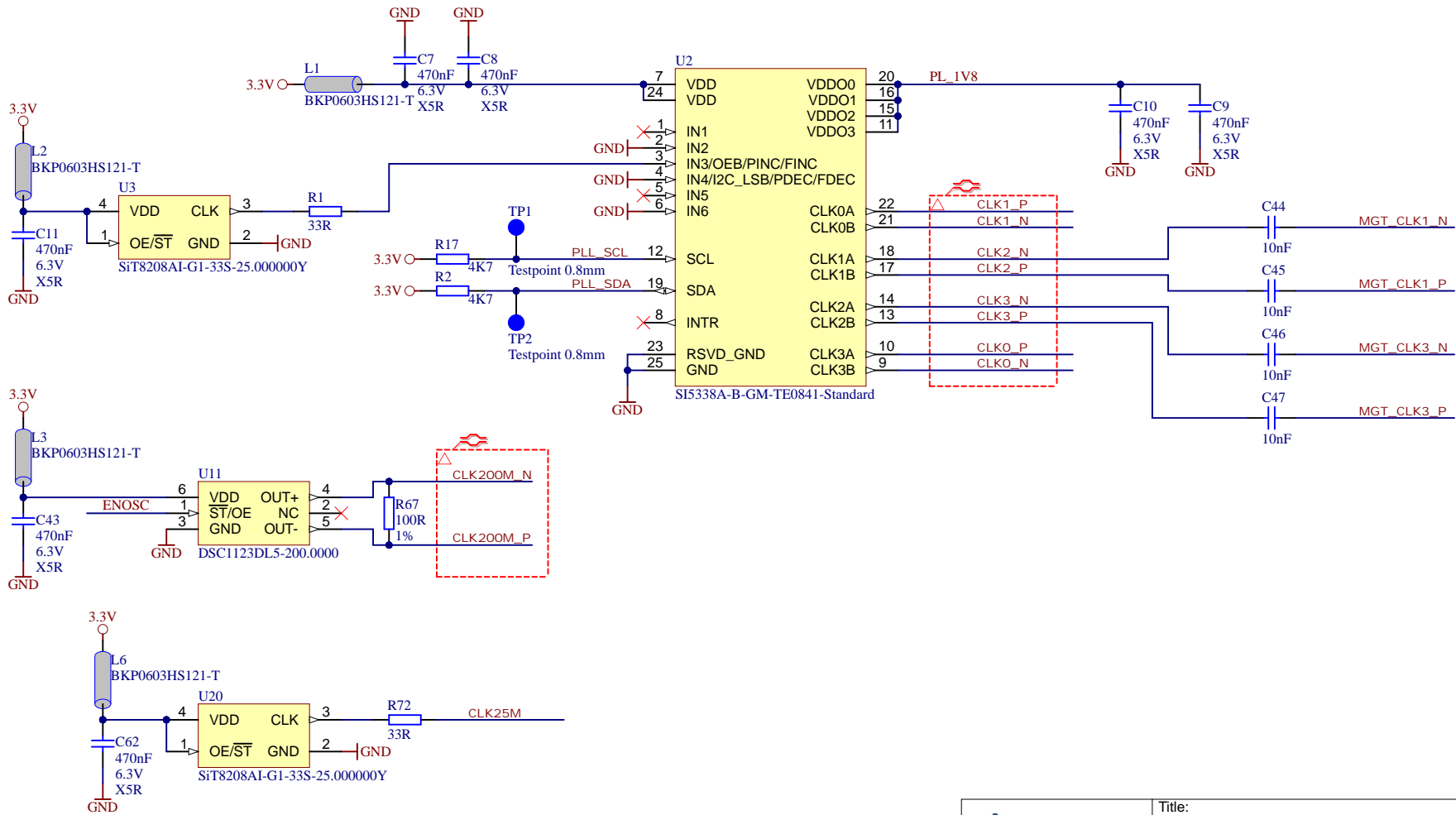
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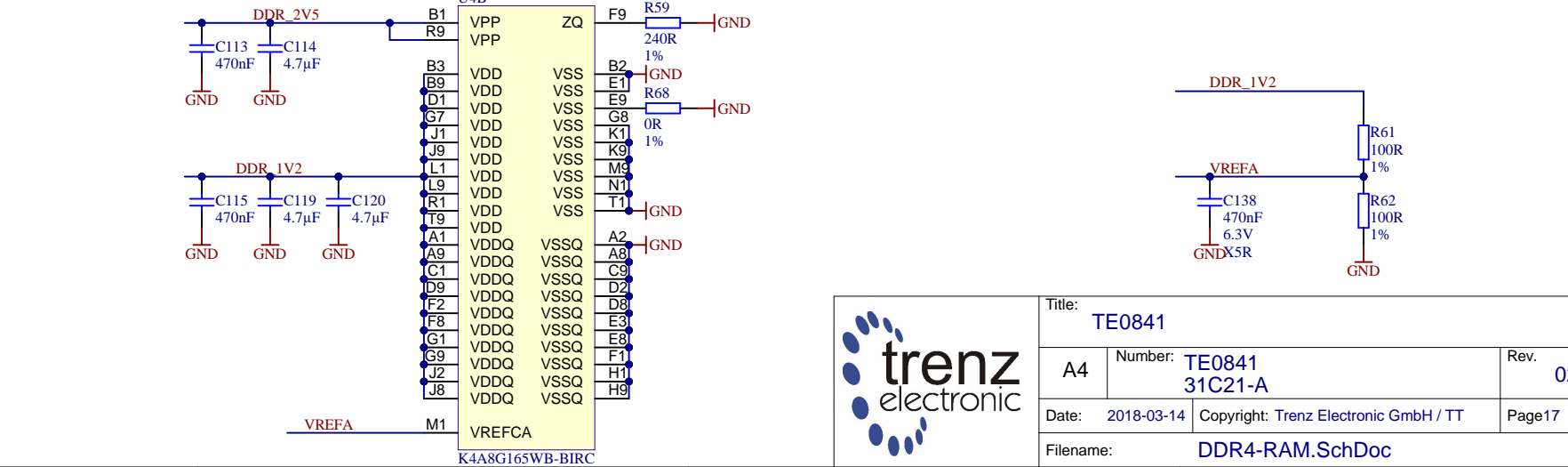
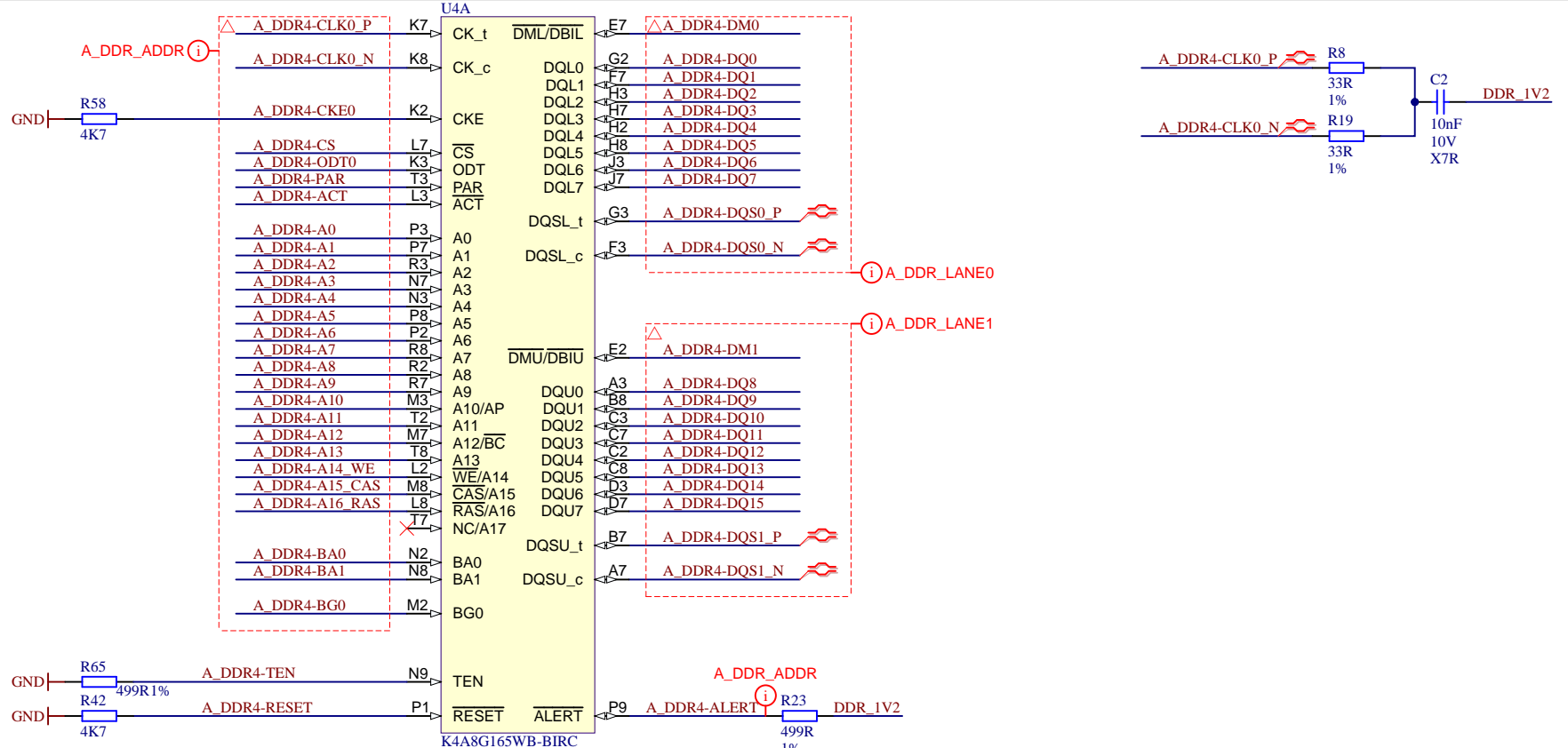
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Filename: Clock.SchDoc		



Title: TE0841		
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Filename: DDR4-RAM.SchDoc		

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A

A

B

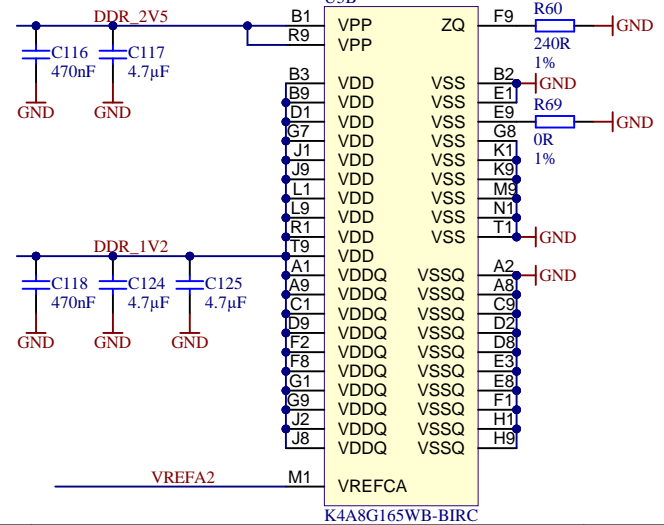
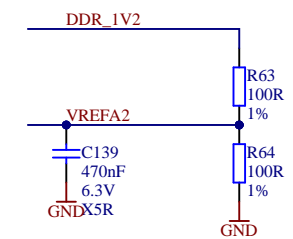
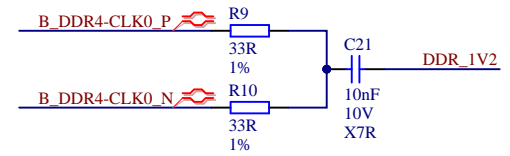
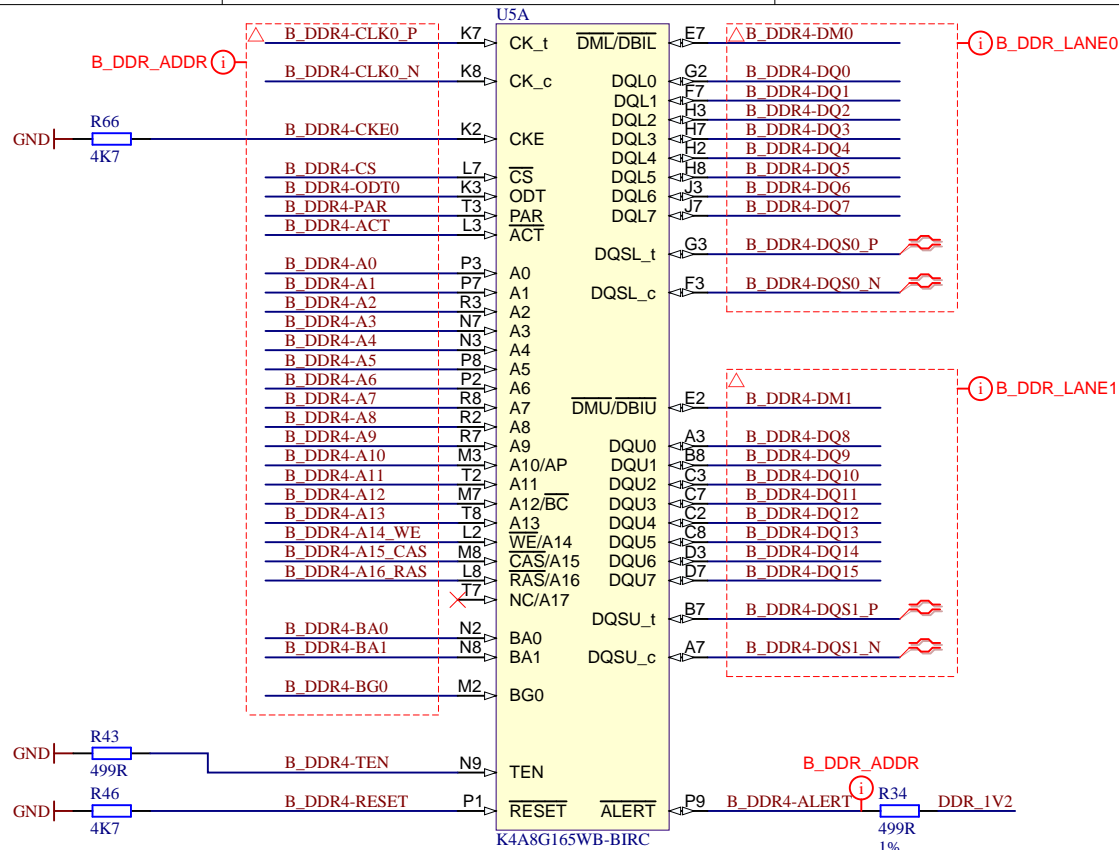
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C

D

D



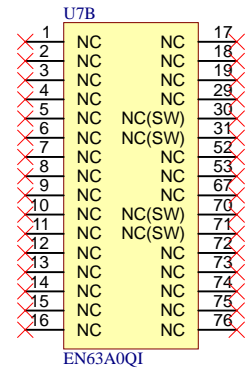
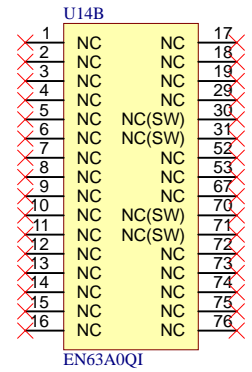
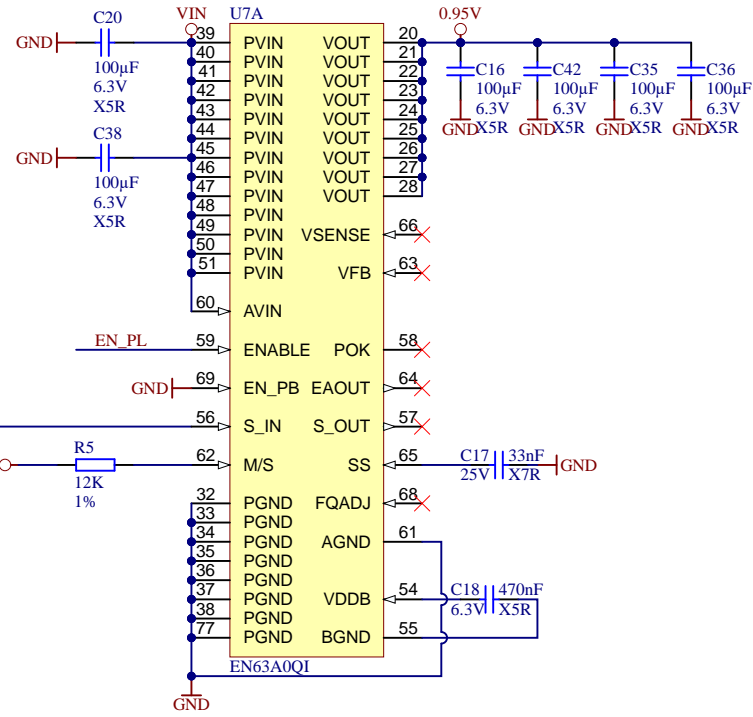
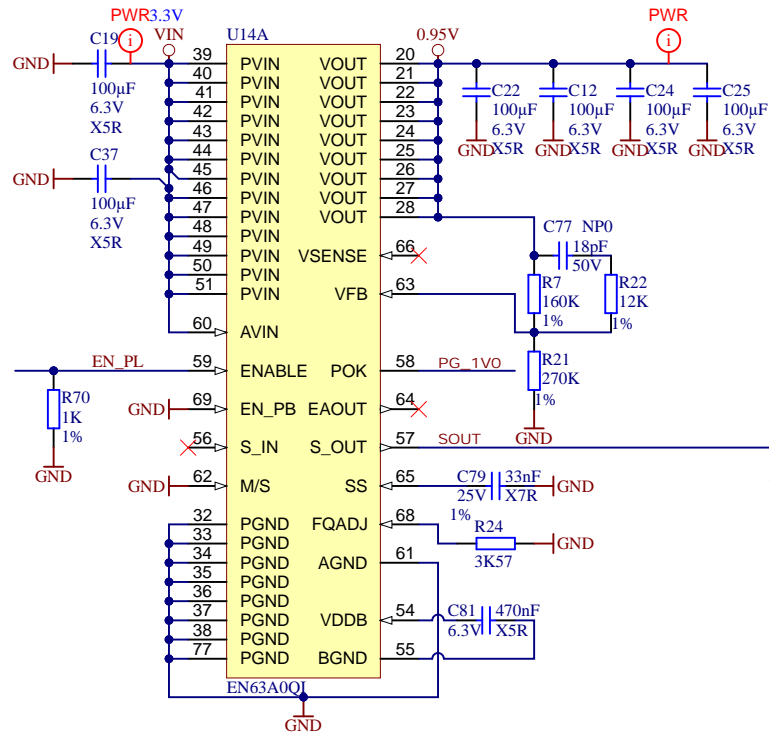
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Filename: DDR4-RAM_2.SchDoc		

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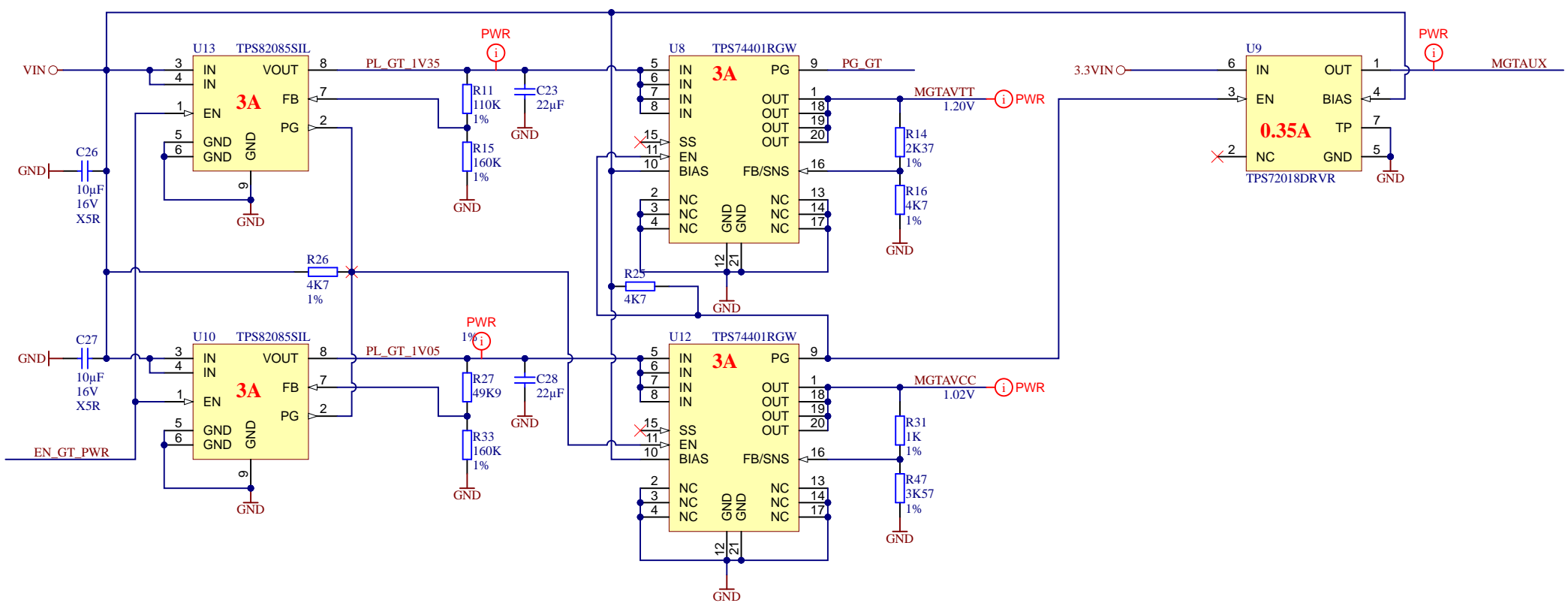
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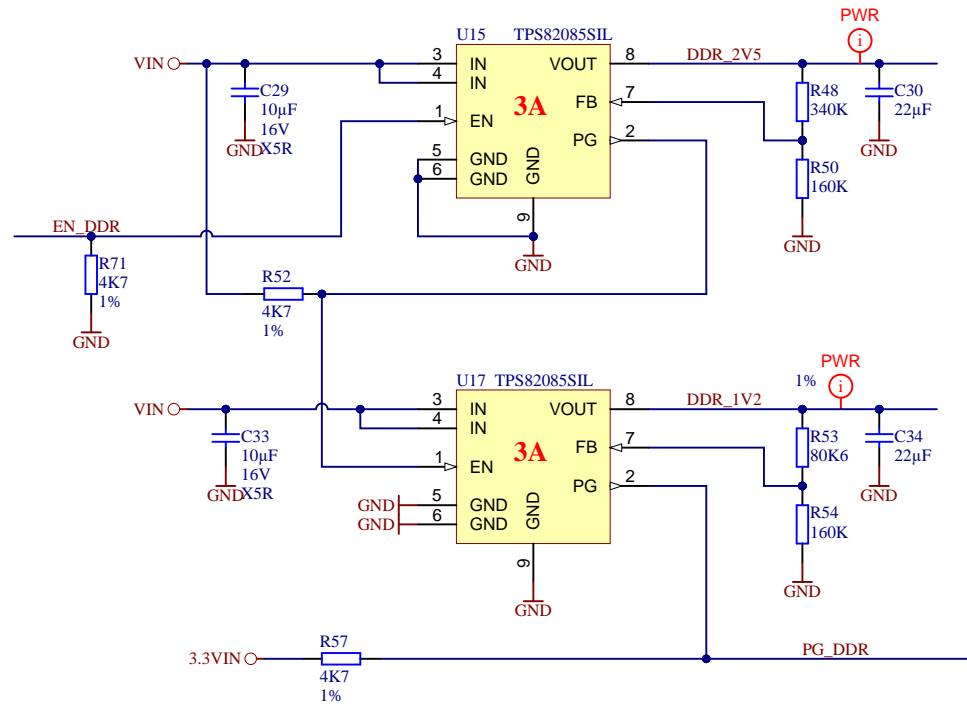
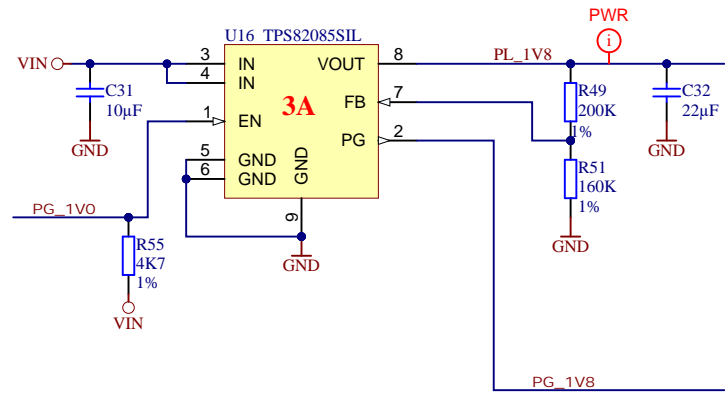
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Title: TE0841		
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Filename: PWR1.SchDoc		



	Title: TE0841	
	A4	Number: TE0841 31C21-A
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	Filename: PWR2.SchDoc	



Title: TE0841		
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Filename: POWER_2.SchDoc		

CHANGES REV01 TO REV01A (08.16.2017):


1) U1: changed schematic symbol. Next pins swapped to mach same polarity order:
 -- AE13 (IO_L6P_T0U_N10_AD6P_64)/AE12 (IO_L6N_T0U_N11_AD6N_64)
 -- J5 (IO_L18P_T2U_N10_AD2P_66)/J4 (IO_L18N_T2U_N11_AD2N_66)

2) Net names changed (no electrical changes):

JM1: swapped signals B64_L6:
 -- B64_L6_N - pin 40 (was pin 42)
 -- B64_L6_P - pin 42 (was pin 40)
 JM3: swapped signals B64_L6:
 -- B66_L18_N - pin 52 (was pin 54)
 -- B66_L18_P - pin 54 (was pin 52)

CHANGES REV01A TO REV02 (03.2018):

- 1) U4 / U5: changed DDR4 chip: NT5AD256M16B2-GN -> K4A4G165WE-BCRC (K4A8G165WB-BIRC)
- 2) Fixed sense connection on DCDC
- 3) U6: changed SPI flash chip: N25Q256A11E1240E-> N25Q512A11G1240E
- 4) Full update LIB
- 5) Added additional resistors for support 16GBit DDR chips
- 6) Added strong pull-down to EN_PL
- 7) Added additional testpoints for I2C bus
- 8) Added additional MEMS oscillator (25MHz)
- 9) Changed pull-up power supply VIN -> 3.3VIN on the PG_DDR net
- 10) Added pull-down on the EN_DDR (04.05.2022)
- 11) S/N Track-it pad set not fitted

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