

U\_FPGA-MGT  
FPGA-MGT.SchDoc

U\_FPGA-MISC  
FPGA-MISC.SchDoc

U\_FPGA-PWR  
FPGA-PWR.SchDoc

U\_FPGA-B44  
FPGA-B44.SchDoc

U\_FPGA-B45  
FPGA-B45.SchDoc

U\_FPGA-B46  
FPGA-B46.SchDoc

U\_FPGA-B47  
FPGA-B47.SchDoc

U\_FPGA-B64  
FPGA-B64.SchDoc

U\_FPGA-B65  
FPGA-B65.SchDoc

U\_FPGA-B66  
FPGA-B66.SchDoc

U\_FPGA-B67  
FPGA-B67.SchDoc

U\_FPGA-B68  
FPGA-B68.SchDoc

U\_DDR4-RAM  
DDR4-RAM.SchDoc

U\_DDR4-RAM\_2  
DDR4-RAM\_2.SchDoc

U\_B2B-Connectors  
B2B-Connectors.SchDoc

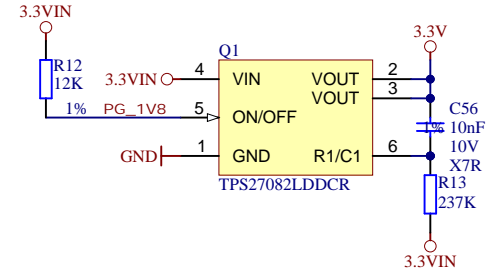
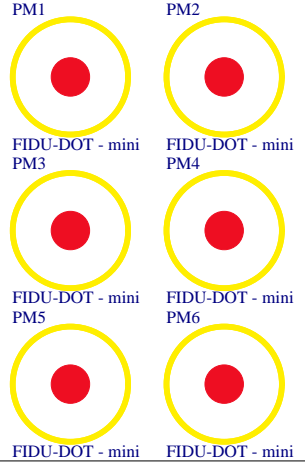
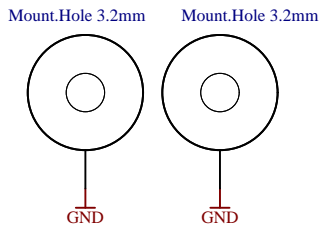
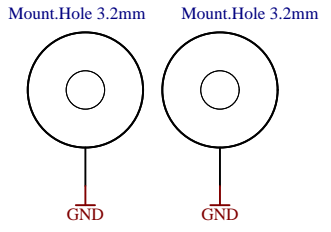
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CPLD.SchDoc

U\_Clock  
Clock.SchDoc

U\_PWR1  
PWR1.SchDoc

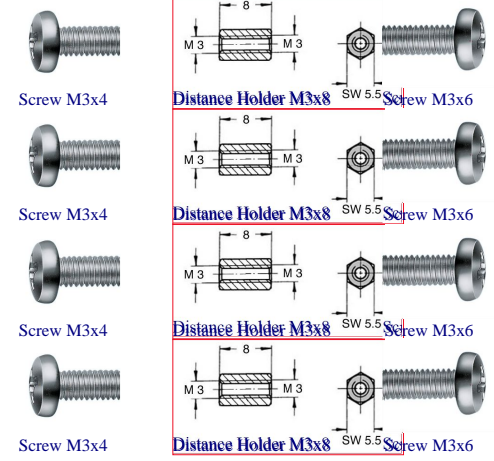
U\_PWR2  
PWR2.SchDoc

U\_POWER\_2  
POWER\_2.SchDoc



Serial  
Serialnumber 6,3 x 6.3mm

Top of Board



Assembly variant	31121-T
Created by	VY
Modified by	VY
Modified at	2020-07-23
SVN Revision	8580



Title: TE0841		
A4	Number: TE0841 31121-T	Rev. 02
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B64 HR 48 IO, 24 LVDS Pairs  
 B65 HR 8 IO, 3.3V  
 MGT 3 Lanes

B66 16 HP IO, 8 LVDS Pairs  
 MGT 4 + 1 Lanes  
 B65 4 IO, 3.3V

B68 HP 18 IO, 9 LVDS Pairs  
 B67 HP 48 IO, 24 LVDS Pairs  
 B67 HP 2 IO

A

A

B

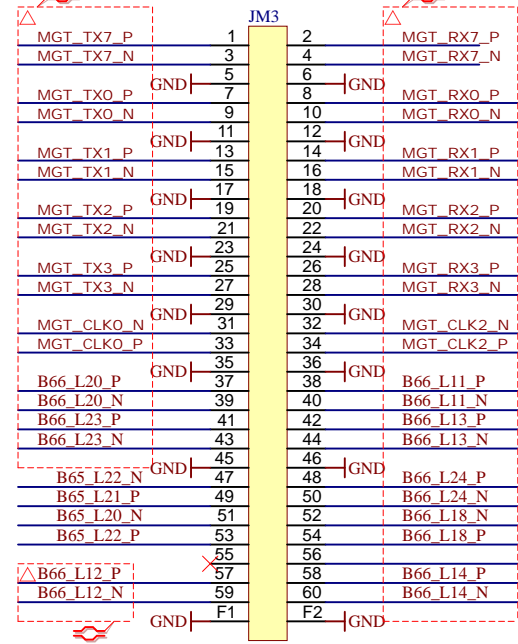
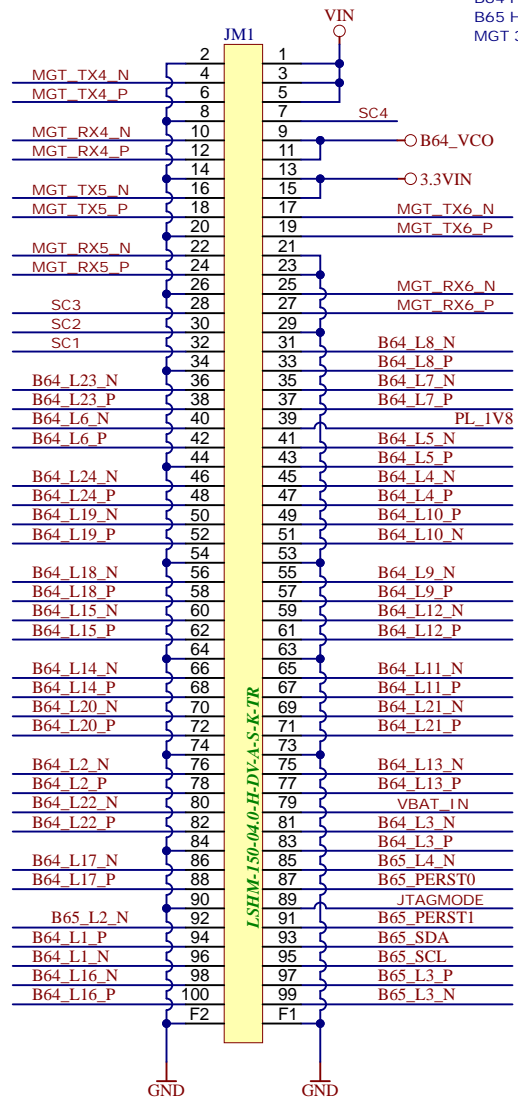
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C

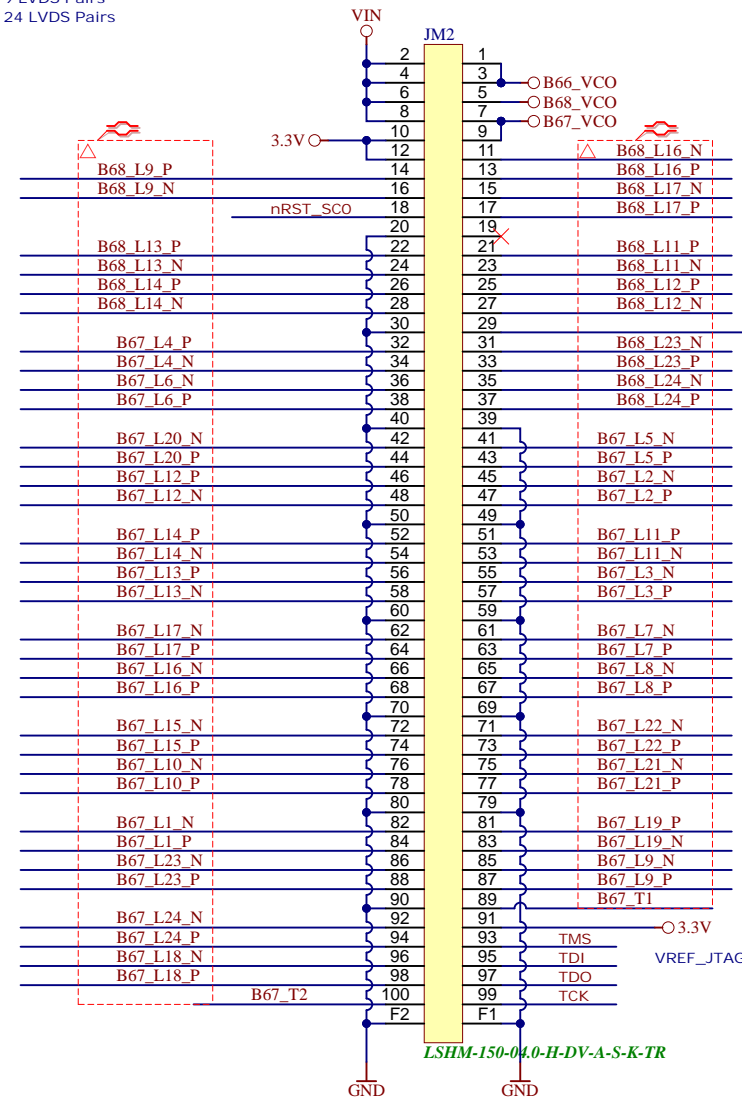
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D

D



LSHM-130-04.0-H-DV-A-S-K-TR



LSHM-150-04.0-H-DV-A-S-K-TR



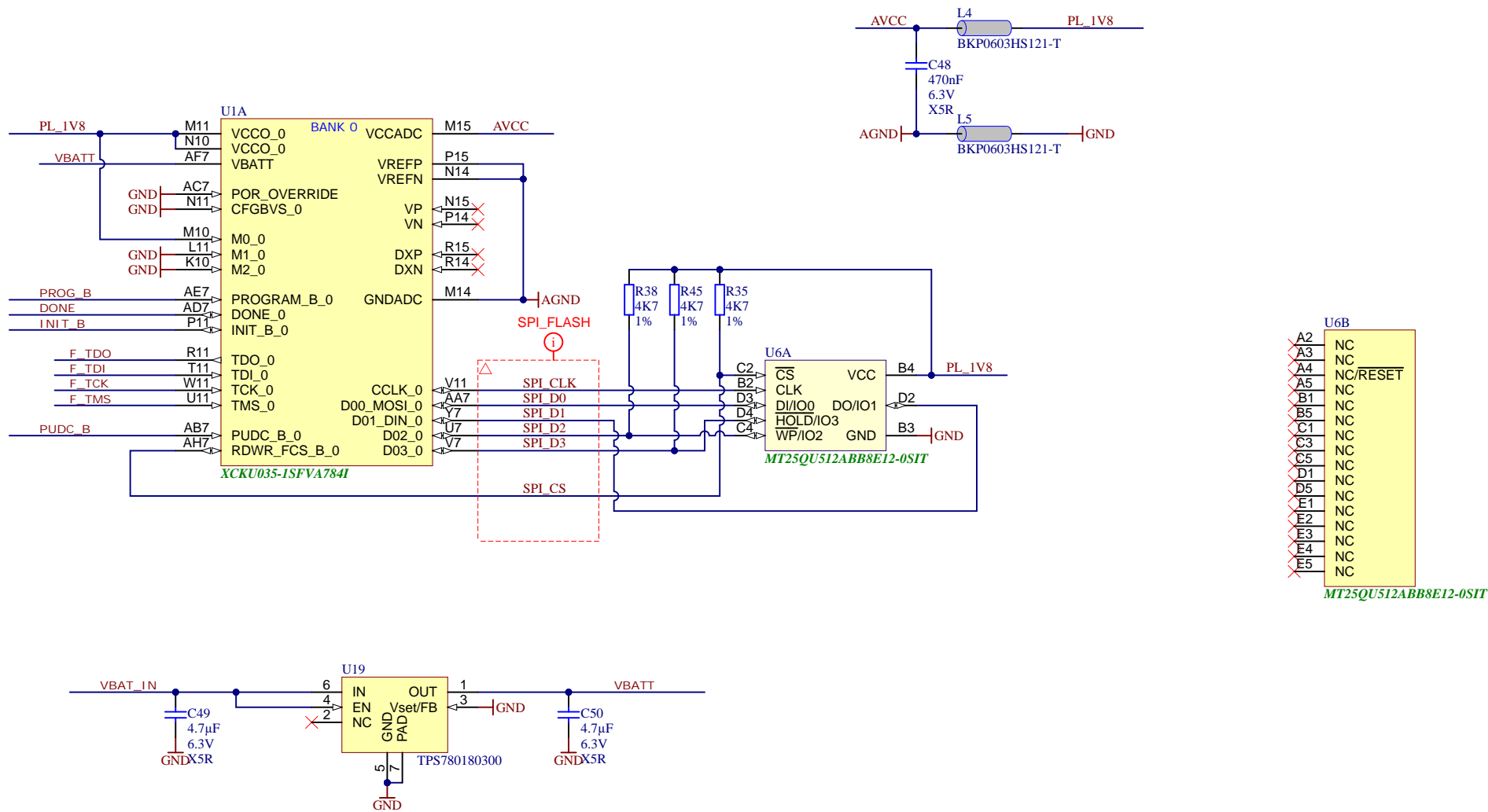
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Filename: B2B-Connectors.SchDoc		


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1

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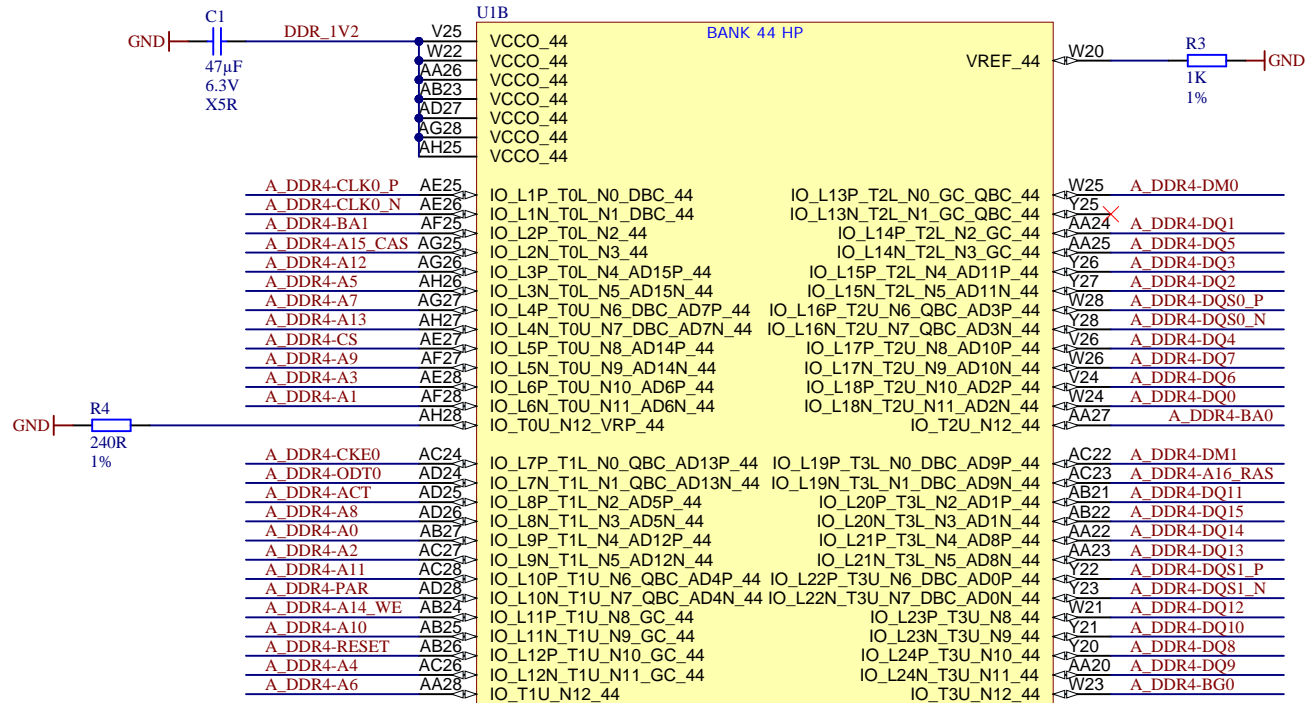
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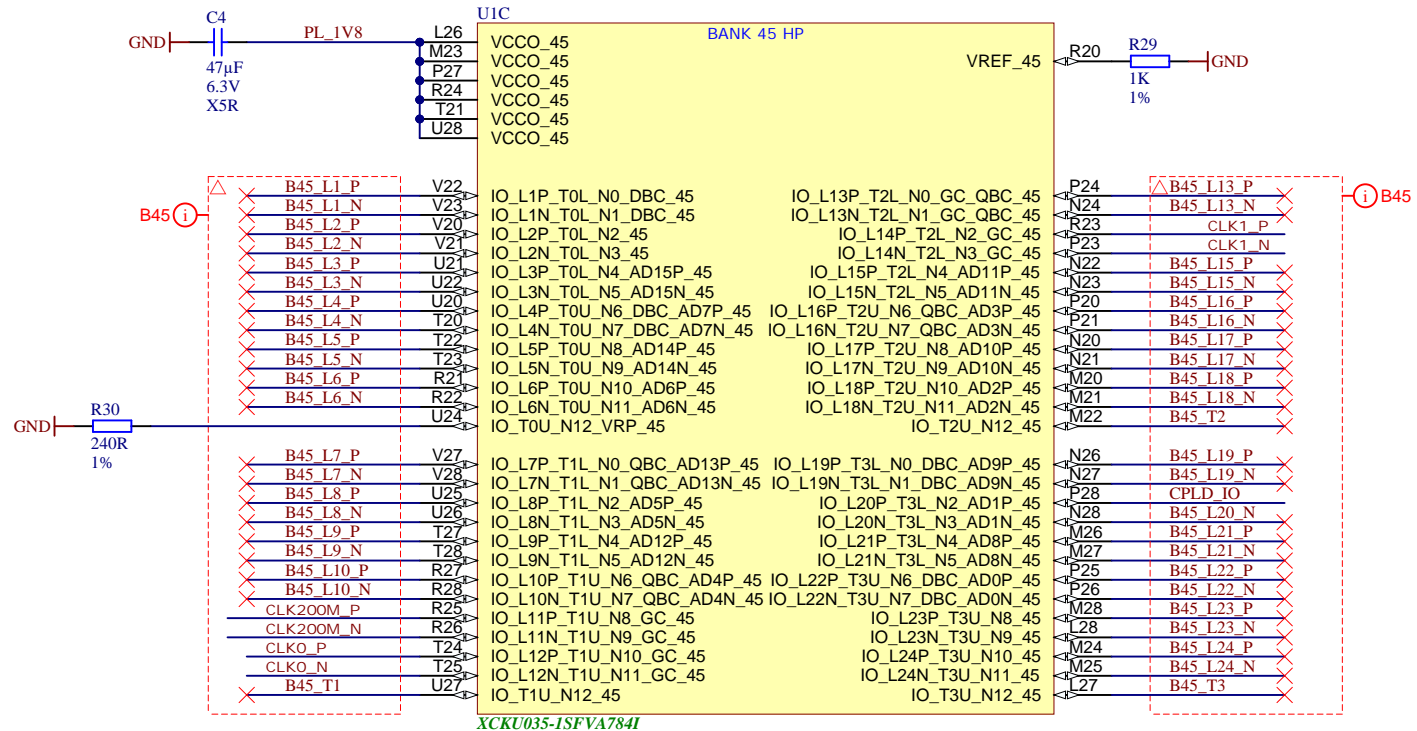
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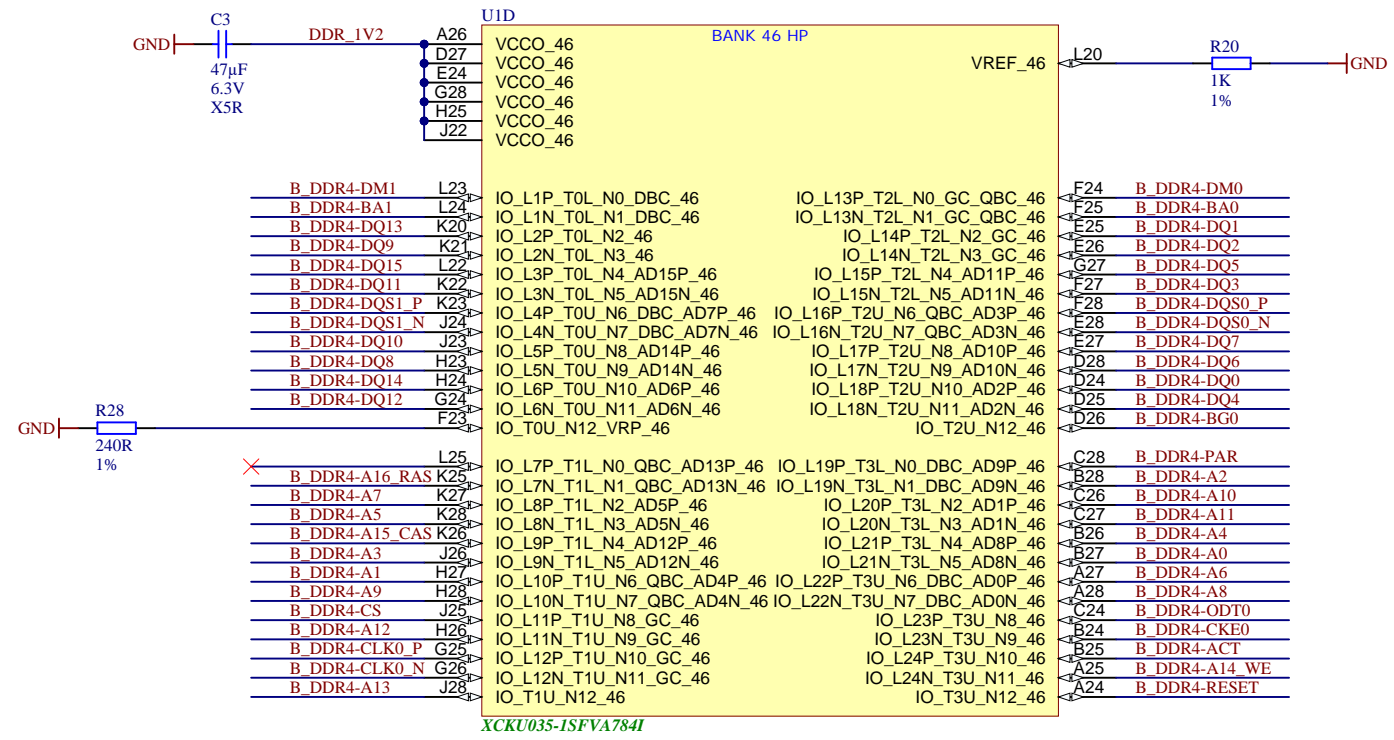

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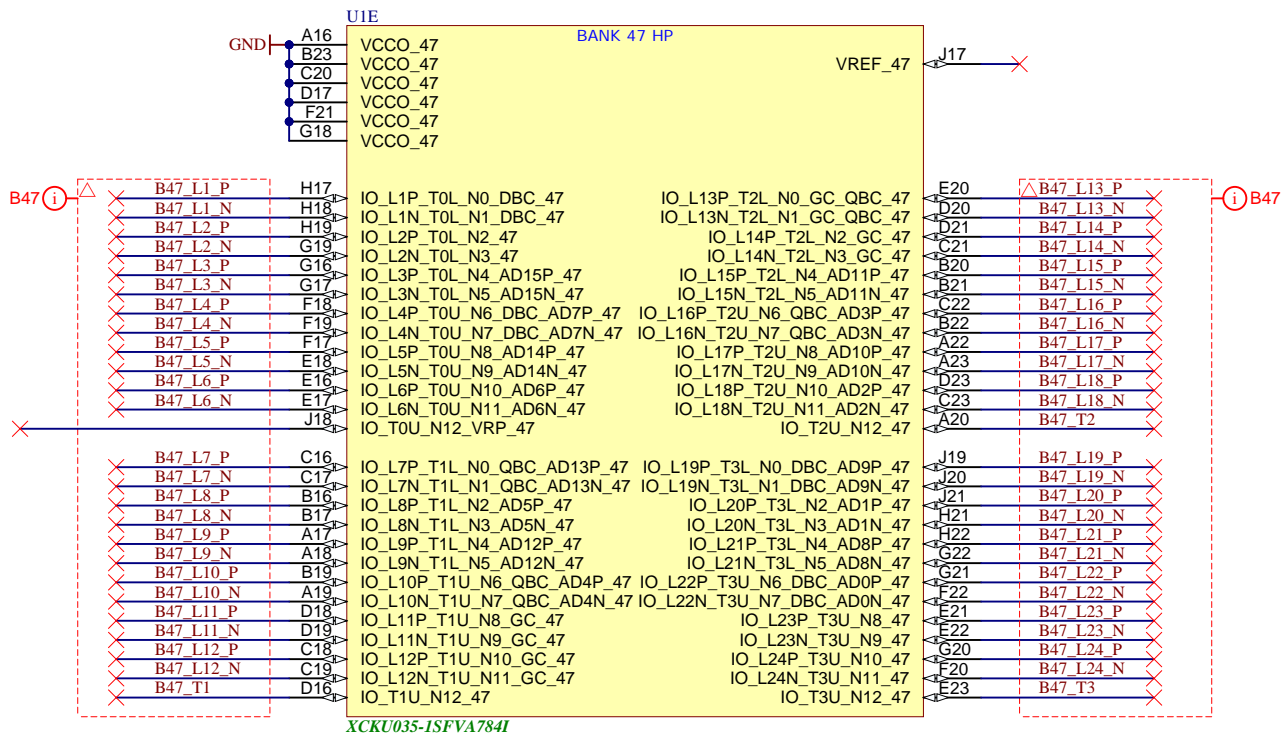
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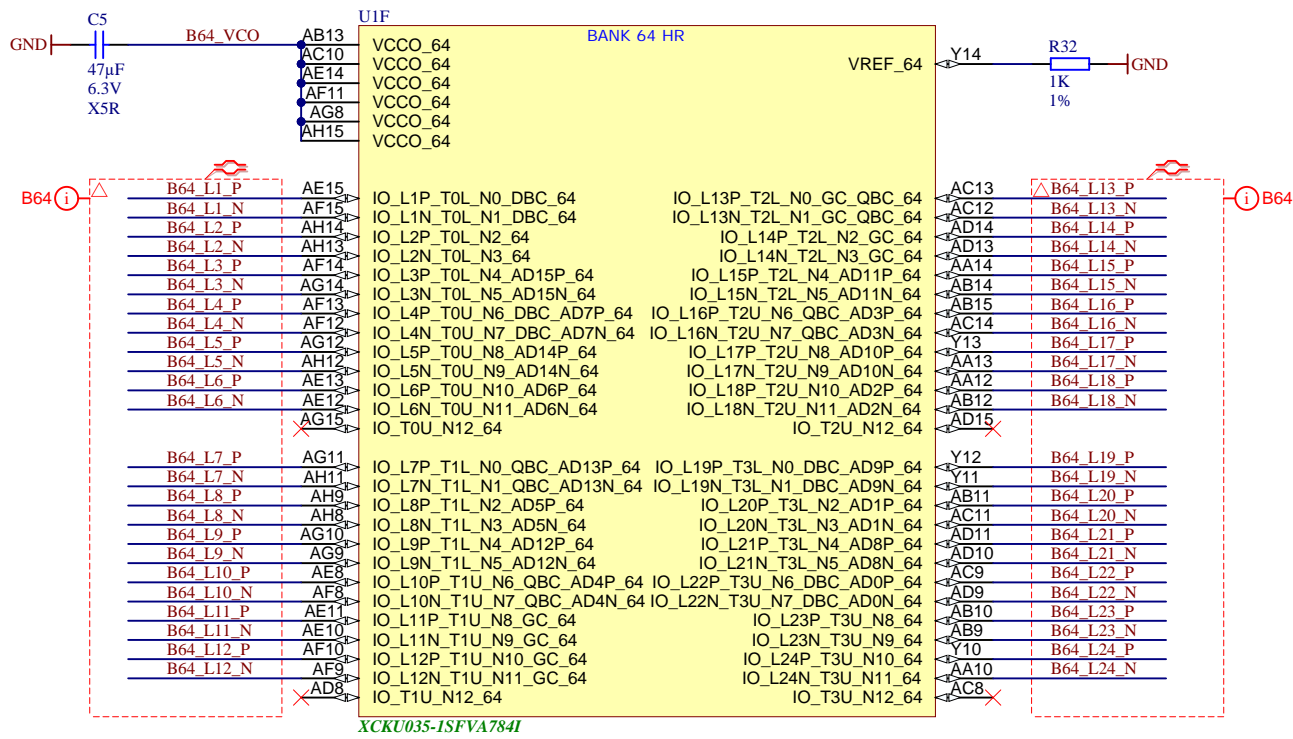
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A4	Number: <b>TE0841 31I21-T</b>	Rev. <b>02</b>
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Filename: <b>FPGA-B45.SchDoc</b>		

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Filename: FPGA-B46.SchDoc		

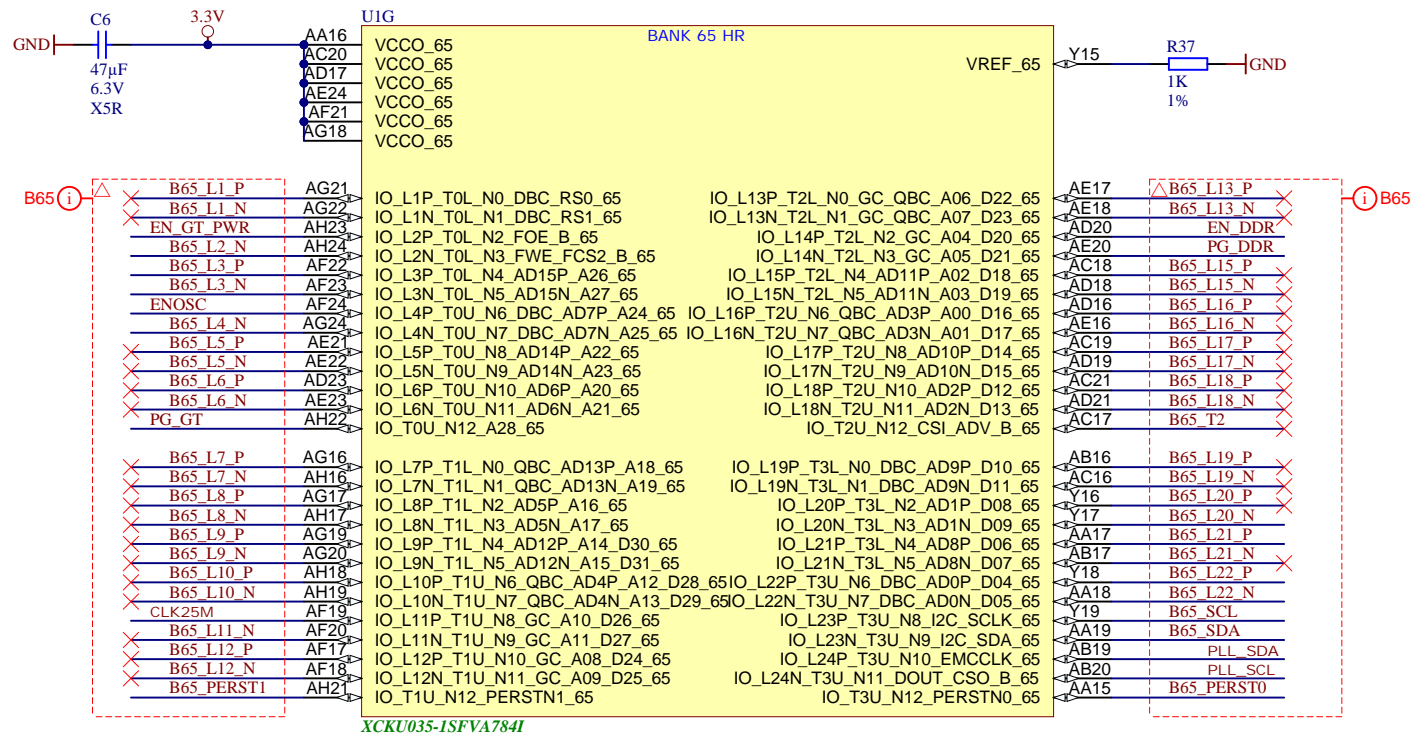


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Date: <b>2018-03-14</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>7</b> of <b>21</b>
Filename: <b>FPGA-B47.SchDoc</b>		



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Filename: <b>FPGA-B64.SchDoc</b>		





Title: TE0841		
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Filename: FPGA-B65.SchDoc		

A

A

B

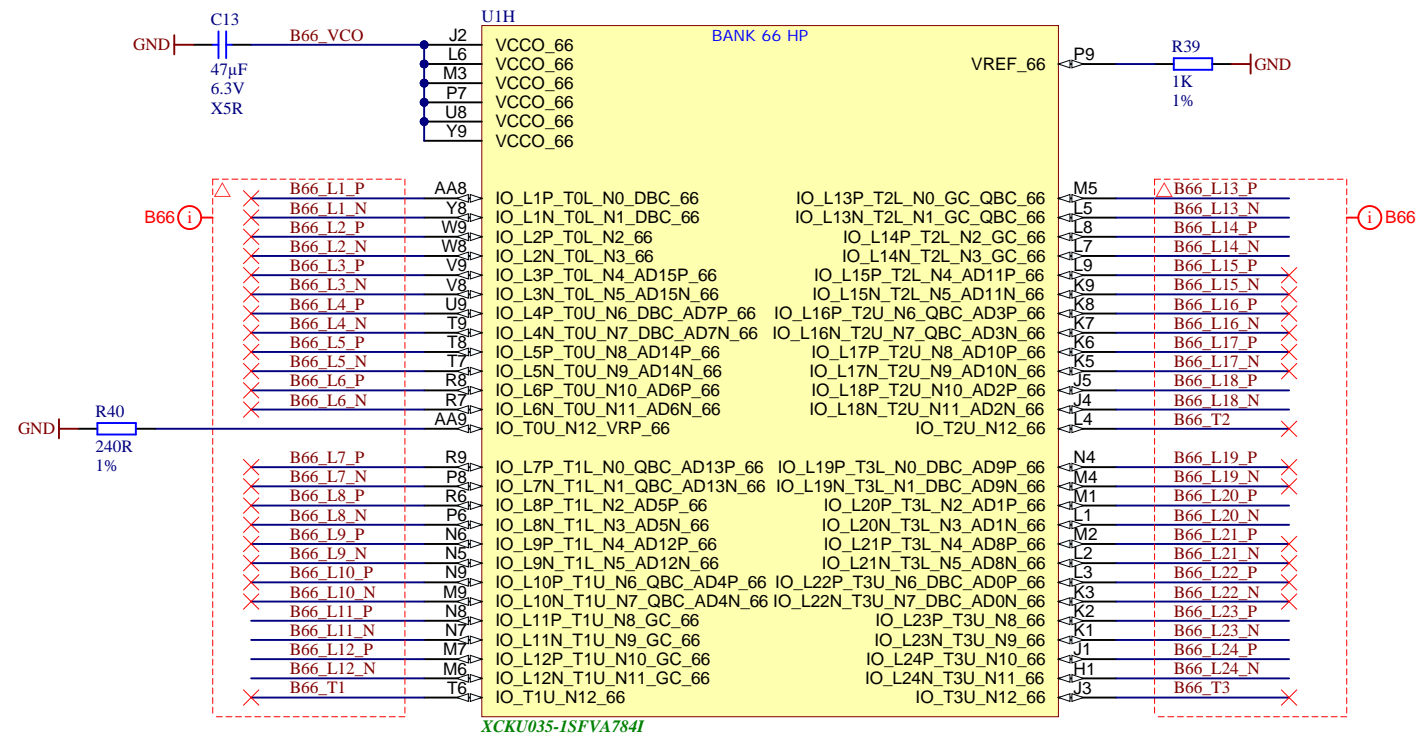

B

C

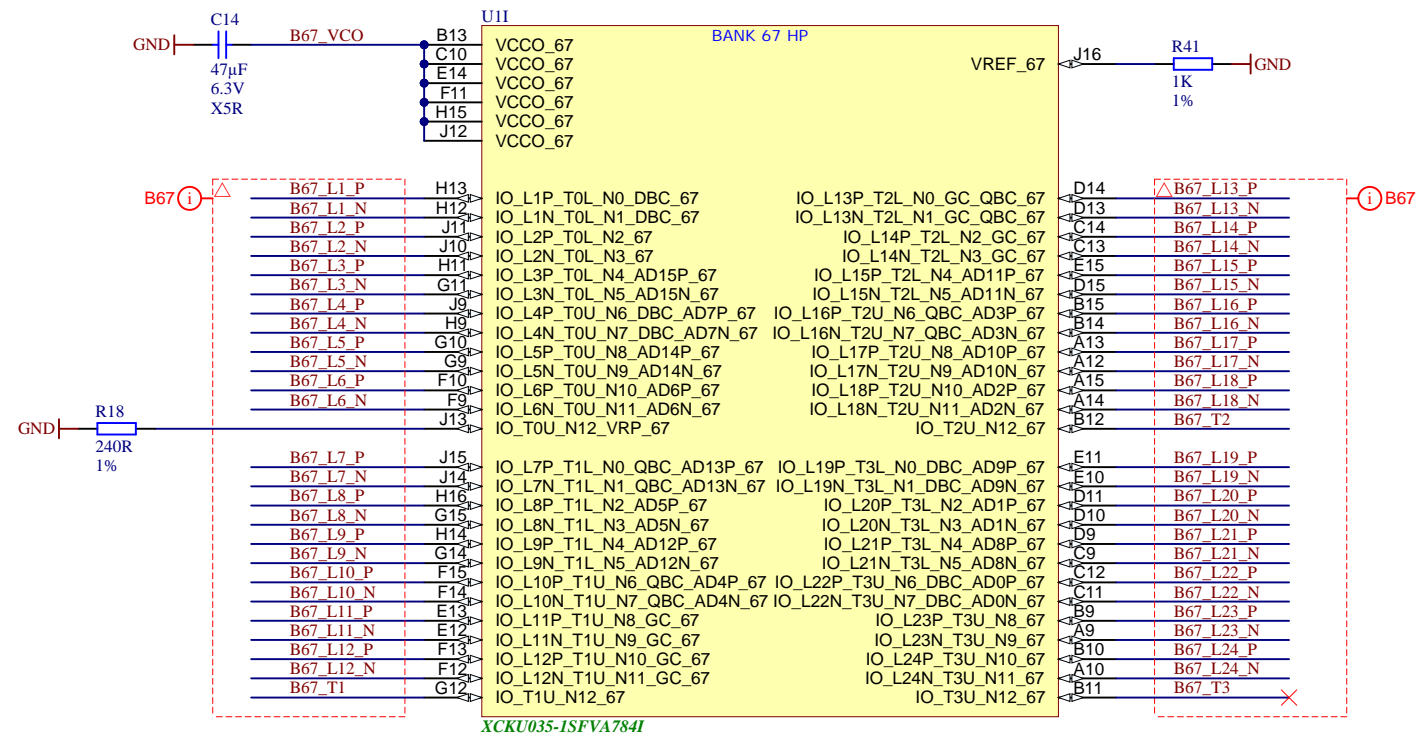
C

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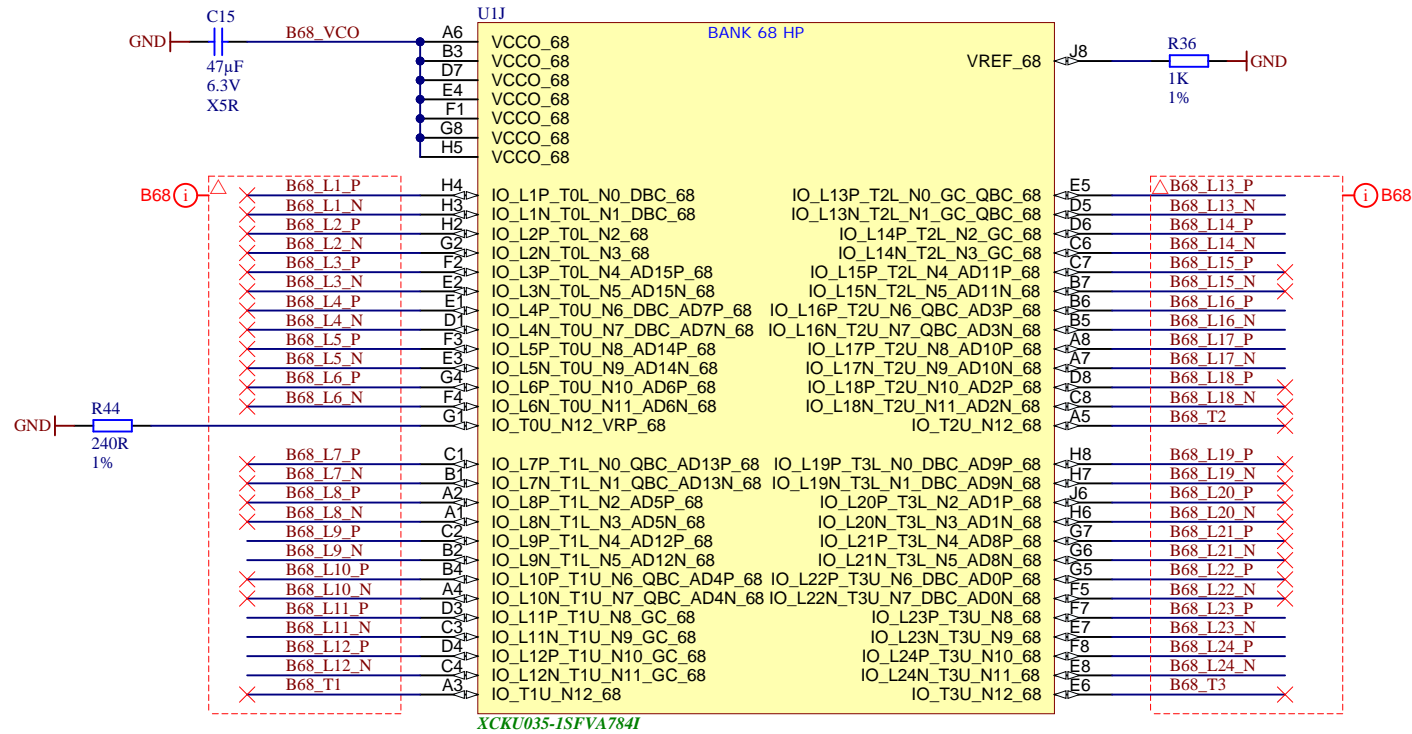
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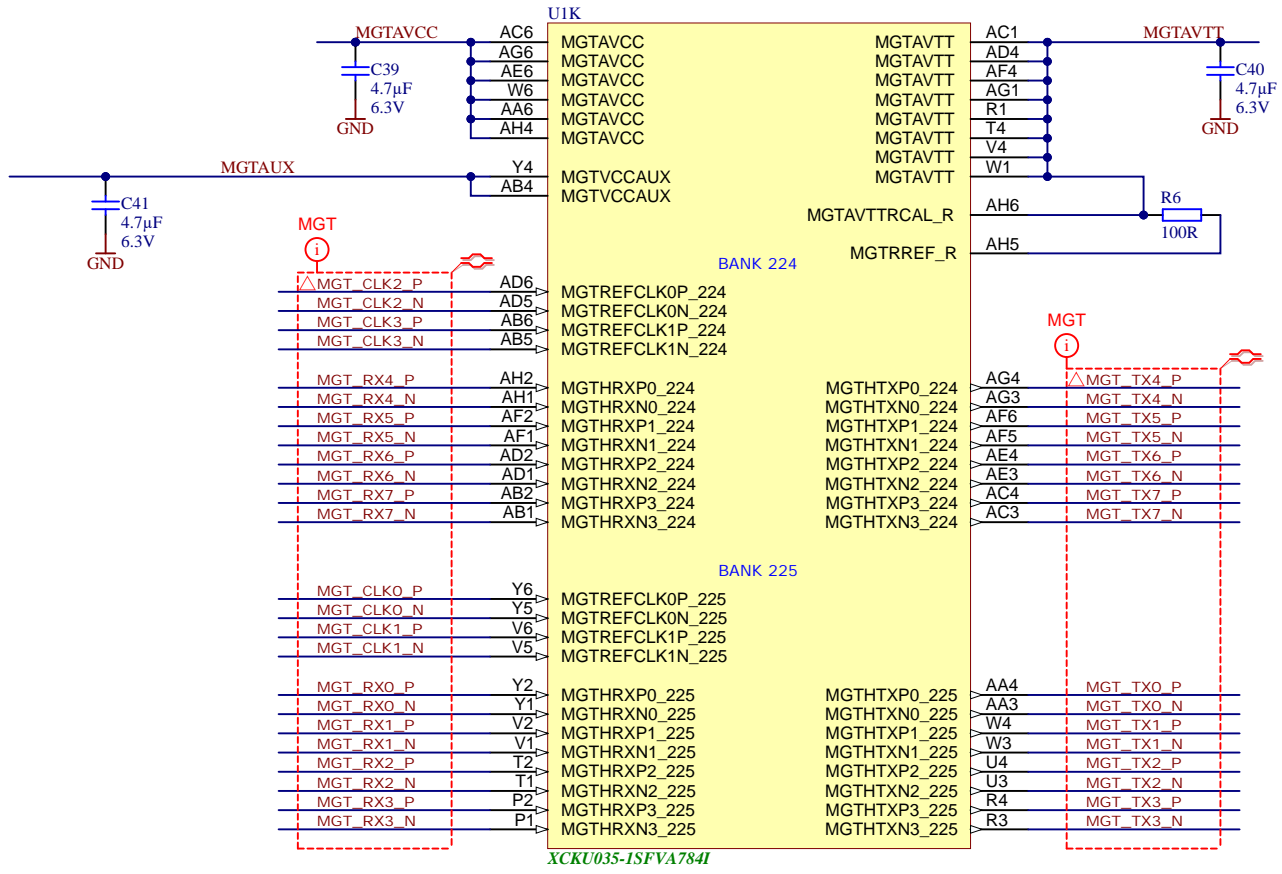
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Filename: <b>FPGA-B66.SchDoc</b>		



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A4	Number: TE0841 31I21-T	Rev. 02
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Filename: FPGA-B67.SchDoc		



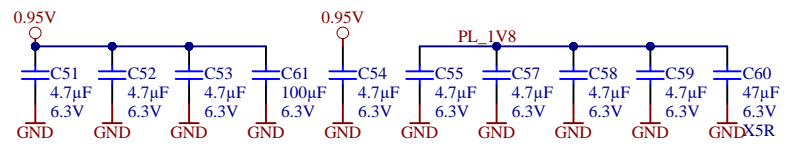
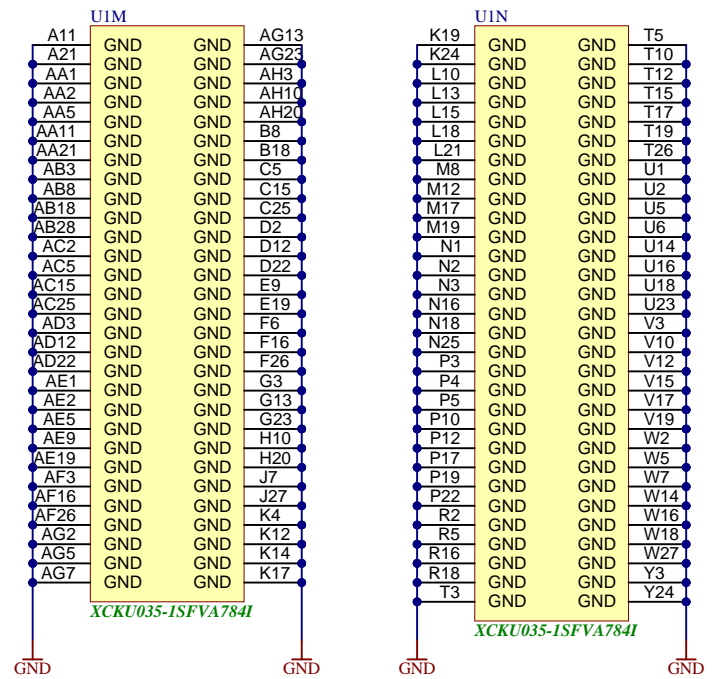
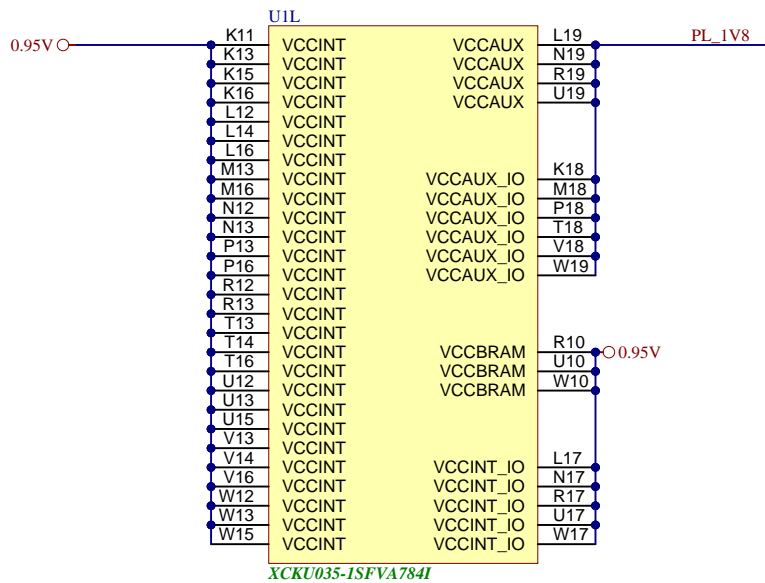

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Filename: FPGA-B68.SchDoc		



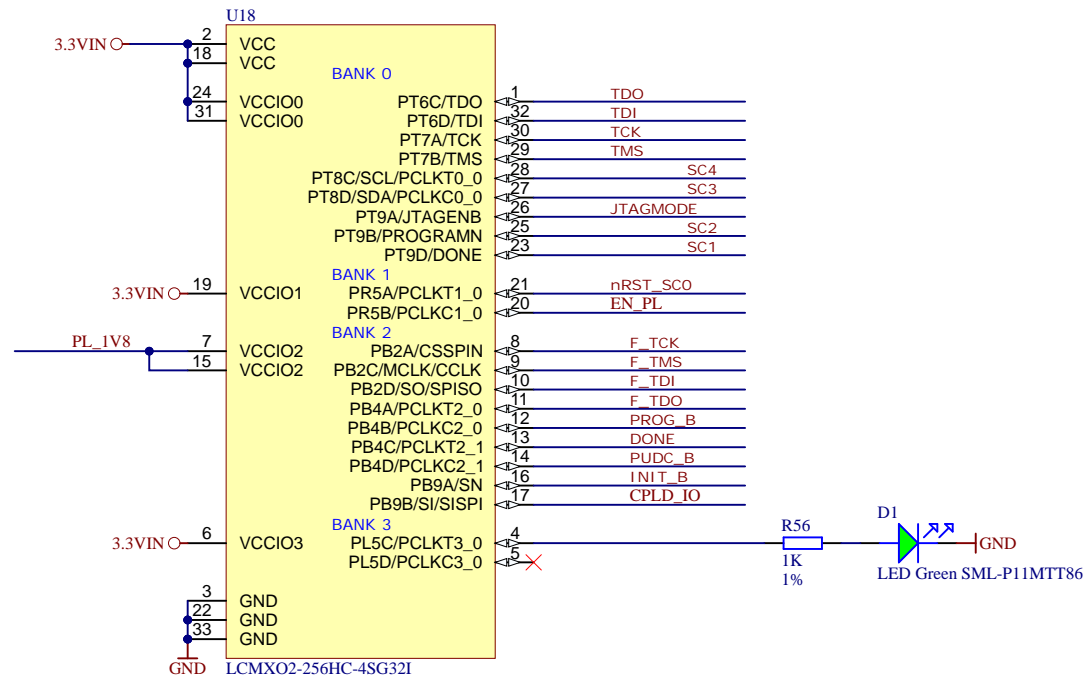
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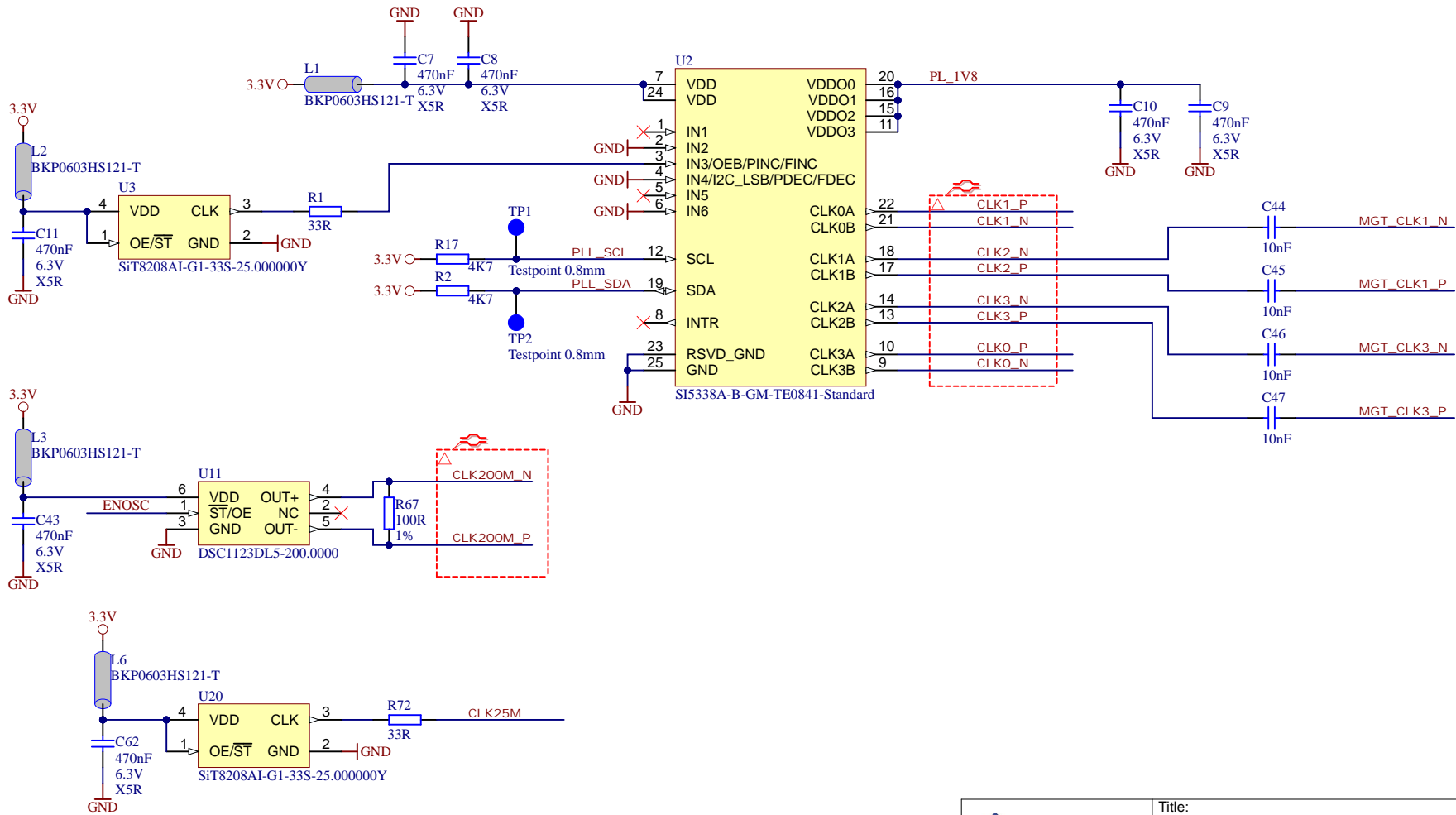
Title: TE0841		
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Filename: FPGA-MGT.SchDoc		





Title: TE0841		
A4	Number: TE0841 31I21-T	Rev. 02
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Filename: FPGA-PWR.SchDoc		

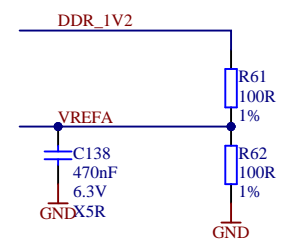
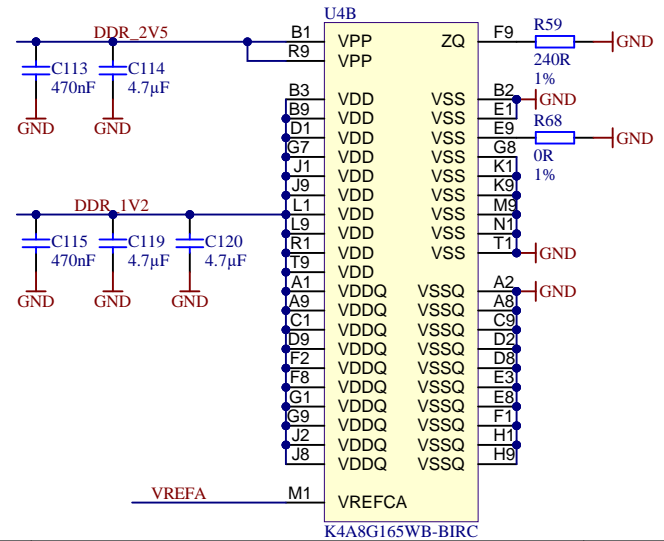
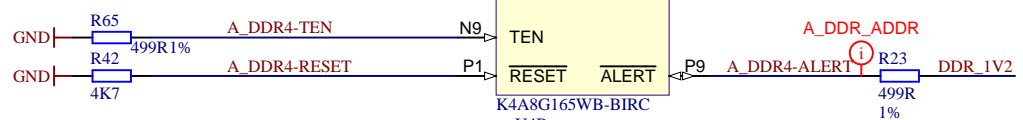
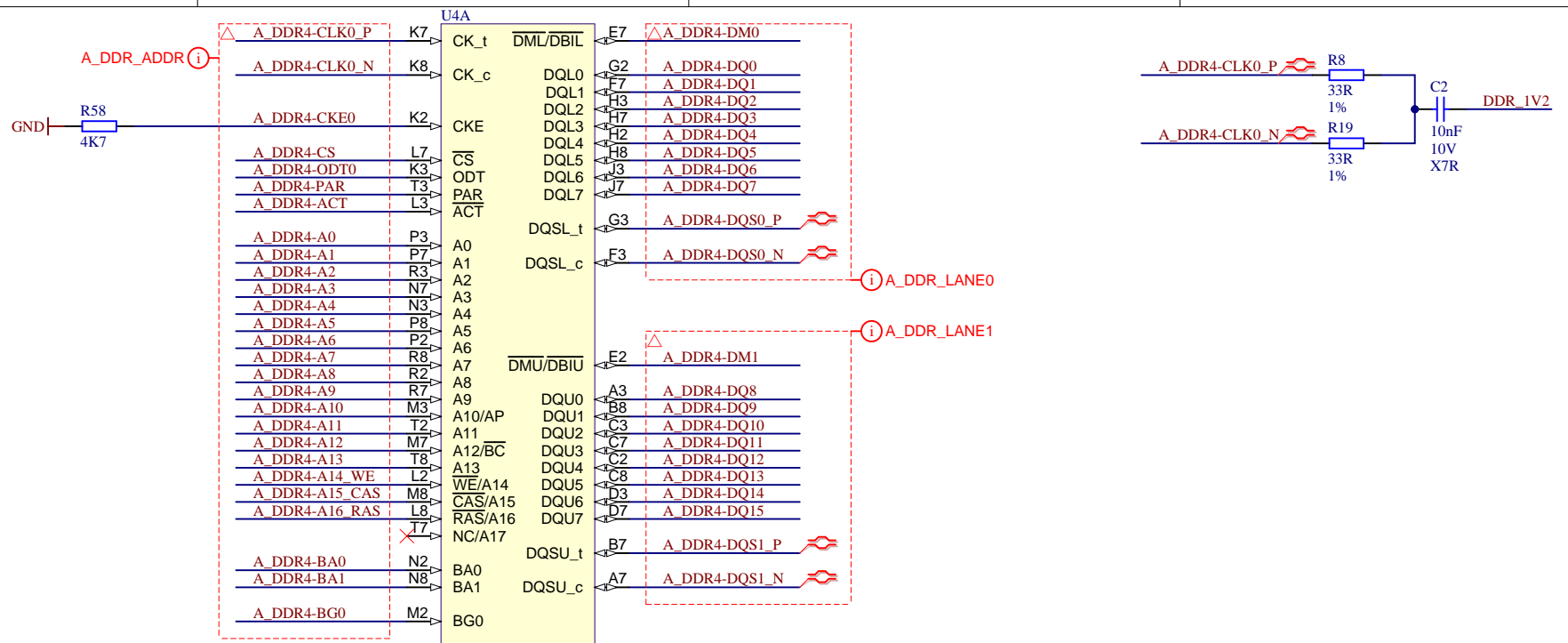


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	Filename: <b>CPLD.SchDoc</b>		



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Filename: <b>Clock.SchDoc</b>			





Title: TE0841		
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Filename: DDR4-RAM.SchDoc		

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A

A

B

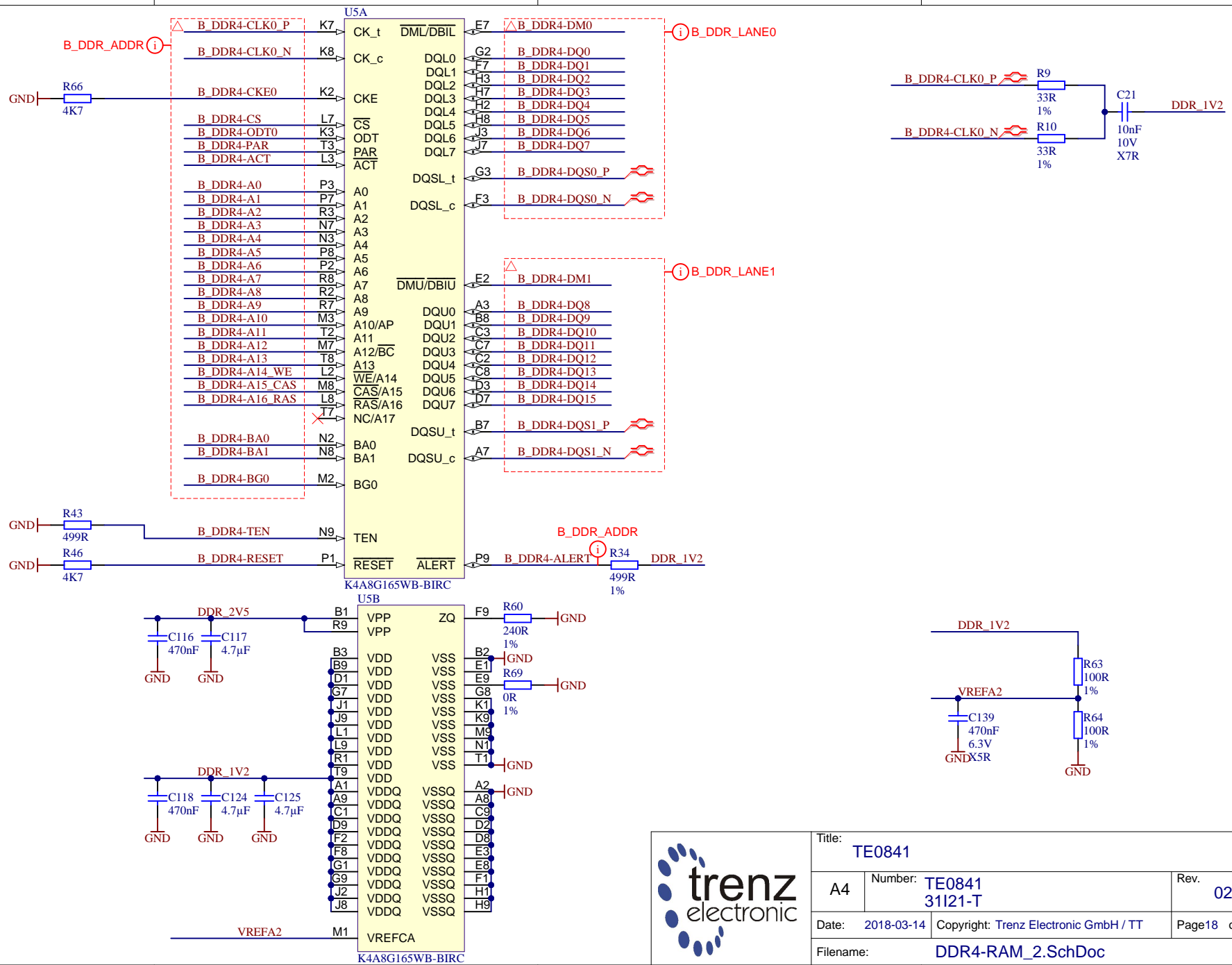
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C

C

D

D



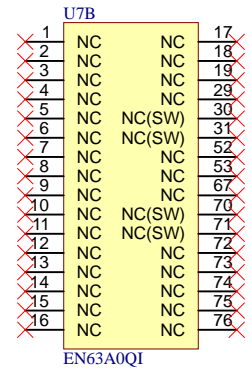
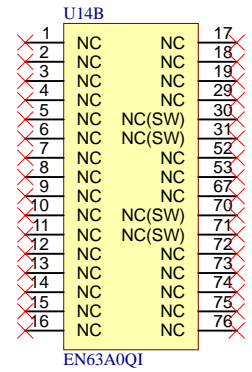
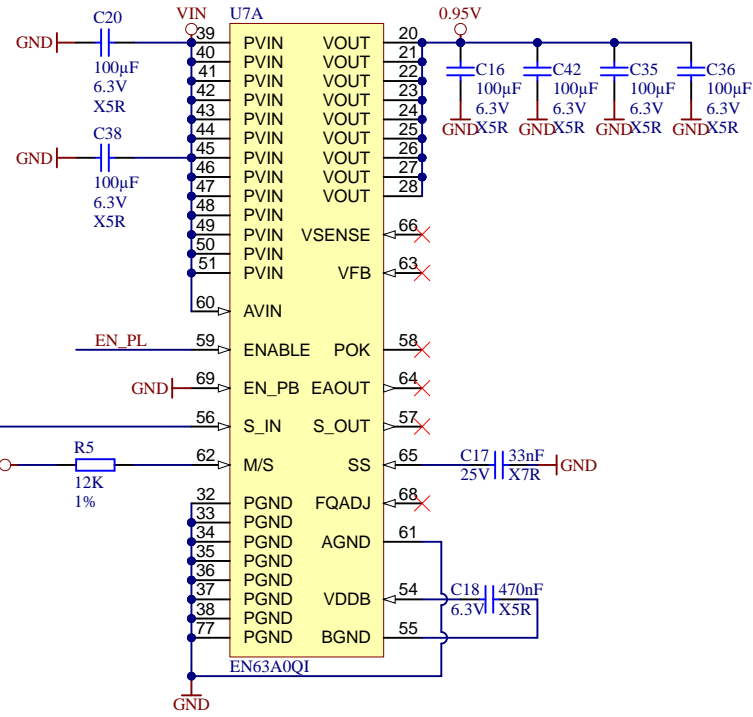
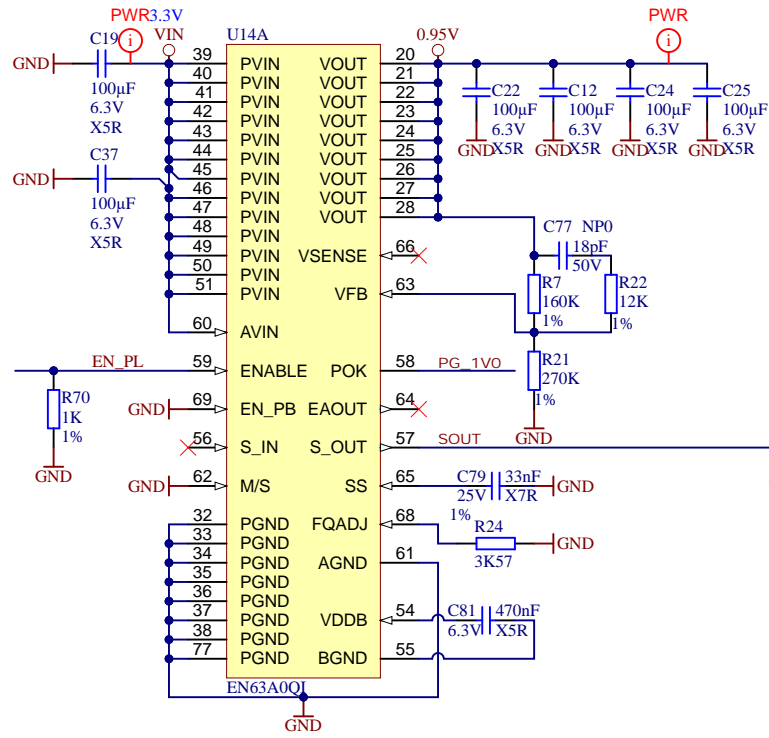
Title: TE0841		
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Filename: DDR4-RAM_2.SchDoc		

1

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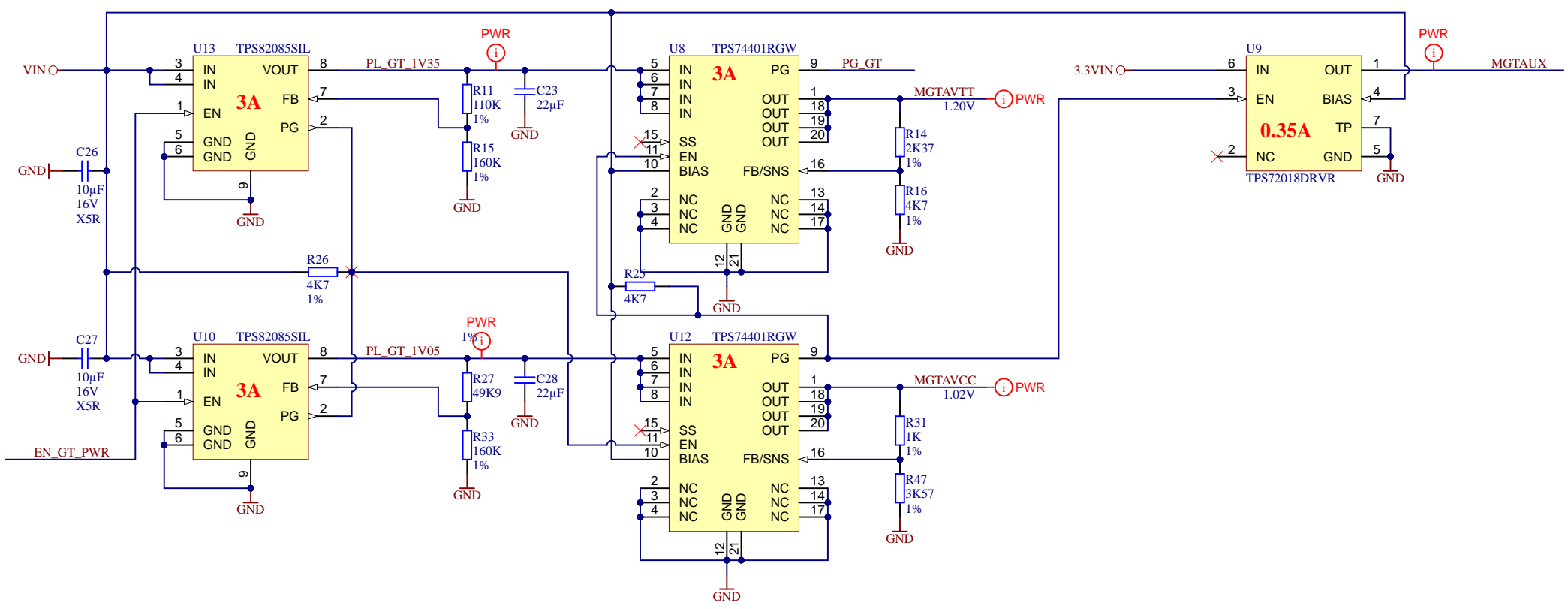
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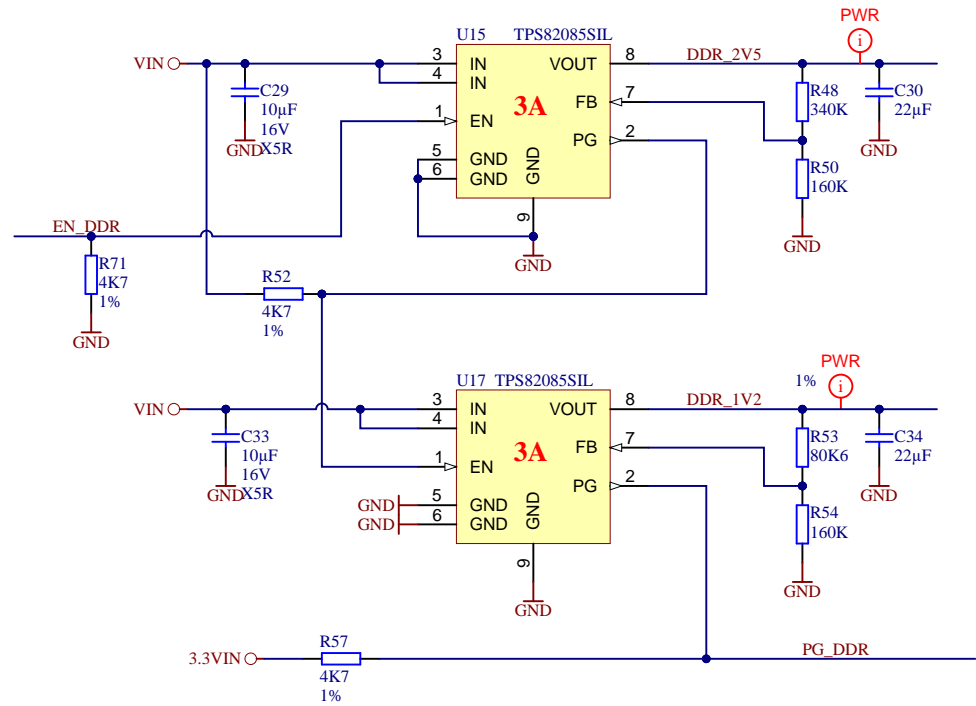
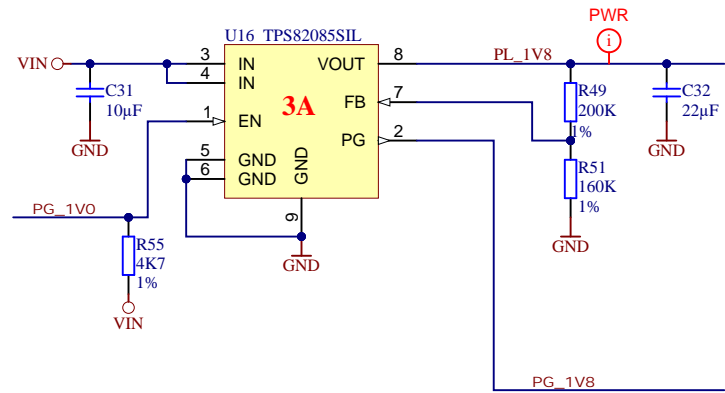


Title: **TE0841**

A4	Number: <b>TE0841 31I21-T</b>	Rev. <b>02</b>
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Filename: <b>PWR1.SchDoc</b>	Page 19 of 21	



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	Filename: PWR2.SchDoc		



Title: TE0841		
A4	Number: TE0841 31121-T	Rev. 02
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Filename: POWER_2.SchDoc		

CHANGES REV01 TO REV01A (08.16.2017):


1) U1: changed schematic symbol. Next pins swapped to mach same polarity order:  
 -- AE13 (IO\_L6P\_T0U\_N10\_AD6P\_64)/AE12 (IO\_L6N\_T0U\_N11\_AD6N\_64)  
 -- J5 (IO\_L18P\_T2U\_N10\_AD2P\_66)/J4 (IO\_L18N\_T2U\_N11\_AD2N\_66)

2) Net names changed (no electrical changes):

JM1: swapped signals B64\_L6:  
 -- B64\_L6\_N - pin 40 (was pin 42)  
 -- B64\_L6\_P - pin 42 (was pin 40)  
 JM3: swapped signals B64\_L6:  
 -- B66\_L18\_N - pin 52 (was pin 54)  
 -- B66\_L18\_P - pin 54 (was pin 52)

CHANGES REV01A TO REV02 ( 03.2018):

- 1) U4 / U5: changed DDR4 chip: NT5AD256M16B2-GN -> K4A4G165WE-BCRC (K4A8G165WB-BIRC)
- 2) Fixed sense connection on DCDC
- 3) U6: changed SPI flash chip: N25Q256A11E1240E-> N25Q512A11G1240E
- 4) Full update LIB
- 5) Added additional resistors for support 16GBit DDR chips
- 6) Added strong pull-down to EN\_PL
- 7) Added additional testpoints for I2C bus
- 8) Added additional MEMS oscillator (25MHz)
- 9) Changed pull-up power supply VIN -> 3.3VIN on the PG\_DDR net
- 10) Added pull-down on the EN\_DDR (04.05.2022)
- 11) S/N Track-it pad set not fitted

	Title: <b>TE0841 - Changes list</b>		
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	Filename: <b>Revision_Changes.SchDoc</b>		