U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-MISC
FPGA-MISC.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

U_FPGA-B44
FPGA-B44.SchDoc

U_FPGA-B45
FPGA-B45.SchDoc

U_FPGA-B46
FPGA-B46.SchDoc

U_FPGA-B47
FPGA-B47.SchDoc

U_FPGA-B64
FPGA-B64.SchDoc

U_FPGA-B65
FPGA-B65.SchDoc

U_FPGA-B66
FPGA-B66.SchDoc

U_FPGA-B67
FPGA-B67.SchDoc

U_FPGA-B68
FPGA-B68.SchDoc

U_DDR4-RAM
DDR4-RAM.SchDoc

U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

U_B2B-Connectors
B2B-Connectors.SchDoc

U_CPLD
CPLD.SchDoc

U_Clock
Clock.SchDoc

U_PWR1
PWR1.SchDoc

U_PWR2
PWR2.SchDoc

U_POWER_2
POWER_2.SchDoc

Mount.Hole 3.2mm
GND

Mount.Hole 3.2mm
GND

Mount.Hole 3.2mm
GND

Mount.Hole 3.2mm
GND

PM1
FIDU-DOT - mini

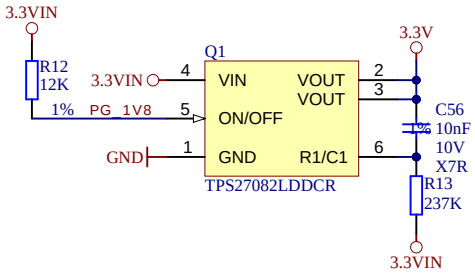
PM2
FIDU-DOT - mini

PM3
FIDU-DOT - mini

PM4
FIDU-DOT - mini

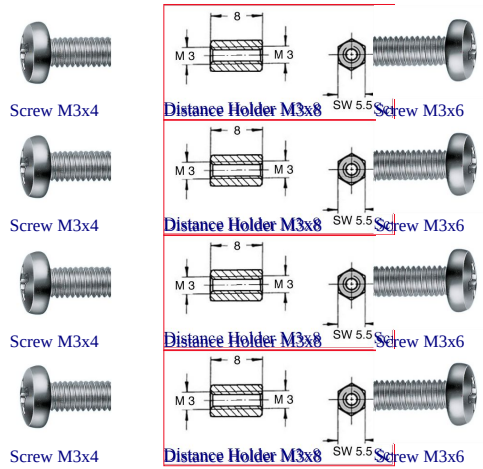
PM5
FIDU-DOT - mini

PM6
FIDU-DOT - mini



Serial
Serial
Serialnumber 6,3 x 6.3mm

Top of Board



Assembly variant	41C21-A
Created by	VY
Modified by	VY
Modified at	2019-07-10
SVN Revision	8580

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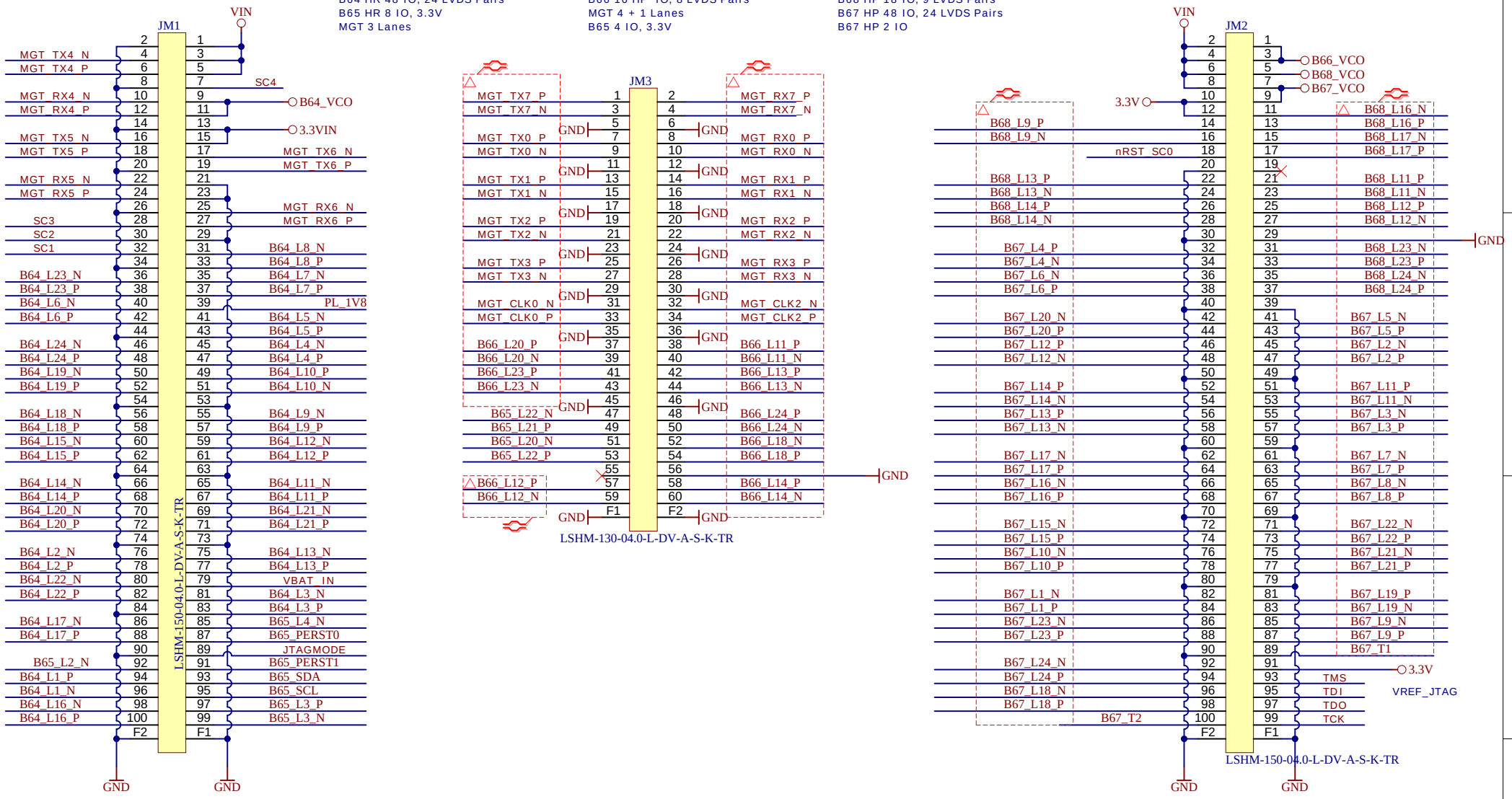
Title: TE0841		
A4	Number: TE0841 41C21-A	Rev. 02
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT	Page1 of 21
Filename: TE0841.SchDoc		



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Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page2 of 21
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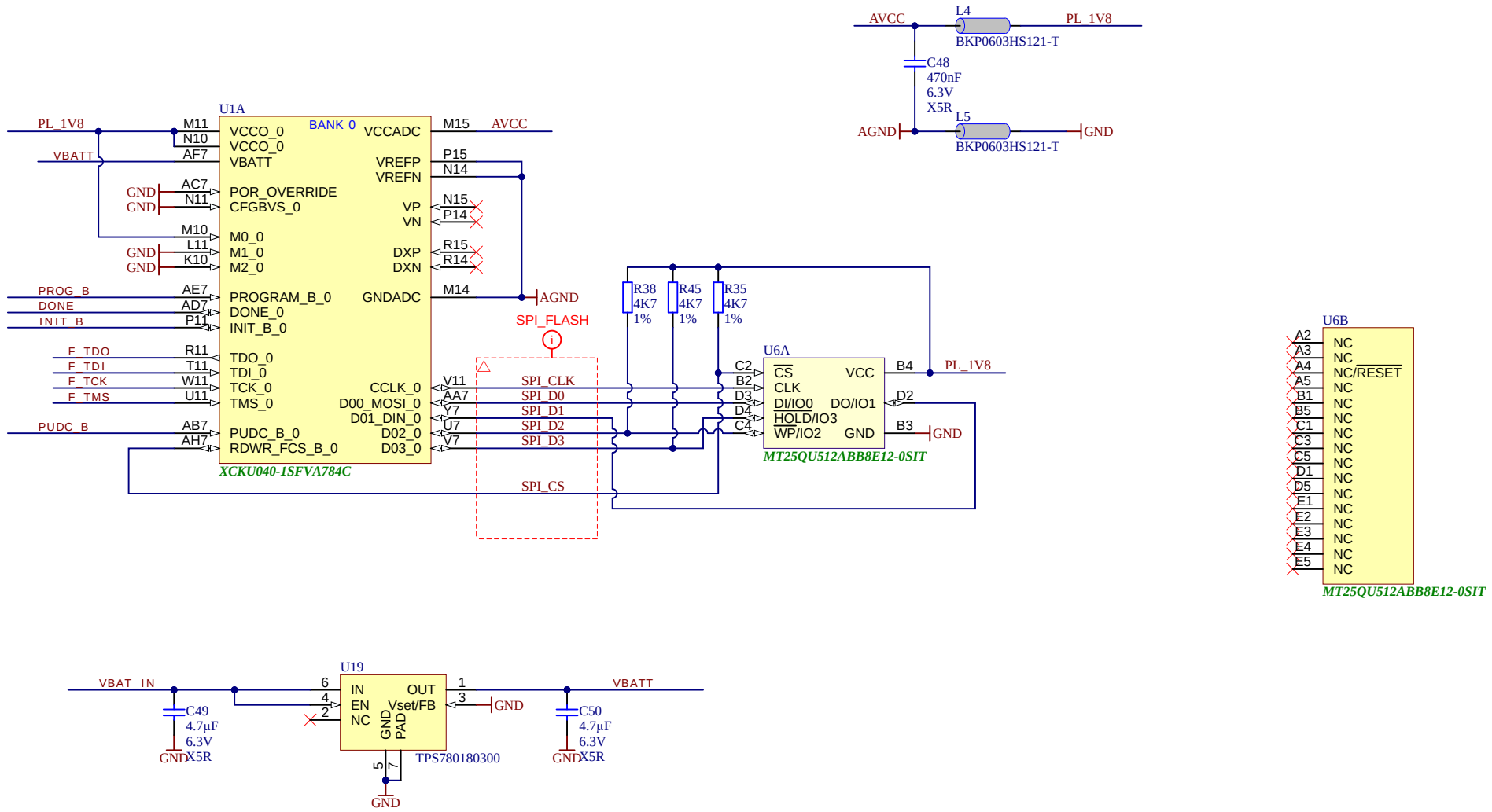

trenz electronic	Title: TE0841		
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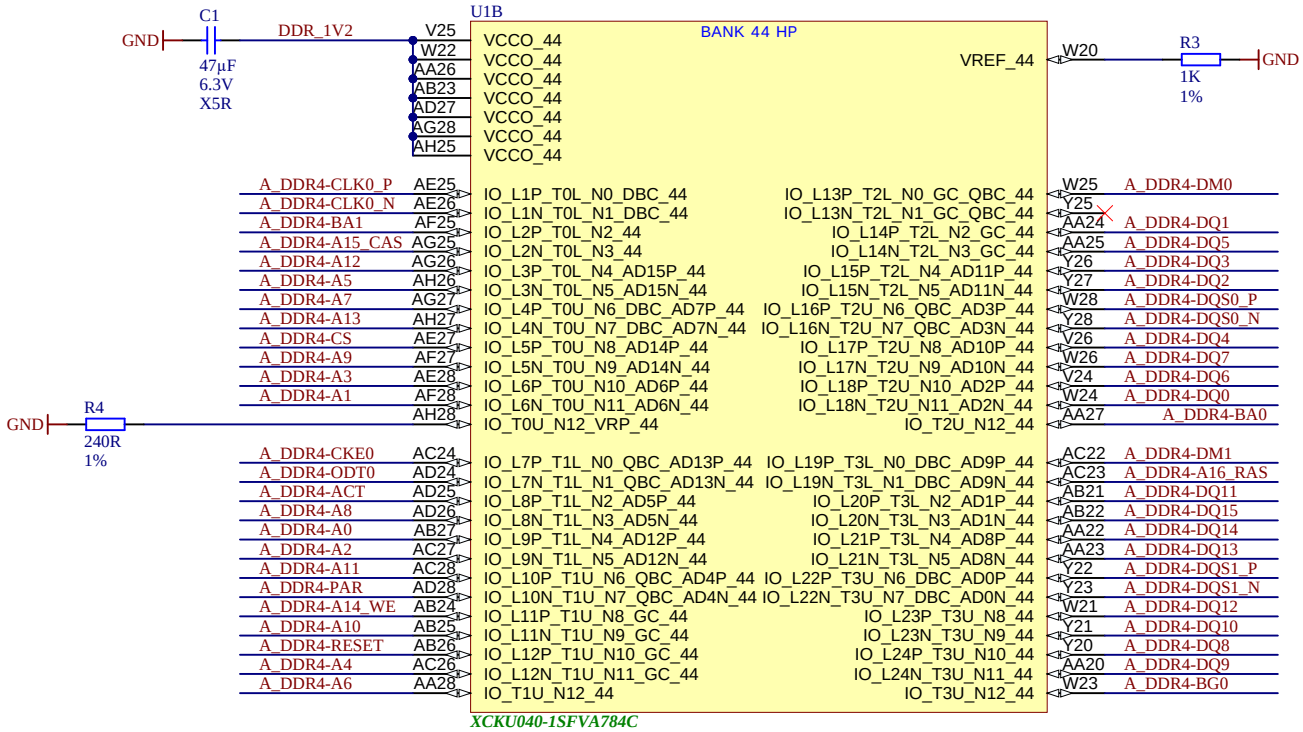
	Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT	Page3 of 21
	Filename: FPGA-MISC.SchDoc		



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	Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT	Page4 of 21
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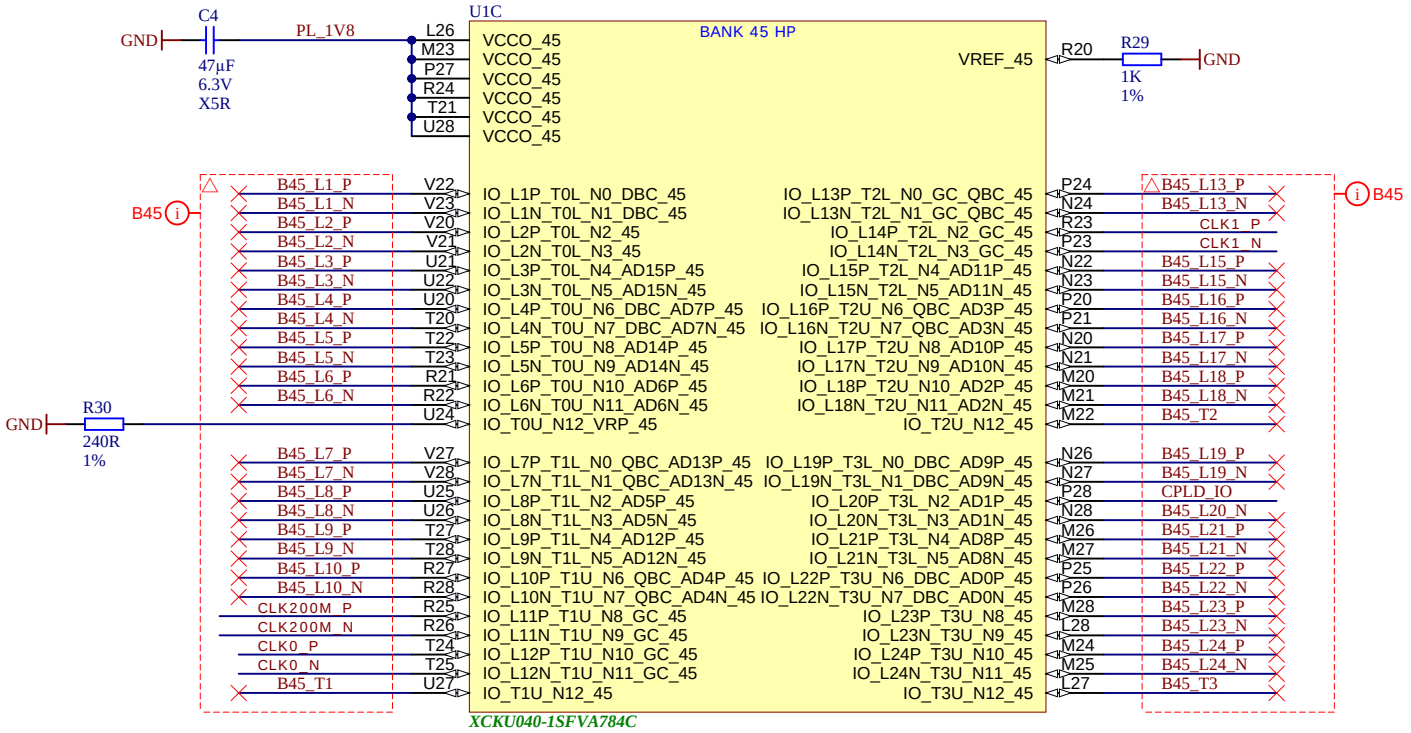

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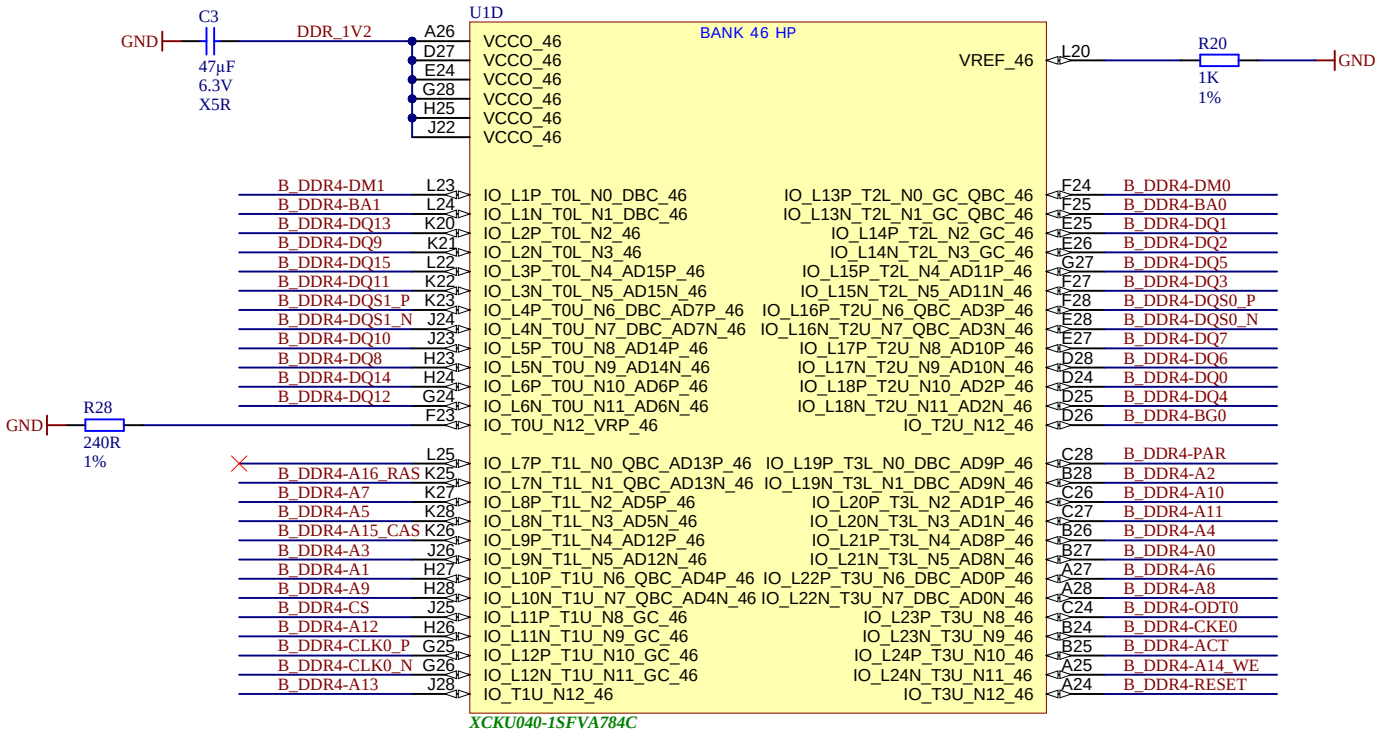
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page5 of 21
Filename: FPGA-B45.SchDoc			



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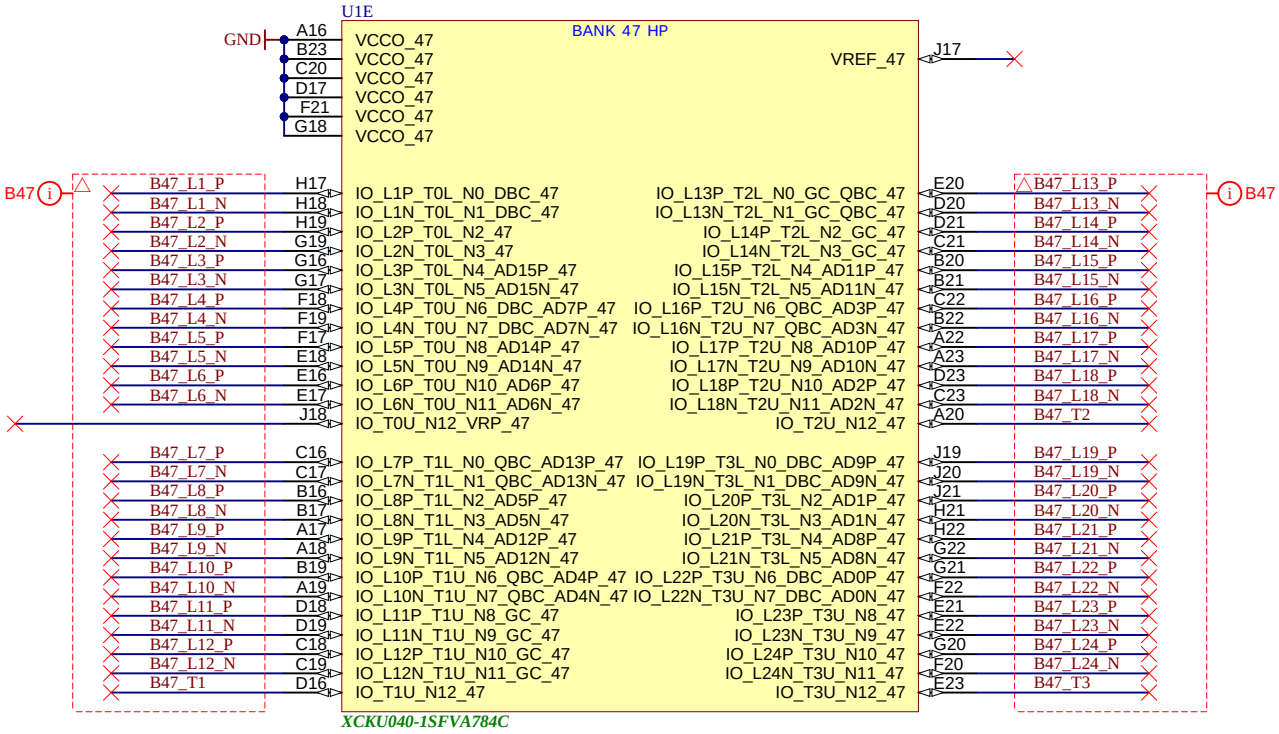
	Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT	Page6 of 21
	Filename: FPGA-B46.SchDoc		



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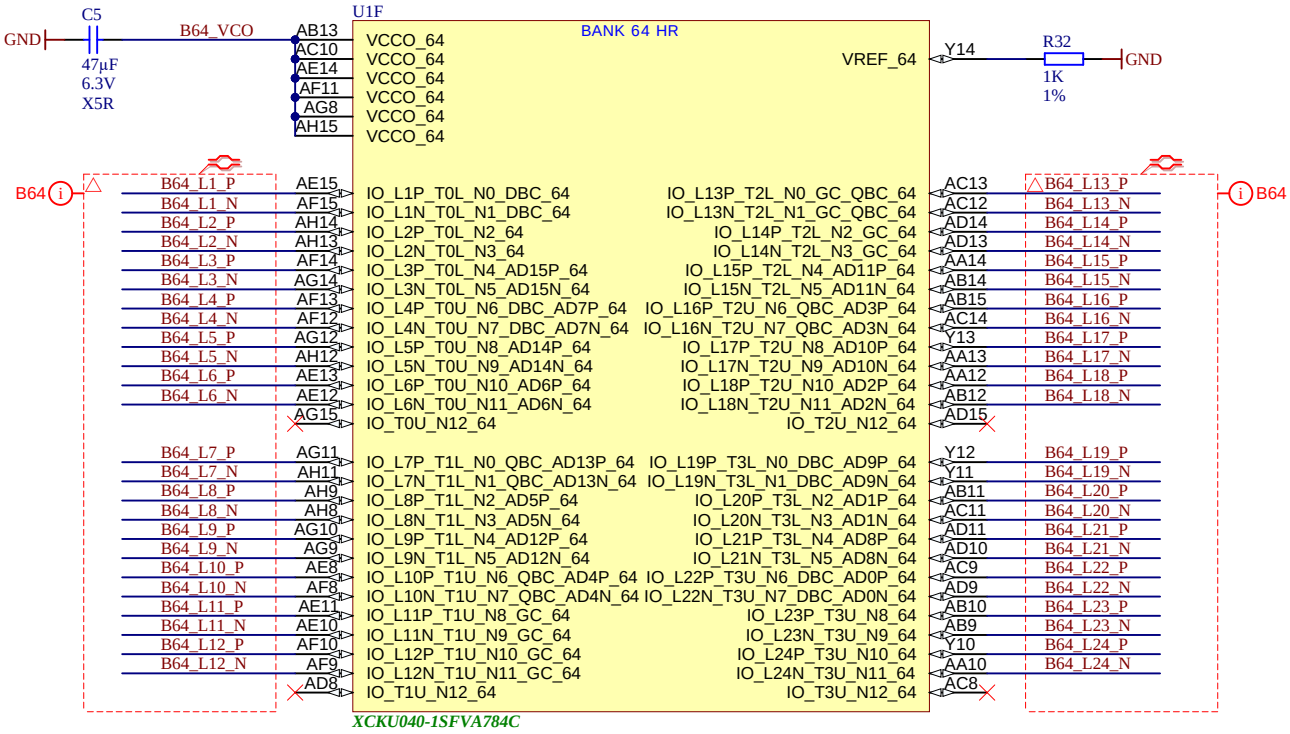
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page7 of 21
Filename: FPGA-B47.SchDoc			



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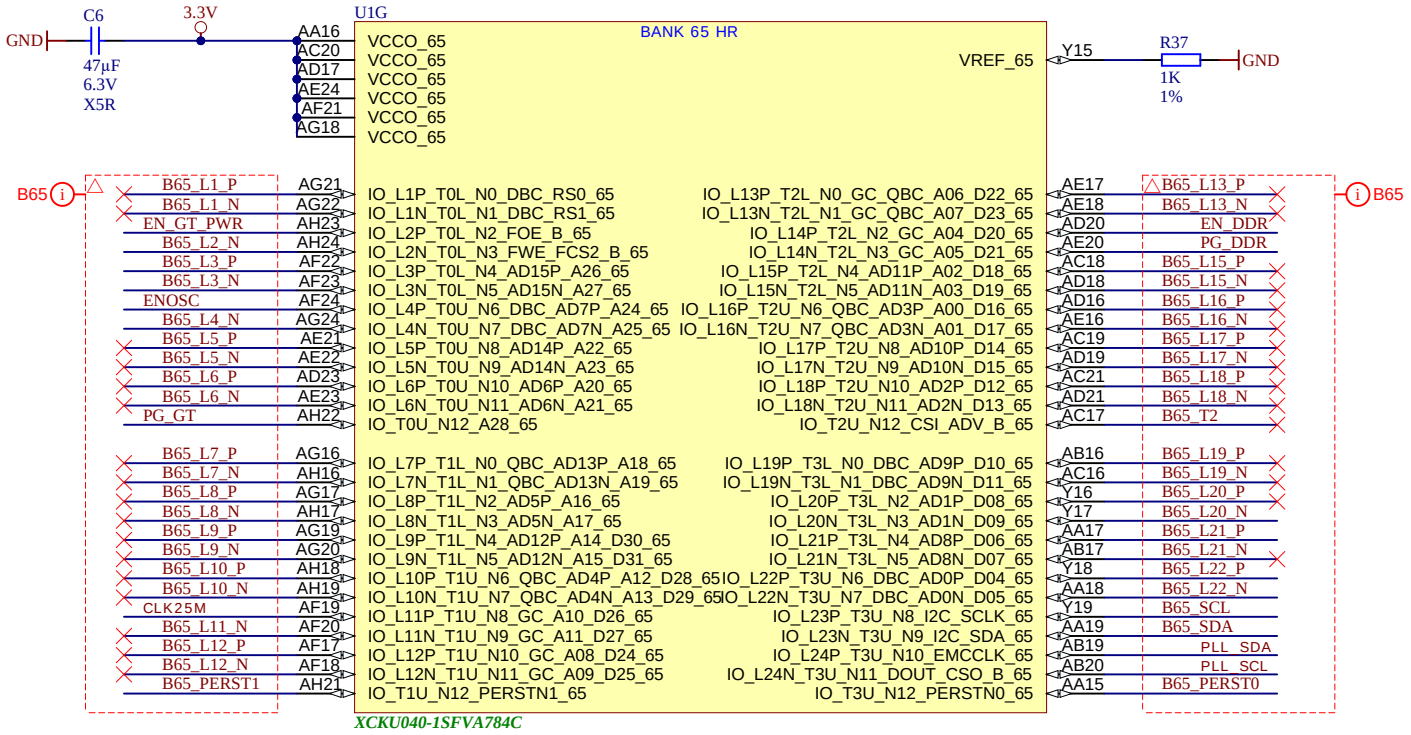
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page8 of 21
Filename: FPGA-B64.SchDoc			



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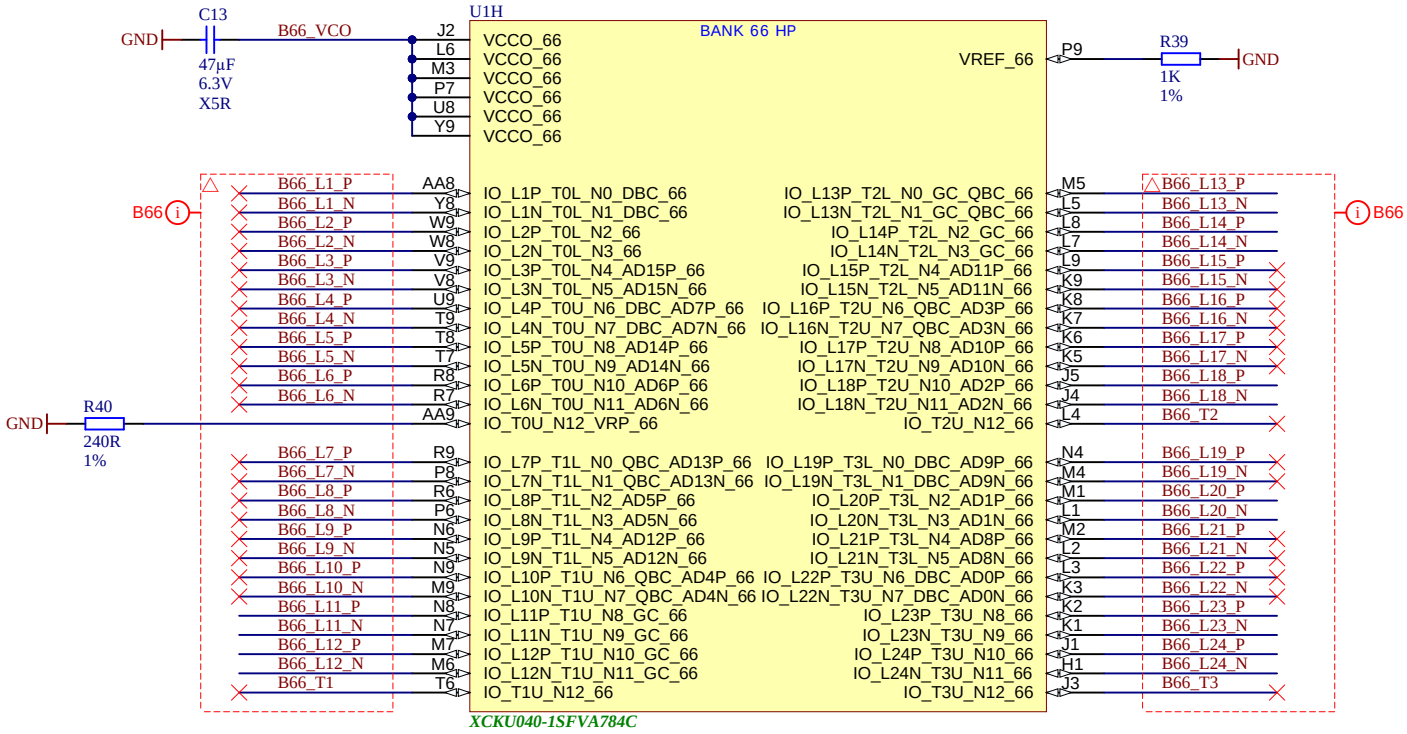
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page9 of 21
Filename: FPGA-B65.SchDoc			



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	Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT	Page10 of 21
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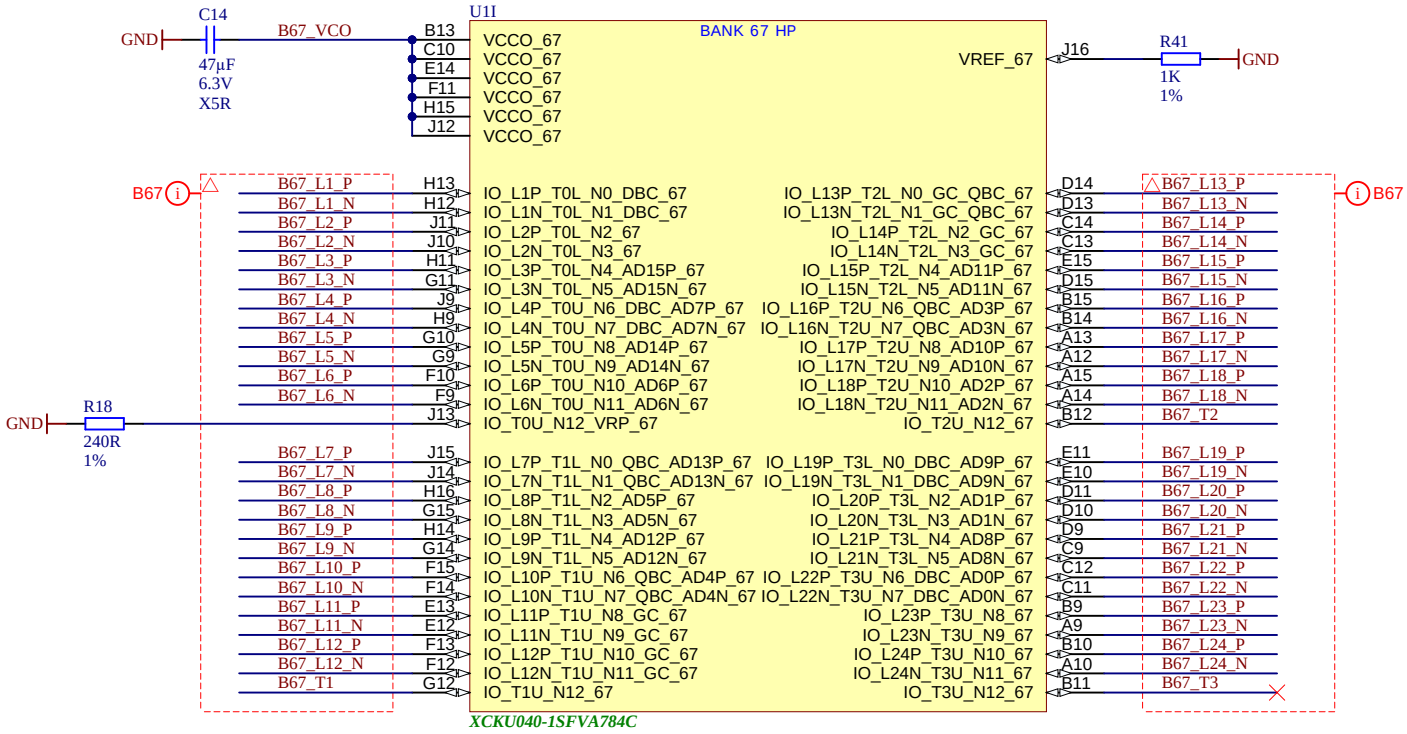

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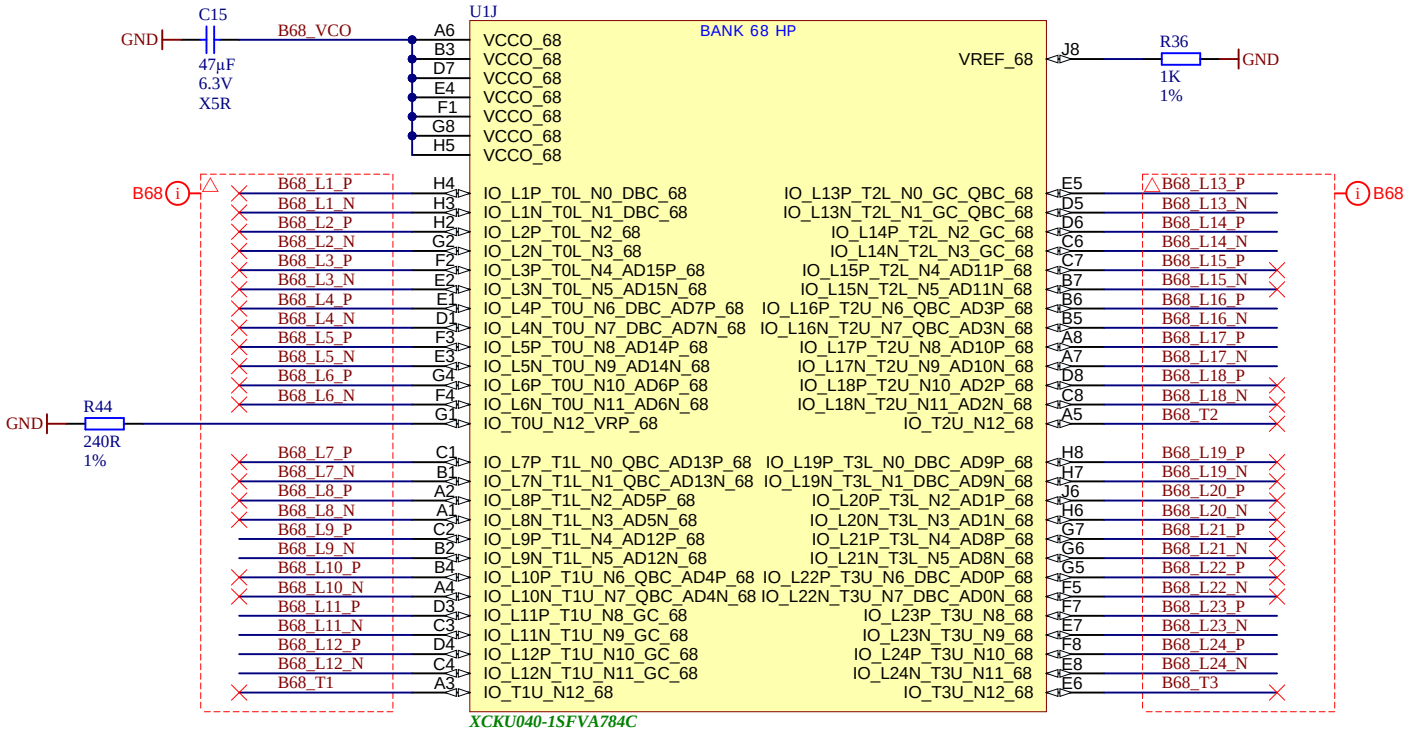
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT	Page 11 of 21
Filename: FPGA-B67.SchDoc		



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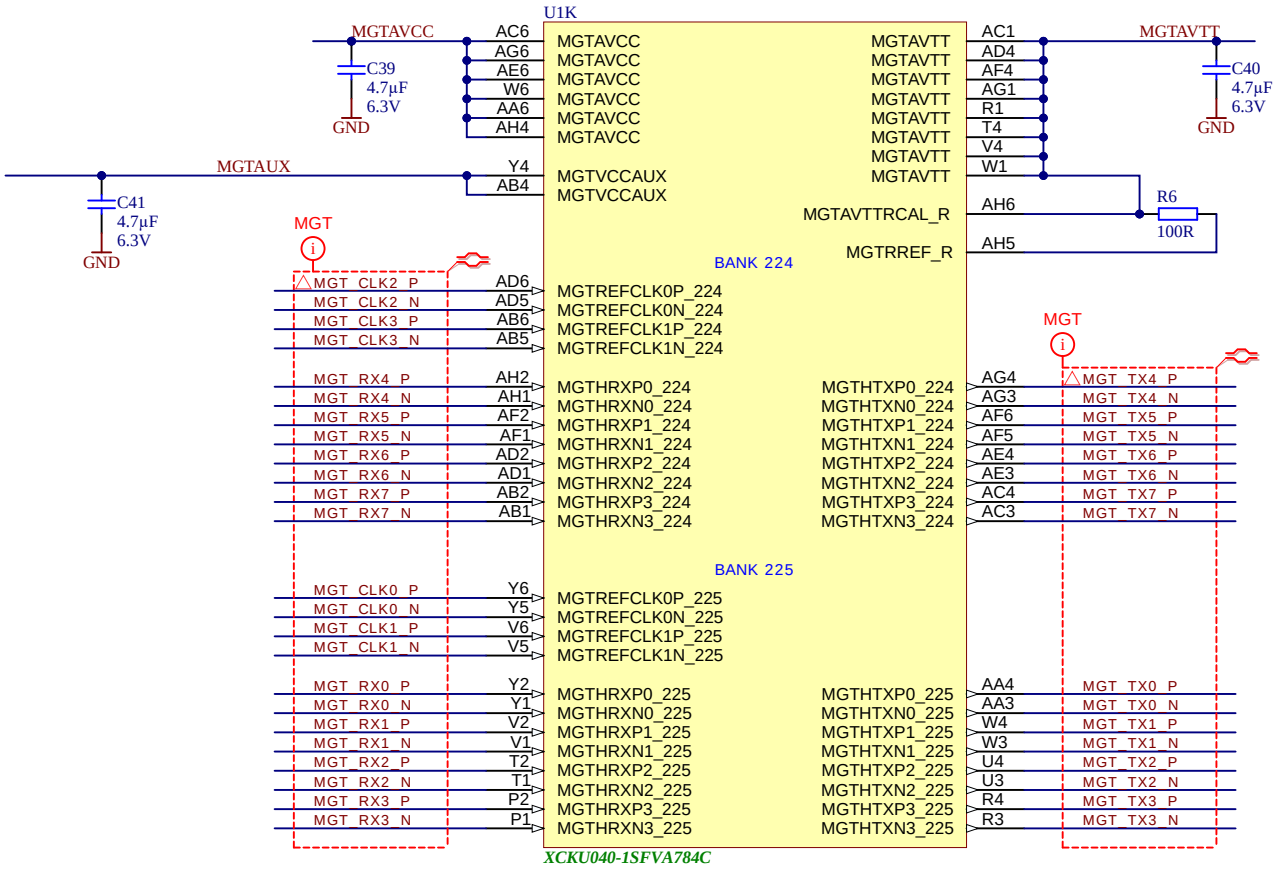
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page12 of 21
Filename: FPGA-B68.SchDoc			



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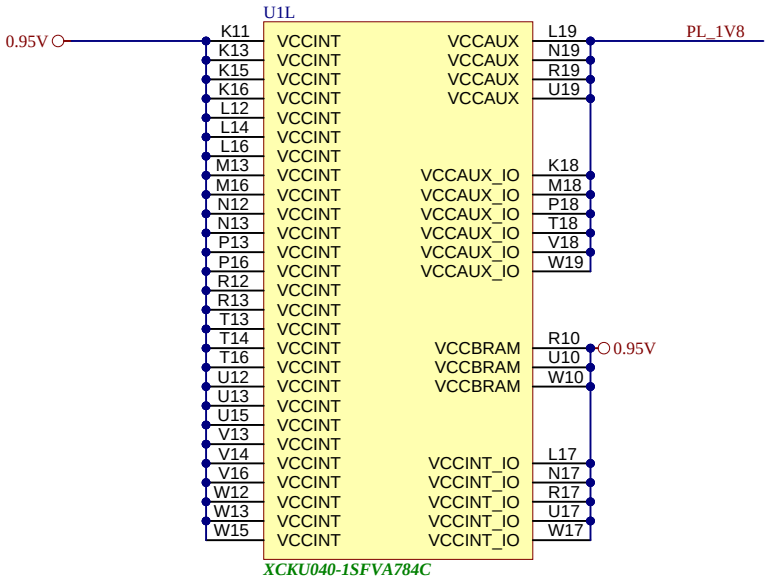
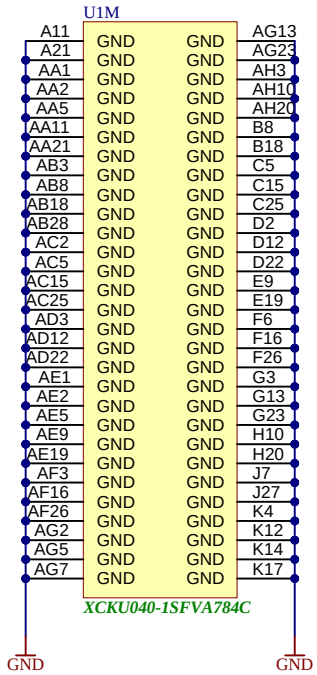
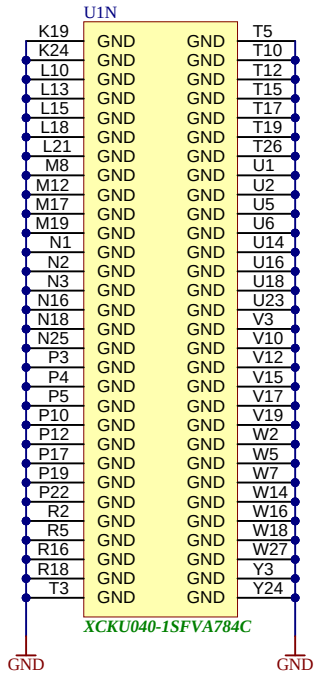
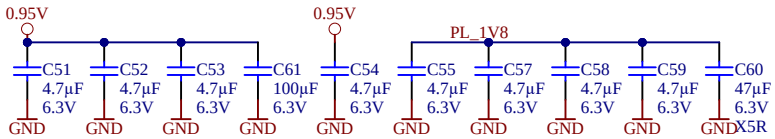
	Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT	Page13 of 21
	Filename: FPGA-MGT.SchDoc		









trenz electronic	Title: TE0841		
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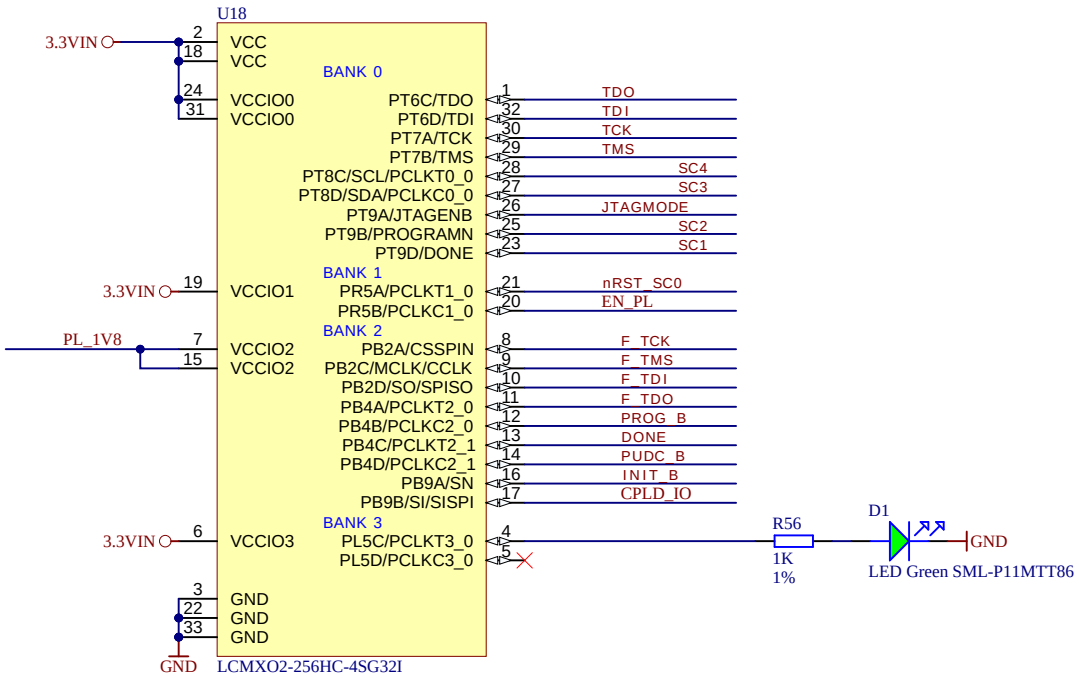
	Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT	Page14 of 21
	Filename: FPGA-PWR.SchDoc		



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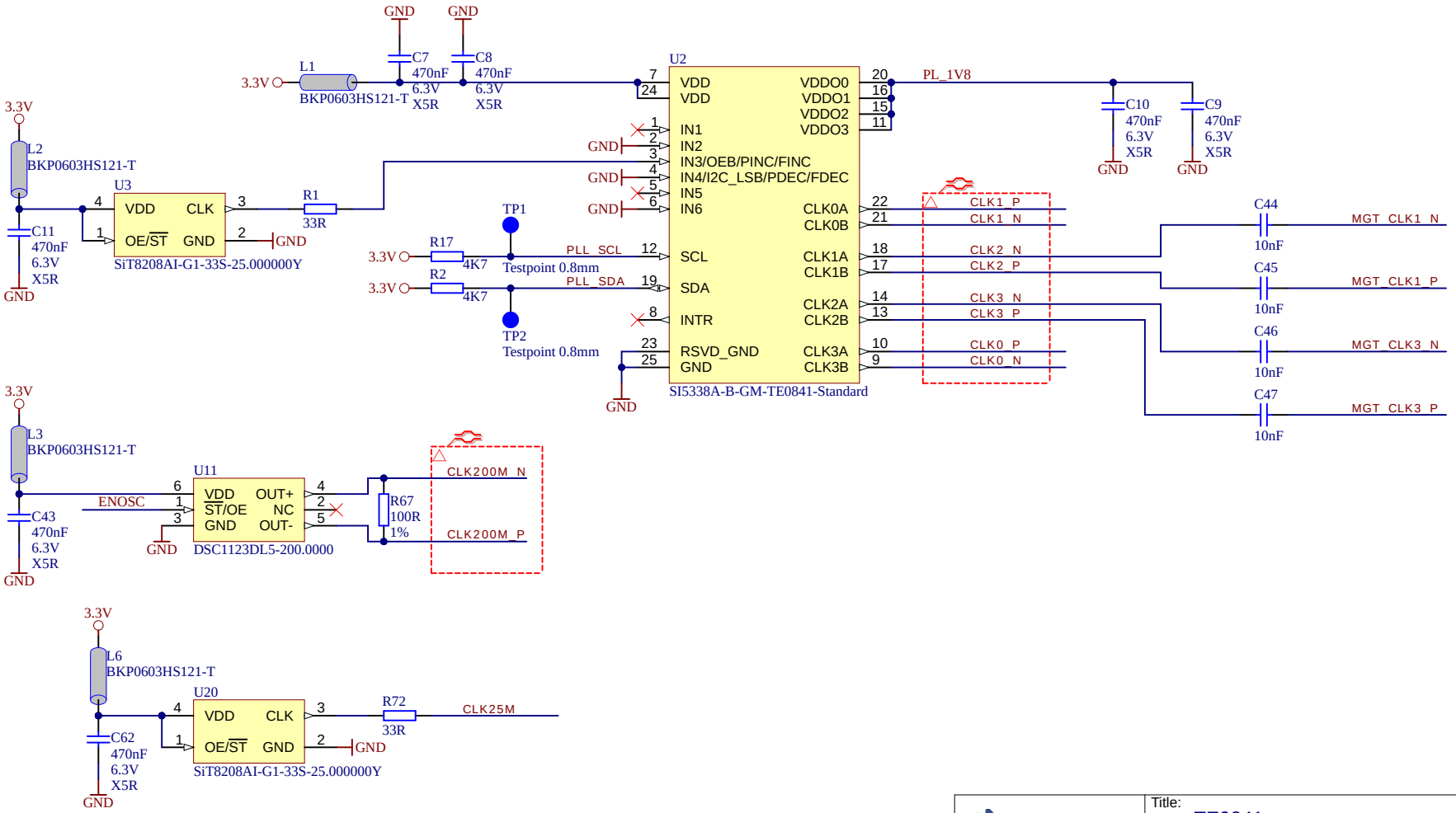
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page15 of 21
Filename: CPLD.SchDoc			



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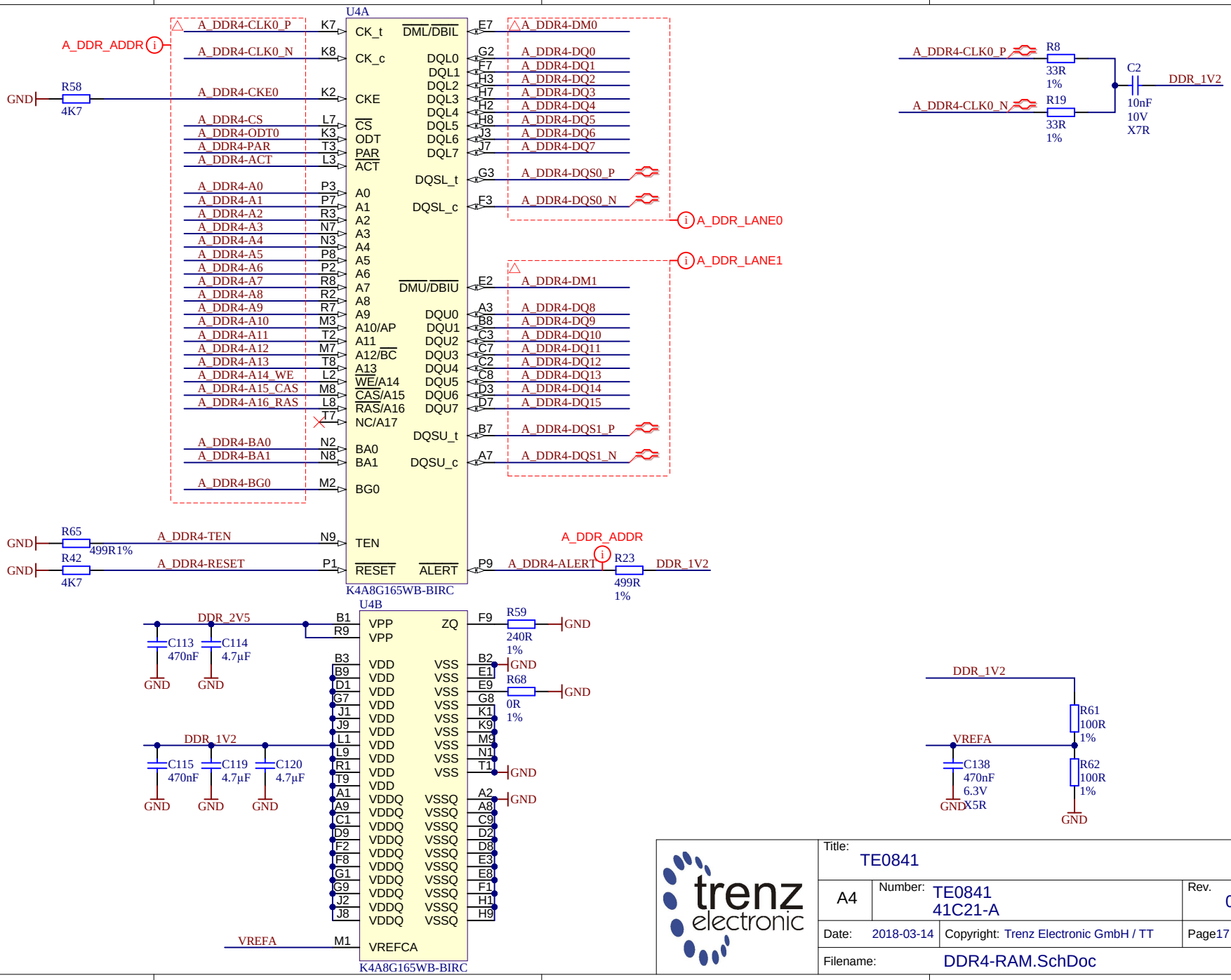
Title: TE0841			
A4	Number: TE0841 41C21-A		Rev. 02
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page16 of 21
Filename: Clock.SchDoc			



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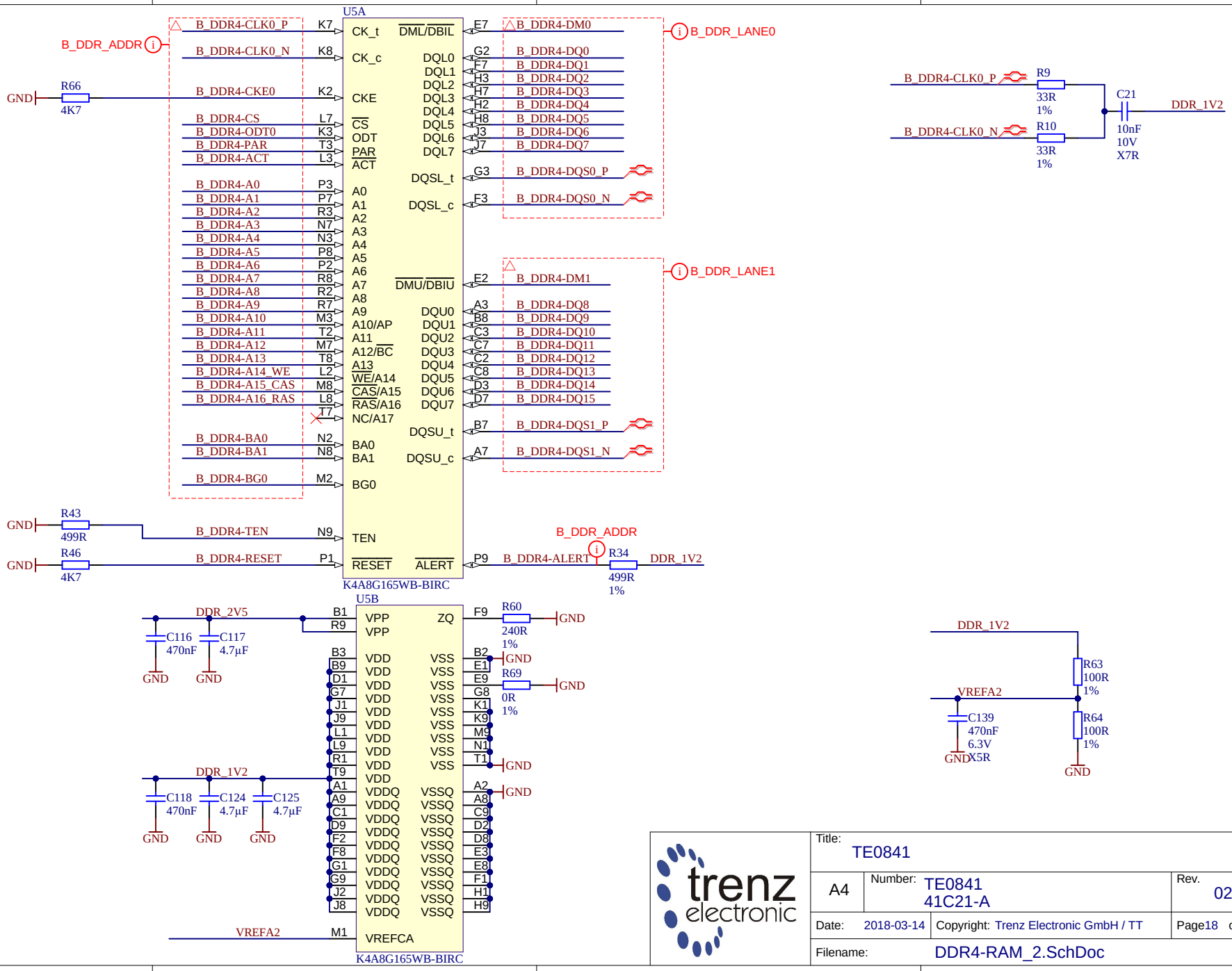
A4	Number: TE0841 41C21-A		Rev. 02
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page17 of 21
Filename: DDR4-RAM.SchDoc			



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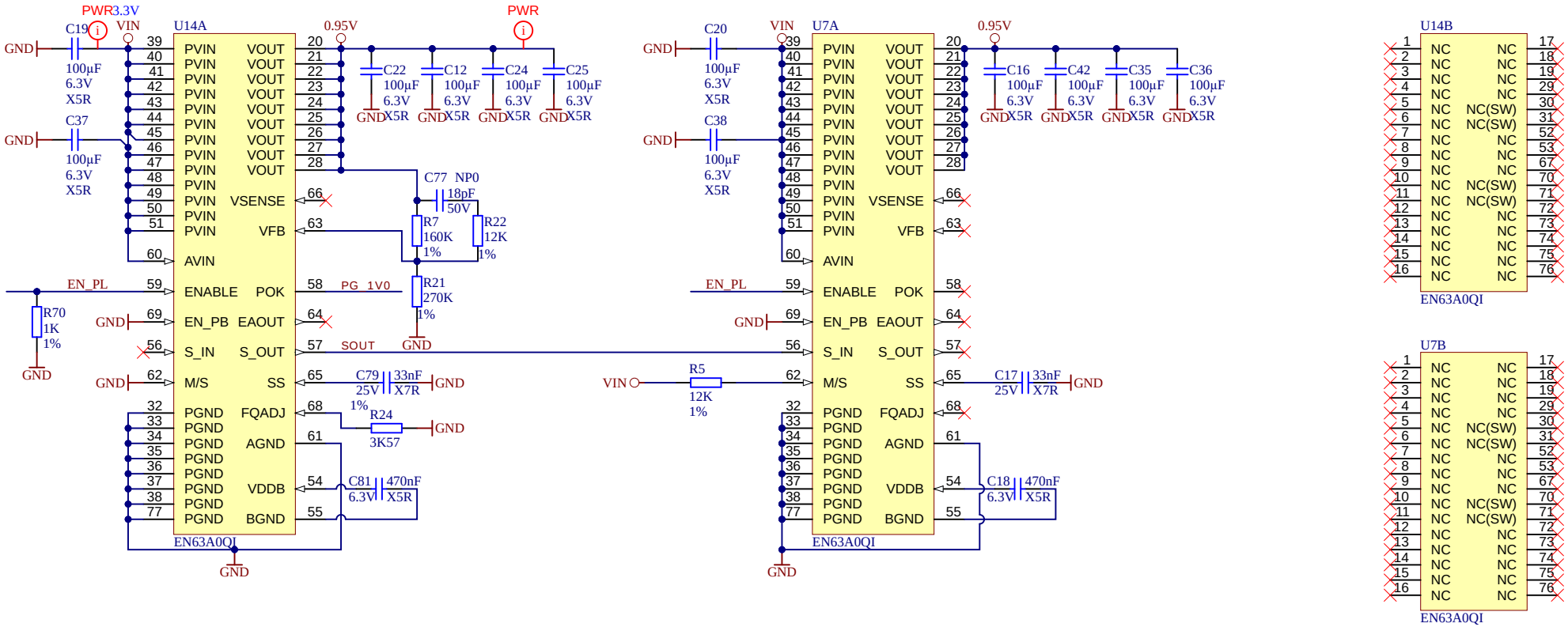
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page18 of 21
Filename: DDR4-RAM_2.SchDoc			



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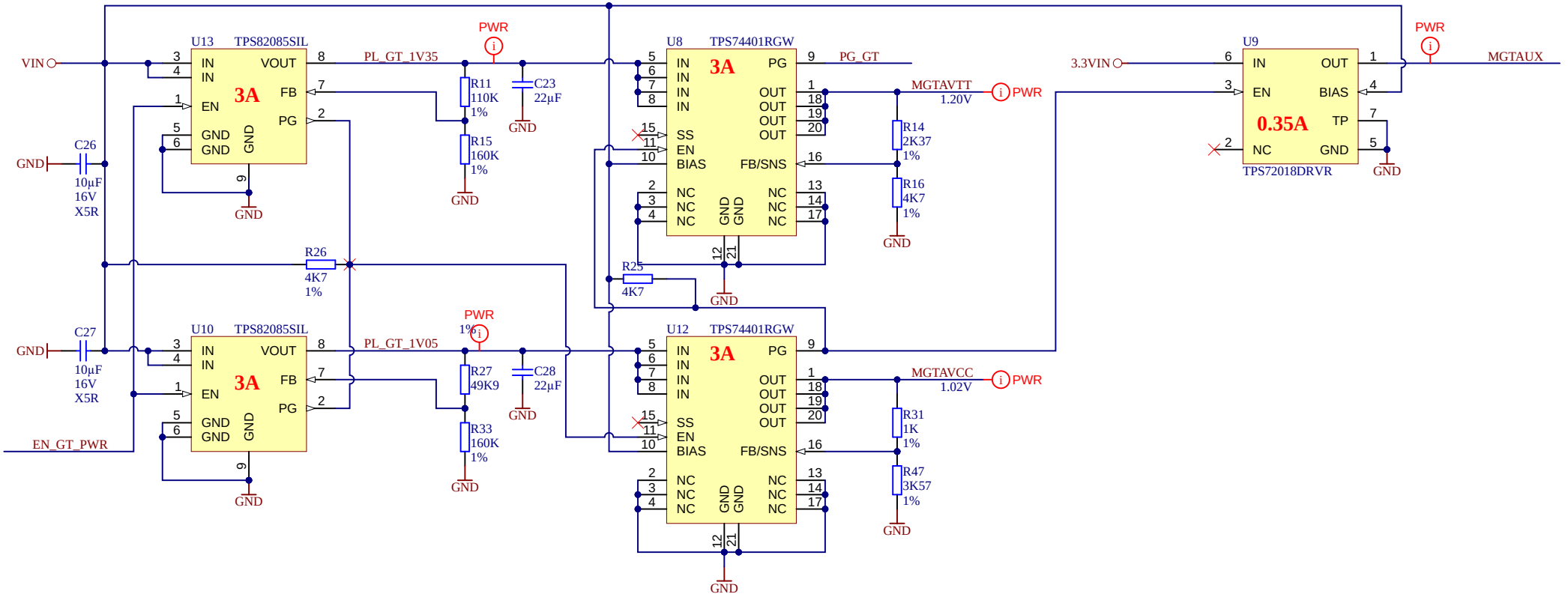
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page19 of 21
Filename: PWR1.SchDoc			



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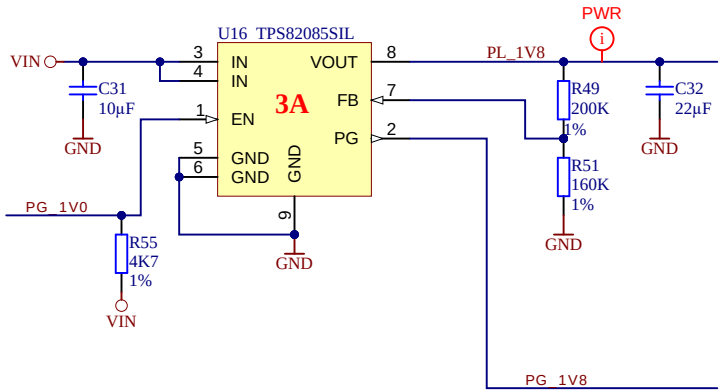
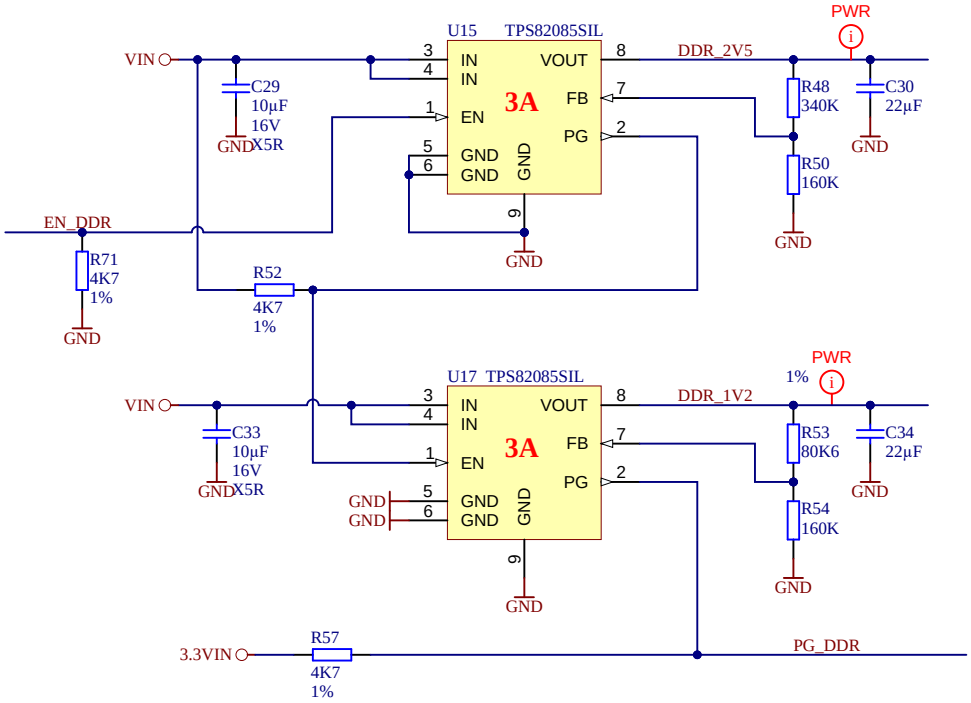
Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT		Page20 of 21
Filename: PWR2.SchDoc			





trenz electronic	Title: TE0841		
	A4	Number: TE0841 41C21-A	Rev. 02
	Date: 2018-03-14	Copyright: Trenz Electronic GmbH / TT	Page21 of 21
	Filename: POWER_2.SchDoc		

CHANGES REV01 TO REV01A (08.16.2017):

1) U1: changed schematic symbol. Next pins swapped to mach same polarity order:
-- AE13 (IO_L6P_T0U_N10_AD6P_64)/AE12 (IO_L6N_T0U_N11_AD6N_64)
-- J5 (IO_L18P_T2U_N10_AD2P_66)/J4 (IO_L18N_T2U_N11_AD2N_66)

2) Net names changed (no electrical changes):
JM1: swapped signals B64_L6:
-- B64_L6_N - pin 40 (was pin 42)
-- B64_L6_P - pin 42 (was pin 40)
JM3: swapped signals B64_L6:
-- B66_L18_N - pin 52 (was pin 54)
-- B66_L18_P - pin 54 (was pin 52)

CHANGES REV01A TO REV02 (03.2018):

1) U4 / U5: changed DDR4 chip: NT5AD256M16B2-GN -> K4A4G165WE-BCRC (K4A8G165WB-BIRC)
2) Fixed sense connection on DCDC
3) U6: changed SPI flash chip: N25Q256A11E1240E-> N25Q512A11G1240E
4) Full update LIB
5) Added additional resistors for support 16GBit DDR chips
6) Added strong pull-down to EN_PL
7) Added additional testpoints for I2C bus
8) Added additional MEMS oscillator (25MHz)
9) Changed pull-up power supply VIN -> 3.3VIN on the PG_DDR net
10) Added pull-down on the EN_DDR
(04.05.2022)
11) S/N Track-it pad set not fitted

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Title: TE0841 - Changes list			
A4	Number: TE0841 41C21-A		Rev. 02
Date: 2018-03-14	Copyright: Trenz Electronic GmbH		Page22 of 22
Filename: Revision_Changes.SchDoc			