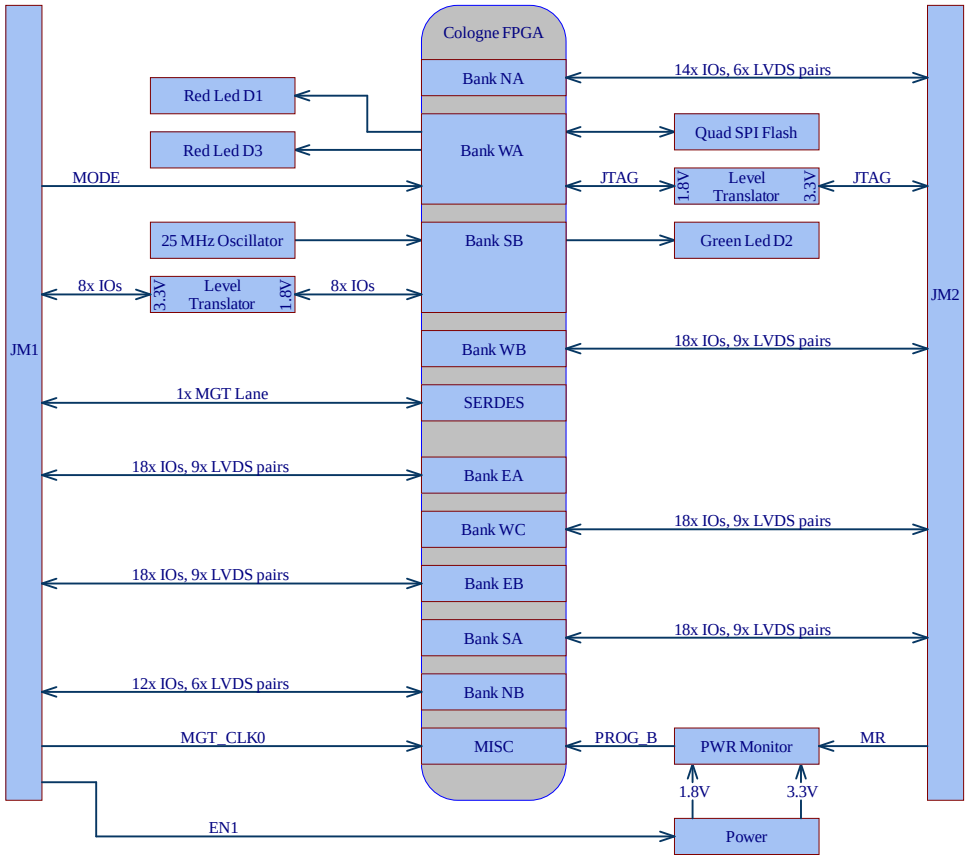
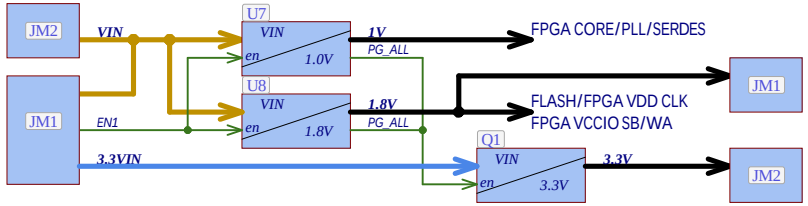
REV	Description	
-01	Initial revision	MT

Title: TEG2000 - Changes list		
A4	Number: TEG2000 P001	Rev. 01
Date: 08-Aug-23	Copyright: Trenz Electronic GmbH	Page 1 of 10
Filename: Revision_Changes.SchDoc		

System Overview



Power Sequence



Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5.0V	+/-5%	Micromodule Power	-
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	-
VCCIOA	IN	1.1 - 2.7V	+/-3%	IO Banks NB/EB/EA	-
VCCIOC	IN	1.1 - 2.7V	+/-3%	IO Bank SA	-
VCCIOD	IN	1.1 - 2.7V	+/-5%	IO Banks NA/WB/WC	-
1.8V	OUT	1.8V	+/-3%	Power for Carrier	-
3.3V	OUT	3.3V	+/-5%	Power for Carrier	-

TEG2000.SchDoc

FPGA-PWR.SchDoc

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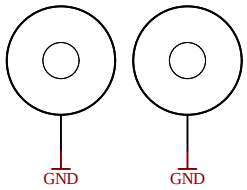
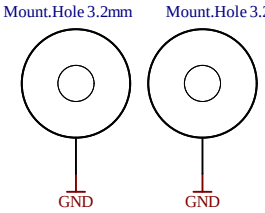
Title: TEG2000 - System Overview		
A4	Number: TEG2000 P001	Rev. 01
Date: 04-Sep-23	Copyright: Trenz Electronic GmbH	Page 2 of 10
Filename: Overview.SchDoc		

Mount.Hole 3.2mm



Mount.Hole 3.2mm

Mount.Hole 3.2mm



Mount.Hole 3.2mm

Serial

Serial

Serialnumber 6,3 x 6.3mm

LOGO

TE Logo PRINT Layer

LOGO PRINT

CE

CE Logo on Top Overlay

CE-TOPOVERLAY

RoHS

RoHS Logo on Top Overlay

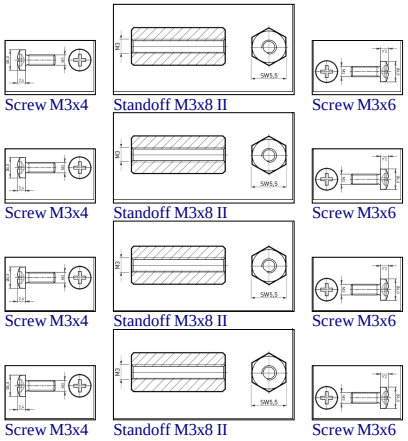
RoHS-TOPOVERLAY

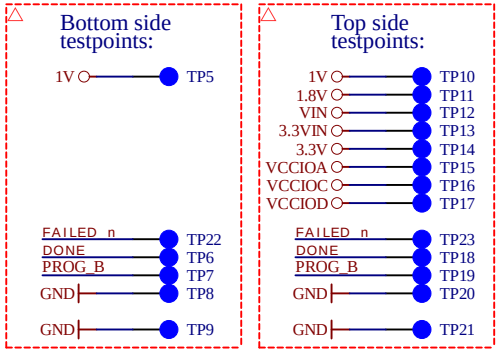
WEEE

WEEE Logo on Top Overlay

WEEE-TOPOVERLAY

Top of Board



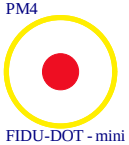


Special notes:

PM1

FIDU-DOT - mini

PM4

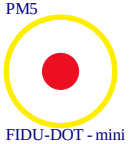


FIDU-DOT - mini

PM2

FIDU-DOT - mini

PM5

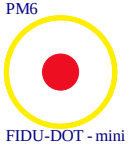


FIDU-DOT - mini

PM3

FIDU-DOT - mini

PM6



FIDU-DOT - mini

Assembly variant	P001
Created by	MT
Modified by	
Modified at	
SVN Revision	18871

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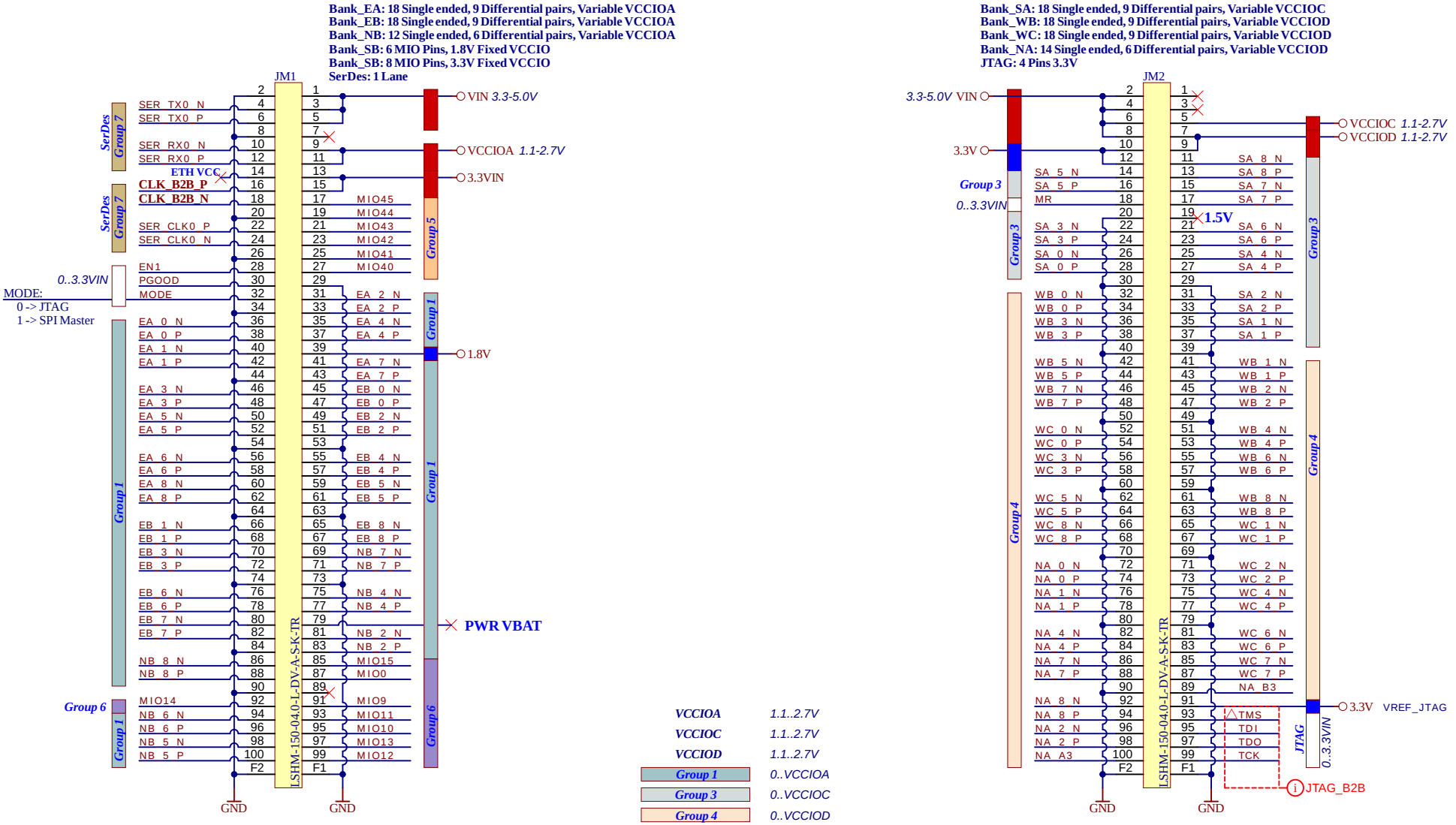
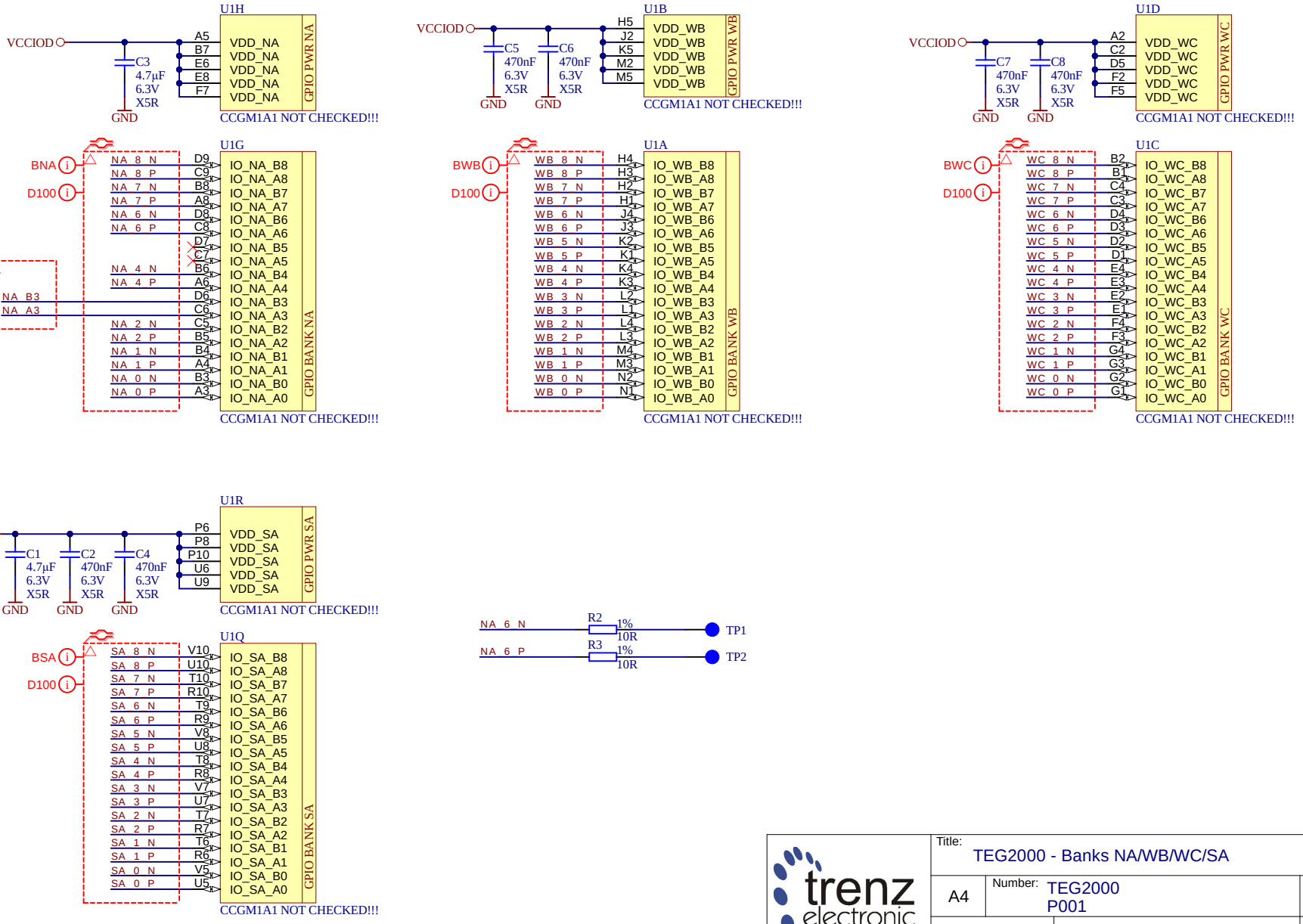
Title: TEG2000		
A4	Number: TEG2000 P001	Rev. 01
Date: 04-Sep-23	Copyright: Trenz Electronic GmbH	Page 3 of 10
Filename: TEG2000.SchDoc		


Bank_EA: 18 Single ended, 9 Differential pairs, Variable VCCIOA
Bank_EB: 18 Single ended, 9 Differential pairs, Variable VCCIOA
Bank_NB: 12 Single ended, 6 Differential pairs, Variable VCCIOA
Bank_SB: 6 MIO Pins, 1.8V Fixed VCCIO
Bank_SB: 8 MIO Pins, 3.3V Fixed VCCIO
SerDes: 1 Lane
JM1
LSHM-150-04.0-L-DV-A-S-K-TR
VIN 3.3-5.0V
VCCIOA 1.1-2.7V
3.3VIN
1.8V
PWR VBAT
GND
SER_TX0_N
SER_TX0_P
SER_RX0_N
SER_RX0_P
ETH VCC
CLK_B2B_P
CLK_B2B_N
SER_CLK0_P
SER_CLK0_N
EN1
PGOOD
MODE
0..3.3VIN
MODE:
0 -> JTAG
1 -> SPI Master
EA_0_N
EA_0_P
EA_1_N
EA_1_P
EA_3_N
EA_3_P
EA_5_N
EA_5_P
EA_6_N
EA_6_P
EA_8_N
EA_8_P
EB_1_N
EB_1_P
EB_3_N
EB_3_P
EB_6_N
EB_6_P
EB_7_N
EB_7_P
NB_8_N
NB_8_P
MIO14
NB_6_N
NB_6_P
NB_5_N
NB_5_P
MIO45
MIO44
MIO43
MIO42
MIO41
MIO40
EA_2_N
EA_2_P
EA_4_N
EA_4_P
EA_7_N
EA_7_P
EB_0_N
EB_0_P
EB_2_N
EB_2_P
EB_4_N
EB_4_P
EB_5_N
EB_5_P
EB_8_N
EB_8_P
NB_7_N
NB_7_P
NB_4_N
NB_4_P
NB_2_N
NB_2_P
MIO15
MIO0
MIO9
MIO11
MIO10
MIO13
MIO12
Group 1
Group 5
Group 6
Group 7
SerDes
Bank_SA: 18 Single ended, 9 Differential pairs, Variable VCCIOC
Bank_WB: 18 Single ended, 9 Differential pairs, Variable VCCIOD
Bank_WC: 18 Single ended, 9 Differential pairs, Variable VCCIOD
Bank_NA: 14 Single ended, 6 Differential pairs, Variable VCCIOD
JTAG: 4 Pins 3.3V
JM2
3.3-5.0V VIN
3.3V
0..3.3VIN
1.5V
VCCIOC 1.1-2.7V
VCCIOD 1.1-2.7V
3.3V VREF_JTAG
JTAG_B2B
TMS
TDI
TDO
TCK
JTAG
SA_8_N
SA_8_P
SA_7_N
SA_7_P
SA_6_N
SA_6_P
SA_4_N
SA_4_P
SA_2_N
SA_2_P
SA_1_N
SA_1_P
SA_5_N
SA_5_P
MR
SA_3_N
SA_3_P
SA_0_N
SA_0_P
WB_0_N
WB_0_P
WB_3_N
WB_3_P
WB_5_N
WB_5_P
WB_7_N
WB_7_P
WC_0_N
WC_0_P
WC_3_N
WC_3_P
WC_5_N
WC_5_P
WC_8_N
WC_8_P
NA_0_N
NA_0_P
NA_1_N
NA_1_P
NA_4_N
NA_4_P
NA_7_N
NA_7_P
NA_8_N
NA_8_P
NA_2_N
NA_2_P
NA_A3
WB_1_N
WB_1_P
WB_2_N
WB_2_P
WB_4_N
WB_4_P
WB_6_N
WB_6_P
WB_8_N
WB_8_P
WC_1_N
WC_1_P
WC_2_N
WC_2_P
WC_4_N
WC_4_P
WC_6_N
WC_6_P
WC_7_N
WC_7_P
NA_B3
Group 3
Group 4
VCCIOA 1.1..2.7V
VCCIOC 1.1..2.7V
VCCIOD 1.1..2.7V
Group 1 0..VCCIOA
Group 3 0..VCCIOC
Group 4 0..VCCIOD
Group 5 0..1.8V
Group 6 0..3.3V
Group 7 SerDes
Special
PWR_in
PWR_out
Some information about Trenz modules compatibility and differences here
trenz electronic
Title: TEG2000 - B2B Connectors
A4
Number: TEG2000 P001
Rev. 01
Date: 29-Aug-23
Copyright: Trenz Electronic GmbH
Page 4 of 10
Filename: B2B-Connectors.SchDoc


U1H
VCCIOD
C3
4.7µF
6.3V
X5R
GND
A5
B7
E6
E8
F7
VDD_NA
VDD_NA
VDD_NA
VDD_NA
VDD_NA
GPIO PWR NA
CCGM1A1 NOT CHECKED!!!
U1B
VCCIOD
C5
470nF
6.3V
X5R
C6
470nF
6.3V
X5R
GND
GND
H5
J2
K5
M2
M5
VDD_WB
VDD_WB
VDD_WB
VDD_WB
VDD_WB
GPIO PWR WB
CCGM1A1 NOT CHECKED!!!
U1D
VCCIOD
C7
470nF
6.3V
X5R
C8
470nF
6.3V
X5R
GND
GND
A2
C2
D5
F2
F5
VDD_WC
VDD_WC
VDD_WC
VDD_WC
VDD_WC
GPIO PWR WC
CCGM1A1 NOT CHECKED!!!
U1G
BNA
D100
BNA
NA_B3
NA_A3
NA_8_N
NA_8_P
NA_7_N
NA_7_P
NA_6_N
NA_6_P
NA_4_N
NA_4_P
NA_2_N
NA_2_P
NA_1_N
NA_1_P
NA_0_N
NA_0_P
D9
C9
B8
A8
D8
C8
D7
C7
B6
A6
D6
C6
C5
B5
B4
A4
B3
A3
IO_NA_B8
IO_NA_A8
IO_NA_B7
IO_NA_A7
IO_NA_B6
IO_NA_A6
IO_NA_B5
IO_NA_A5
IO_NA_B4
IO_NA_A4
IO_NA_B3
IO_NA_A3
IO_NA_B2
IO_NA_A2
IO_NA_B1
IO_NA_A1
IO_NA_B0
IO_NA_A0
GPIO BANK NA
CCGM1A1 NOT CHECKED!!!
U1A
BWB
D100
WB_8_N
WB_8_P
WB_7_N
WB_7_P
WB_6_N
WB_6_P
WB_5_N
WB_5_P
WB_4_N
WB_4_P
WB_3_N
WB_3_P
WB_2_N
WB_2_P
WB_1_N
WB_1_P
WB_0_N
WB_0_P
H4
H3
H2
H1
J4
J3
K2
K1
K4
K3
L2
L1
L4
L3
M4
M3
N2
N1
IO_WB_B8
IO_WB_A8
IO_WB_B7
IO_WB_A7
IO_WB_B6
IO_WB_A6
IO_WB_B5
IO_WB_A5
IO_WB_B4
IO_WB_A4
IO_WB_B3
IO_WB_A3
IO_WB_B2
IO_WB_A2
IO_WB_B1
IO_WB_A1
IO_WB_B0
IO_WB_A0
GPIO BANK WB
CCGM1A1 NOT CHECKED!!!
U1C
BWC
D100
WC_8_N
WC_8_P
WC_7_N
WC_7_P
WC_6_N
WC_6_P
WC_5_N
WC_5_P
WC_4_N
WC_4_P
WC_3_N
WC_3_P
WC_2_N
WC_2_P
WC_1_N
WC_1_P
WC_0_N
WC_0_P
B2
B1
C4
C3
D4
D3
D2
D1
E4
E3
E2
E1
F4
F3
G4
G3
G2
G1
IO_WC_B8
IO_WC_A8
IO_WC_B7
IO_WC_A7
IO_WC_B6
IO_WC_A6
IO_WC_B5
IO_WC_A5
IO_WC_B4
IO_WC_A4
IO_WC_B3
IO_WC_A3
IO_WC_B2
IO_WC_A2
IO_WC_B1
IO_WC_A1
IO_WC_B0
IO_WC_A0
GPIO BANK WC
CCGM1A1 NOT CHECKED!!!
U1R
VCCIOC
C1
4.7µF
6.3V
X5R
C2
470nF
6.3V
X5R
C4
470nF
6.3V
X5R
GND
GND
GND
P6
P8
P10
U6
U9
VDD_SA
VDD_SA
VDD_SA
VDD_SA
VDD_SA
GPIO PWR SA
CCGM1A1 NOT CHECKED!!!
U1Q
BSA
D100
SA_8_N
SA_8_P
SA_7_N
SA_7_P
SA_6_N
SA_6_P
SA_5_N
SA_5_P
SA_4_N
SA_4_P
SA_3_N
SA_3_P
SA_2_N
SA_2_P
SA_1_N
SA_1_P
SA_0_N
SA_0_P
V10
U10
T10
R10
T9
R9
V8
U8
T8
R8
V7
U7
T7
R7
T6
R6
V5
U5
IO_SA_B8
IO_SA_A8
IO_SA_B7
IO_SA_A7
IO_SA_B6
IO_SA_A6
IO_SA_B5
IO_SA_A5
IO_SA_B4
IO_SA_A4
IO_SA_B3
IO_SA_A3
IO_SA_B2
IO_SA_A2
IO_SA_B1
IO_SA_A1
IO_SA_B0
IO_SA_A0
GPIO BANK SA
CCGM1A1 NOT CHECKED!!!
NA_6_N
NA_6_P
R2
R3
1%
10R
1%
10R
TP1
TP2
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Title: TEG2000 - Banks NA/WB/WC/SA
A4
Number: TEG2000 P001
Rev. 01
Date: 16-Aug-23
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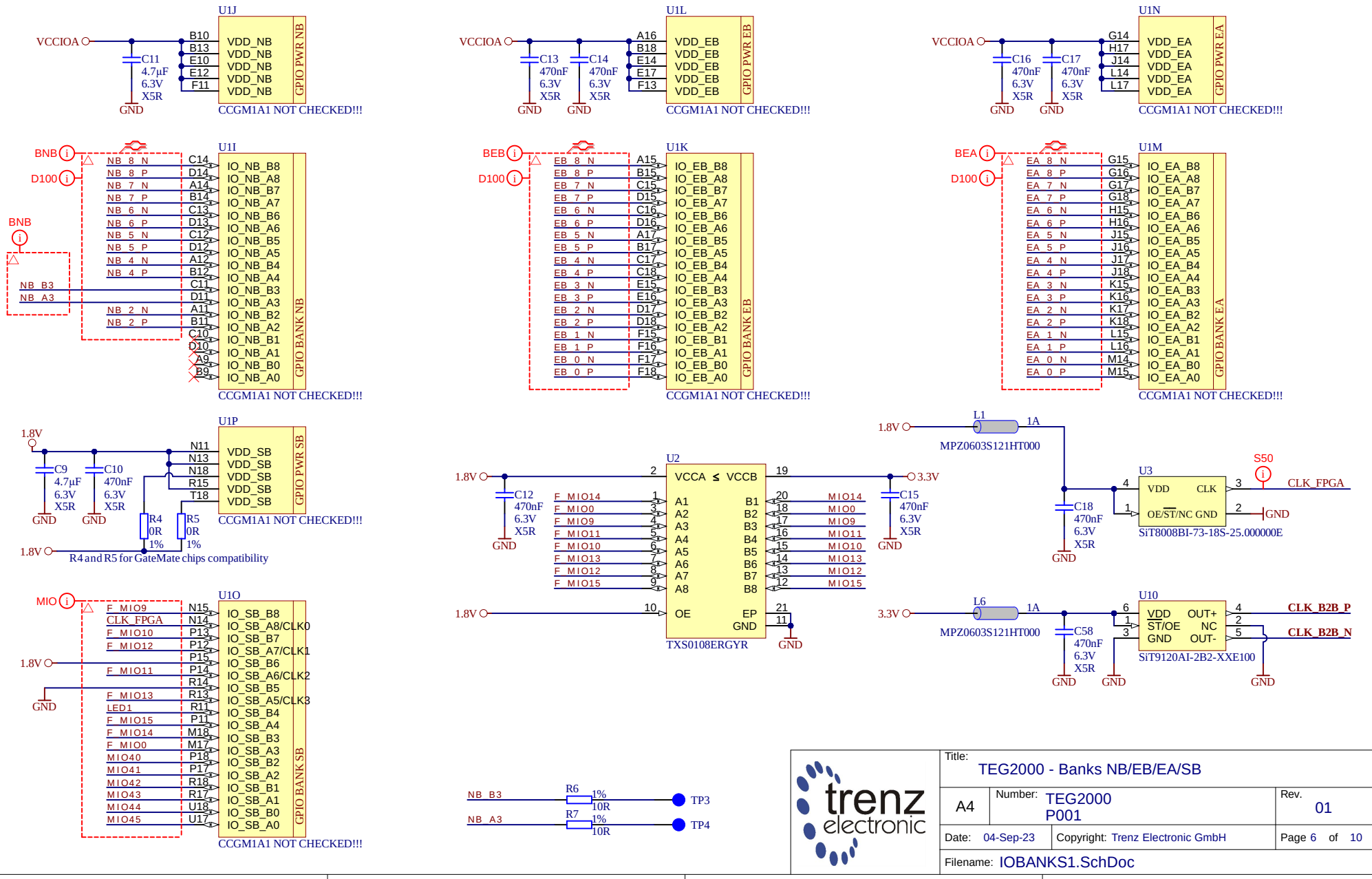
Page 5 of 10
Filename: IOBANKS0.SchDoc


U1J
VCCIOA
C11 4.7µF 6.3V X5R
GND
B10 B13 E10 E12 F11
VDD_NB
GPIO PWR NB
CCGM1A1 NOT CHECKED!!!
U1L
VCCIOA
C13 470nF 6.3V X5R
C14 470nF 6.3V X5R
A16 B18 E14 E17 F13
VDD_EB
GPIO PWR EB
CCGM1A1 NOT CHECKED!!!
U1N
VCCIOA
C16 470nF 6.3V X5R
C17 470nF 6.3V X5R
G14 H17 J14 L14 L17
VDD_EA
GPIO PWR EA
CCGM1A1 NOT CHECKED!!!
U1I
BNB
D100
NB_8_N NB_8_P NB_7_N NB_7_P NB_6_N NB_6_P NB_5_N NB_5_P NB_4_N NB_4_P NB_3 NB_A3 NB_2_N NB_2_P
C14 D14 A14 B14 C13 D13 C12 A12 B12 C11 D11 A11 B11 C10 D10 A9 B9
IO_NB_B8 IO_NB_A8 IO_NB_B7 IO_NB_A7 IO_NB_B6 IO_NB_A6 IO_NB_B5 IO_NB_A5 IO_NB_B4 IO_NB_A4 IO_NB_B3 IO_NB_A3 IO_NB_B2 IO_NB_A2 IO_NB_B1 IO_NB_A1 IO_NB_B0 IO_NB_A0
GPIO BANK NB
CCGM1A1 NOT CHECKED!!!
U1K
BEB
D100
EB_8_N EB_8_P EB_7_N EB_7_P EB_6_N EB_6_P EB_5_N EB_5_P EB_4_N EB_4_P EB_3_N EB_3_P EB_2_N EB_2_P EB_1_N EB_1_P EB_0_N EB_0_P
A15 B15 C15 D15 C16 D16 A17 B17 C17 C18 E15 E16 D17 D18 F15 F16 F17 F18
IO_EB_B8 IO_EB_A8 IO_EB_B7 IO_EB_A7 IO_EB_B6 IO_EB_A6 IO_EB_B5 IO_EB_A5 IO_EB_B4 IO_EB_A4 IO_EB_B3 IO_EB_A3 IO_EB_B2 IO_EB_A2 IO_EB_B1 IO_EB_A1 IO_EB_B0 IO_EB_A0
GPIO BANK EB
CCGM1A1 NOT CHECKED!!!
U1M
BEA
D100
EA_8_N EA_8_P EA_7_N EA_7_P EA_6_N EA_6_P EA_5_N EA_5_P EA_4_N EA_4_P EA_3_N EA_3_P EA_2_N EA_2_P EA_1_N EA_1_P EA_0_N EA_0_P
G15 G16 G17 G18 H15 H16 J15 J16 J17 J18 K15 K16 K17 K18 L15 L16 M14 M15
IO_EA_B8 IO_EA_A8 IO_EA_B7 IO_EA_A7 IO_EA_B6 IO_EA_A6 IO_EA_B5 IO_EA_A5 IO_EA_B4 IO_EA_A4 IO_EA_B3 IO_EA_A3 IO_EA_B2 IO_EA_A2 IO_EA_B1 IO_EA_A1 IO_EA_B0 IO_EA_A0
GPIO BANK EA
CCGM1A1 NOT CHECKED!!!
U1P
1.8V
C9 4.7µF 6.3V X5R
C10 470nF 6.3V X5R
GND
R4 0R 1%
R5 0R 1%
1.8V
R4 and R5 for GateMate chips compatibility
N11 N13 N18 R15 T18
VDD_SB
GPIO PWR SB
CCGM1A1 NOT CHECKED!!!
U2
1.8V
C12 470nF 6.3V X5R
GND
VCCA ≤ VCCB
A1 A2 A3 A4 A5 A6 A7 A8 OE
B1 B2 B3 B4 B5 B6 B7 B8 EP GND
F_MIO14 F_MIO0 F_MIO9 F_MIO11 F_MIO10 F_MIO13 F_MIO12 F_MIO15
MIO14 MIO0 MIO9 MIO11 MIO10 MIO13 MIO12 MIO15
1.8V
3.3V
C15 470nF 6.3V X5R
GND
TXS0108ERGYR
L1
1.8V
MPZ0603S121HT000
C18 470nF 6.3V X5R
GND
U3
VDD CLK OE/ST/NC GND
S50
CLK_FPGA
GND
SiT8008BI-73-18S-25.000000E
MIO
F_MIO9 CLK_FPGA F_MIO10 F_MIO12 F_MIO11 F_MIO13 LED1 F_MIO15 F_MIO14 F_MIO0 MIO40 MIO41 MIO42 MIO43 MIO44 MIO45
N15 N14 P13 P12 P15 P14 R14 R13 R11 P11 M18 M17 P18 P17 R18 R17 U18 U17
IO_SB_B8 IO_SB_A8/CLK0 IO_SB_B7 IO_SB_A7/CLK1 IO_SB_B6 IO_SB_A6/CLK2 IO_SB_B5 IO_SB_A5/CLK3 IO_SB_B4 IO_SB_A4 IO_SB_B3 IO_SB_A3 IO_SB_B2 IO_SB_A2 IO_SB_B1 IO_SB_A1 IO_SB_B0 IO_SB_A0
GPIO BANK SB
CCGM1A1 NOT CHECKED!!!
1.8V
GND
3.3V
L6
MPZ0603S121HT000
C58 470nF 6.3V X5R
GND
U10
VDD ST/OE GND OUT+ NC OUT-
CLK_B2B_P
CLK_B2B_N
SiT9120AI-2B2-XXE100
NB_B3
R6 1% 10R
TP3
NB_A3
R7 1% 10R
TP4
trenz electronic
Title: TEG2000 - Banks NB/EB/EA/SB
A4
Number: TEG2000 P001
Rev. 01
Date: 04-Sep-23
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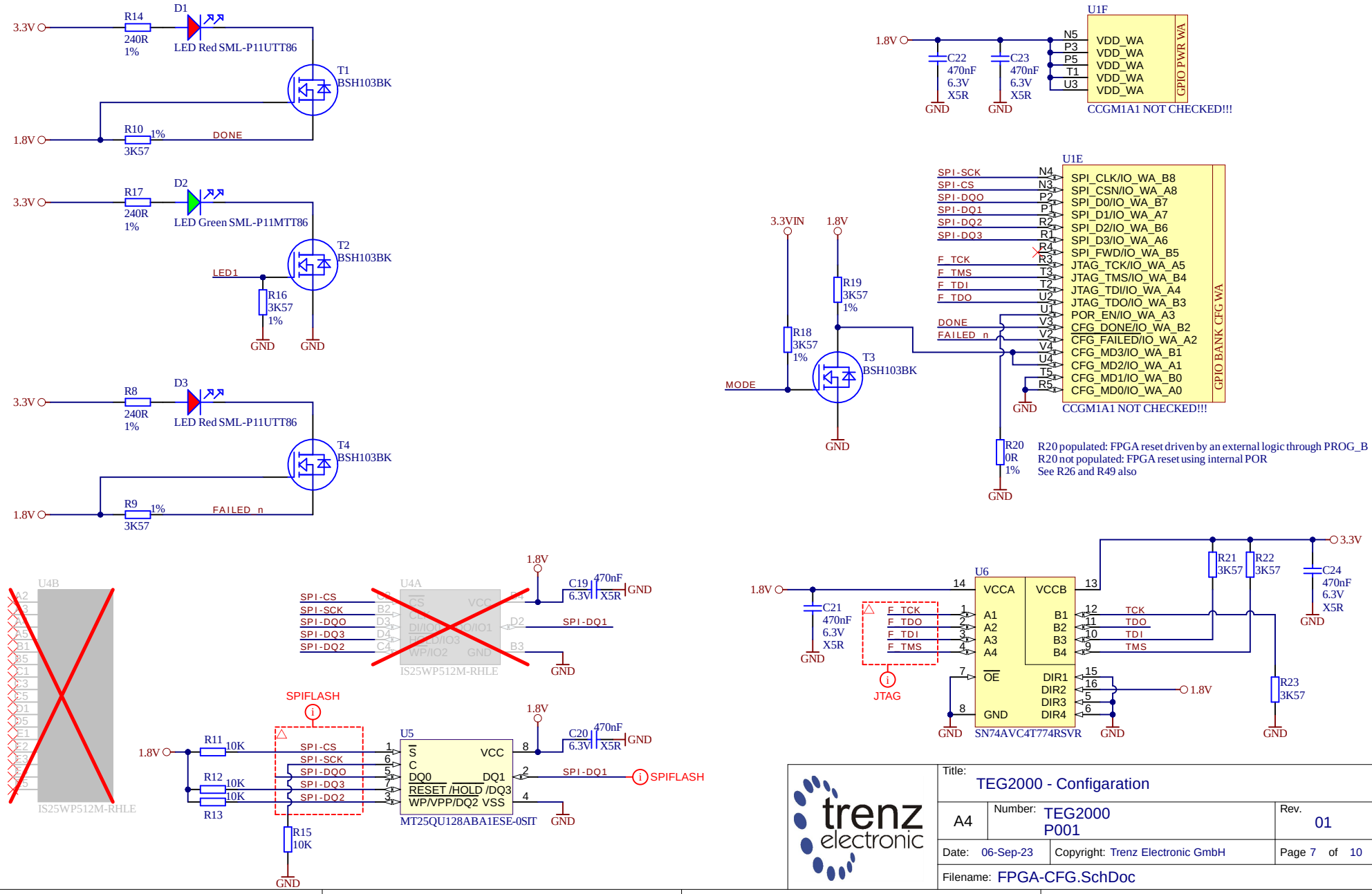
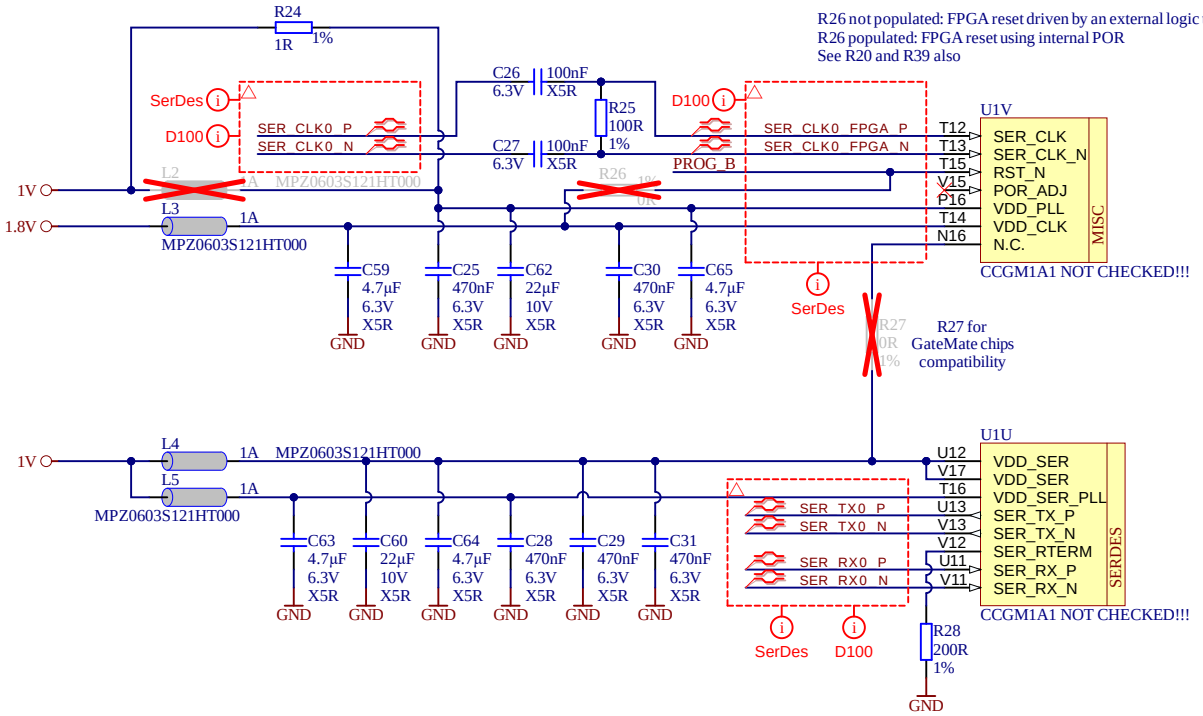
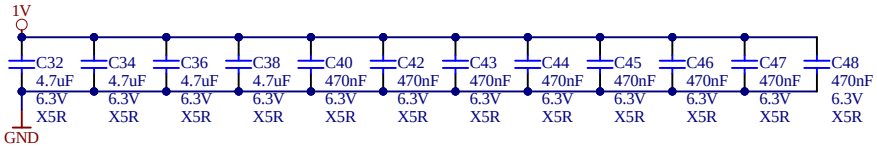
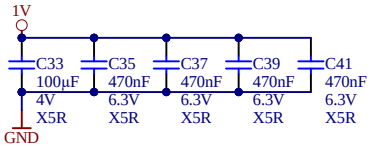
Page 6 of 10
Filename: IOBANKS1.SchDoc

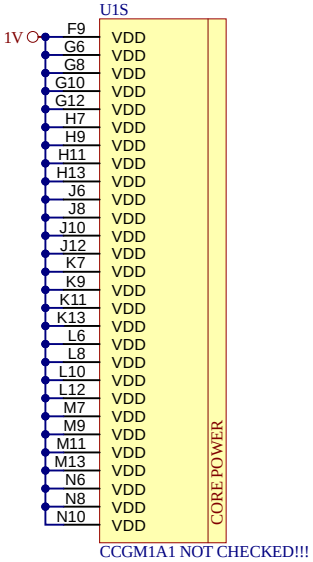

3.3V
R14
240R
1%
D1
LED Red SML-P11UTT86
T1
BSH103BK
1.8V
R10
1%
DONE
3K57
3.3V
R17
240R
1%
D2
LED Green SML-P11MTT86
T2
BSH103BK
LED1
R16
3K57
1%
GND
GND
3.3V
R8
240R
1%
D3
LED Red SML-P11UTT86
T4
BSH103BK
1.8V
R9
1%
FAILED_n
3K57
U1F
1.8V
C22
470nF
6.3V
X5R
C23
470nF
6.3V
X5R
GND
GND
N5
P3
P5
T1
U3
VDD_WA
VDD_WA
VDD_WA
VDD_WA
VDD_WA
GPIO PWR WA
CCGM1A1 NOT CHECKED!!!
U1E
3.3VIN
1.8V
R19
3K57
1%
R18
3K57
1%
MODE
T3
BSH103BK
GND
SPI-SCK
SPI-CS
SPI-DQO
SPI-DQ1
SPI-DQ2
SPI-DQ3
F_TCK
F_TMS
F_TDI
F_TDO
DONE
FAILED_n
N4
N3
P2
P1
R2
R1
R4
R3
T3
T2
U2
U1
V3
V2
V4
U4
T5
R5
SPI_CLK/IO_WA_B8
SPI_CSN/IO_WA_A8
SPI_D0/IO_WA_B7
SPI_D1/IO_WA_A7
SPI_D2/IO_WA_B6
SPI_D3/IO_WA_A6
SPI_FWD/IO_WA_B5
JTAG_TCK/IO_WA_A5
JTAG_TMS/IO_WA_B4
JTAG_TDI/IO_WA_A4
JTAG_TDO/IO_WA_B3
POR_EN/IO_WA_A3
CFG_DONE/IO_WA_B2
CFG_FAILED/IO_WA_A2
CFG_MD3/IO_WA_B1
CFG_MD2/IO_WA_A1
CFG_MD1/IO_WA_B0
CFG_MD0/IO_WA_A0
GPIO BANK CFG WA
GND
CCGM1A1 NOT CHECKED!!!
R20
0R
1%
GND
R20 populated: FPGA reset driven by an external logic through PROG_B
R20 not populated: FPGA reset using internal POR
See R26 and R49 also
U4B
IS25WP512M-RHLE
U4A
SPI-CS
SPI-SCK
SPI-DQO
SPI-DQ3
SPI-DQ2
B2
D3
D4
C4
VCC
D2
B3
GND
IS25WP512M-RHLE
1.8V
C19
470nF
6.3V
X5R
GND
SPI-DQ1
GND
SPIFLASH
1.8V
R11
10K
R12
10K
R13
10K
SPI-CS
SPI-SCK
SPI-DQO
SPI-DQ3
SPI-DQ2
U5
S
C
DQ0
RESET /HOLD /DQ3
WP/VPP/DQ2
DQ1
VSS
VCC
1
6
5
7
3
8
2
4
MT25QU128ABA1ESE-0SIT
1.8V
C20
470nF
6.3V
X5R
GND
SPI-DQ1
SPIFLASH
R15
10K
GND
U6
1.8V
C21
470nF
6.3V
X5R
GND
F_TCK
F_TDO
F_TDI
F_TMS
JTAG
14
1
2
3
4
7
8
VCCA
A1
A2
A3
A4
OE
GND
VCCB
B1
B2
B3
B4
DIR1
DIR2
DIR3
DIR4
13
12
11
10
9
15
16
5
6
TCK
TDO
TDI
TMS
1.8V
SN74AVC4T774RSVR
GND
GND
R21
3K57
R22
3K57
R23
3K57
3.3V
C24
470nF
6.3V
X5R
GND
GND
trenz
electronic
Title:
TEG2000 - Configaration
A4
Number:
TEG2000
P001
Rev.
01
Date:
06-Sep-23
Copyright:
Trenz Electronic GmbH
Page 7 of 10
Filename:
FPGA-CFG.SchDoc

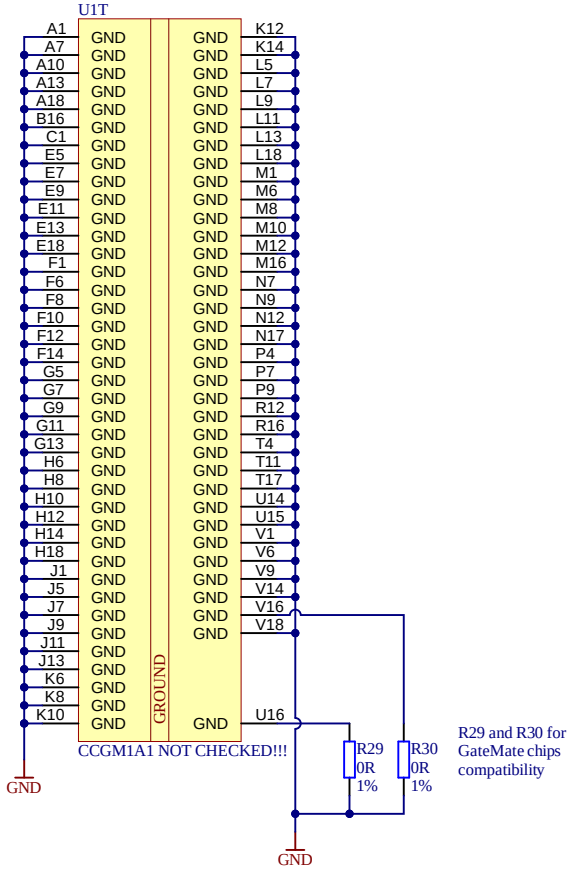


trenz electronic	Title: TEG2000 - MGT		
	A4	Number: TEG2000 P001	Rev. 01
	Date: 05-Sep-23	Copyright: Trenz Electronic GmbH	Page 8 of 10
	Filename: FPGA-MGT.SchDoc		

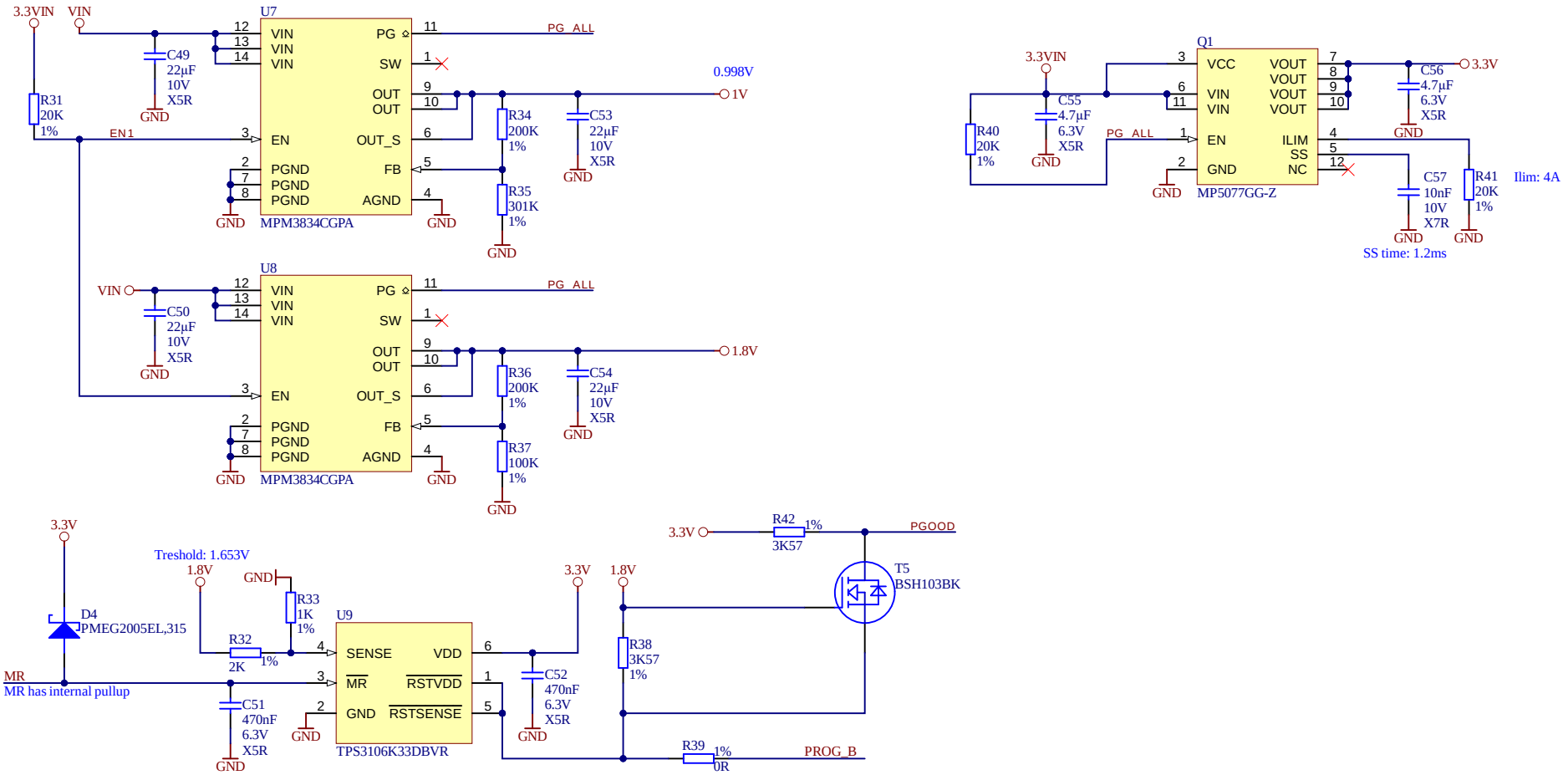








trenz electronic	Title: TEG2000 - FPGA PWR	
A4	Number: TEG2000 P001	Rev. 01
Date: 22-Aug-23	Copyright: Trenz Electronic GmbH	Page 9 of 10
Filename: FPGA-PWR.SchDoc		



R39 populated: FPGA reset driven by an external logic through PROG_B
R39 not populated: FPGA reset using internal POR
See R20 and R26 also

trenz electronic	Title: TEG2000 - POWER	
A4	Number: TEG2000 P001	Rev. 01
Date: 29-Aug-23	Copyright: Trenz Electronic GmbH	Page 10 of 10
Filename: PWR.SchDoc		