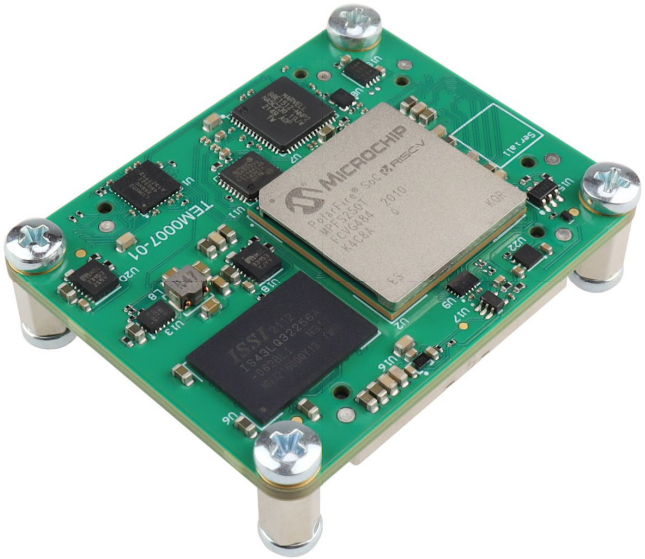
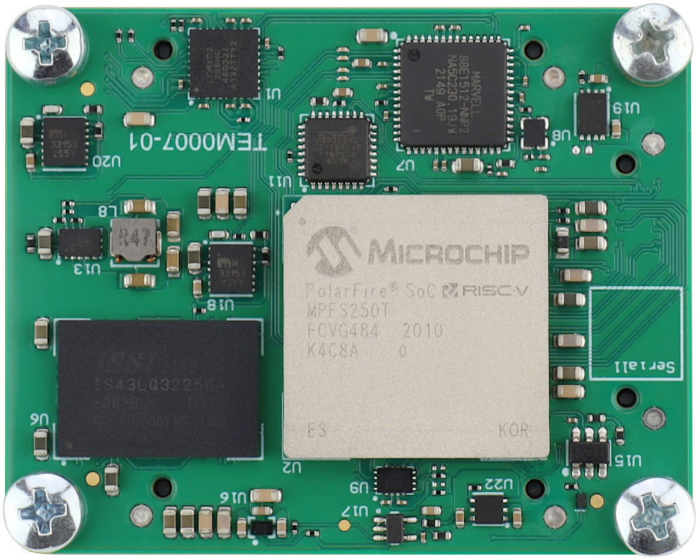
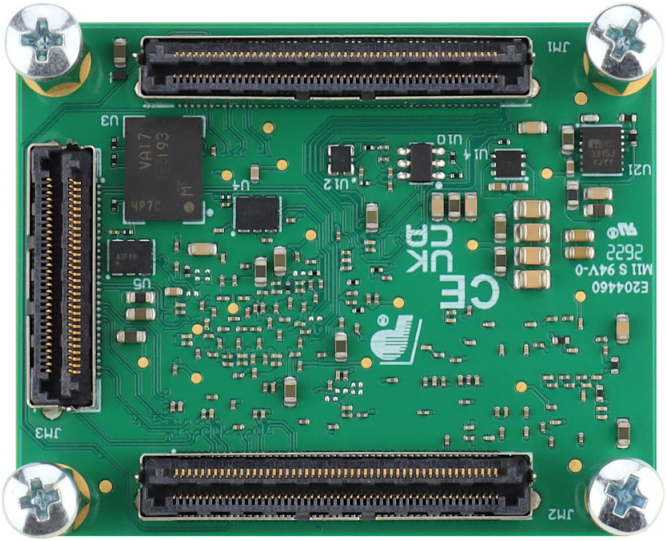






Regarding the usage of our schematics and alike documentation for Trenz module TEM0007.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TEM0007 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

| | | | |
|---|---|---|---|
| trenz electronic | Title: TEM0007 - Legal Notices | | |
| | A4 | Number: TEM0007 CAA11-A | Rev. 01 |
| | Date: 2021-08-01 | Copyright: Trenz Electronic GmbH | Page 1 of 17 |
| | Filename: Legal Notices Modules.SchDoc | | |

B2B_Connector
B2B_Connector.SchDoc

CPLD
CPLD.SchDoc

FPGA1
FPGA1.SchDoc

FPGA2
FPGA2.SchDoc

FPGA3
FPGA3.SchDoc

FPGA4
FPGA4.SchDoc

FPGA5
FPGA5.SchDoc

FPGA6
FPGA6.SchDoc

FPGA_PWR
FPGA_PWR.SchDoc

LPDDR4
LPDDR4.SchDoc

ETH-PHY
ETH-PHY.SchDoc

USB-PHY
USB-PHY.SchDoc

POWER1
POWER1.SchDoc

POWER2
POWER2.SchDoc

UKCA1

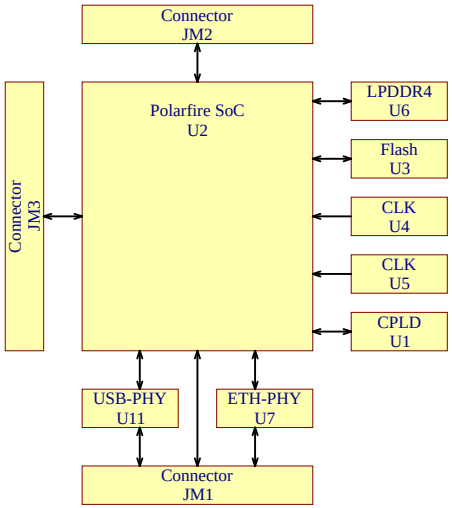
UKCA Logo on Top Overlay

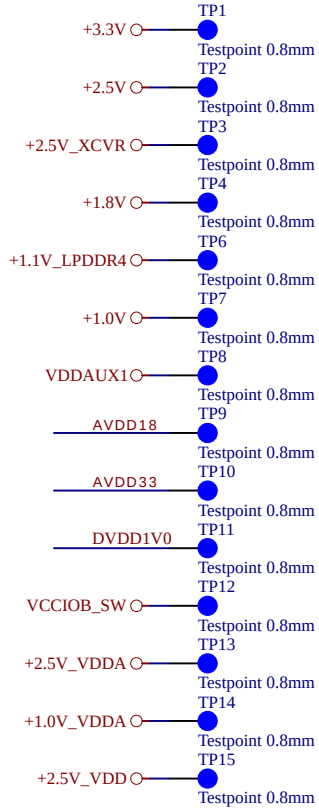
UKCA-TOPOVERLAY

CE1

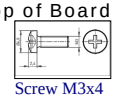
CE Logo on Top Overlay

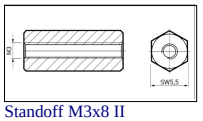
CE-TOPOVERLAY

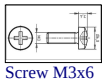


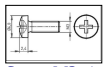




Top of Board


Screw M3x4


Standoff M3x8 II


Screw M3x6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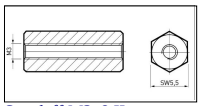
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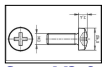
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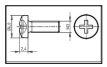
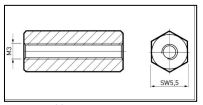

Screw M3x4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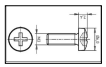
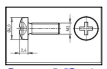

Screw M3x6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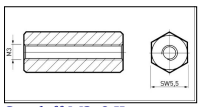
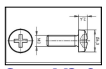
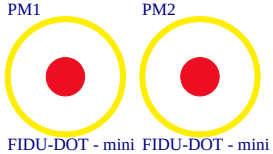
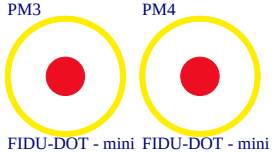

Standoff M3x8 II


Screw M3x6

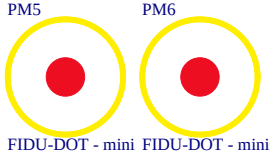
PM1 PM2


FIDU-DOT - mini FIDU-DOT - mini

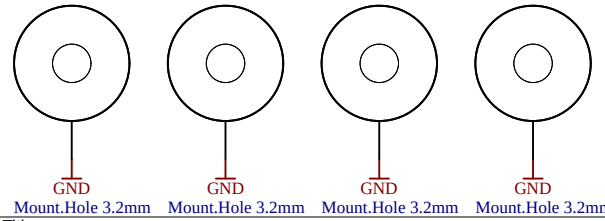
PM3 PM4


FIDU-DOT - mini FIDU-DOT - mini

PM5 PM6


FIDU-DOT - mini FIDU-DOT - mini

Serial1
Serial
Serialnumber 6,3 x 6.3mm




| | | | |
|---|---|---|---|
| | Title: TEM0007 | | |
| A4 | Number: TEM0007 CAA11-A | | Rev. 01 |
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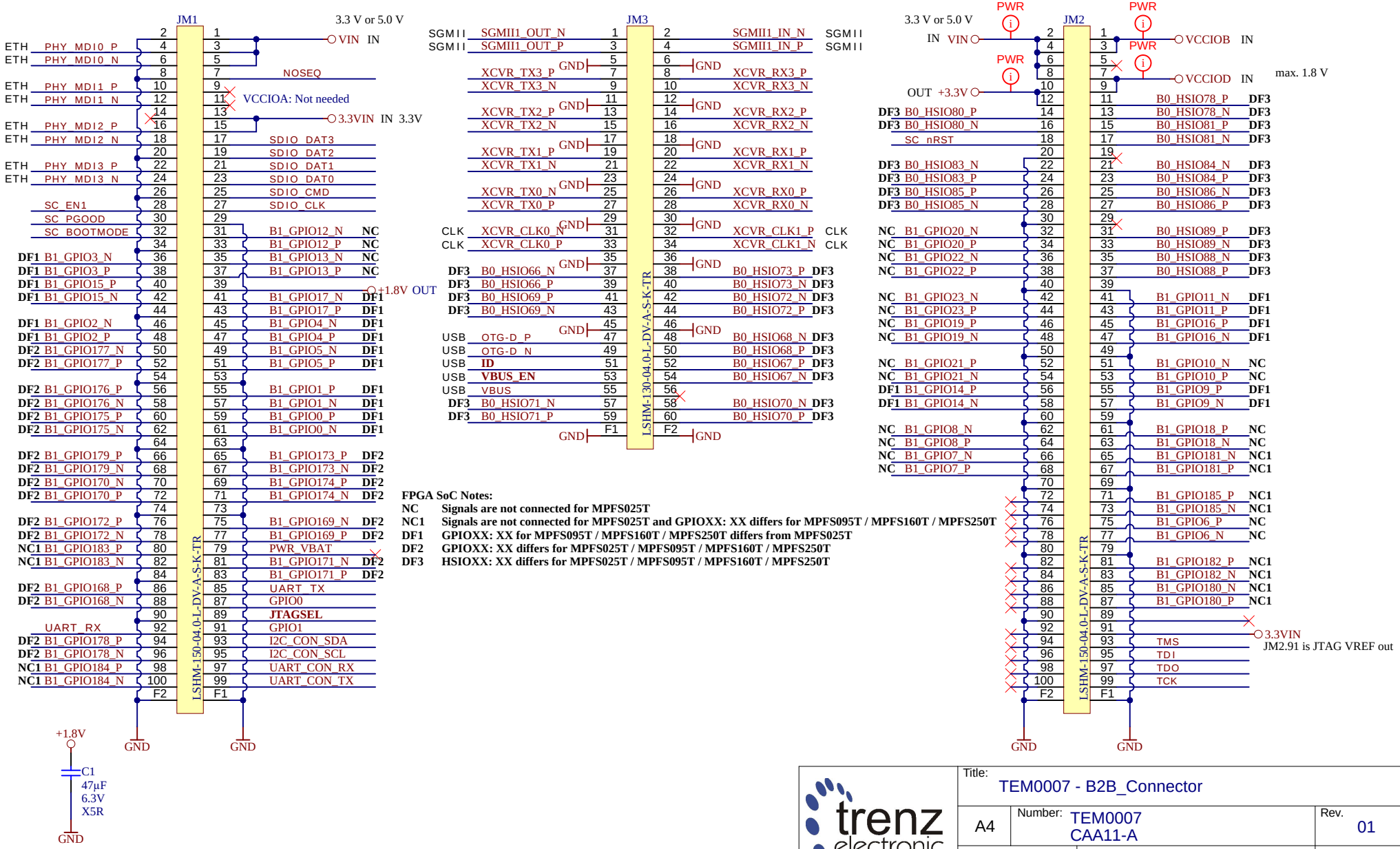
| Filename: TEM0007.SchDoc | | | |

**SD ETH**
B1: 48 IO, 24 Differential Pairs, VCCIOB Fixed VCCIO
B4: 8 GPIO, 3.3 V Fixed VCCIO

**USB MGT SGMII**
B1: 16 IO, 8 Differential Pairs, VCCIOD Fixed VCCIO

**JTAG: 3.3V Levels**
B1: 36 IO, 18 Differential Pairs, VCCIOB Fixed VCCIO
B0: 18 IO, 9 Differential Pairs, VCCIOD Fixed VCCIO




**FPGA SoC Notes:**

| | |
|---|---|
| **NC** | **Signals are not connected for MPFS025T** |
| **NC1** | **Signals are not connected for MPFS025T and GPIOXX: XX differs for MPFS095T / MPFS160T / MPFS250T** |
| **DF1** | **GPIOXX: XX for MPFS095T / MPFS160T / MPFS250T differs from MPFS025T** |
| **DF2** | **GPIOXX: XX differs for MPFS025T / MPFS095T / MPFS160T / MPFS250T** |
| **DF3** | **HSIOXX: XX differs for MPFS025T / MPFS095T / MPFS160T / MPFS250T** |

**Attention: Consider the I/O Glitch issues in document DS60001681A!**

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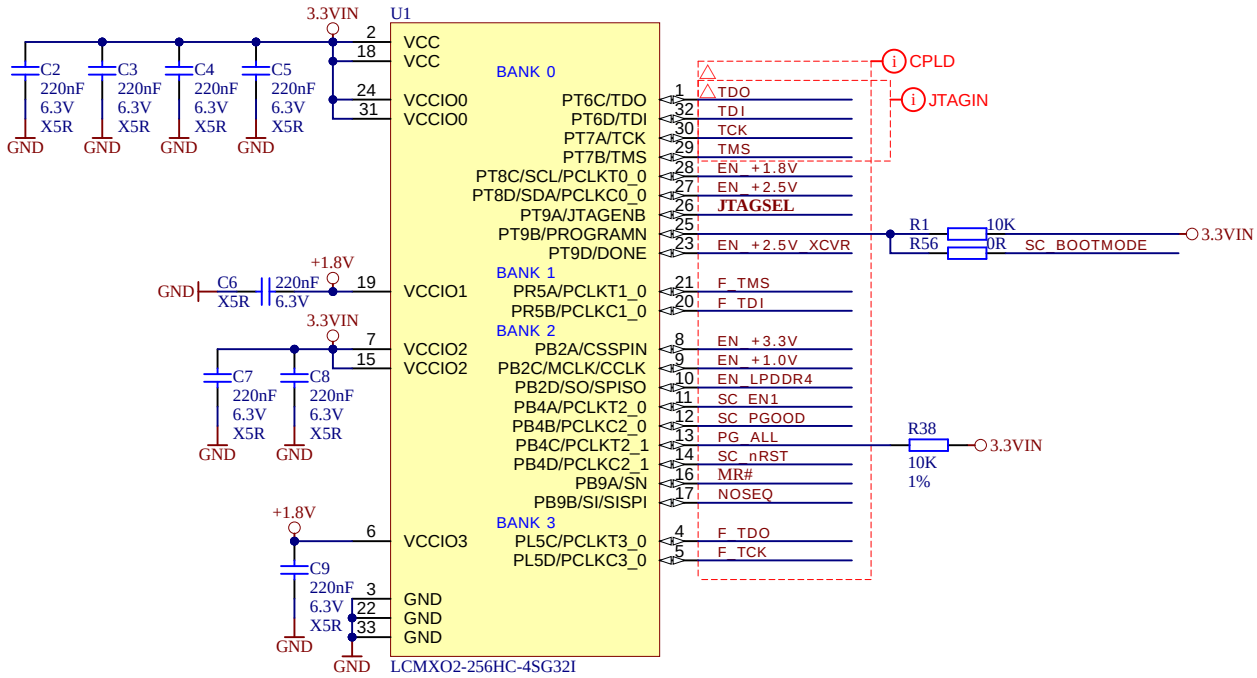
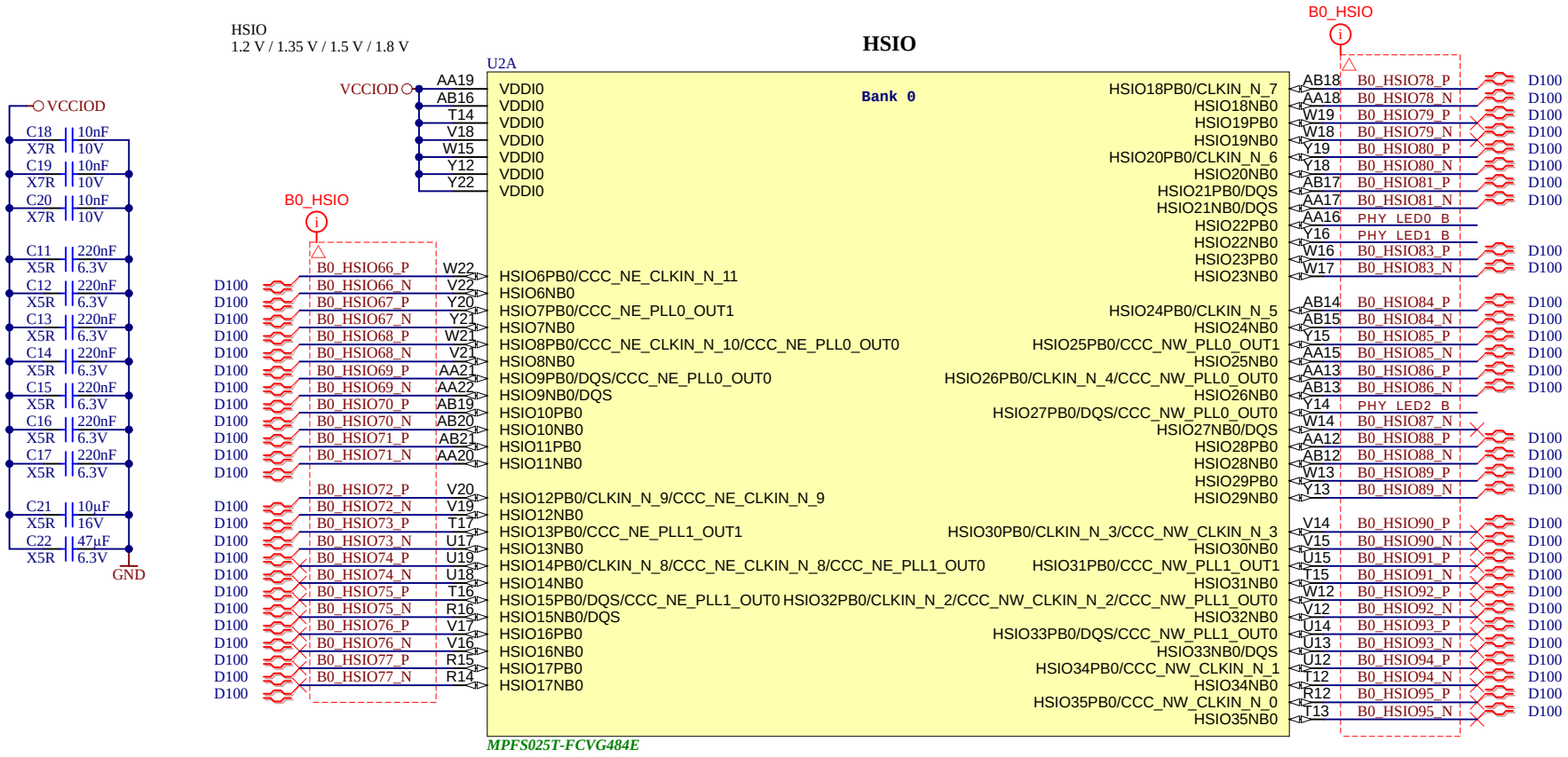
| | | |
|---|---|---|
| Title: TEM0007 - B2B_Connector | | |
| A4 | Number: TEM0007 CAA11-A | Rev. 01 |
| Date: 02.02.2023 | Copyright: Trenz Electronic GmbH | Page 3 of 17 |
| Filename: B2B_Connector.SchDoc | | |




| | | | |
|---|---|---|---|
| trenz electronic | Title: TEM0007 - CPLD | | |
| A4 | Number: TEM0007 CAA11-A | | Rev. 01 |
| Date: 21.06.2022 | Copyright: Trenz Electronic GmbH | | Page 4 of 17 |
| Filename: CPLD.SchDoc | | | |

**Attention:**
**1.) Consider the I/O Glitch issues in document DS60001681A!**
**2.) Using LVDS in HSIO bank needs an externally 100 Ohm resistor according to DS60001681A!**




**HSIOXX: XX differs for MPFS250T / MPFS095T / MPFS160T / MPFS025T**

| | | | |
|---|---|---|---|
| trenz electronic | Title: TEM0007 - FPGA1 | | |
| | A4 | Number: TEM0007 CAA11-A | Rev. 01 |
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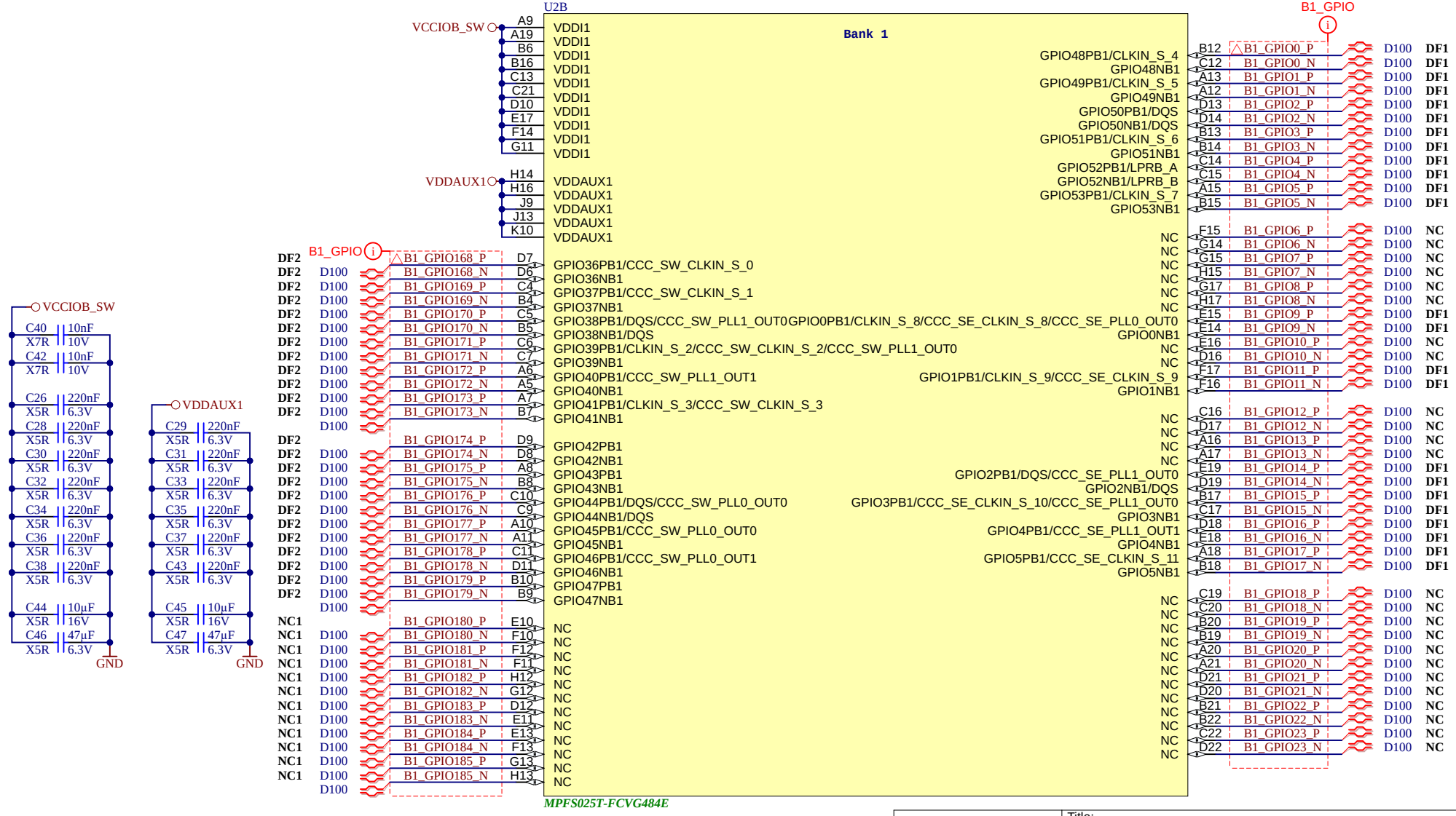
| | Filename: FPGA1.SchDoc | | |

**Attention: Consider the I/O Glitch issues in document DS60001681A!**

GPIO
1.2 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V

# GPIO

U2B




**FPGA SoC Notes:**

| | |
|---|---|
| **NC** | **Signals are not connected for MPFS025T** |
| **NC1** | **Signals are not connected for MPFS025T and GPIOXX: XX differs for MPFS095T / MPFS160T / MPFS250T** |
| **DF1** | **GPIOXX: XX for MPFS095T / MPFS160T / MPFS250T differs from MPFS025T** |
| **DF2** | **GPIOXX: XX differs for MPFS025T / MPFS095T / MPFS160T / MPFS250T** |

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| | | |
|---|---|---|
| Title: TEM0007 - FPGA2 | | |
| A4 | Number: TEM0007 CAA11-A | Rev. 01 |
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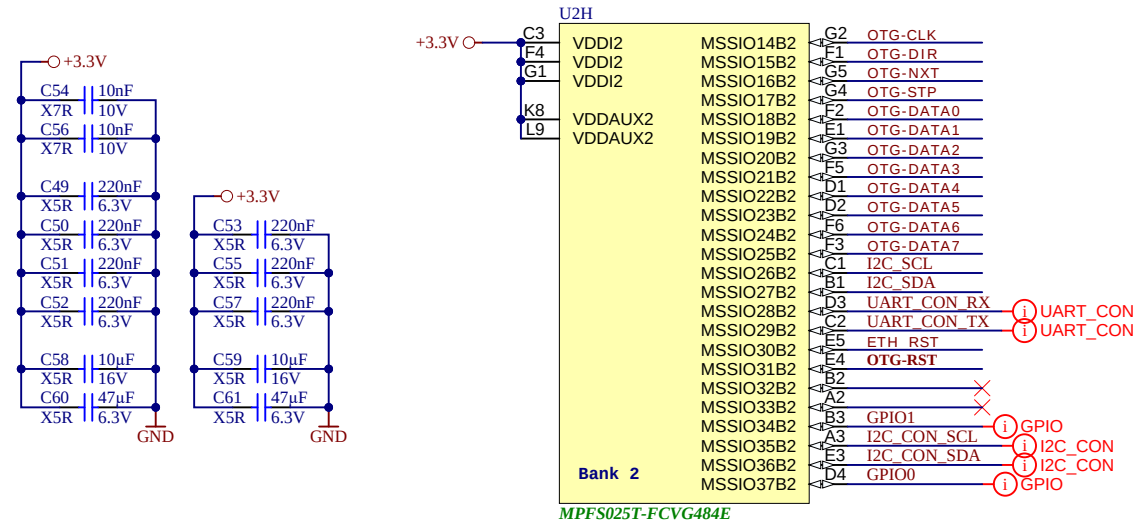
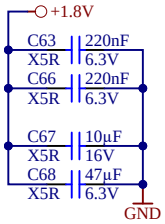
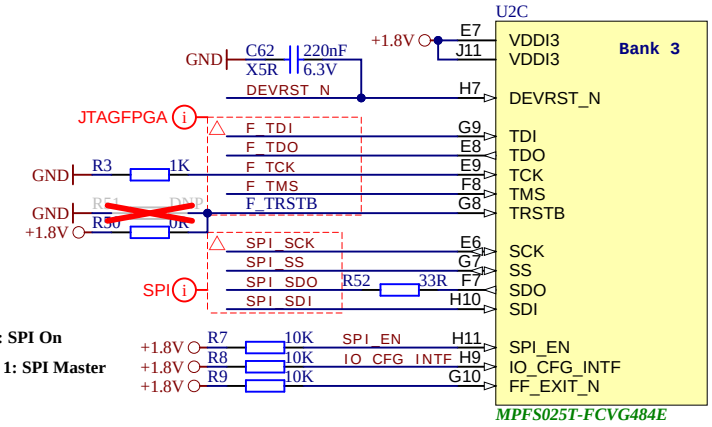
| Filename: FPGA2.SchDoc | | |

**Attention: Consider the I/O Glitch issues in document DS60001681A!**

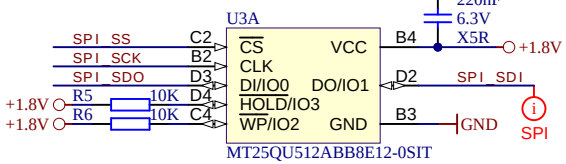


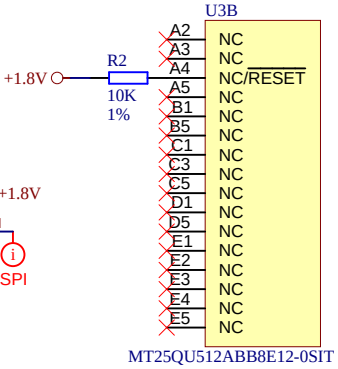




**0: SPI Off 1: SPI On**

**0: SPI Slave 1: SPI Master**




| | | | |
|---|---|---|---|
| trenz electronic | Title: TEM0007 - FPGA3 | | |
| A4 | Number: TEM0007 CAA11-A | | Rev. 01 |
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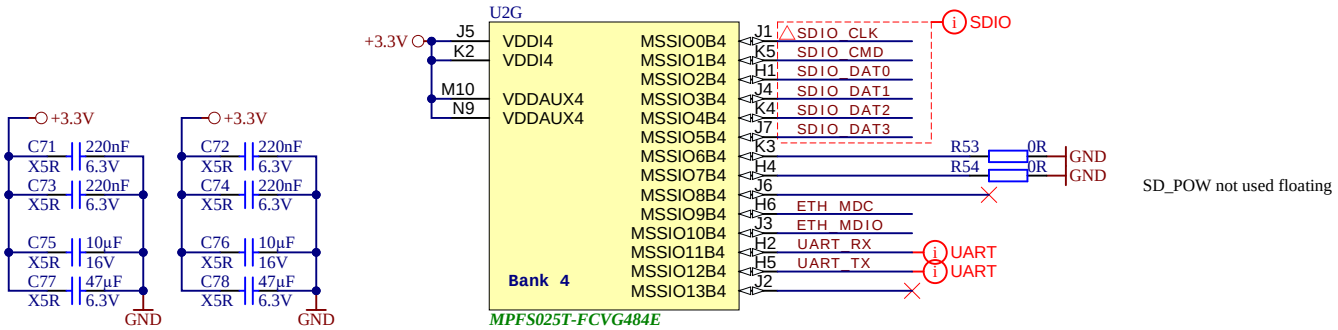
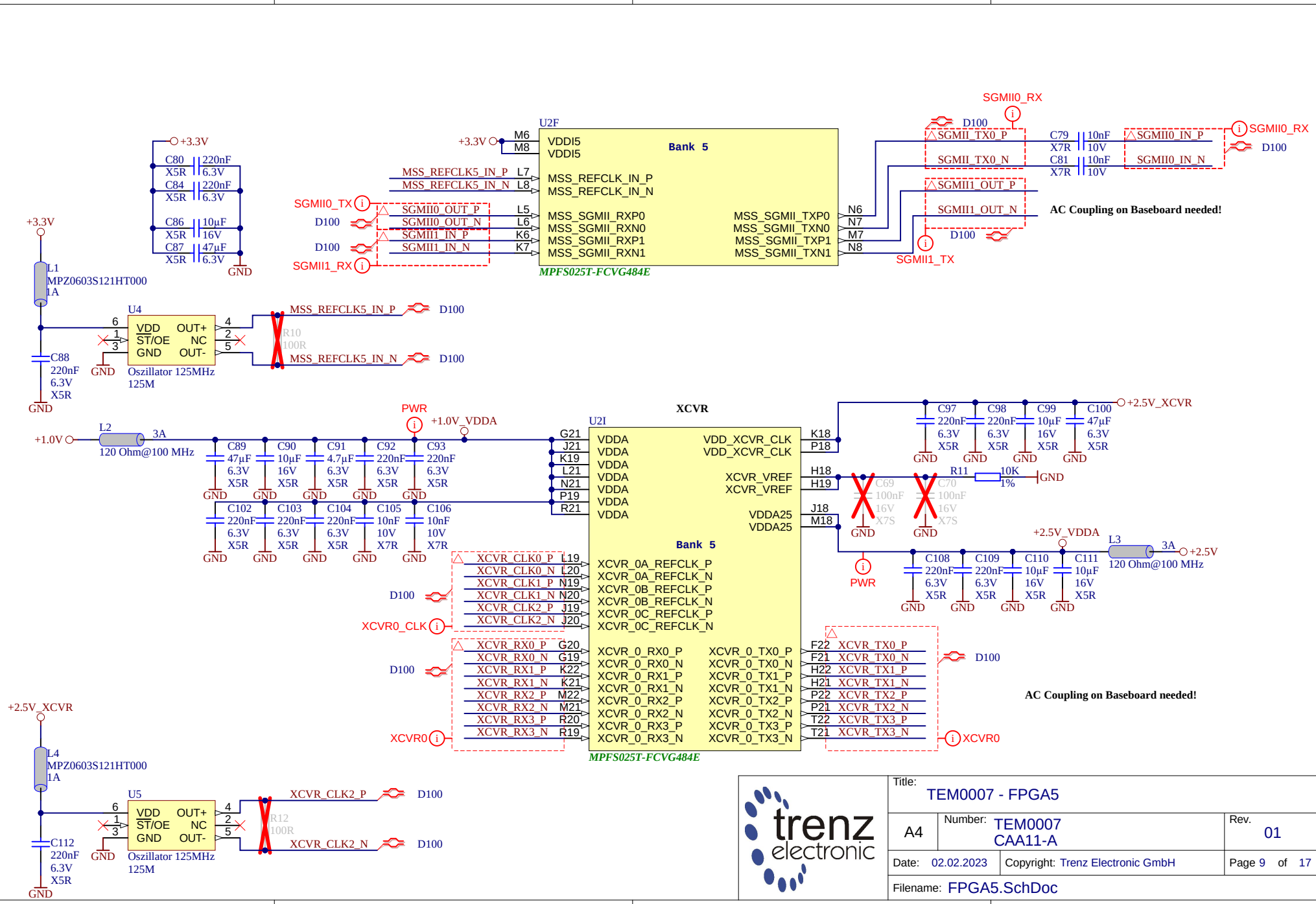
| Filename: FPGA3.SchDoc | | | |

**Attention: Consider the I/O Glitch issues in document DS60001681A!**




SD_POW not used floating

| | | | |
|---|---|---|---|
| trenz electronic | Title: TEM0007 - FPGA4 | | |
| | A4 | Number: TEM0007 CAA11-A | Rev. 01 |
| | Date: 02.02.2023 | Copyright: Trenz Electronic GmbH | Page 8 of 17 |
| | Filename: FPGA4.SchDoc | | |


U2F
Bank 5
MPFS025T-FCVG484E
SGMII0_RX
SGMII0_TX
SGMII1_RX
SGMII1_TX
AC Coupling on Baseboard needed!
U4
Oszillator 125MHz
125M
L1
MPZ0603S121HT000
1A
L2
120 Ohm@100 MHz
3A
XCVR
U2I
Bank 5
MPFS025T-FCVG484E
XCVR0_CLK
XCVR0
AC Coupling on Baseboard needed!
L3
120 Ohm@100 MHz
L4
MPZ0603S121HT000
1A
U5
Oszillator 125MHz
125M
Title: TEM0007 - FPGA5
A4
Number: TEM0007 CAA11-A
Rev. 01
Date: 02.02.2023
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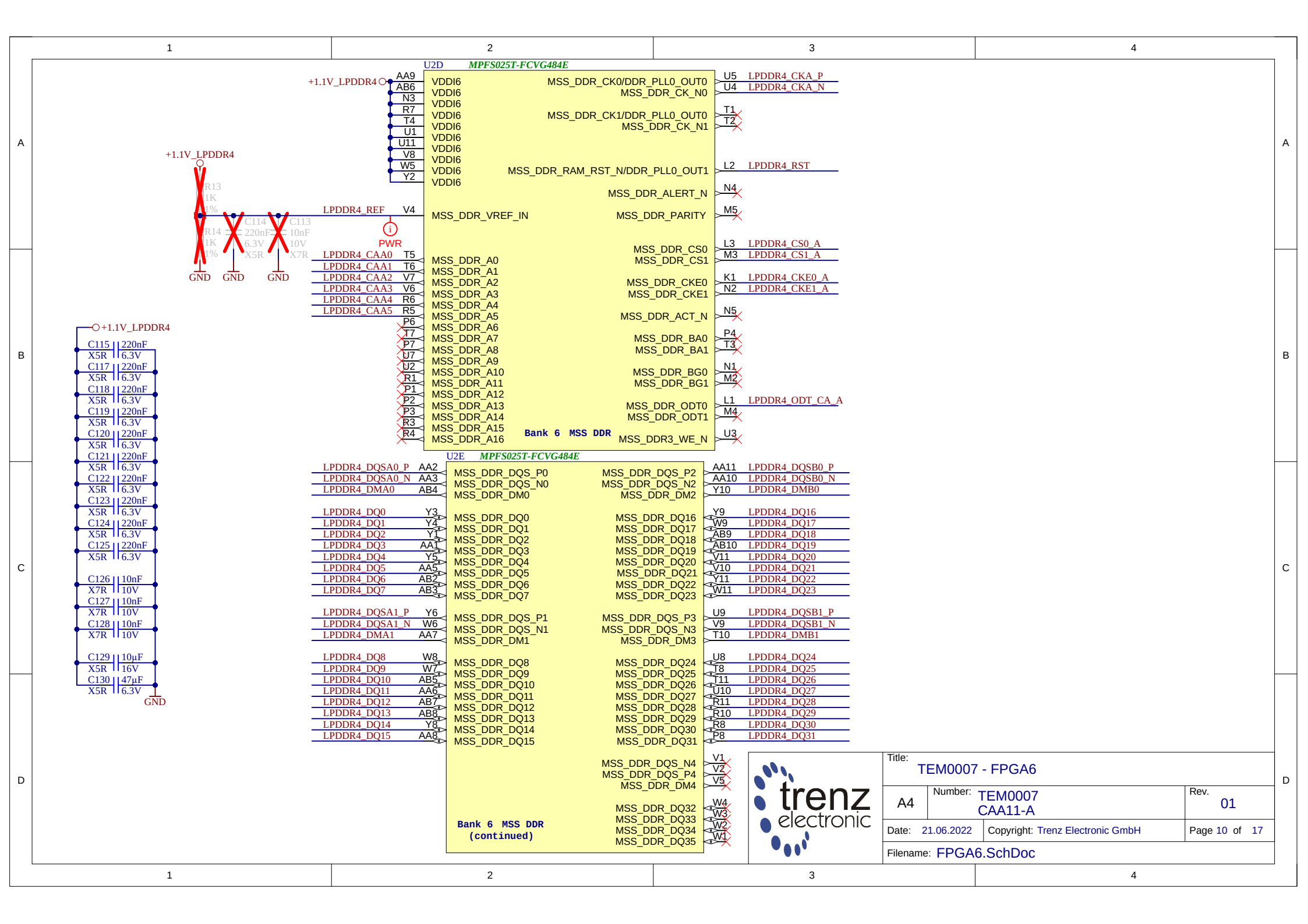
Page 9 of 17
Filename: FPGA5.SchDoc


U2D
MPFS025T-FCVG484E
+1.1V_LPDDR4
VDDI6
MSS_DDR_CK0/DDR_PLL0_OUT0
MSS_DDR_CK_N0
MSS_DDR_CK1/DDR_PLL0_OUT0
MSS_DDR_CK_N1
MSS_DDR_RAM_RST_N/DDR_PLL0_OUT1
MSS_DDR_ALERT_N
MSS_DDR_PARITY
MSS_DDR_VREF_IN
LPDDR4_REF
PWR
LPDDR4_CKA_P
LPDDR4_CKA_N
LPDDR4_RST
LPDDR4_CS0_A
LPDDR4_CS1_A
LPDDR4_CKE0_A
LPDDR4_CKE1_A
LPDDR4_ODT_CA_A
MSS_DDR_CS0
MSS_DDR_CS1
MSS_DDR_CKE0
MSS_DDR_CKE1
MSS_DDR_ACT_N
MSS_DDR_BA0
MSS_DDR_BA1
MSS_DDR_BG0
MSS_DDR_BG1
MSS_DDR_ODT0
MSS_DDR_ODT1
MSS_DDR3_WE_N
MSS_DDR_A0
MSS_DDR_A1
MSS_DDR_A2
MSS_DDR_A3
MSS_DDR_A4
MSS_DDR_A5
MSS_DDR_A6
MSS_DDR_A7
MSS_DDR_A8
MSS_DDR_A9
MSS_DDR_A10
MSS_DDR_A11
MSS_DDR_A12
MSS_DDR_A13
MSS_DDR_A14
MSS_DDR_A15
MSS_DDR_A16
Bank 6 MSS DDR
R13 1K 1%
R14 1K 1%
C114 220nF 6.3V X5R
C113 10nF 10V X7R
GND
U2E
MPFS025T-FCVG484E
MSS_DDR_DQS_P0
MSS_DDR_DQS_N0
MSS_DDR_DM0
MSS_DDR_DQS_P2
MSS_DDR_DQS_N2
MSS_DDR_DM2
MSS_DDR_DQ0
MSS_DDR_DQ1
MSS_DDR_DQ2
MSS_DDR_DQ3
MSS_DDR_DQ4
MSS_DDR_DQ5
MSS_DDR_DQ6
MSS_DDR_DQ7
MSS_DDR_DQ16
MSS_DDR_DQ17
MSS_DDR_DQ18
MSS_DDR_DQ19
MSS_DDR_DQ20
MSS_DDR_DQ21
MSS_DDR_DQ22
MSS_DDR_DQ23
MSS_DDR_DQS_P1
MSS_DDR_DQS_N1
MSS_DDR_DM1
MSS_DDR_DQS_P3
MSS_DDR_DQS_N3
MSS_DDR_DM3
MSS_DDR_DQ8
MSS_DDR_DQ9
MSS_DDR_DQ10
MSS_DDR_DQ11
MSS_DDR_DQ12
MSS_DDR_DQ13
MSS_DDR_DQ14
MSS_DDR_DQ15
MSS_DDR_DQ24
MSS_DDR_DQ25
MSS_DDR_DQ26
MSS_DDR_DQ27
MSS_DDR_DQ28
MSS_DDR_DQ29
MSS_DDR_DQ30
MSS_DDR_DQ31
MSS_DDR_DQS_N4
MSS_DDR_DQS_P4
MSS_DDR_DM4
MSS_DDR_DQ32
MSS_DDR_DQ33
MSS_DDR_DQ34
MSS_DDR_DQ35
Bank 6 MSS DDR (continued)
LPDDR4_DQSA0_P
LPDDR4_DQSA0_N
LPDDR4_DMA0
LPDDR4_DQSB0_P
LPDDR4_DQSB0_N
LPDDR4_DMB0
LPDDR4_DQ0
LPDDR4_DQ1
LPDDR4_DQ2
LPDDR4_DQ3
LPDDR4_DQ4
LPDDR4_DQ5
LPDDR4_DQ6
LPDDR4_DQ7
LPDDR4_DQ16
LPDDR4_DQ17
LPDDR4_DQ18
LPDDR4_DQ19
LPDDR4_DQ20
LPDDR4_DQ21
LPDDR4_DQ22
LPDDR4_DQ23
LPDDR4_DQSA1_P
LPDDR4_DQSA1_N
LPDDR4_DMA1
LPDDR4_DQSB1_P
LPDDR4_DQSB1_N
LPDDR4_DMB1
LPDDR4_DQ8
LPDDR4_DQ9
LPDDR4_DQ10
LPDDR4_DQ11
LPDDR4_DQ12
LPDDR4_DQ13
LPDDR4_DQ14
LPDDR4_DQ15
LPDDR4_DQ24
LPDDR4_DQ25
LPDDR4_DQ26
LPDDR4_DQ27
LPDDR4_DQ28
LPDDR4_DQ29
LPDDR4_DQ30
LPDDR4_DQ31
C115 220nF X5R 6.3V
C117 220nF X5R 6.3V
C118 220nF X5R 6.3V
C119 220nF X5R 6.3V
C120 220nF X5R 6.3V
C121 220nF X5R 6.3V
C122 220nF X5R 6.3V
C123 220nF X5R 6.3V
C124 220nF X5R 6.3V
C125 220nF X5R 6.3V
C126 10nF X7R 10V
C127 10nF X7R 10V
C128 10nF X7R 10V
C129 10µF X5R 16V
C130 47µF X5R 6.3V
Title: TEM0007 - FPGA6
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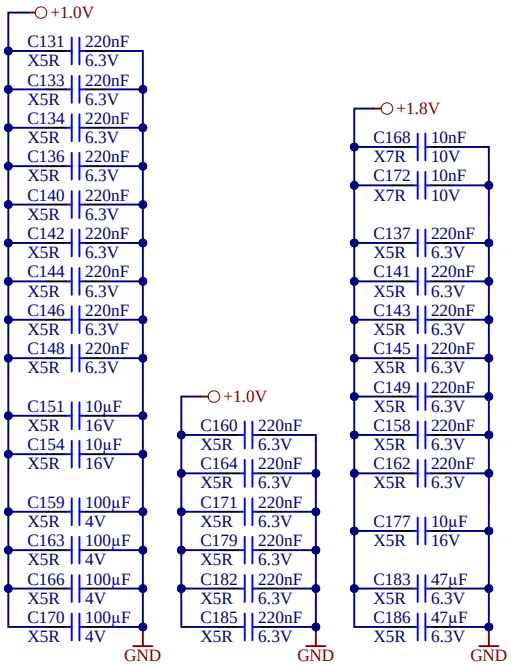
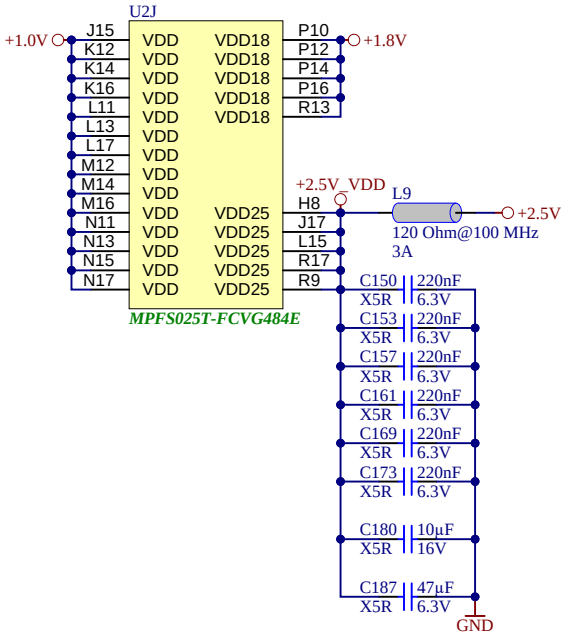
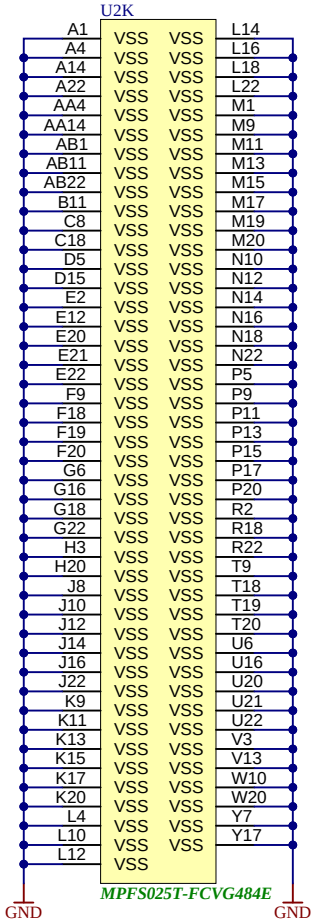
Filename: FPGA6.SchDoc




Both VDDA and VDD_XCVR_CLK supplies must be powered when any of the transceivers are used. VDD_XCVR_CLK must power on within the I/O calibration time (as specified for the device in Libero). VDDA and VDD_XCVR_CLK must both then remain powered during operation. If VDDA needs to be powered down, VDD_XCVR_CLK must also be powered down. There is no required sequence for powering up or down VDDA and VDD_XCVR_CLK.

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other I/O supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the I/O supplies of some I/O banks remain powered off).

VDD - For fabric core and transceiver/PCIe blocks.
VDD18 - For fabric programming and RC oscillators.
VDD25 - For corner phase-locked loop (PLLs) and on-chip non-volatile memory (sNVM).
VDDIx - For I/O banks.
VDDAUXx - For GPIO and HSIO banks.
VDDA - For transceiver.
VDDA25 - For transceiver PLLs.
VDD_XCVR_CLK - For transceiver reference clock input buffers.

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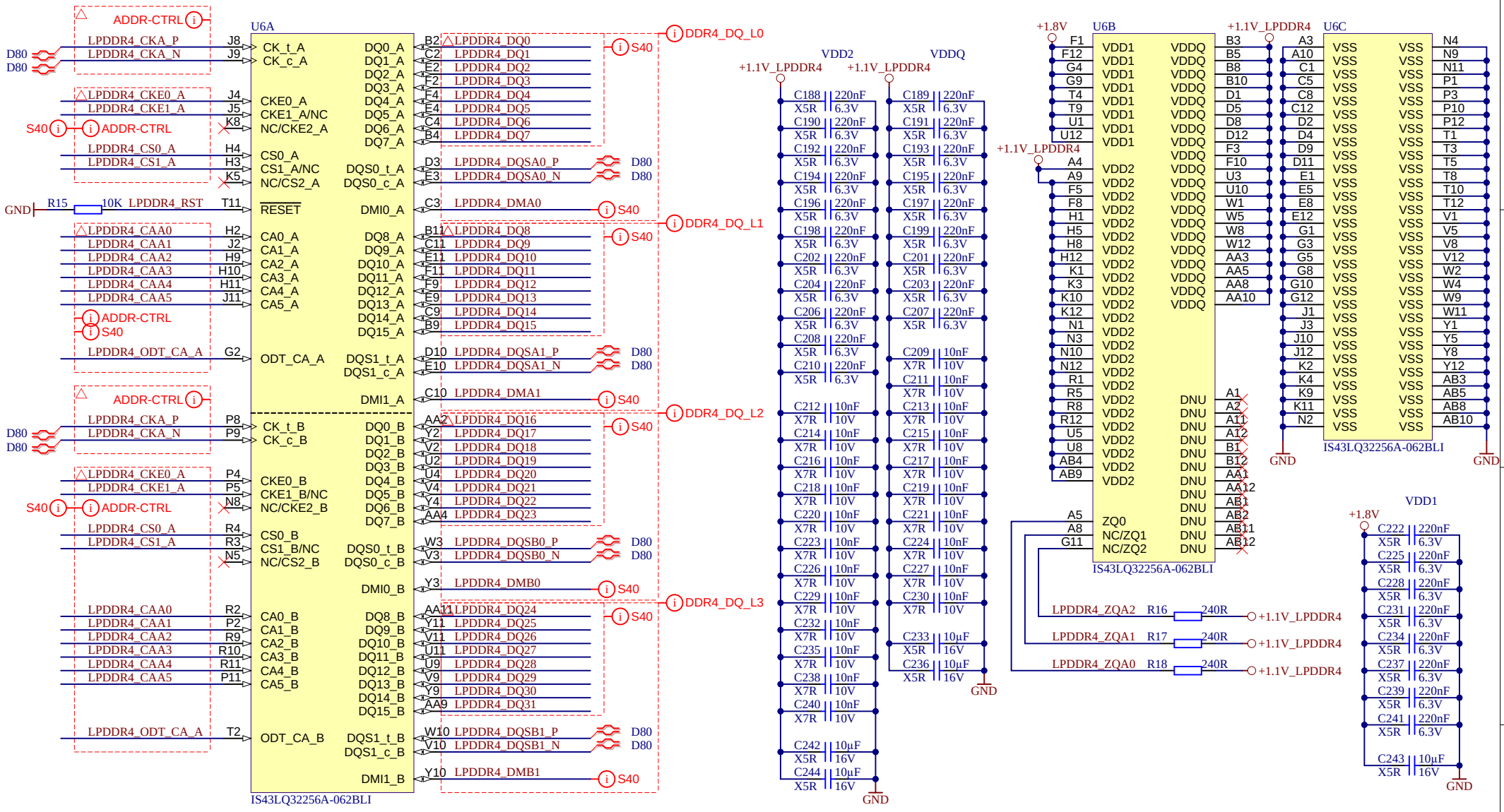


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| trenz electronic | Title: TEM0007 - LPDDR4 | | |
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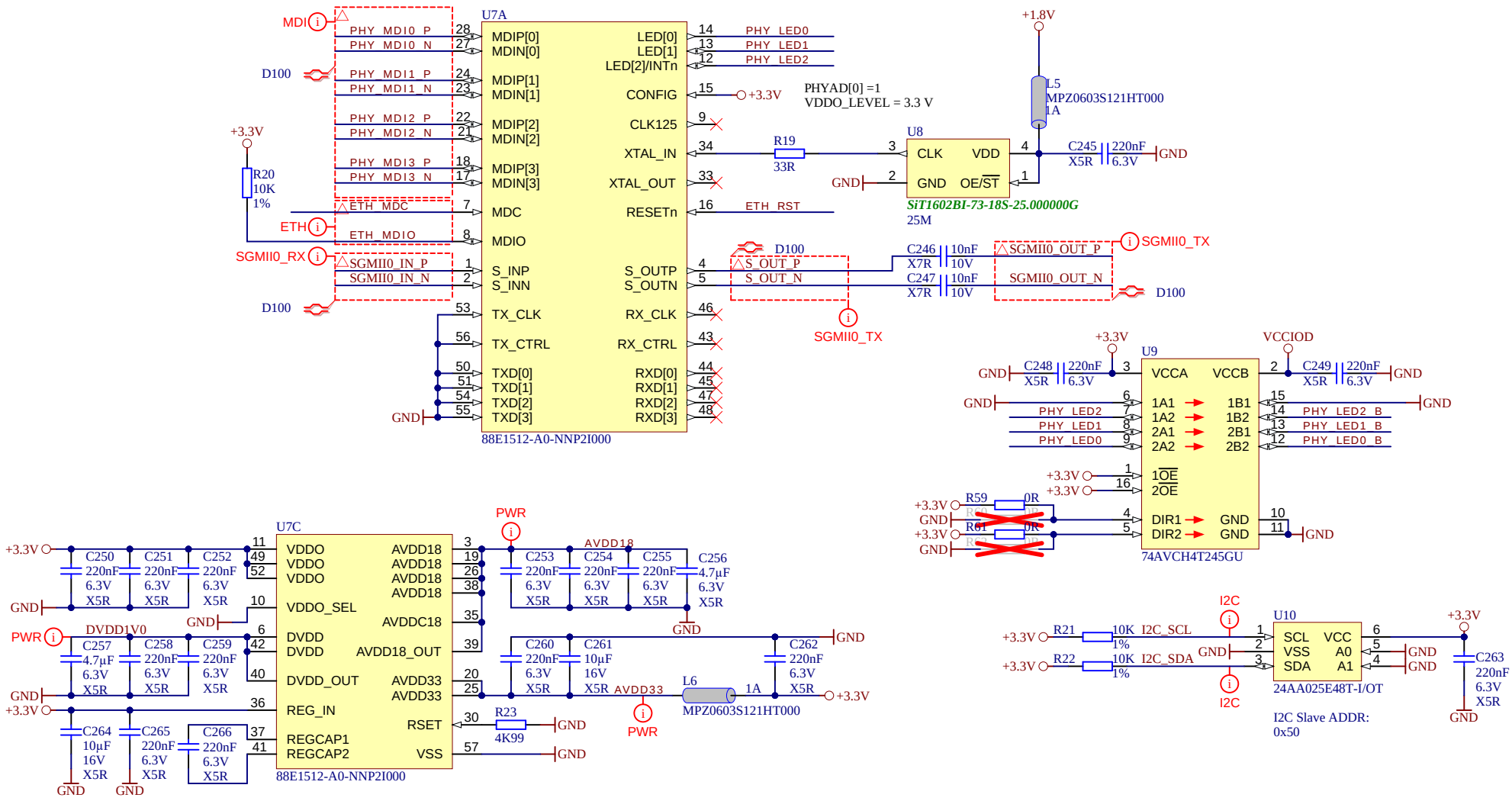
| Filename: LPDDR4.SchDoc | | | |

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| trenz electronic | Title: TEM0007 - ETH-PHY | | |
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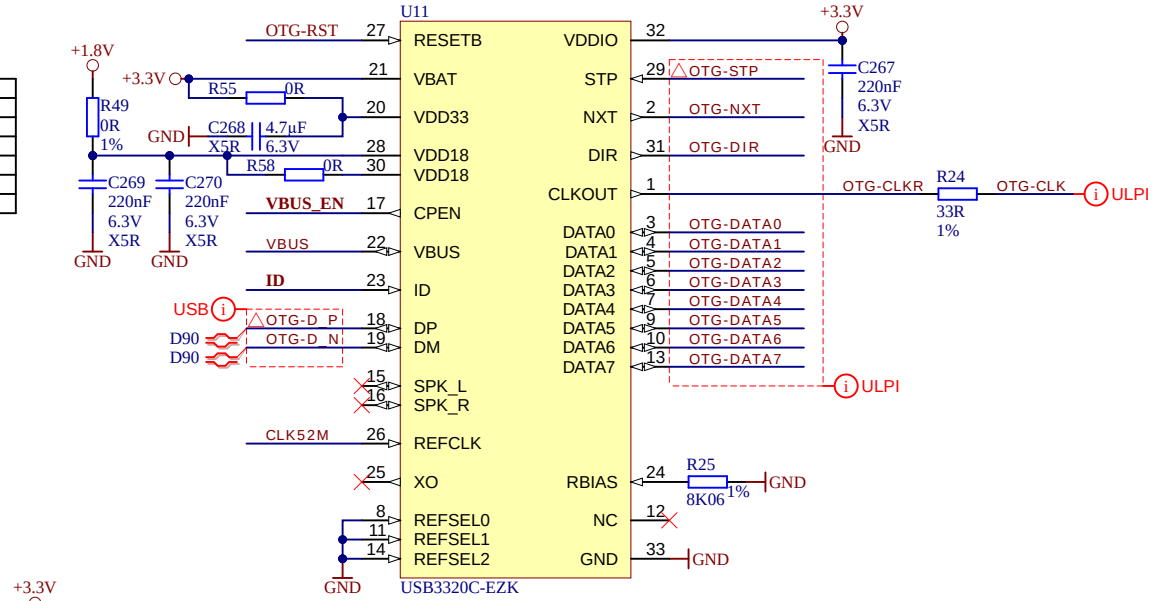
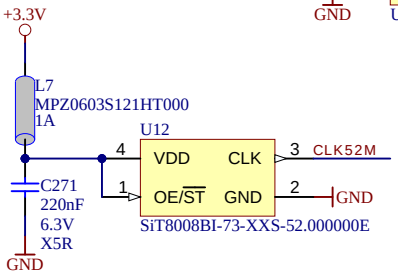
| | USB3320: | USB3340: |
|---|---|---|
| R49 | 0R | DNP |
| R55 | 0R | DNP |
| R58 | 0R | DNP |
| C268 | 4.7 uF | 1.0 uF |
| C269 | 0.1 uF | 1.0 uF |
| C270 | 0.1 uF | 1.0 uF |

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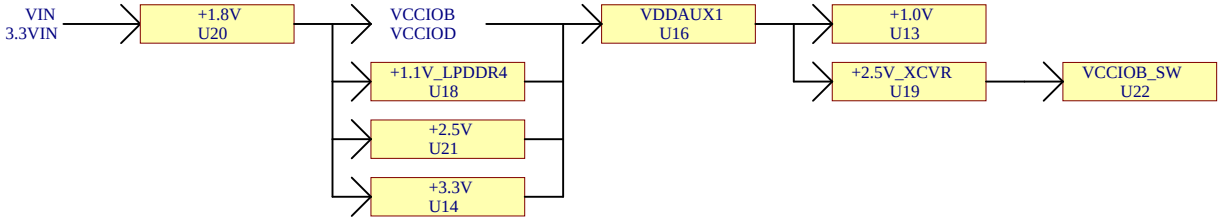
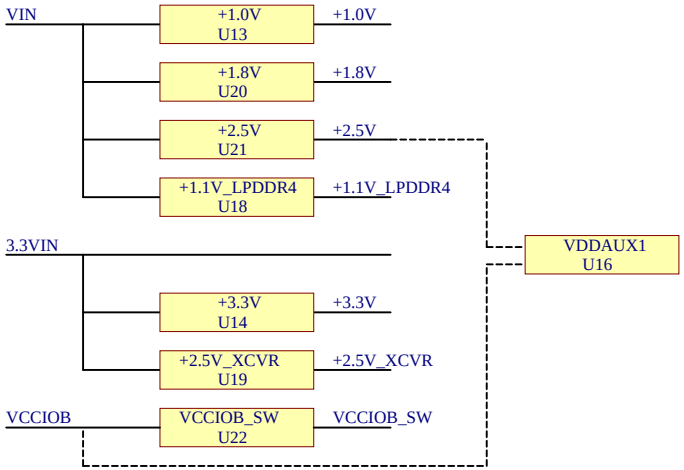
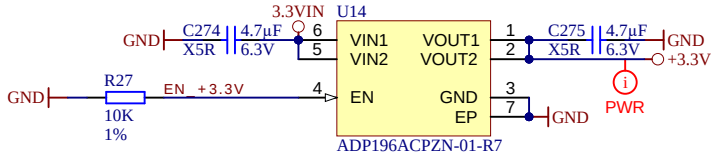
## Recommended Power Supply Sequencing

**The final power sequende depends on the CPLD.**

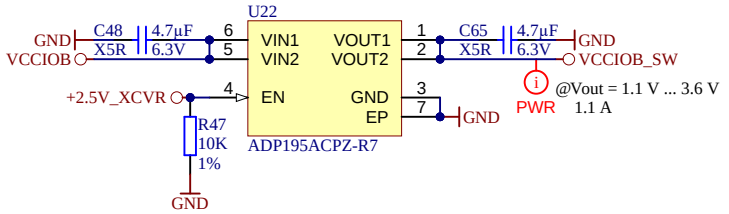


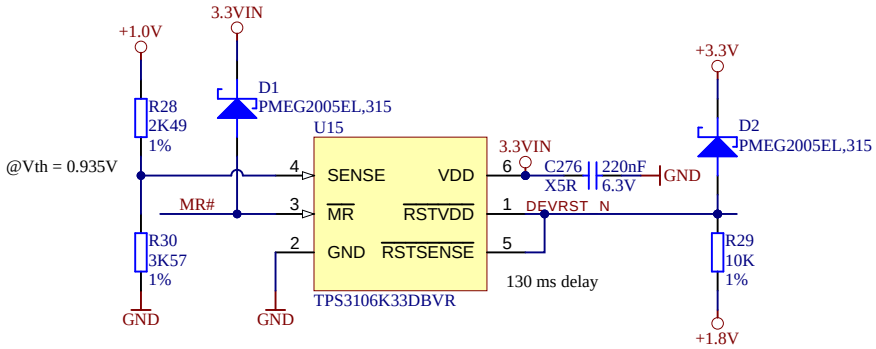

## Power Supply Structure



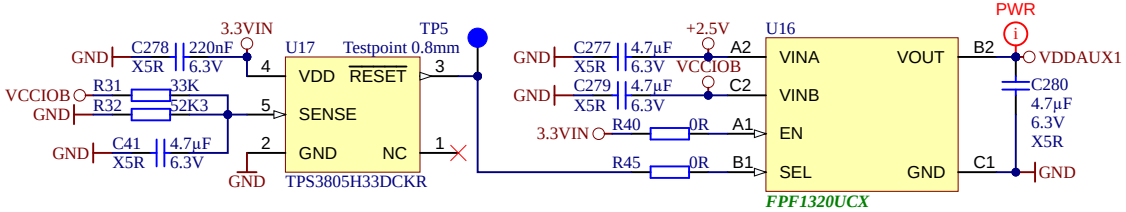




## Needed for IO Glitch Prevention!




VINA -> OUT for VCCIOB < 2.03 V
VINB -> OUT for VCCIOB > 2.03 V




VCCIOB < 2.03 V → RESET# = SEL = L → VOUT = VINA = +2.5 V
VCCIOB > 2.03 V → RESET# = SEL = H → VOUT = VINB = VCCIOB

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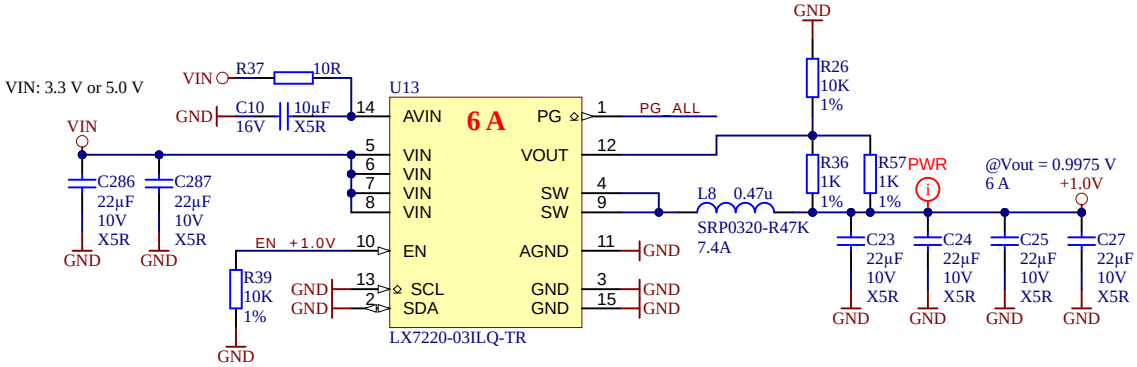


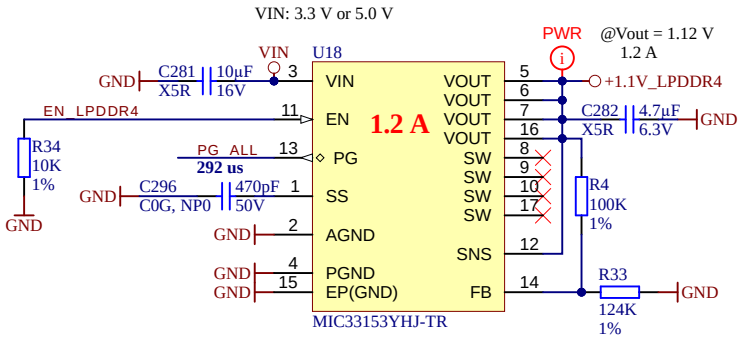


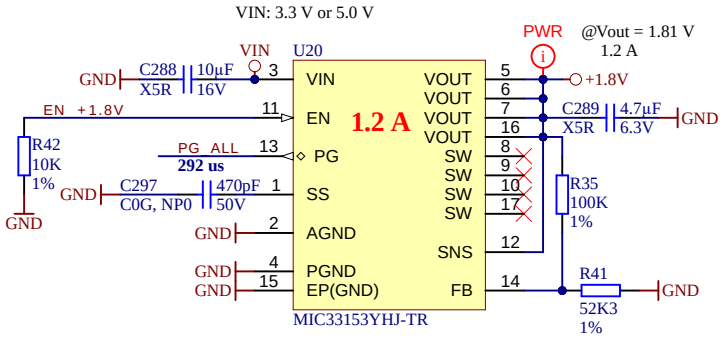


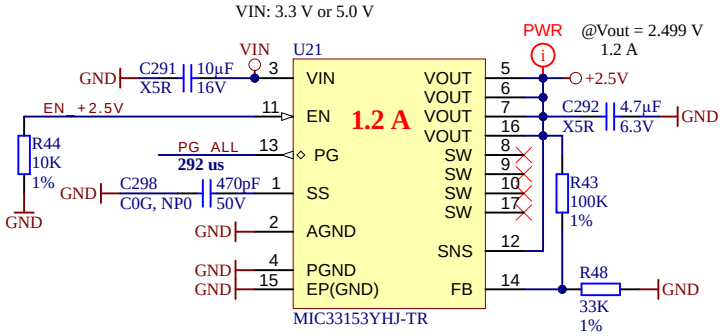


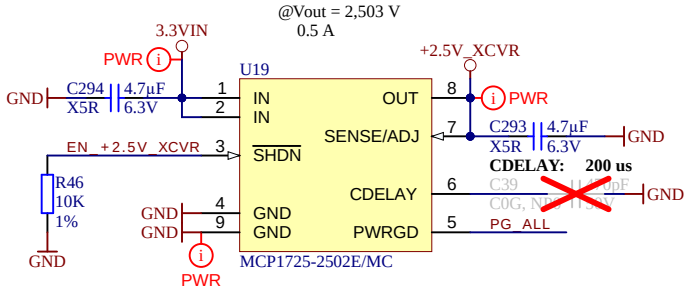


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| REV | DATE | Description | |
|---|---|---|---|
| -05 | | Initial revision | ED |
| | 2023-09-04 | 1. Changed power switch U16 from FPF1321BUCX to FPF1320UCX.<br>2. Updated revision history. | ED |

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|---|---|---|---|
| trenz electronic | Title: TEM0007 - Revision Changes List | | |
| | A4 | Number: TEM0007 CAA11-A | Rev. 01 |
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| | Drawn by: | Filename: Revision Changes.SchDoc | |