


Regarding the usage of our schematics and alike documentation for Trenz module TEM0007.

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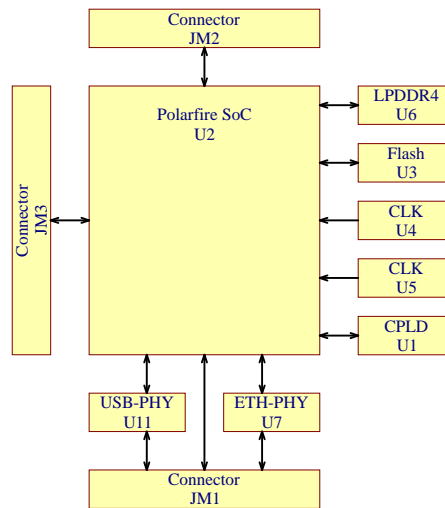
Schematics and other handouts serve for informational purposes only!

	Title: TEM0007 - Legal Notices		
	A4	Number: TEM0007 CAD11-A	Rev. 01
	Date: 2021-08-01	Copyright: Trenz Electronic GmbH	Page 1 of 17
	Filename: Legal Notices Modules.SchDoc		

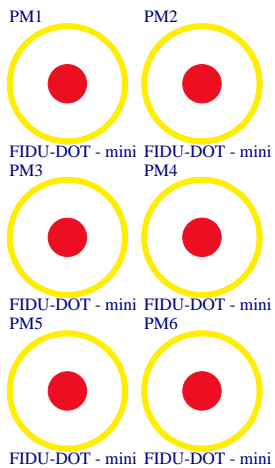
- B2B_Connector
- B2B_Connector.SchDoc
- CPLD
- CPLD.SchDoc
- FPGA1
- FPGA1.SchDoc
- FPGA2
- FPGA2.SchDoc
- FPGA3
- FPGA3.SchDoc
- FPGA4
- FPGA4.SchDoc
- FPGA5
- FPGA5.SchDoc
- FPGA6
- FPGA6.SchDoc
- FPGA_PWR
- FPGA_PWR.SchDoc
- LPDDR4
- LPDDR4.SchDoc
- ETH-PHY
- ETH-PHY.SchDoc
- USB-PHY
- USB-PHY.SchDoc
- POWER1
- POWER1.SchDoc
- POWER2
- POWER2.SchDoc

UKCA1
UKCA Logo on Top Overlay

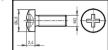
CE1
CE Logo on Top Overlay



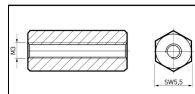
- +3.3V ○ TP1 Testpoint 0.8mm
- +2.5V ○ TP2 Testpoint 0.8mm
- +2.5V_XCVR ○ TP3 Testpoint 0.8mm
- +1.8V ○ TP4 Testpoint 0.8mm
- +1.1V_LPDDR4 ○ TP6 Testpoint 0.8mm
- +1.0V ○ TP7 Testpoint 0.8mm
- VDDAUX1 ○ TP8 Testpoint 0.8mm
- AVDD18 ○ TP9 Testpoint 0.8mm
- AVDD33 ○ TP10 Testpoint 0.8mm
- DVDD1V0 ○ TP11 Testpoint 0.8mm
- VCCIOB_SW ○ TP12 Testpoint 0.8mm
- +2.5V_VDDA ○ TP13 Testpoint 0.8mm
- +1.0V_VDDA ○ TP14 Testpoint 0.8mm
- +2.5V_VDD ○ TP15 Testpoint 0.8mm



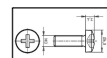
Top of Board



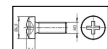
Screw M3x4



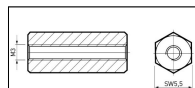
Standoff M3x8 II



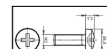
Screw M3x6



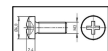
Screw M3x4



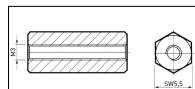
Standoff M3x8 II



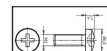
Screw M3x6



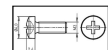
Screw M3x4



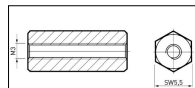
Standoff M3x8 II



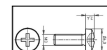
Screw M3x6



Screw M3x4

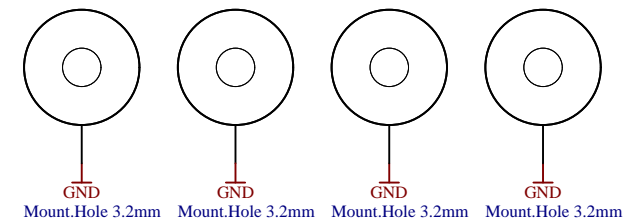


Standoff M3x8 II



Screw M3x6

Serial1
Serial
Serialnumber 6,3 x 6.3mm



GND Mount.Hole 3.2mm GND Mount.Hole 3.2mm GND Mount.Hole 3.2mm GND Mount.Hole 3.2mm

Title: TEM007

A4 Number: TEM007 CAD11-A Rev. 01

Date: 21.06.2022 Copyright: Trenz Electronic GmbH Page 2 of 17

Filename: TEM007.SchDoc

SD ETH

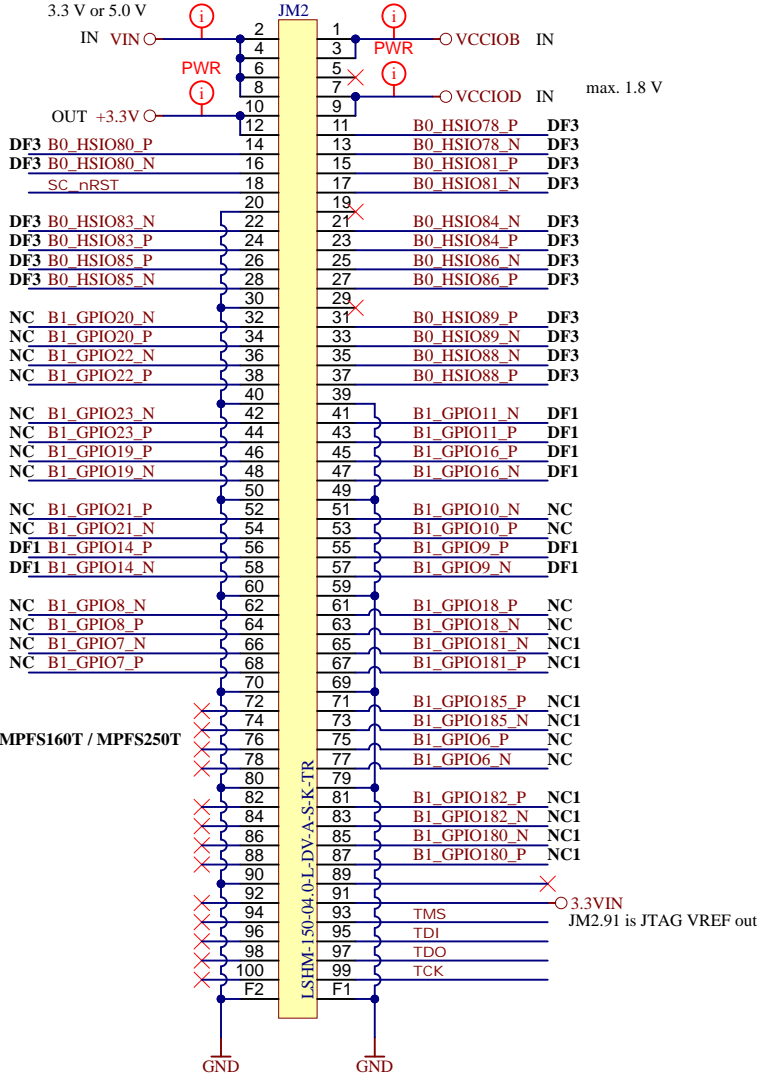
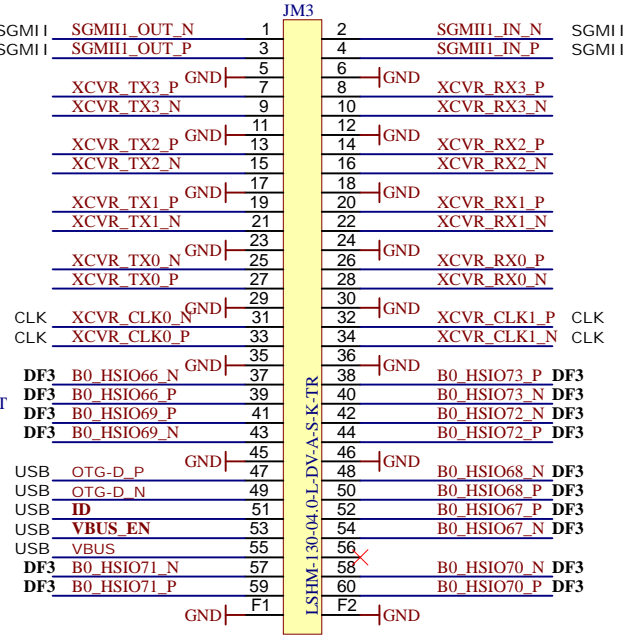
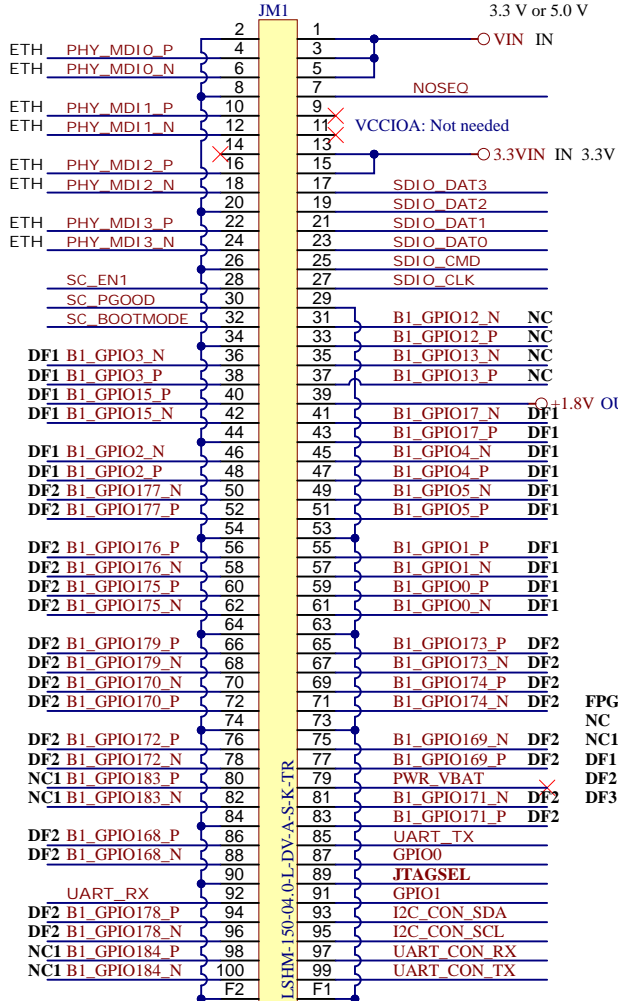
B1: 48 IO, 24 Differential Pairs, VCCIOB Fixed VCCIO
B4: 8 GPIO, 3.3 V Fixed VCCIO

USB MGT SGMII

B1: 16 IO, 8 Differential Pairs, VCCIOD Fixed VCCIO

JTAG: 3.3V Levels

B1: 36 IO, 18 Differential Pairs, VCCIOB Fixed VCCIO
B0: 18 IO, 9 Differential Pairs, VCCIOD Fixed VCCIO



FPGA SoC Notes:

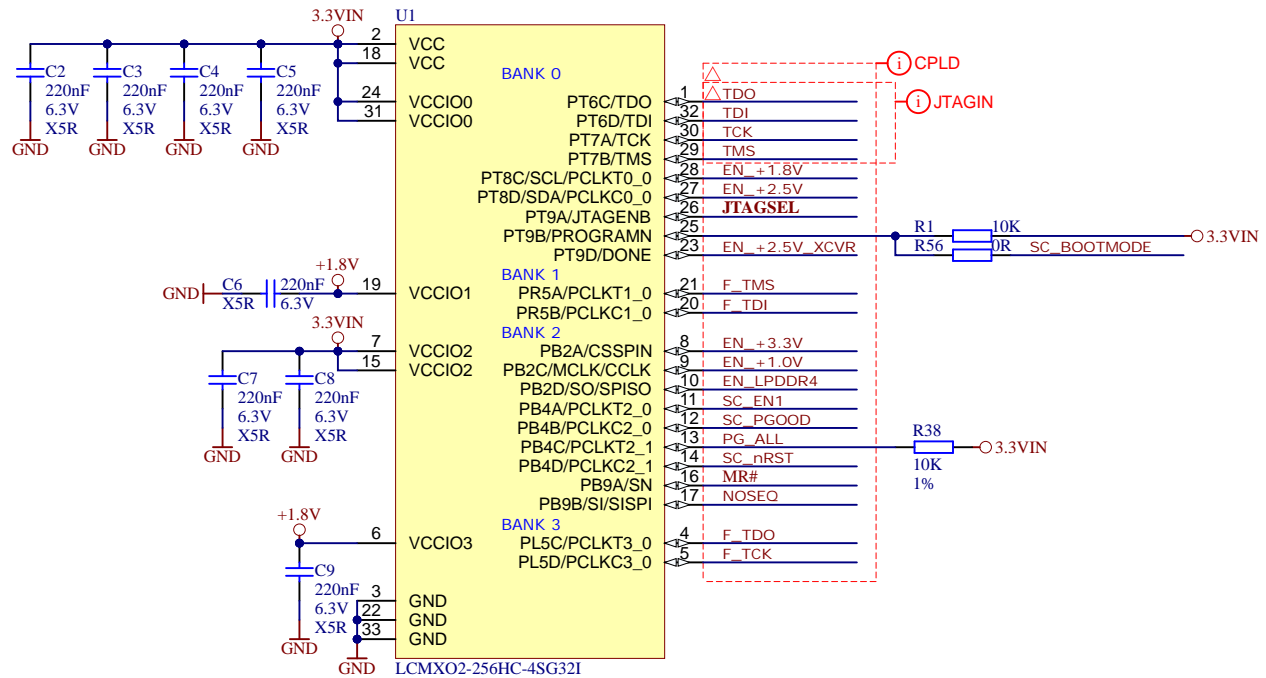
- NC Signals are not connected for MPFS025T
- NC1 Signals are not connected for MPFS025T and GPIOXX: XX differs for MPFS095T / MPFS160T / MPFS250T
- DF1 GPIOXX: XX for MPFS095T / MPFS160T / MPFS250T differs from MPFS025T
- DF2 GPIOXX: XX differs for MPFS025T / MPFS095T / MPFS160T / MPFS250T
- DF3 HSI0XX: XX differs for MPFS025T / MPFS095T / MPFS160T / MPFS250T




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Title: TEM007 - B2B_Connector		
A4	Number: TEM007 CAD11-A	Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH	Page 3 of 17
Filename: B2B_Connector.SchDoc		

Attention: Consider the I/O Glitch issues in document DS60001681A!

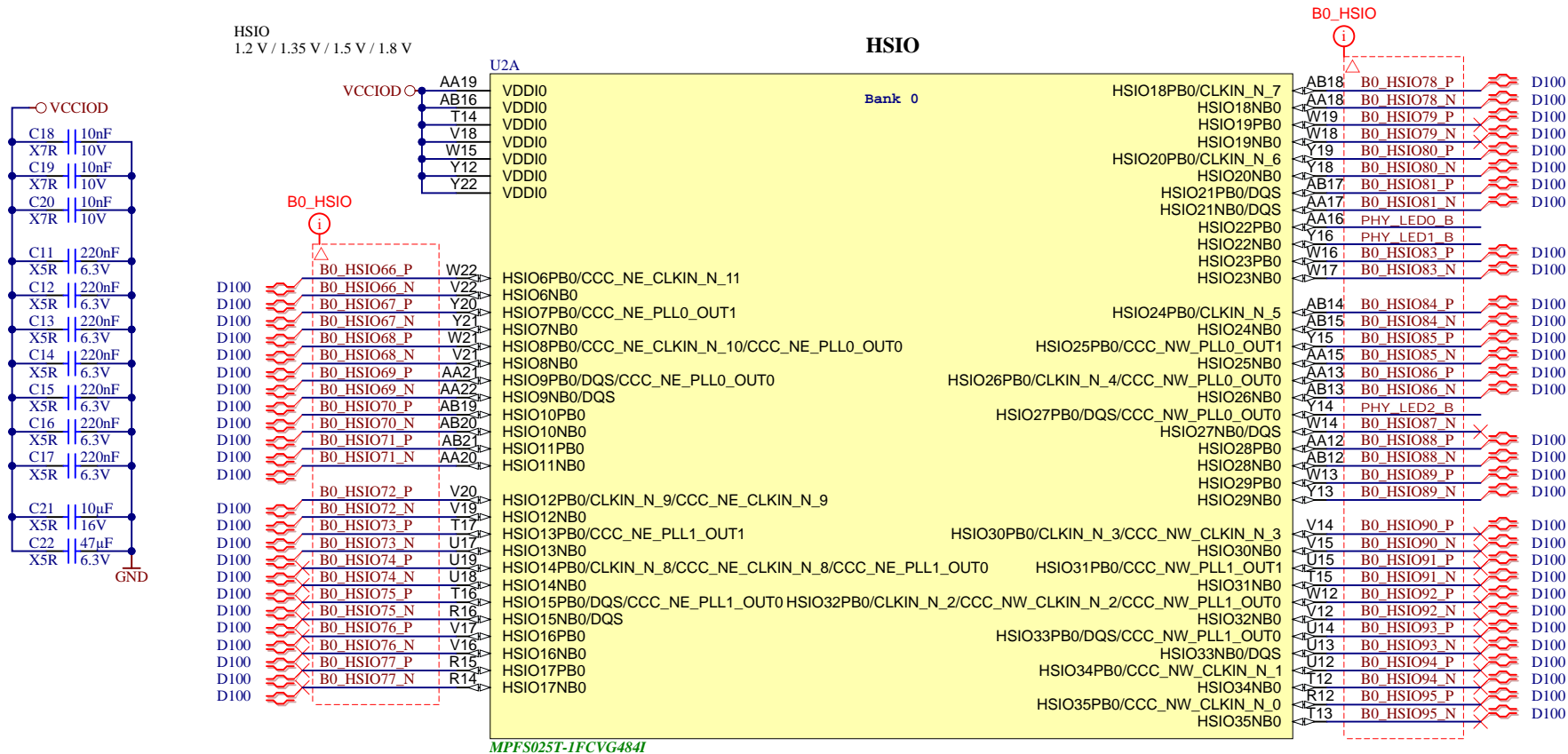


		Title: TEM0007 - CPLD	
		A4	Number: TEM0007 CAD11-A
Date: 21.06.2022		Copyright: Trenz Electronic GmbH	
Date: 21.06.2022		Page 4 of 17	
Filename: CPLD.SchDoc			

Attention:

1.) Consider the I/O Glitch issues in document DS60001681A!

2.) Using LVDS in HSIO bank needs an externally 100 Ohm resistor according to DS60001681A!



Title: TEM007 - FPGA1		
A4	Number: TEM007 CAD11-A	Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH	Page 5 of 17
Filename: FPGA1.SchDoc		

GPIO
1.2 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V

Attention: Consider the I/O Glitch issues in document DS60001681A!

GPIO

A

B

C

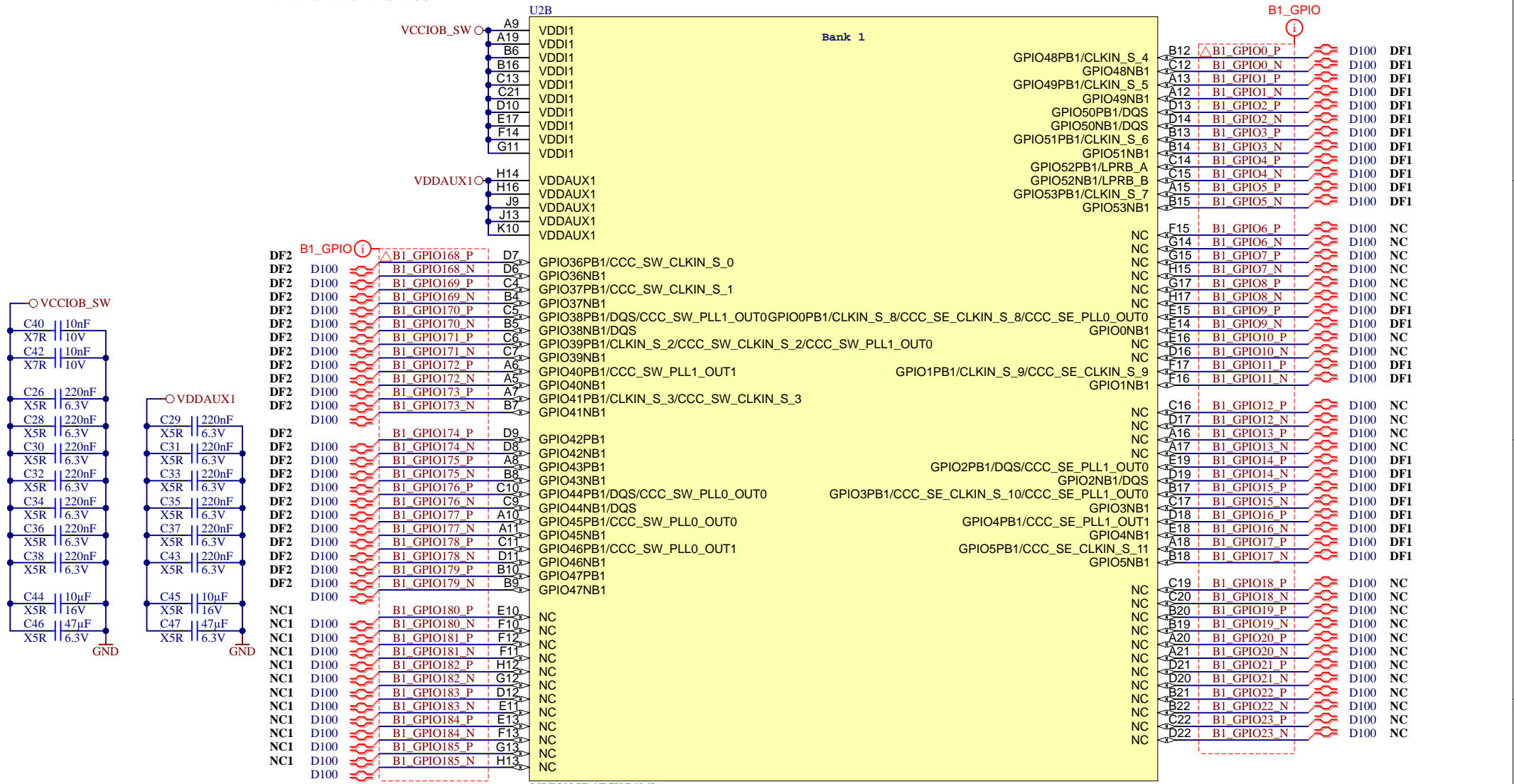
D

A

B

C

D



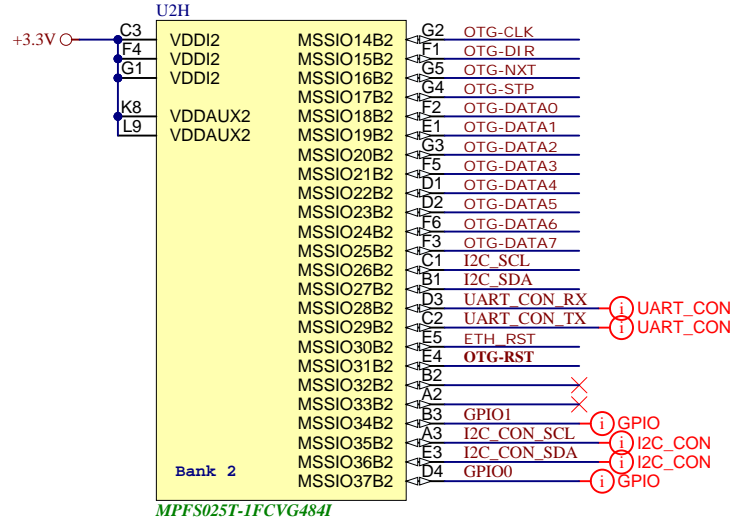
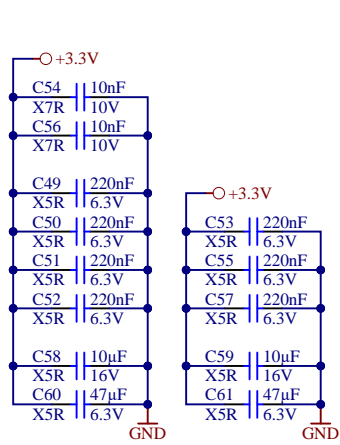
MPFS025T-IFCVG484I

FPGA SoC Notes:
 NC Signals are not connected for MPFS025T
 NC1 Signals are not connected for MPFS025T and GPIOXX: XX differs for MPFS095T / MPFS160T / MPFS250T
 DF1 GPIOXX: XX for MPFS095T / MPFS160T / MPFS250T differs from MPFS025T
 DF2 GPIOXX: XX differs for MPFS025T / MPFS095T / MPFS160T / MPFS250T



Title: TEM0007 - FPGA2		
A4	Number: TEM0007 CAD11-A	Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH	Page 6 of 17
Filename: FPGA2.SchDoc		

Attention: Consider the I/O Glitch issues in document DS60001681A!



A

B

C

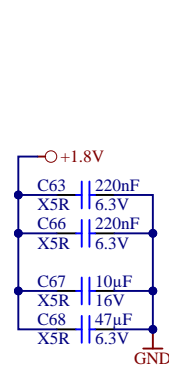
D

1

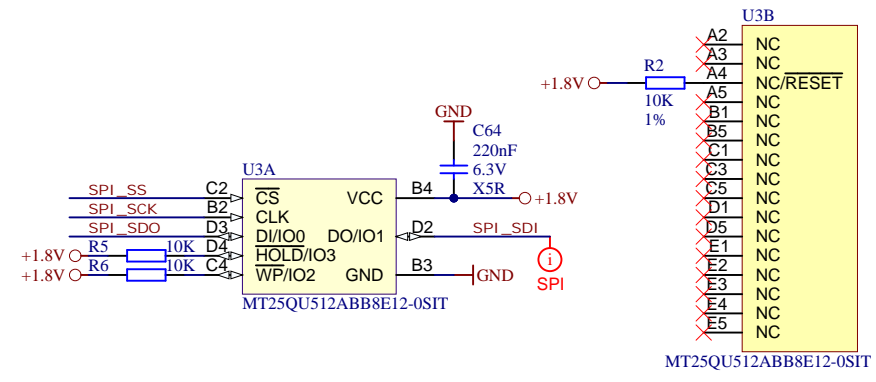
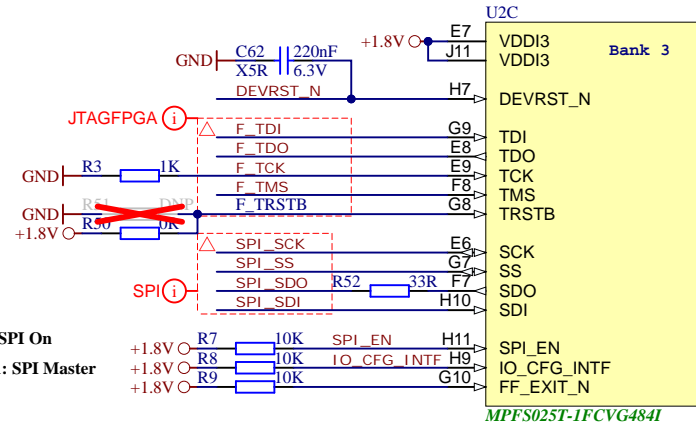
2

3

4



0: SPI Off 1: SPI On
0: SPI Slave 1: SPI Master



Title: TEM0007 - FPGA3		
A4	Number: TEM0007 CAD11-A	Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH	Page 7 of 17
Filename: FPGA3.SchDoc		

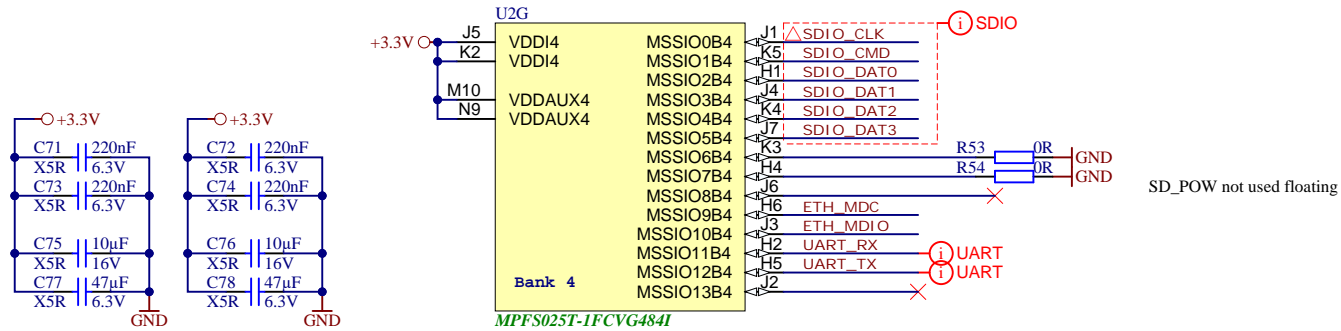
1


2

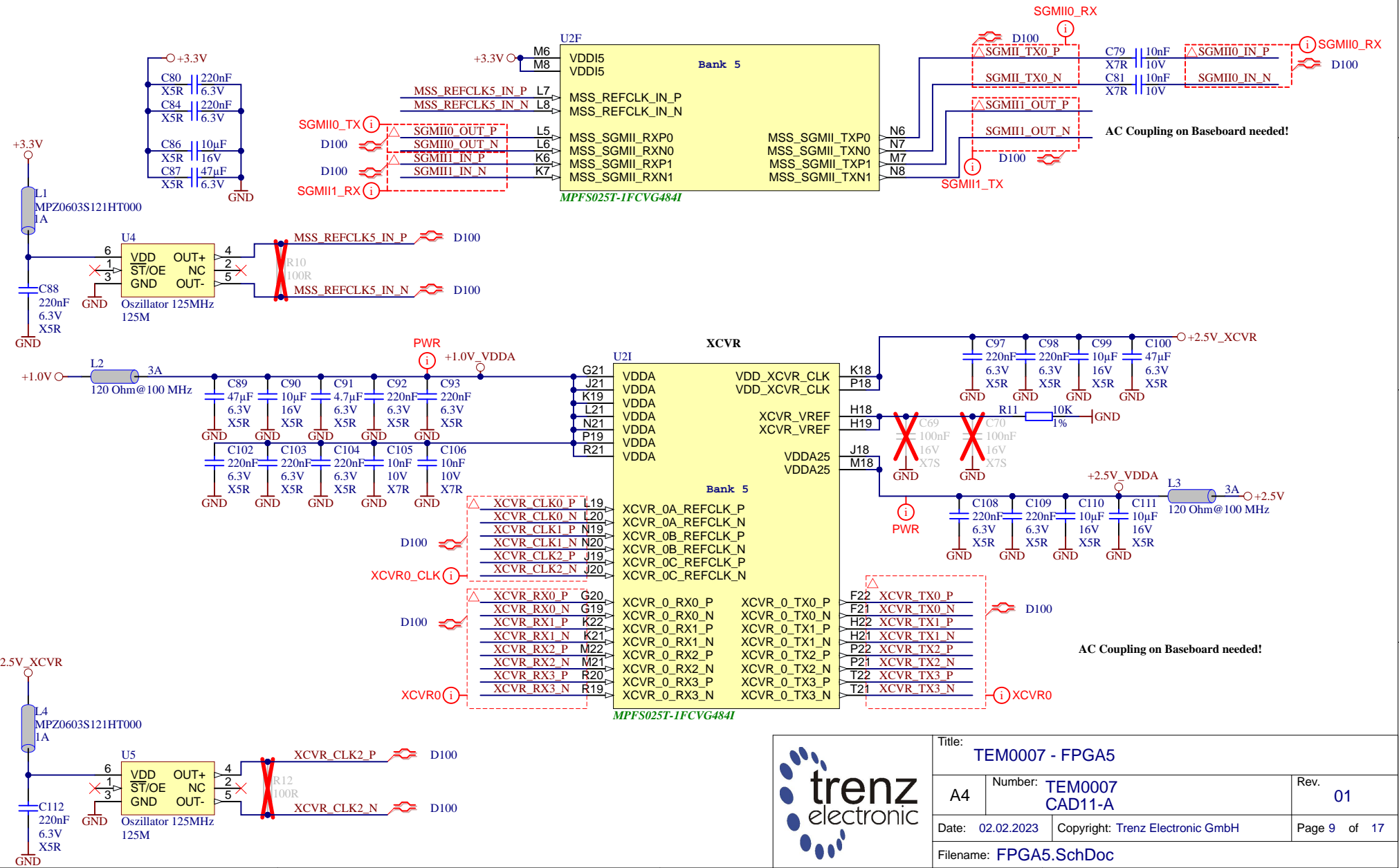
3

4

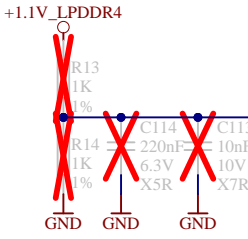
Attention: Consider the I/O Glitch issues in document DS60001681A!



		Title: TEM0007 - FPGA4	
		A4	Number: TEM0007 CAD11-A
Date: 02.02.2023		Copyright: Trenz Electronic GmbH	
Filename: FPGA4.SchDoc		Page 8 of 17	



Title: TEM007 - FPGA5		
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Date: 02.02.2023	Copyright: Trenz Electronic GmbH	Page 9 of 17
Filename: FPGA5.SchDoc		



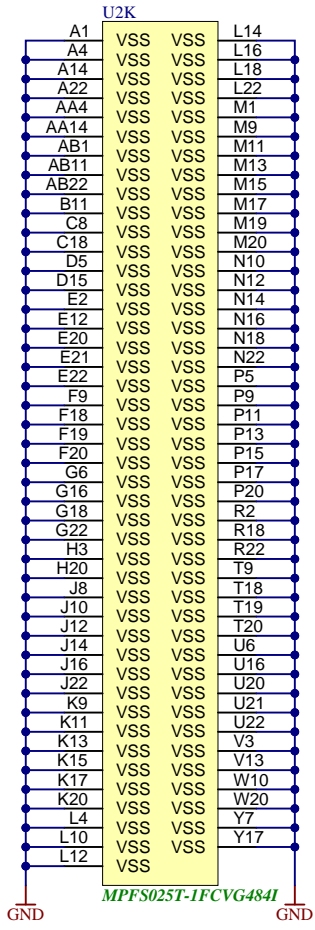
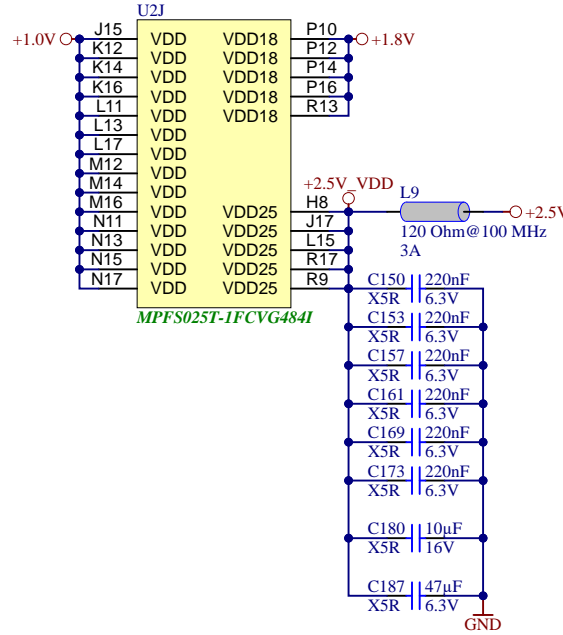
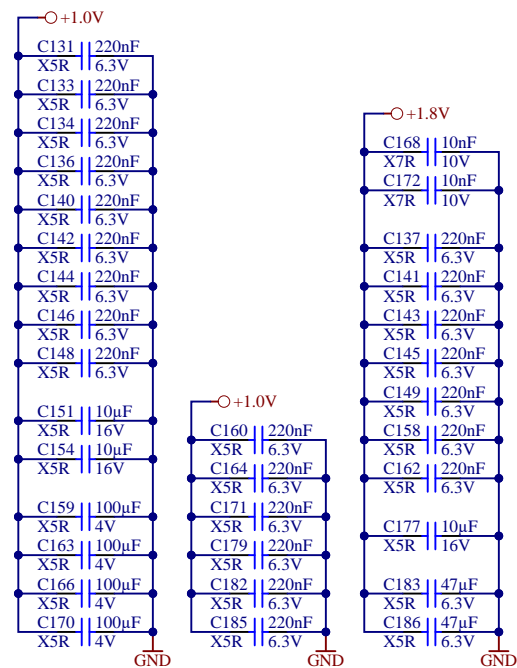
U2D MPFS025T-1FCVG484I			
AA9	VDDI6	MSS_DDR_CK0/DDR_PLL0_OUT0	U5 LPDDR4_CKA_P
AB6	VDDI6	MSS_DDR_CK0	U4 LPDDR4_CKA_N
N3	VDDI6		
R7	VDDI6	MSS_DDR_CK1/DDR_PLL0_OUT0	T1
T4	VDDI6	MSS_DDR_CK1	T2
U1	VDDI6		
U11	VDDI6		
V8	VDDI6		
W5	VDDI6	MSS_DDR_RAM_RST_N/DDR_PLL0_OUT1	L2 LPDDR4_RST
Y2	VDDI6		
		MSS_DDR_ALERT_N	N4
		MSS_DDR_VREF_IN	M5
		MSS_DDR_CS0	L3 LPDDR4_CS0_A
		MSS_DDR_CS1	M3 LPDDR4_CS1_A
		MSS_DDR_CKE0	K1 LPDDR4_CKE0_A
		MSS_DDR_CKE1	N2 LPDDR4_CKE1_A
		MSS_DDR_ACT_N	N5
		MSS_DDR_A6	P4
		MSS_DDR_BA0	T3
		MSS_DDR_BA1	
		MSS_DDR_BG0	N1
		MSS_DDR_BG1	M2
		MSS_DDR_ODT0	L1 LPDDR4_ODT_CA_A
		MSS_DDR_ODT1	M4
		MSS_DDR_A15	U3
		MSS_DDR_A16	
		MSS_DDR3_WE_N	

U2E MPFS025T-1FCVG484I			
AA2	MSS_DDR_DQS_P0	MSS_DDR_DQS_P2	AA11 LPDDR4_DQSB0_P
AA3	MSS_DDR_DQS_N0	MSS_DDR_DQS_N2	AA10 LPDDR4_DQSB0_N
AB4	MSS_DDR_DM0	MSS_DDR_DM2	Y10 LPDDR4_DMB0
Y3	MSS_DDR_DQ0	MSS_DDR_DQ16	Y9 LPDDR4_DQ16
Y4	MSS_DDR_DQ1	MSS_DDR_DQ17	W9 LPDDR4_DQ17
Y1	MSS_DDR_DQ2	MSS_DDR_DQ18	AB9 LPDDR4_DQ18
AA1	MSS_DDR_DQ3	MSS_DDR_DQ19	AB10 LPDDR4_DQ19
Y5	MSS_DDR_DQ4	MSS_DDR_DQ20	V11 LPDDR4_DQ20
AA5	MSS_DDR_DQ5	MSS_DDR_DQ21	V10 LPDDR4_DQ21
AB2	MSS_DDR_DQ6	MSS_DDR_DQ22	Y11 LPDDR4_DQ22
AB3	MSS_DDR_DQ7	MSS_DDR_DQ23	W11 LPDDR4_DQ23
Y6	MSS_DDR_DQS_P1	MSS_DDR_DQS_P3	U9 LPDDR4_DQSB1_P
W6	MSS_DDR_DQS_N1	MSS_DDR_DQS_N3	V9 LPDDR4_DQSB1_N
AA7	MSS_DDR_DM1	MSS_DDR_DM3	T10 LPDDR4_DMB1
W8	MSS_DDR_DQ8	MSS_DDR_DQ24	U8 LPDDR4_DQ24
W7	MSS_DDR_DQ9	MSS_DDR_DQ25	T8 LPDDR4_DQ25
AB5	MSS_DDR_DQ10	MSS_DDR_DQ26	T11 LPDDR4_DQ26
AA6	MSS_DDR_DQ11	MSS_DDR_DQ27	U10 LPDDR4_DQ27
AB7	MSS_DDR_DQ12	MSS_DDR_DQ28	R11 LPDDR4_DQ28
AB8	MSS_DDR_DQ13	MSS_DDR_DQ29	R10 LPDDR4_DQ29
Y8	MSS_DDR_DQ14	MSS_DDR_DQ30	R8 LPDDR4_DQ30
AA8	MSS_DDR_DQ15	MSS_DDR_DQ31	P8 LPDDR4_DQ31
		MSS_DDR_DQS_N4	V1
		MSS_DDR_DQS_P4	V2
		MSS_DDR_DM4	V5
		MSS_DDR_DQ32	W4
		MSS_DDR_DQ33	W3
		MSS_DDR_DQ34	W2
		MSS_DDR_DQ35	W1

Bank 6 MSS DDR
(continued)



Title: TEM0007 - FPGA6			
A4	Number: TEM0007 CAD11-A	Rev. 01	
Date: 21.06.2022	Copyright: Trenz Electronic GmbH	Page 10 of 17	
Filename: FPGA6.SchDoc			



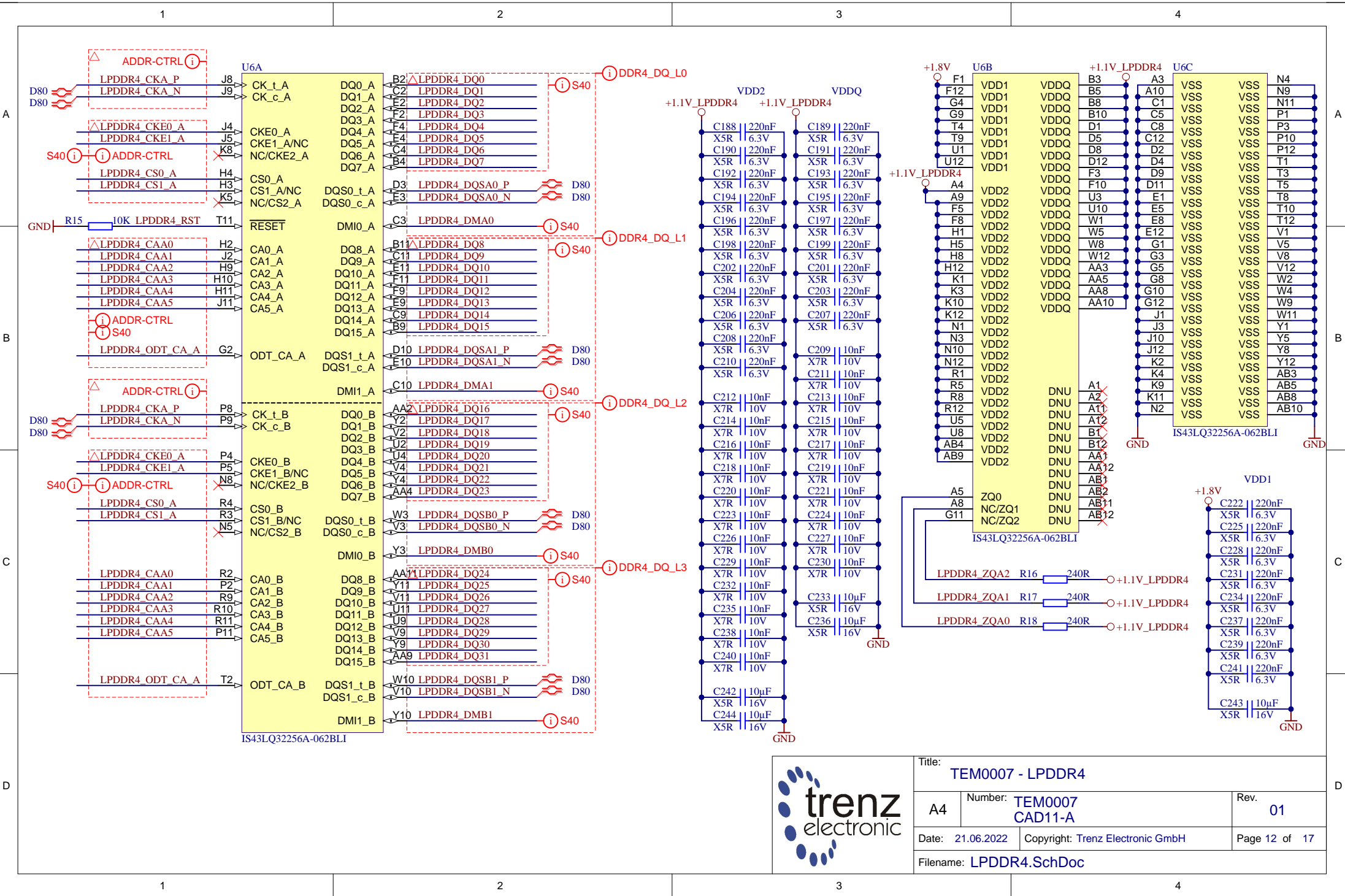
Both VDDA and VDD_XCVR_CLK supplies must be powered when any of the transceivers are used. VDD_XCVR_CLK must power on within the I/O calibration time (as specified for the device in Libero). VDDA and VDD_XCVR_CLK must both then remain powered during operation. If VDDA needs to be powered down, VDD_XCVR_CLK must also be powered down. There is no required sequence for powering up or down VDDA and VDD_XCVR_CLK.

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other I/O supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the I/O supplies of some I/O banks remain powered off).

VDD - For fabric core and transceiver/PCIe blocks.
 VDD18 - For fabric programming and RC oscillators.
 VDD25 - For corner phase-locked loop (PLLs) and on-chip non-volatile memory (sNVM).
 VDDIx - For I/O banks.
 VDDAUXx - For GPIO and HSIO banks.
 VDDA - For transceiver.
 VDDA25 - For transceiver PLLs.
 VDD_XCVR_CLK - For transceiver reference clock input buffers.



Title: TEM007 - FPGA_PWR		
A4	Number: TEM007 CAD11-A	Rev. 01
Date: 21.06.2022	Copyright: Trenz Electronic GmbH	Page 11 of 17
Filename: FPGA_PWR.SchDoc		



Title: TEM007 - LPDDR4		
A4	Number: TEM007 CAD11-A	Rev. 01
Date: 21.06.2022	Copyright: Trenz Electronic GmbH	Page 12 of 17
Filename: LPDDR4.SchDoc		

A

B

C

D

1

2

3

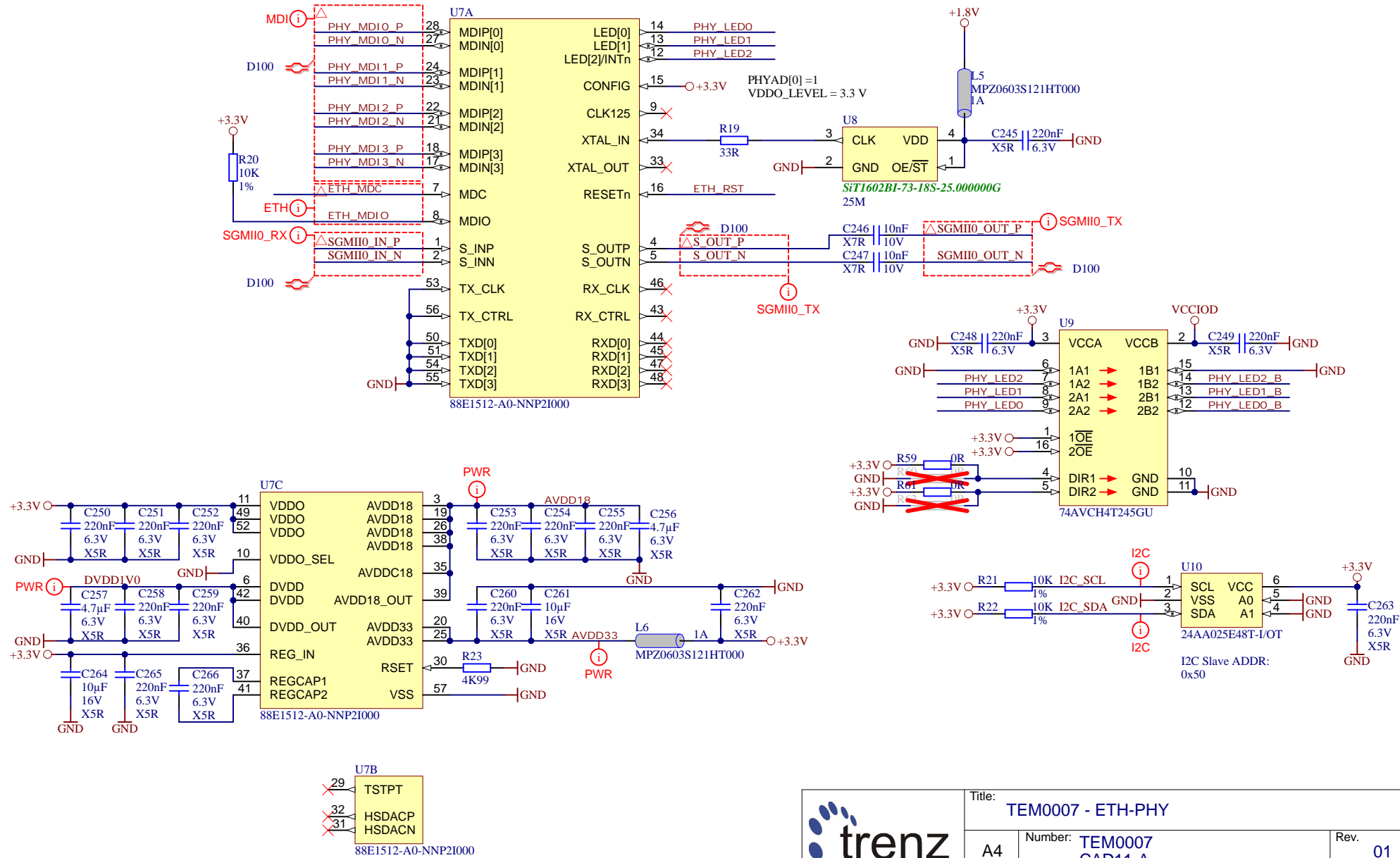
4

A

B

C

D



Title: TEM007 - ETH-PHY		
A4	Number: TEM007 CAD11-A	Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH	Page 13 of 17
Filename: ETH-PHY.SchDoc		

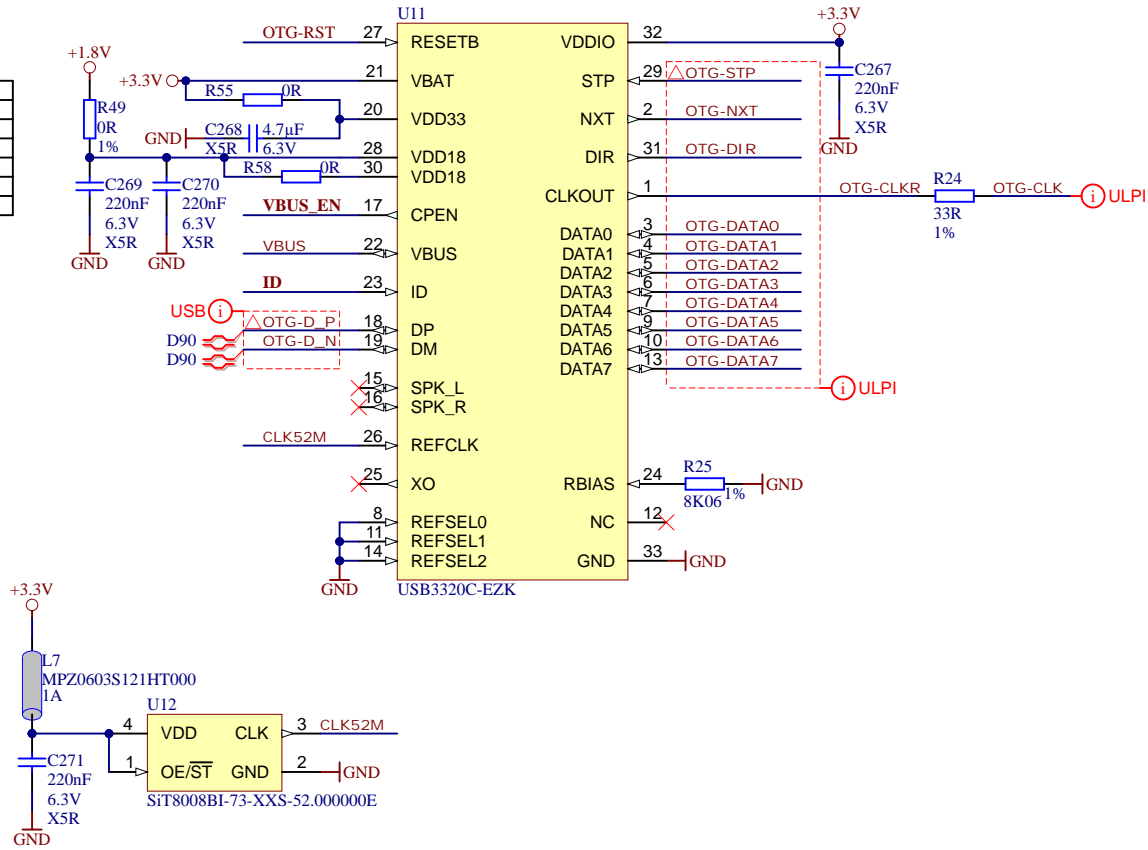
1


2

3

4

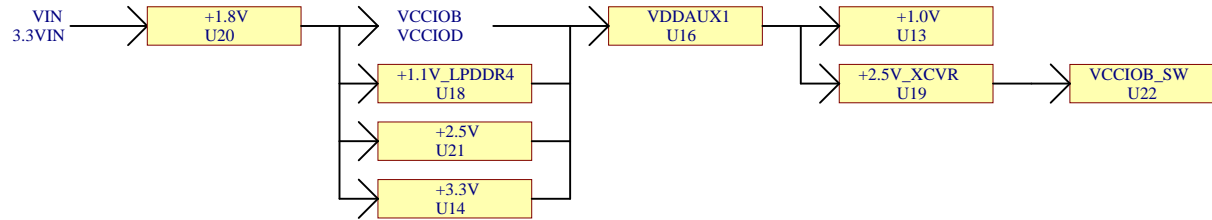
	USB3320:	USB3340:
R49	0R	DNP
R55	0R	DNP
R58	0R	DNP
C268	4.7 uF	1.0 uF
C269	0.1 uF	1.0 uF
C270	0.1 uF	1.0 uF



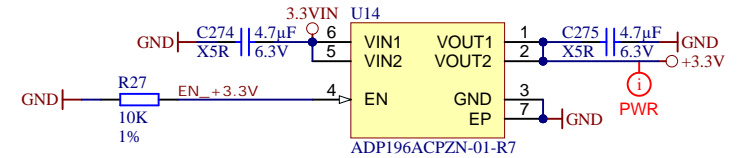
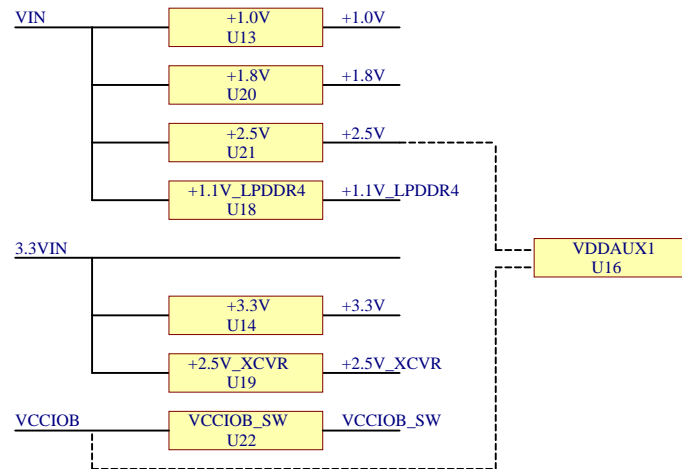
		Title: TEM0007 - USB-PHY	
		A4	Number: TEM0007 CAD11-A
Date: 02.02.2023		Copyright: Trenz Electronic GmbH	
Filename: USB-PHY.SchDoc		Page 14 of 17	

Recommended Power Supply Sequencing

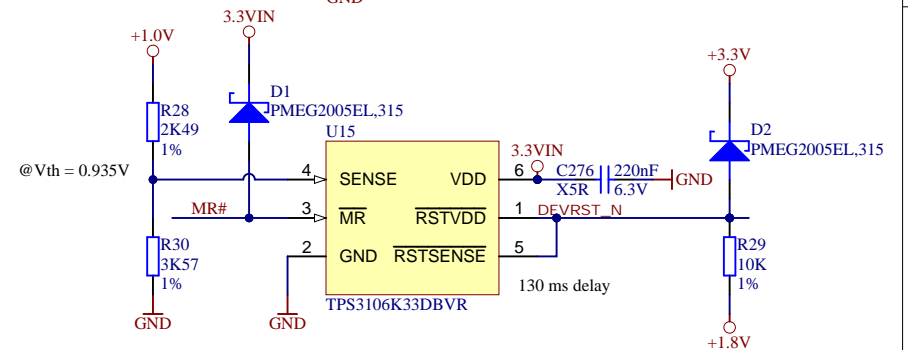
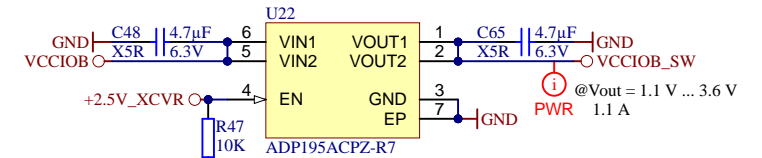
The final power sequende depends on the CPLD.



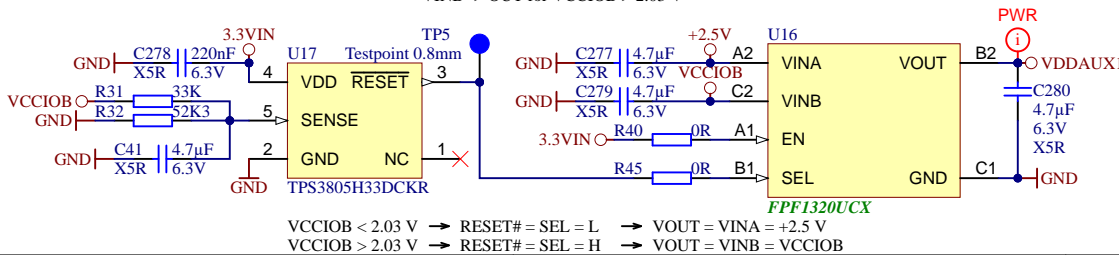
Power Supply Structure



Needed for IO Glitch Prevention!



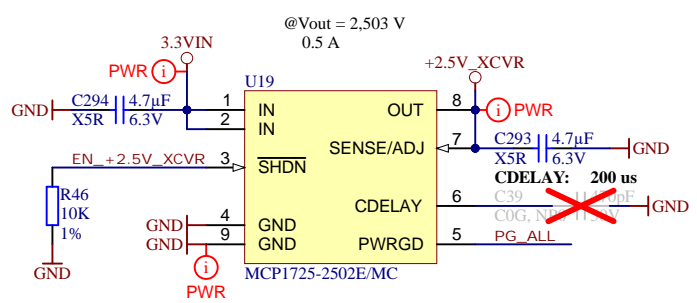
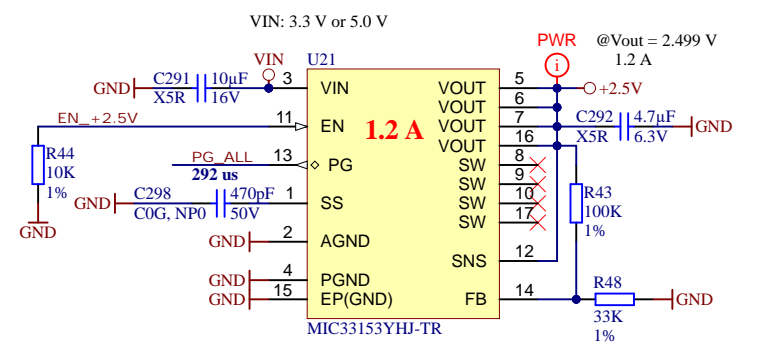
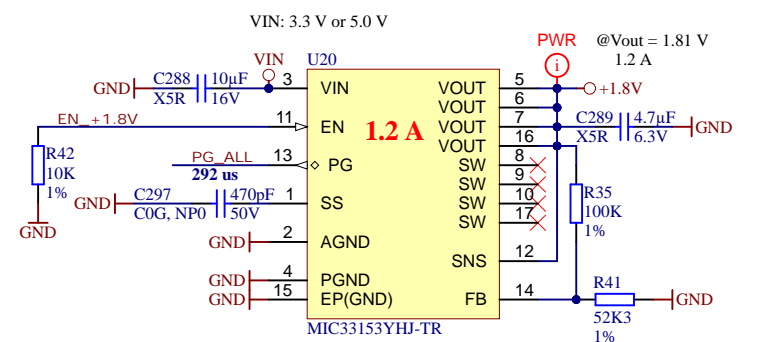
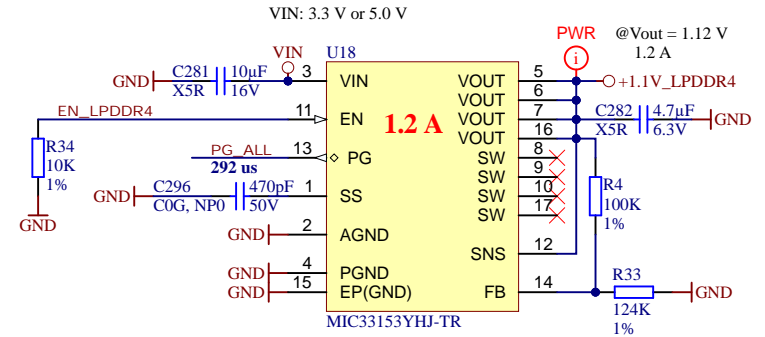
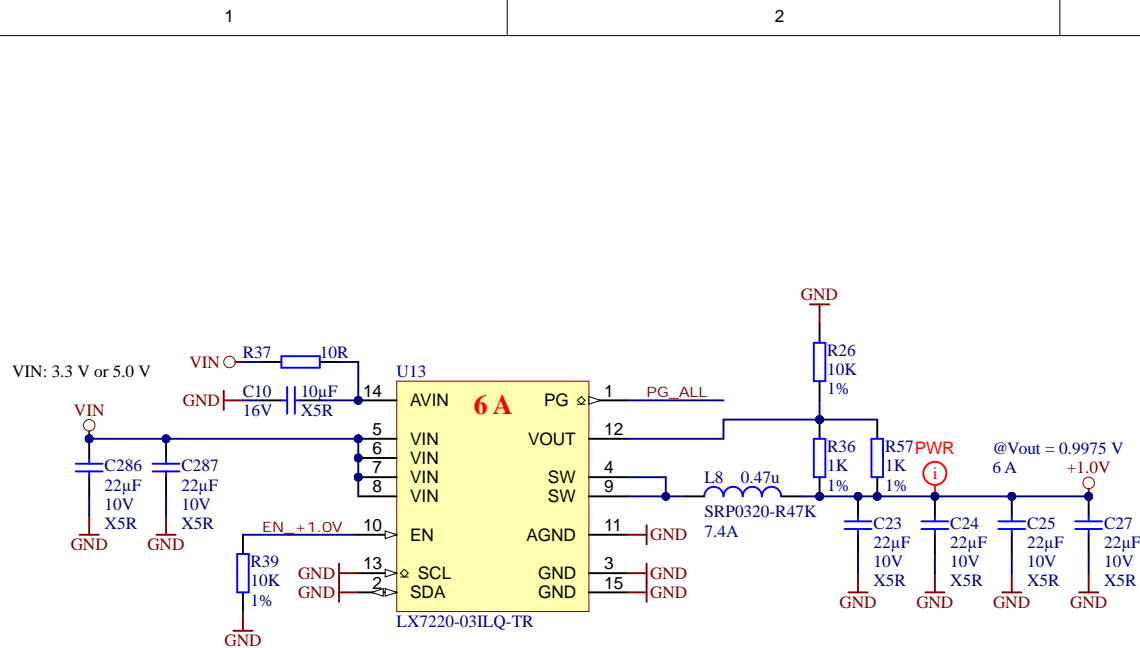
VINA -> OUT for VCCIOB < 2.03 V
VINB -> OUT for VCCIOB > 2.03 V



VCCIOB < 2.03 V -> RESET# = SEL = L -> VOUT = VINA = +2.5 V
VCCIOB > 2.03 V -> RESET# = SEL = H -> VOUT = VINB = VCCIOB



Title: TEM007 - POWER1		
A4	Number: TEM007 CAD11-A	Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH	Page 15 of 17
Filename: POWER1.SchDoc		



			Title: TEM007 - POWER2	
			A4	Number: TEM007 CAD11-A
Date: 02.02.2023		Copyright: Trenz Electronic GmbH		Page 16 of 17
Filename: POWER2.SchDoc				

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REV	DATE	Description	
-05	2023-09-04	Initial revision 1. Changed power switch U16 from FPF1321BUCX to FPF1320UCX. 2. Updated revision history.	ED ED

B


B

C

C

D

D

			Title: TEM0007 - Revision Changes List		
			A4	Number: TEM0007 CAD11-A	Rev. 01
Date: 2021-10-22		Copyright: Trenz Electronic GmbH		Page 17 of 17	
Drawn by:			Filename: Revision Changes.SchDoc		

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4