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Schematics and other handouts serve for informational purposes only!

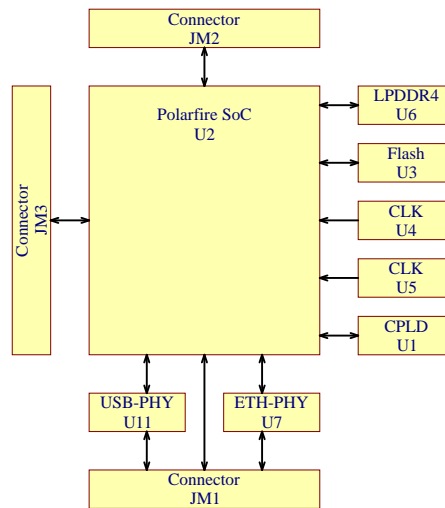


Title: TEM0007 - Legal Notices		
A4	Number: TEM0007 CHD11-A	Rev. 01
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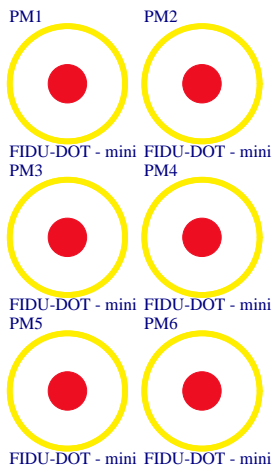
- B2B_Connector
- B2B_Connector.SchDoc
- CPLD
- CPLD.SchDoc
- FPGA1
- FPGA1.SchDoc
- FPGA2
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- FPGA5
- FPGA5.SchDoc
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- LPDDR4
- LPDDR4.SchDoc
- ETH-PHY
- ETH-PHY.SchDoc
- USB-PHY
- USB-PHY.SchDoc
- POWER1
- POWER1.SchDoc
- POWER2
- POWER2.SchDoc

UKCA1
UKCA Logo on Top Overlay

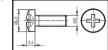
CE1
CE Logo on Top Overlay



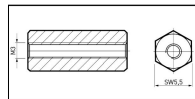
- +3.3V ○ TP1 Testpoint 0.8mm
- +2.5V ○ TP2 Testpoint 0.8mm
- +2.5V_XCVR ○ TP3 Testpoint 0.8mm
- +1.8V ○ TP4 Testpoint 0.8mm
- +1.1V_LPDDR4 ○ TP6 Testpoint 0.8mm
- +1.0V ○ TP7 Testpoint 0.8mm
- VDDAUX1 ○ TP8 Testpoint 0.8mm
- AVDD18 ○ TP9 Testpoint 0.8mm
- AVDD33 ○ TP10 Testpoint 0.8mm
- DVDD1V0 ○ TP11 Testpoint 0.8mm
- VCCIOB_SW ○ TP12 Testpoint 0.8mm
- +2.5V_VDDA ○ TP13 Testpoint 0.8mm
- +1.0V_VDDA ○ TP14 Testpoint 0.8mm
- +2.5V_VDD ○ TP15 Testpoint 0.8mm



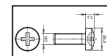
Top of Board



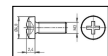
Screw M3x4



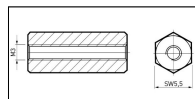
Standoff M3x8 II



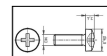
Screw M3x6



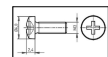
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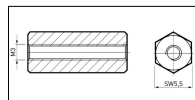
Standoff M3x8 II



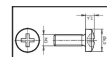
Screw M3x6



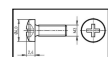
Screw M3x4



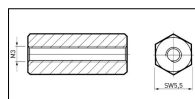
Standoff M3x8 II



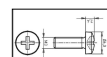
Screw M3x6



Screw M3x4

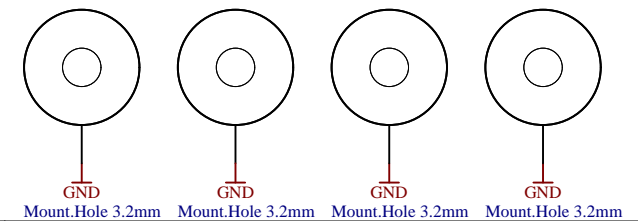


Standoff M3x8 II



Screw M3x6

Serial1
Serial
Serialnumber 6,3 x 6.3mm



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SD ETH

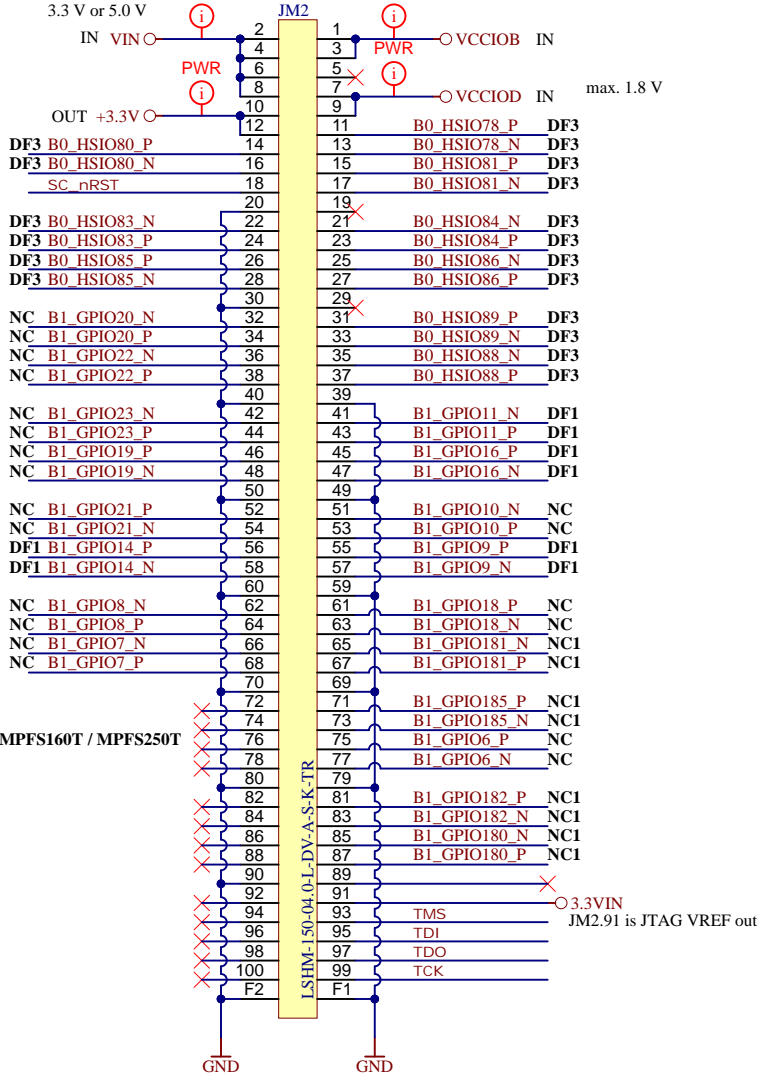
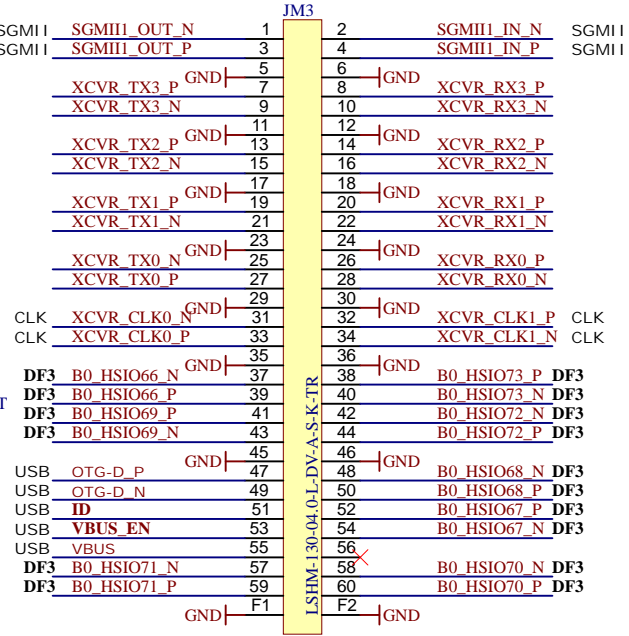
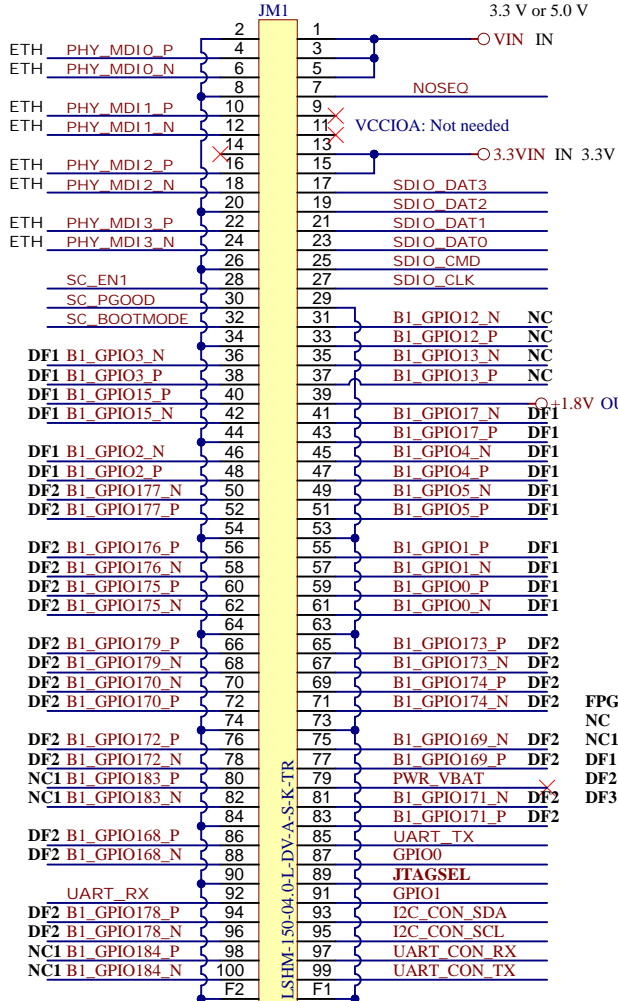
B1: 48 IO, 24 Differential Pairs, VCCIOB Fixed VCCIO
B4: 8 GPIO, 3.3 V Fixed VCCIO

USB MGT SGMII

B1: 16 IO, 8 Differential Pairs, VCCIOD Fixed VCCIO

JTAG: 3.3V Levels

B1: 36 IO, 18 Differential Pairs, VCCIOB Fixed VCCIO
B0: 18 IO, 9 Differential Pairs, VCCIOD Fixed VCCIO



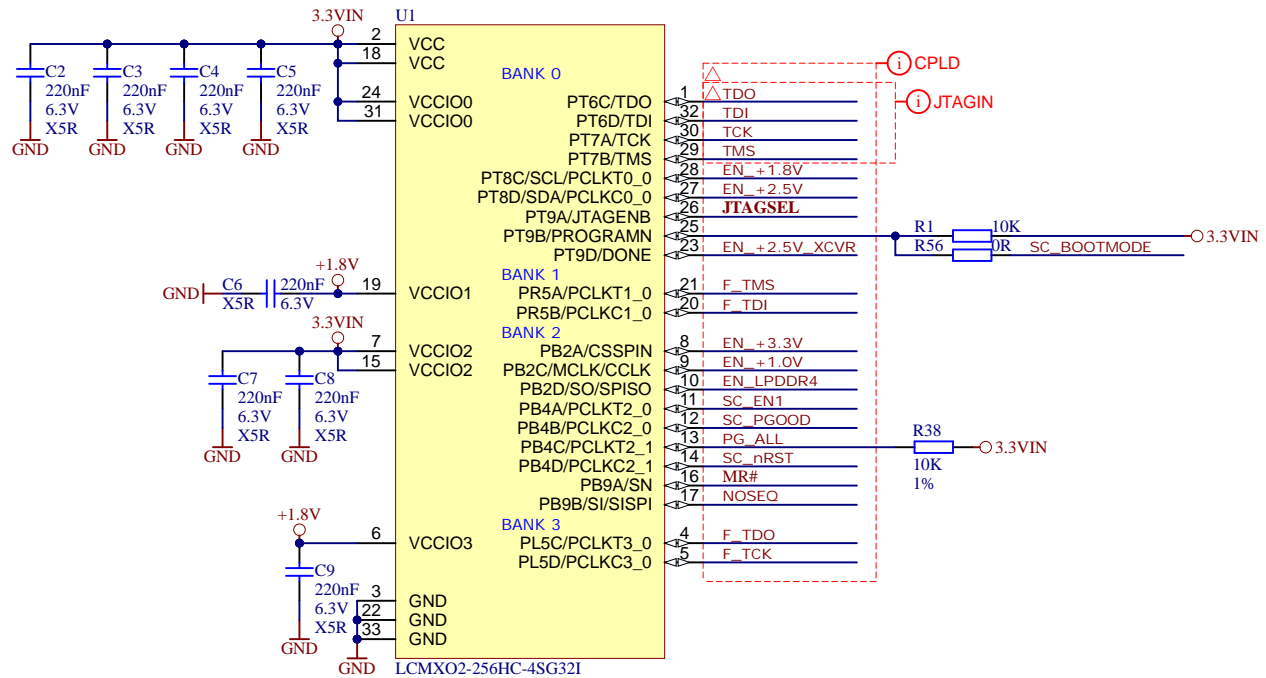
FPGA SoC Notes:


- NC Signals are not connected for MPFS025T
- NC1 Signals are not connected for MPFS025T and GPIOXX: XX differs for MPFS095T / MPFS160T / MPFS250T
- DF1 GPIOXX: XX for MPFS095T / MPFS160T / MPFS250T differs from MPFS025T
- DF2 GPIOXX: XX differs for MPFS025T / MPFS095T / MPFS160T / MPFS250T
- DF3 HSI0XX: XX differs for MPFS025T / MPFS095T / MPFS160T / MPFS250T



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Attention: Consider the I/O Glitch issues in document DS60001681A!



		Title: TEM0007 - CPLD	
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Attention:

1.) Consider the I/O Glitch issues in document DS60001681A!

2.) Using LVDS in HSIO bank needs an externally 100 Ohm resistor according to DS60001681A!

A

A

B

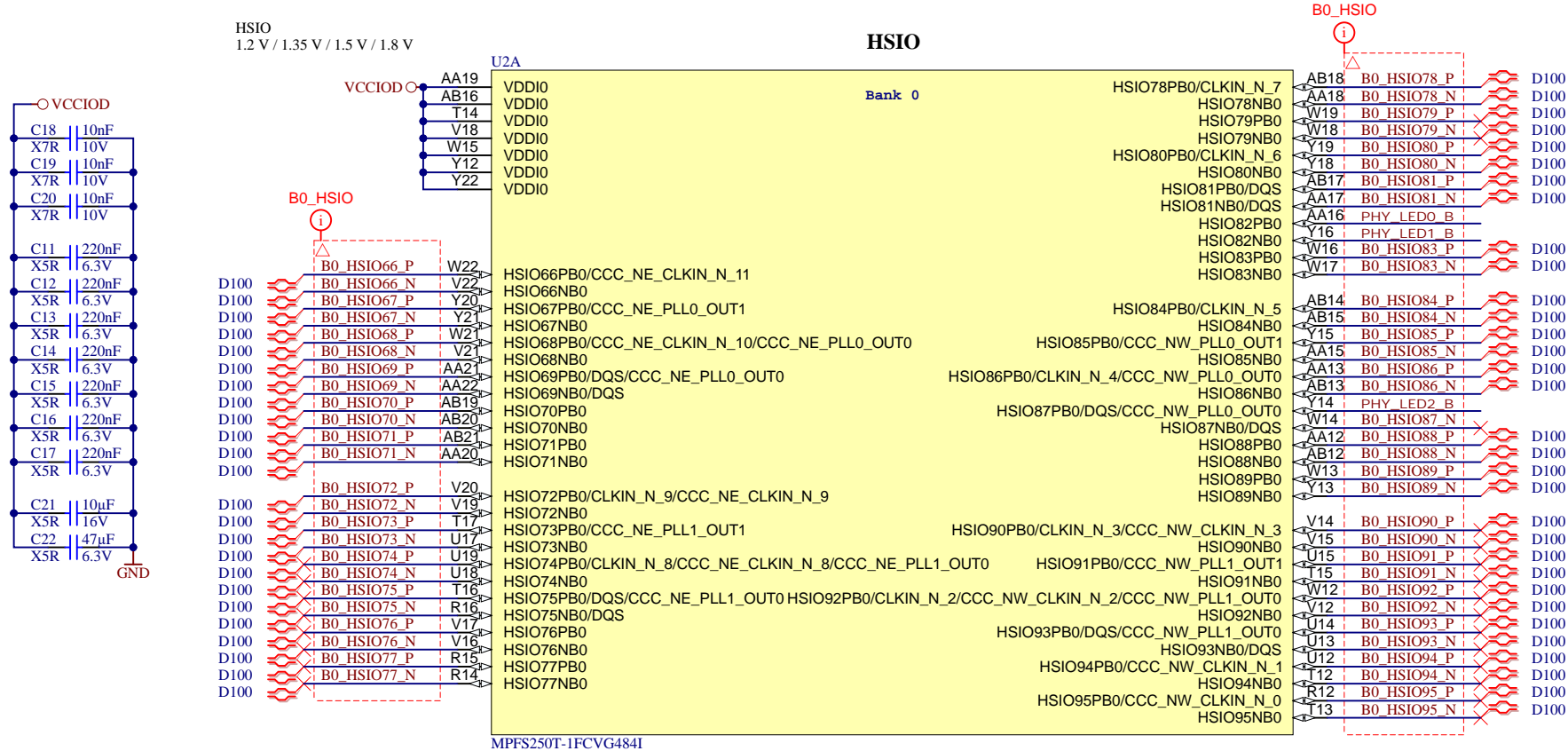
B

C

C

D

D



Title: TEM007 - FPGA1		
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Attention: Consider the I/O Glitch issues in document DS60001681A!

GPIO
1.2 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V

GPIO

A

A

B

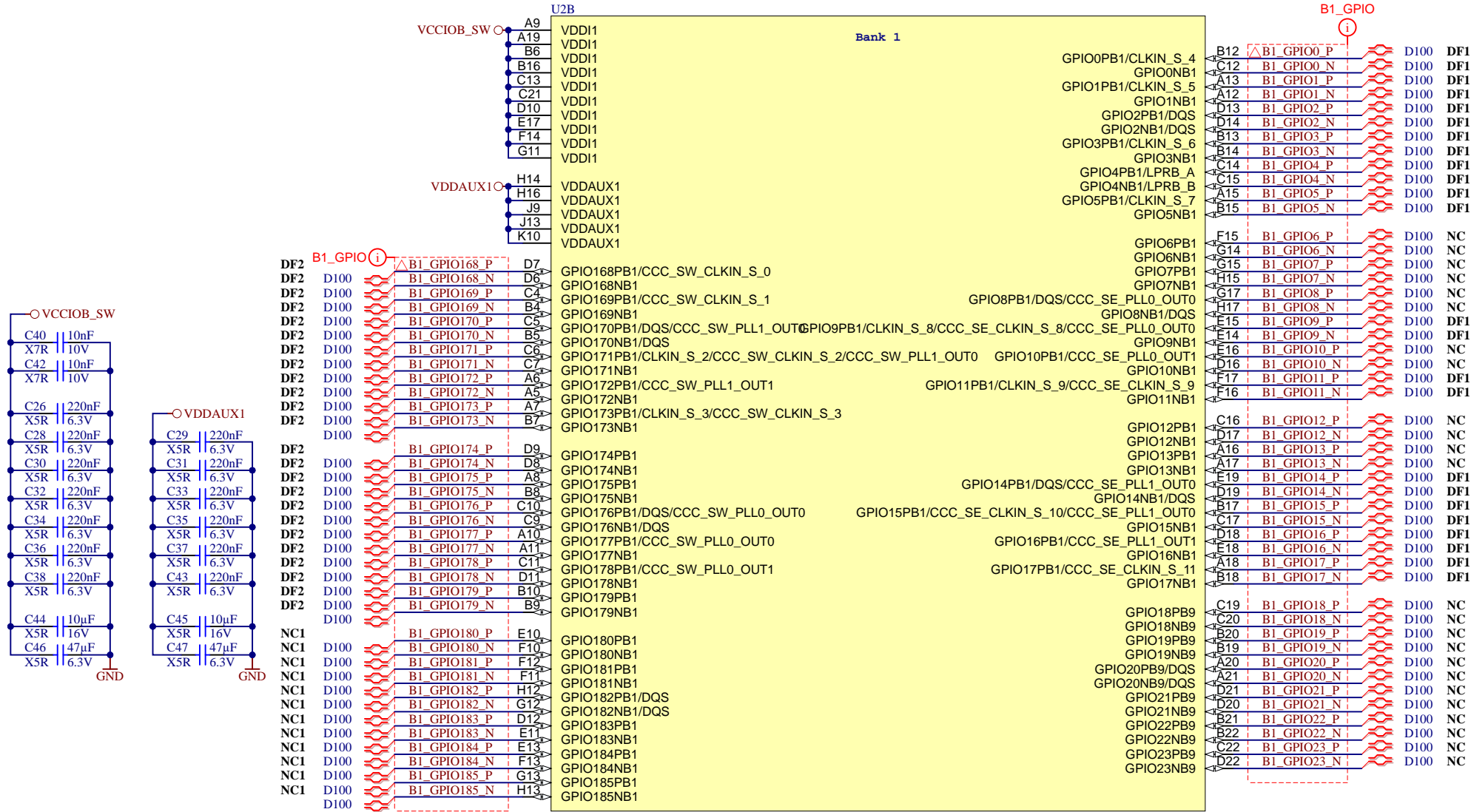
B

C

C

D

D



MPFS250T-1FCVG484I

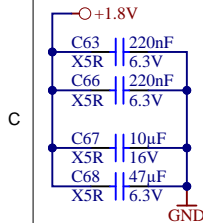
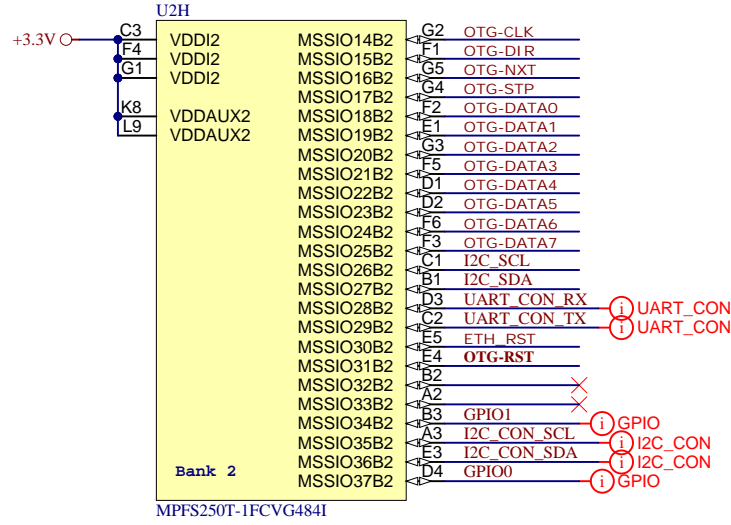
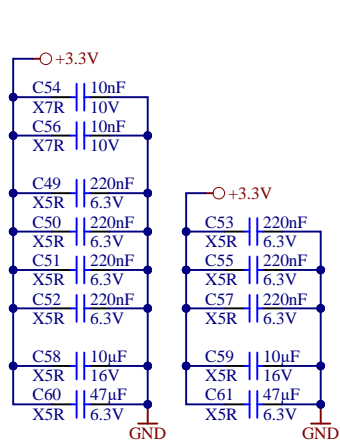
FPGA SoC Notes:

- NC Signals are not connected for MPFS025T
- NC1 Signals are not connected for MPFS025T and GPIOXX: XX differs for MPFS095T / MPFS160T / MPFS250T
- DF1 GPIOXX: XX for MPFS095T / MPFS160T / MPFS250T differs from MPFS025T
- DF2 GPIOXX: XX differs for MPFS025T / MPFS095T / MPFS160T / MPFS250T

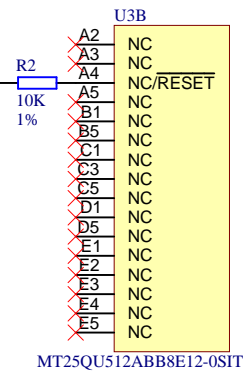
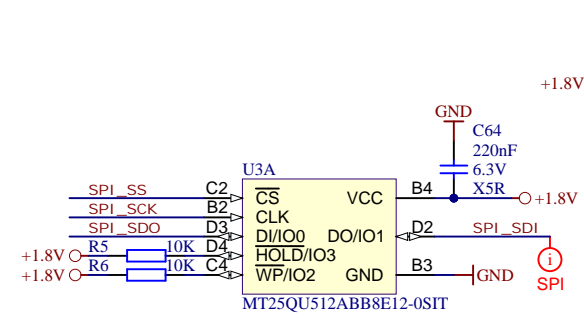
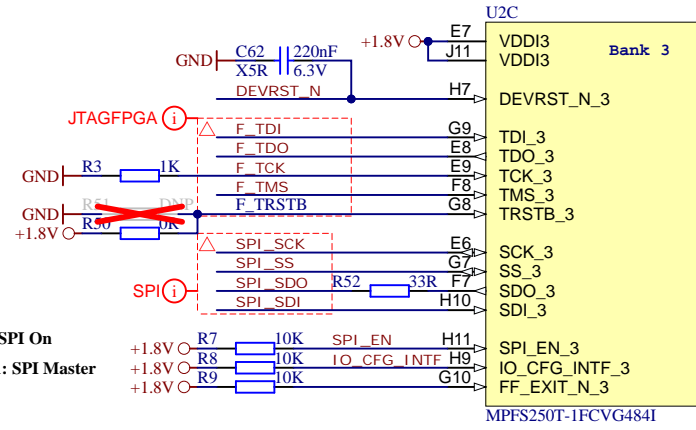



Title: TEM0007 - FPGA2		
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Attention: Consider the I/O Glitch issues in document DS60001681A!

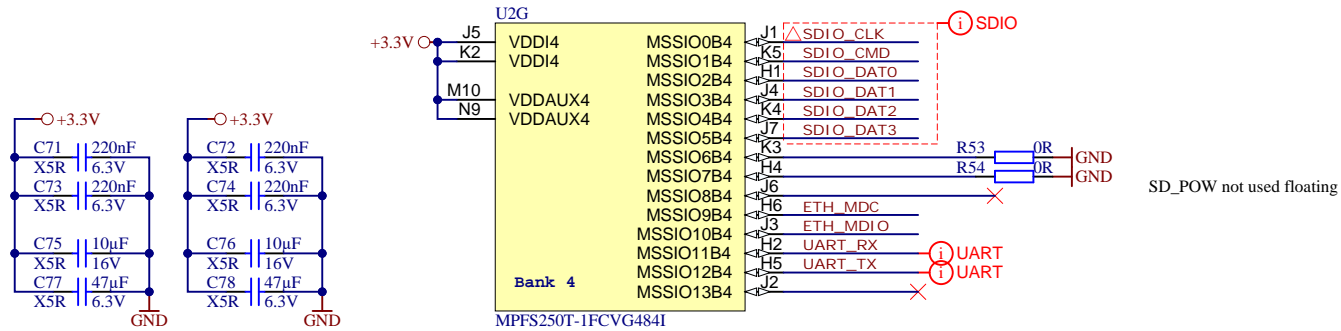


0: SPI Off 1: SPI On
0: SPI Slave 1: SPI Master

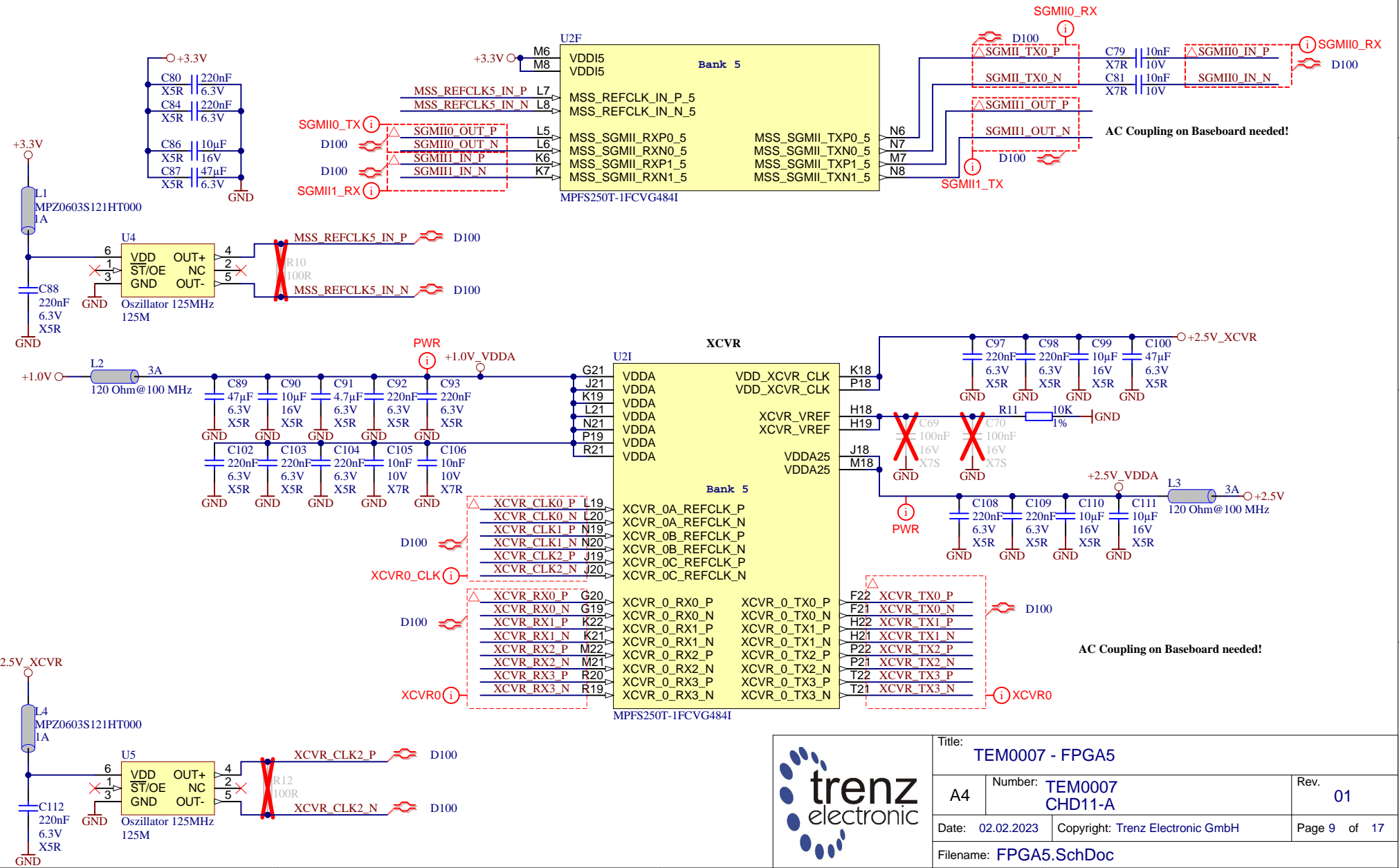


		Title: TEM0007 - FPGA3	
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Attention: Consider the I/O Glitch issues in document DS60001681A!

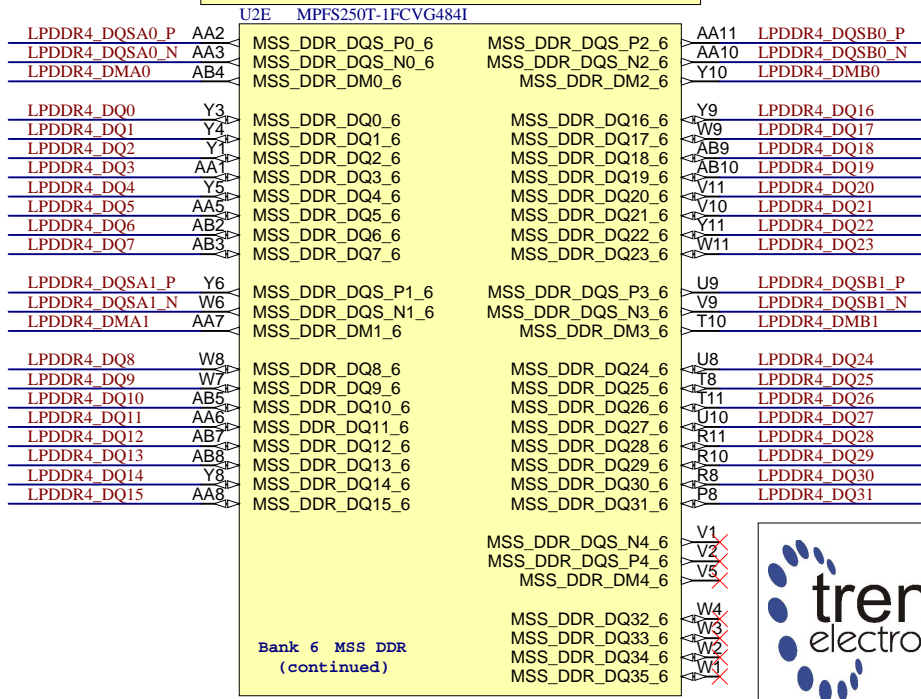
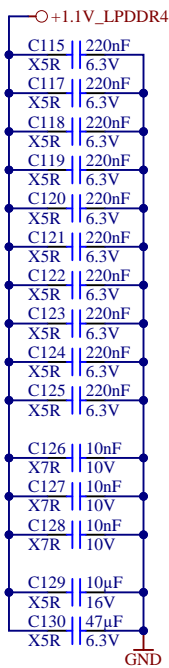
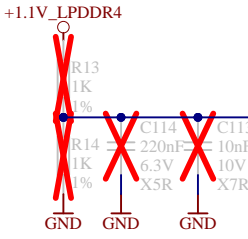
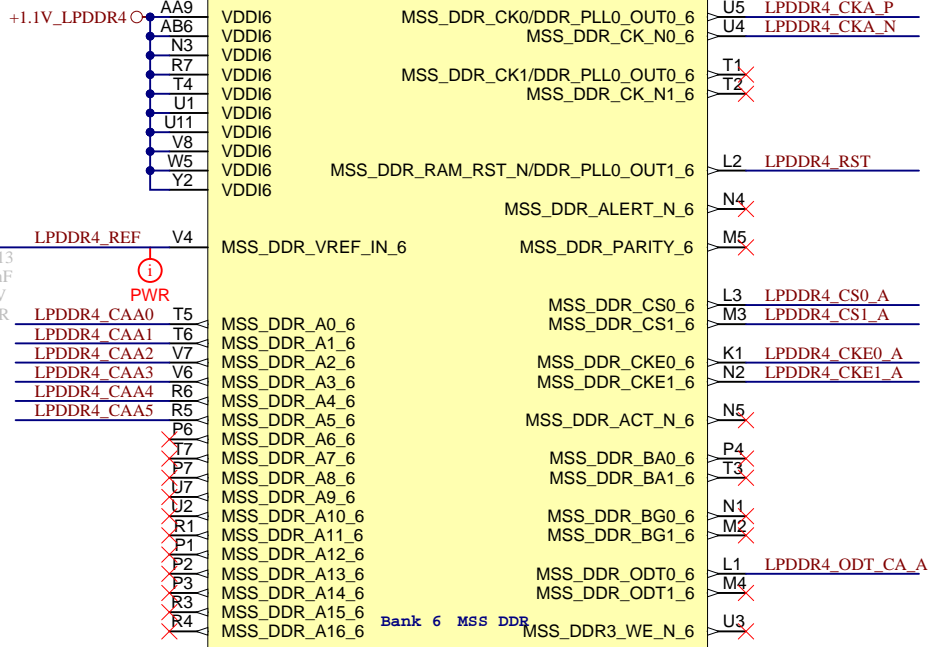


	Title: TEM0007 - FPGA4		
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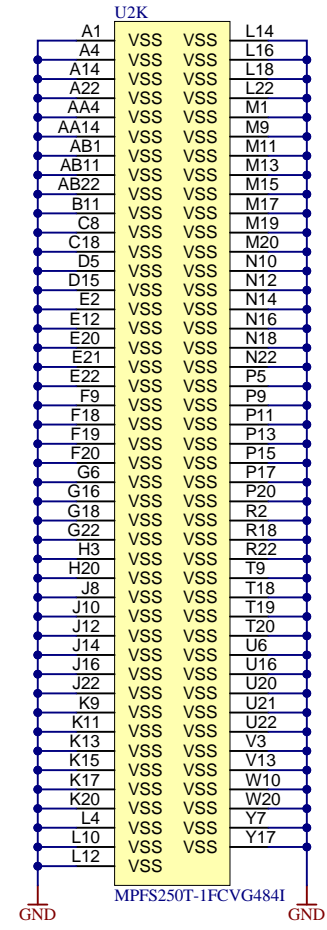
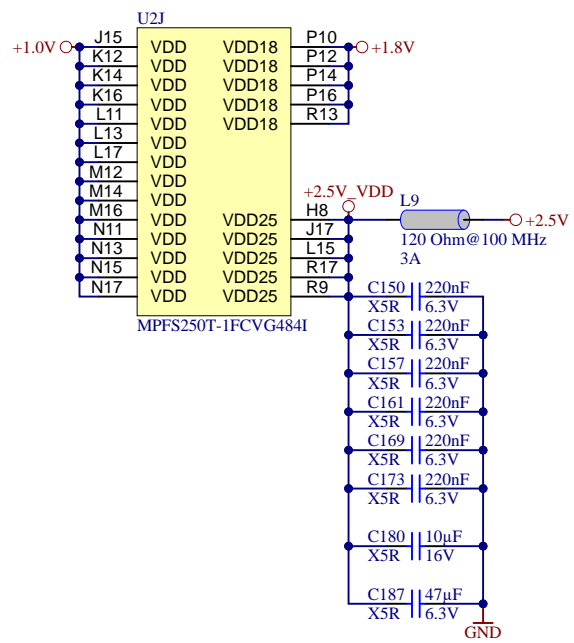
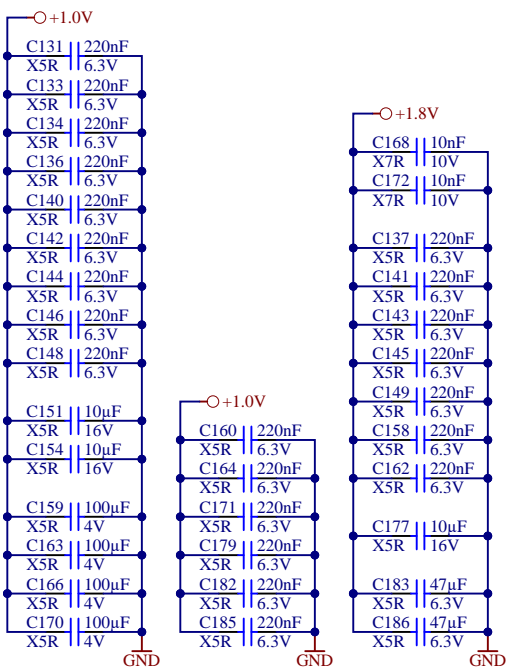


Title: TEM007 - FPGA5		
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U2D MPFS250T-1FCVG484I



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Both VDDA and VDD_XCVR_CLK supplies must be powered when any of the transceivers are used. VDD_XCVR_CLK must power on within the I/O calibration time (as specified for the device in Libero). VDDA and VDD_XCVR_CLK must both then remain powered during operation. If VDDA needs to be powered down, VDD_XCVR_CLK must also be powered down. There is no required sequence for powering up or down VDDA and VDD_XCVR_CLK.

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other I/O supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the I/O supplies of some I/O banks remain powered off).

VDD - For fabric core and transceiver/PCIe blocks.
 VDD18 - For fabric programming and RC oscillators.
 VDD25 - For corner phase-locked loop (PLLs) and on-chip non-volatile memory (sNVM).
 VDDIx - For I/O banks.
 VDDAUXx - For GPIO and HSIO banks.
 VDDA - For transceiver.
 VDDA25 - For transceiver PLLs.
 VDD_XCVR_CLK - For transceiver reference clock input buffers.



Title: TEM007 - FPGA_PWR		
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A

A

B

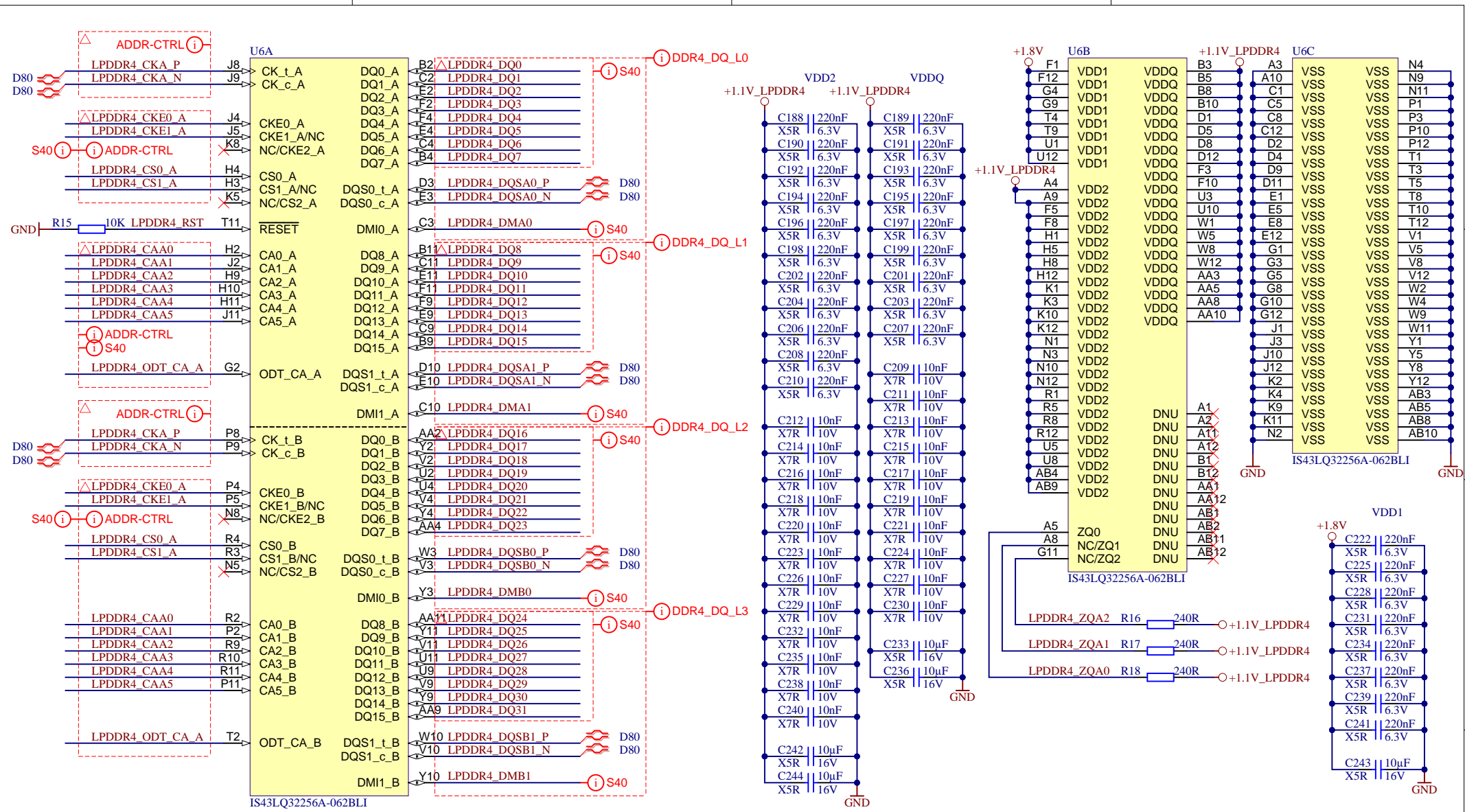
B

C

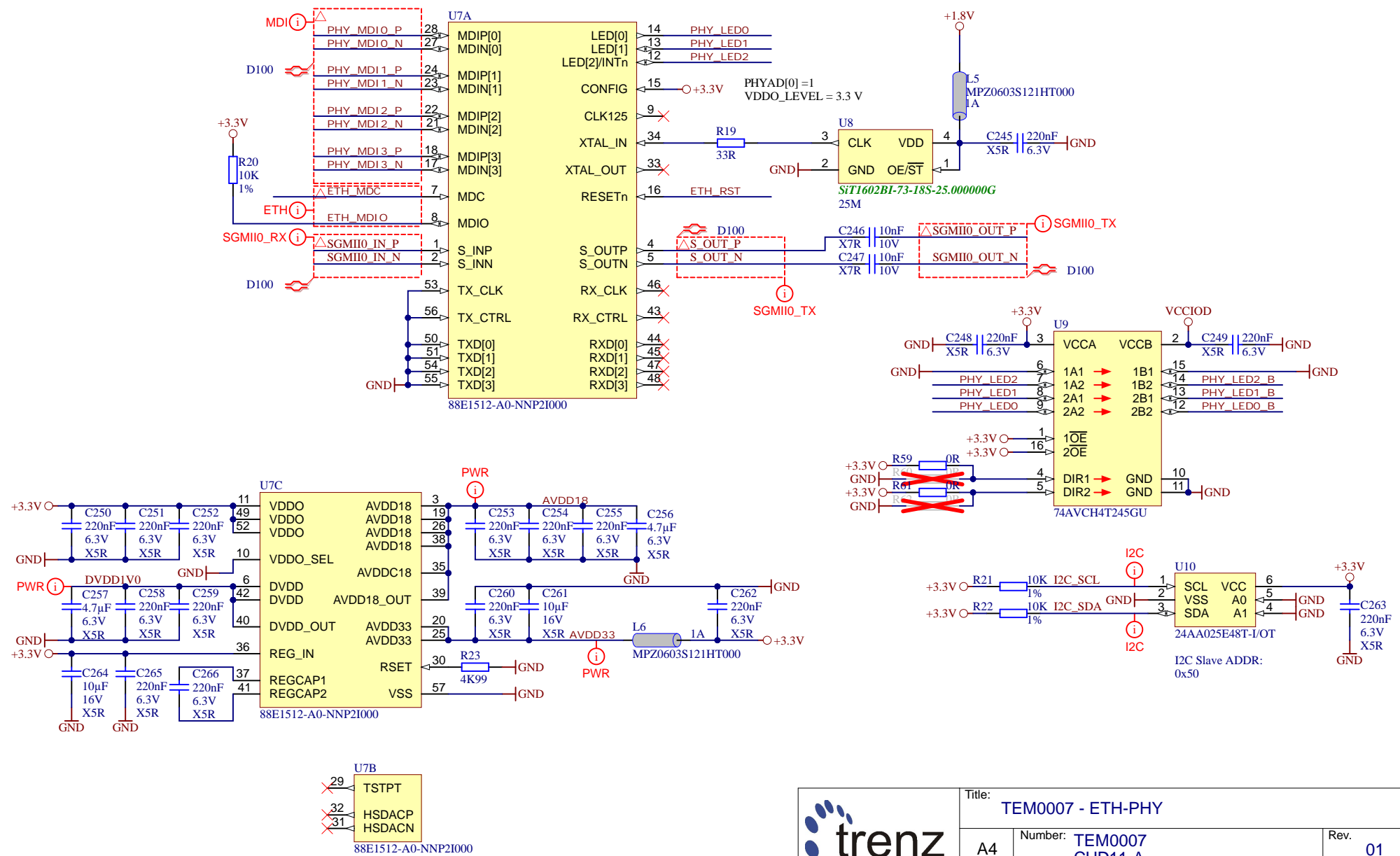
C

D

D

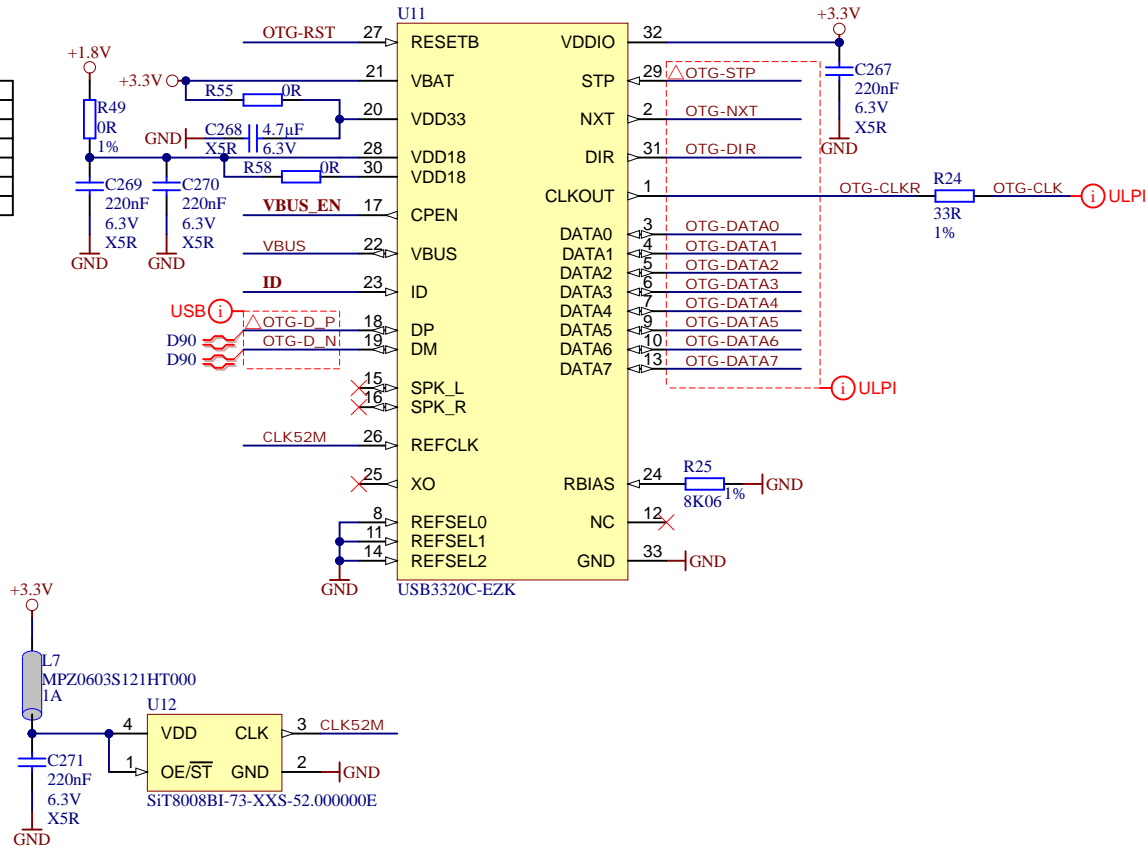


Title: TEM007 - LPDDR4		
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Title: TEM0007 - ETH-PHY		
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	USB3320:	USB3340:
R49	0R	DNP
R55	0R	DNP
R58	0R	DNP
C268	4.7 uF	1.0 uF
C269	0.1 uF	1.0 uF
C270	0.1 uF	1.0 uF



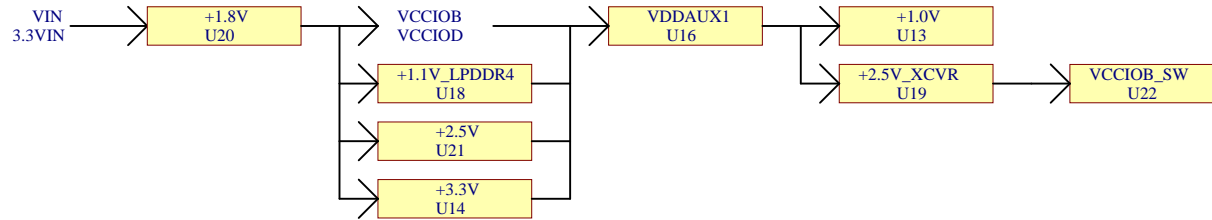
	Title: TEM0007 - USB-PHY	
	A4	Number: TEM0007 CHD11-A
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	Filename: USB-PHY.SchDoc	

Rev. 01

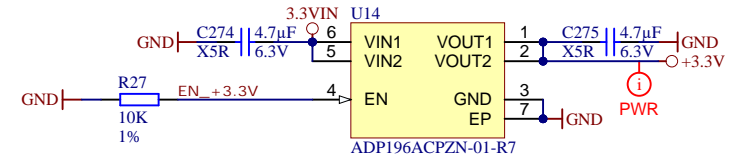
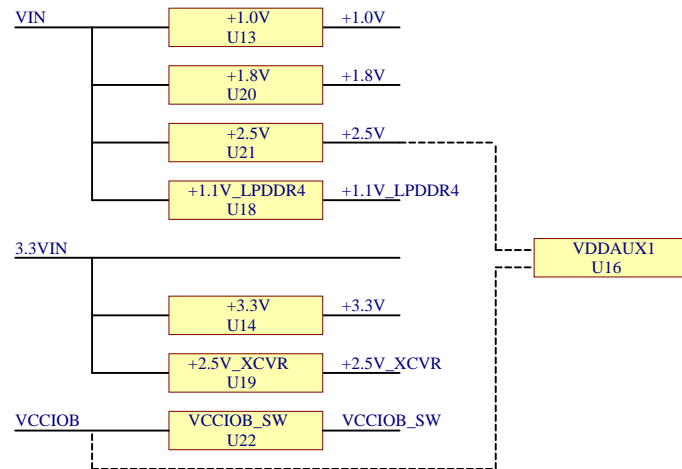
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Recommended Power Supply Sequencing

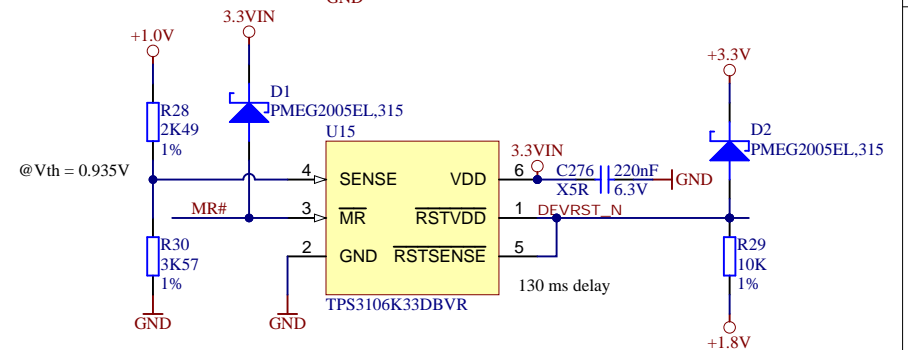
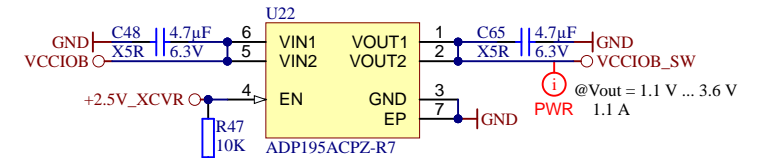
The final power sequende depends on the CPLD.



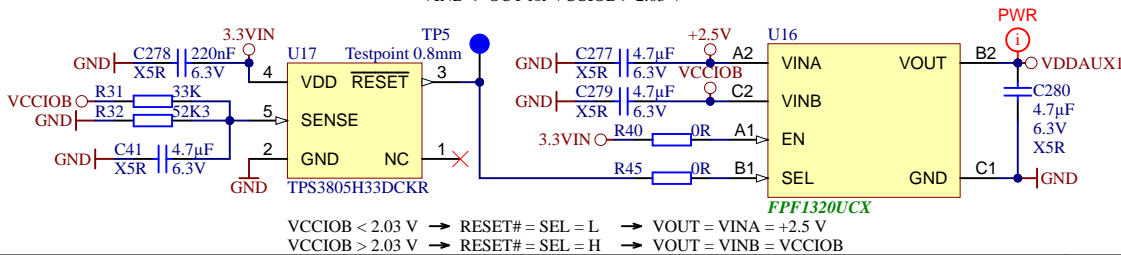
Power Supply Structure



Needed for IO Glitch Prevention!



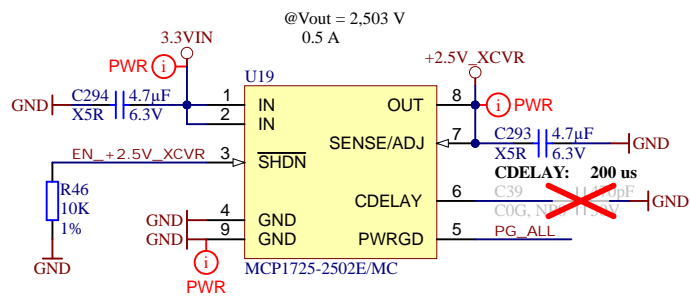
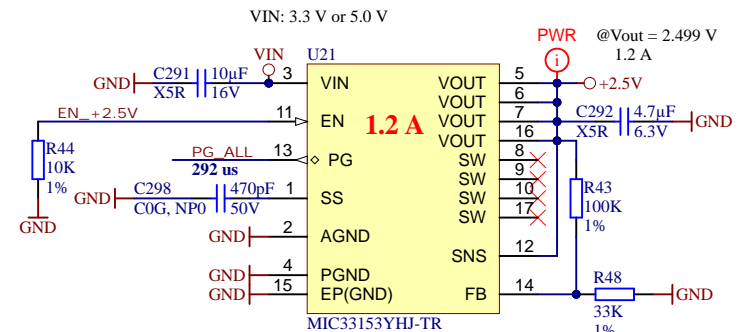
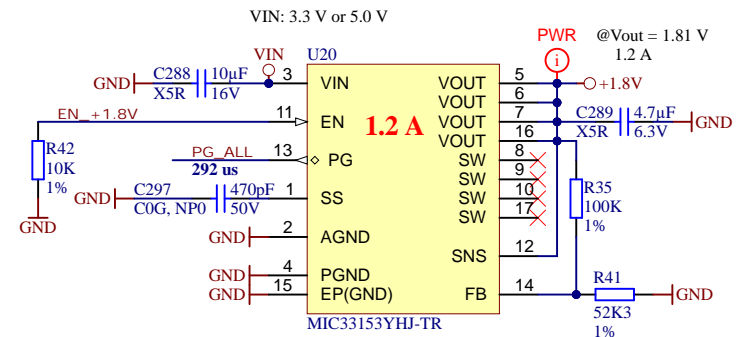
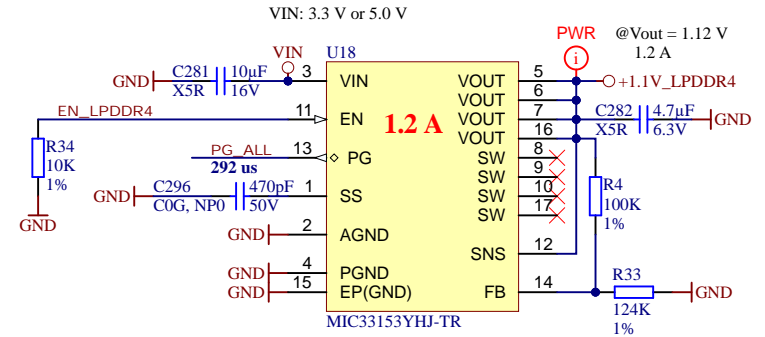
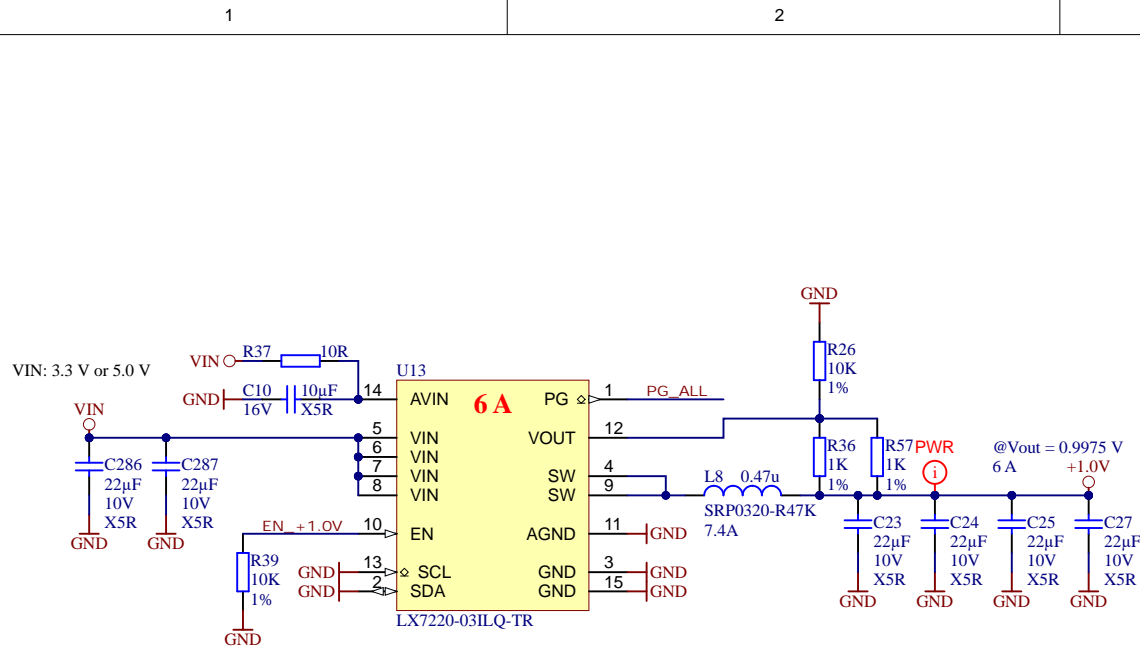
VINA -> OUT for VCCIOB < 2.03 V
VINB -> OUT for VCCIOB > 2.03 V



VCCIOB < 2.03 V -> RESET# = SEL = L -> VOUT = VINA = +2.5 V
VCCIOB > 2.03 V -> RESET# = SEL = H -> VOUT = VINB = VCCIOB



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1

2

3

4

A

A

REV	DATE	Description	
-05	2023-09-04	Initial revision 1. Changed power switch U16 from FPF1321BUCX to FPF1320UCX. 2. Updated revision history.	ED ED

B


B

C

C

D

D

			Title: TEM0007 - Revision Changes List		
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Drawn by:			Filename: Revision Changes.SchDoc		

1

2

3

4