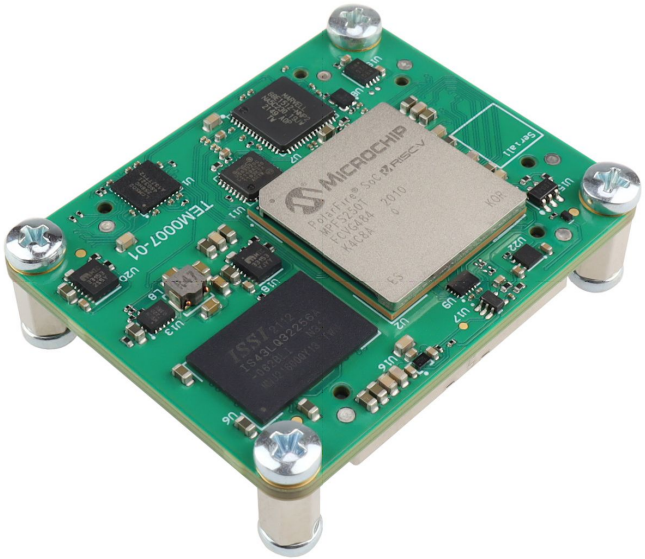
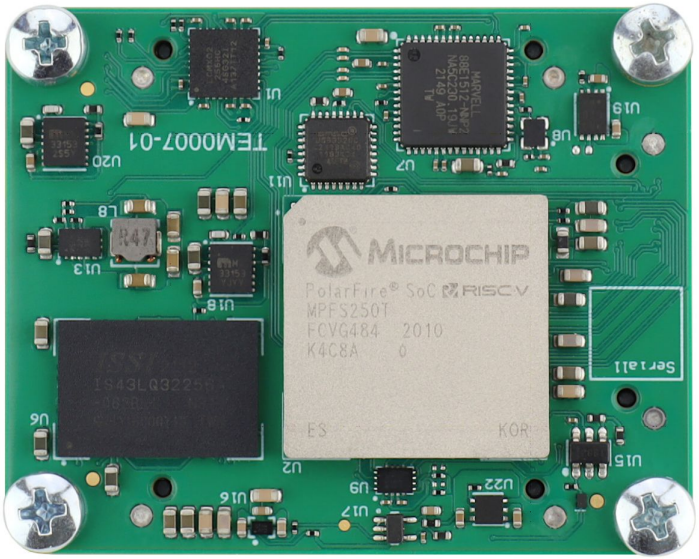
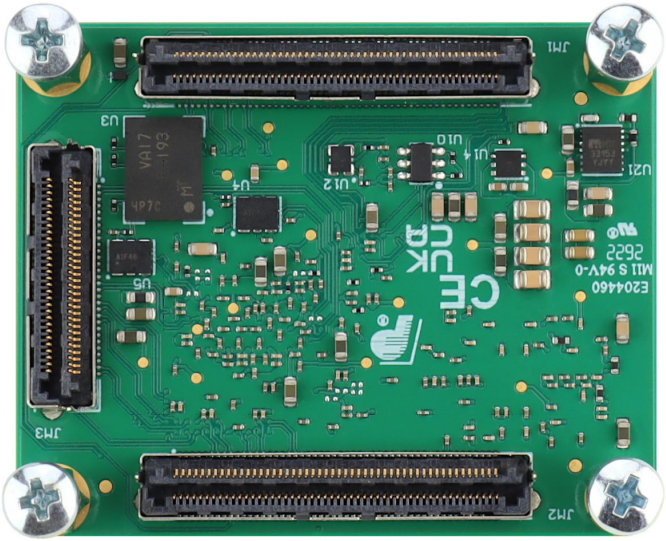






Regarding the usage of our schematics and alike documentation for Trenz module TEM0007.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TEM0007 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TEM0007 - Legal Notices		
	A4	Number: TEM0007 CHE11-A	Rev. 01
	Date: 2021-08-01	Copyright: Trenz Electronic GmbH	Page 1 of 17
	Filename: Legal Notices Modules.SchDoc		

B2B_Connector
B2B_Connector.SchDoc

CPLD
CPLD.SchDoc

FPGA1
FPGA1.SchDoc

FPGA2
FPGA2.SchDoc

FPGA3
FPGA3.SchDoc

FPGA4
FPGA4.SchDoc

FPGA5
FPGA5.SchDoc

FPGA6
FPGA6.SchDoc

FPGA_PWR
FPGA_PWR.SchDoc

LPDDR4
LPDDR4.SchDoc

ETH-PHY
ETH-PHY.SchDoc

USB-PHY
USB-PHY.SchDoc

POWER1
POWER1.SchDoc

POWER2
POWER2.SchDoc

UKCA1

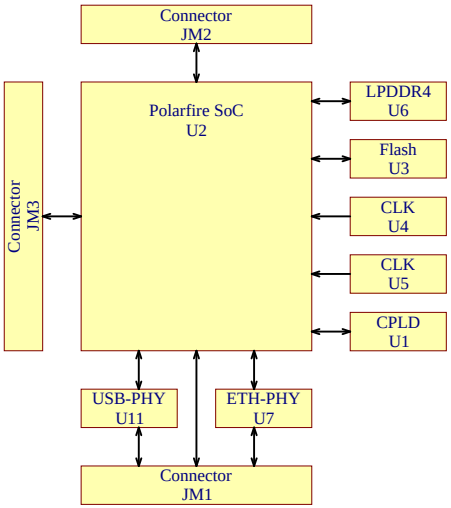
UKCA Logo on Top Overlay

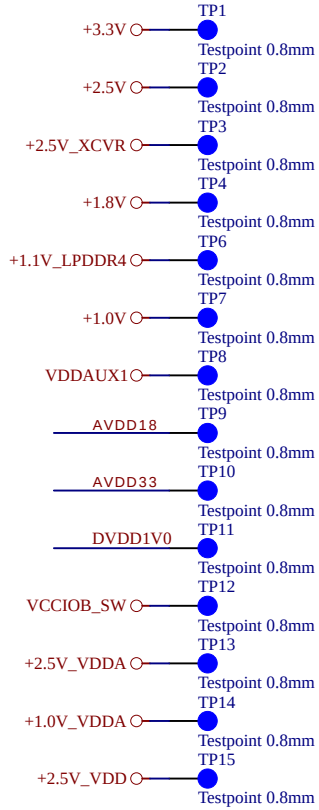
UKCA-TOPOVERLAY

CE1

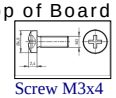
CE Logo on Top Overlay

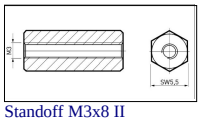
CE-TOPOVERLAY

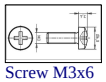


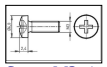


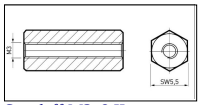
Top of Board

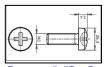

Screw M3x4

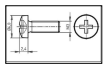

Standoff M3x8 II

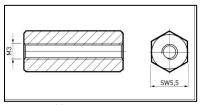

Screw M3x6

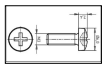

Screw M3x4

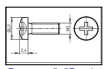

Standoff M3x8 II

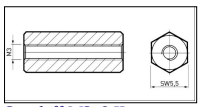

Screw M3x6

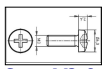

Screw M3x4


Standoff M3x8 II

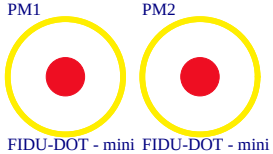

Screw M3x6


Screw M3x4

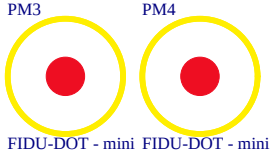

Standoff M3x8 II


Screw M3x6

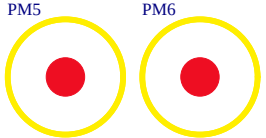
PM1 PM2


FIDU-DOT - mini FIDU-DOT - mini

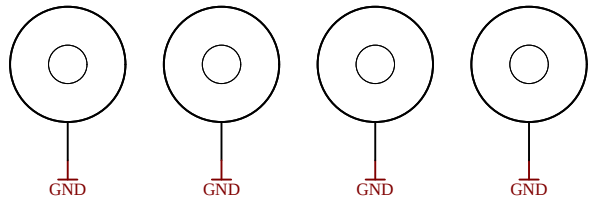
PM3 PM4


FIDU-DOT - mini FIDU-DOT - mini

PM5 PM6


FIDU-DOT - mini FIDU-DOT - mini

Serial1
Serial
Serialnumber 6,3 x 6.3mm

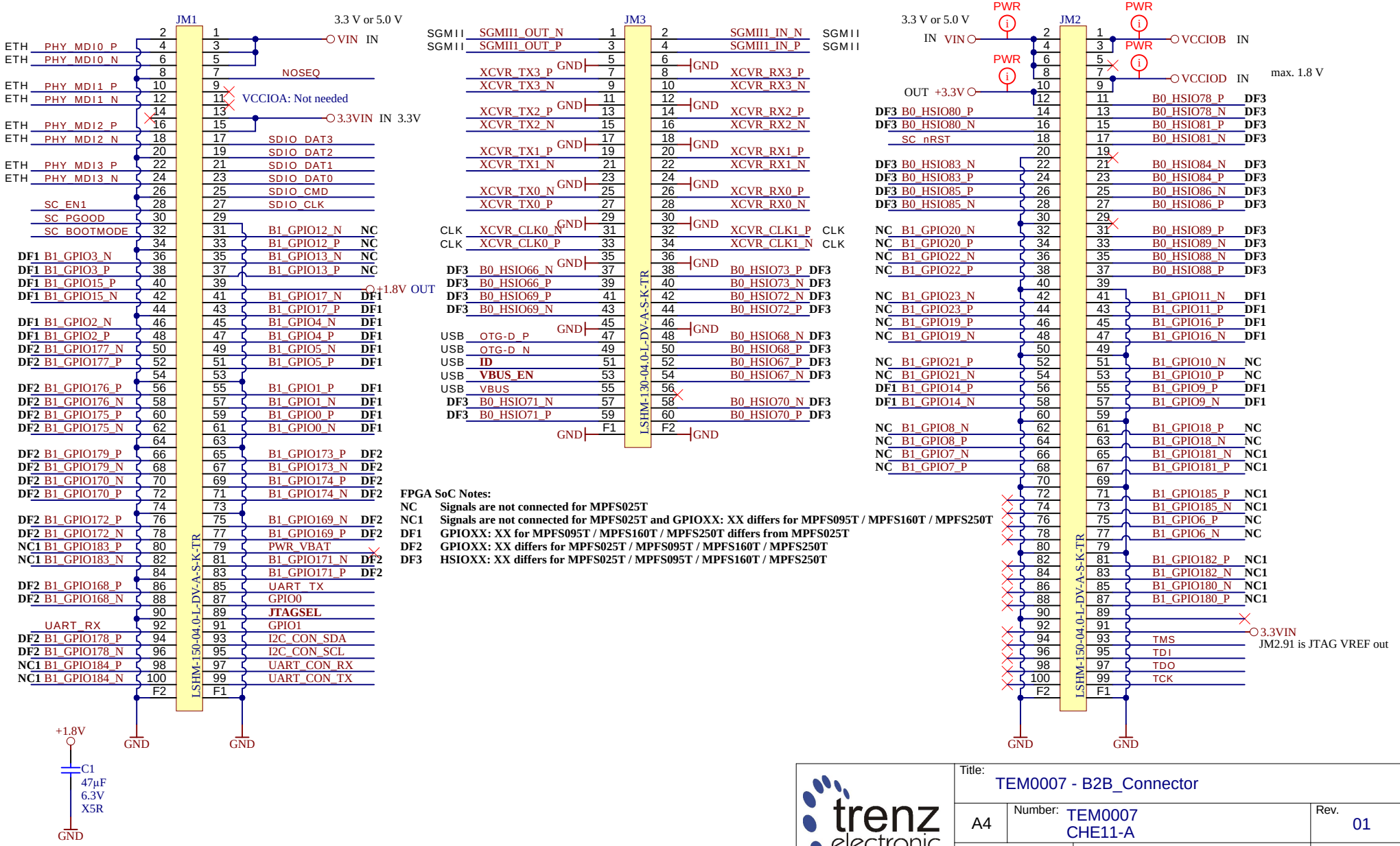


Title: TEM0007			
A4	Number: TEM0007 CHE11-A		Rev. 01
Date: 21.06.2022	Copyright: Trenz Electronic GmbH		Page 2 of 17
Filename: TEM0007.SchDoc			

SD ETH
B1: 48 IO, 24 Differential Pairs, VCCIOB Fixed VCCIO
B4: 8 GPIO, 3.3 V Fixed VCCIO

USB MGT SGMII
B1: 16 IO, 8 Differential Pairs, VCCIOD Fixed VCCIO

JTAG: 3.3V Levels
B1: 36 IO, 18 Differential Pairs, VCCIOB Fixed VCCIO
B0: 18 IO, 9 Differential Pairs, VCCIOD Fixed VCCIO



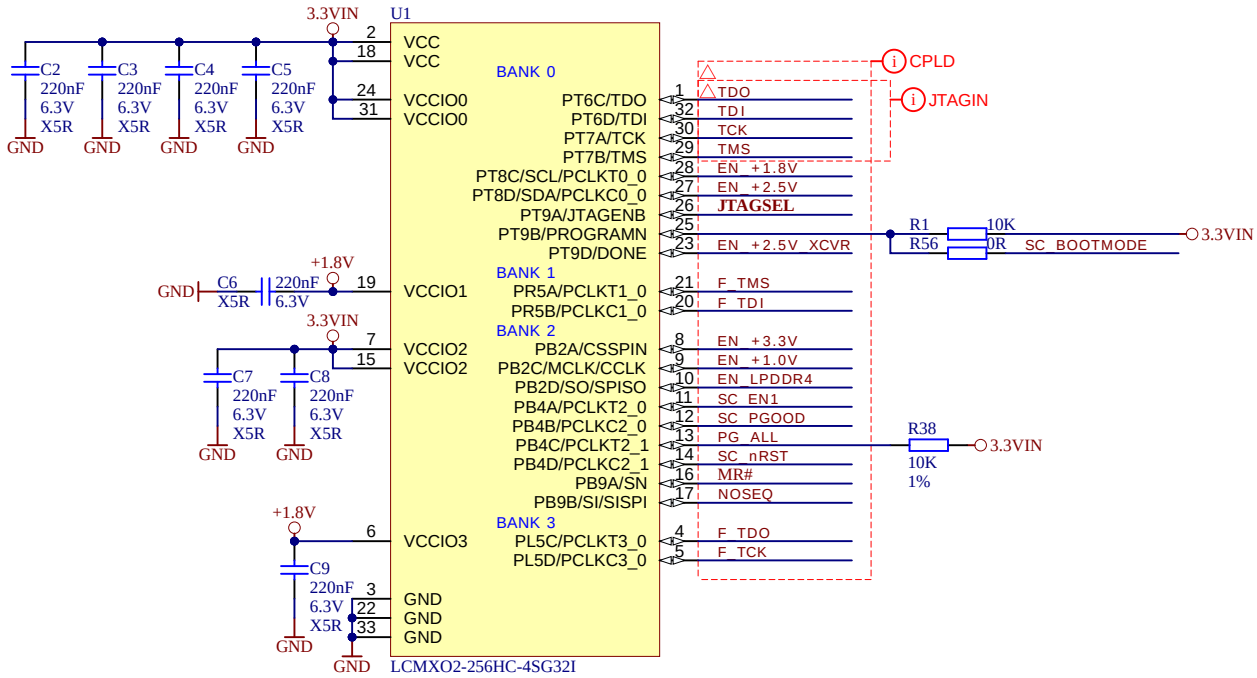
FPGA SoC Notes:

NC	**Signals are not connected for MPFS025T**
NC1	**Signals are not connected for MPFS025T and GPIOXX: XX differs for MPFS095T / MPFS160T / MPFS250T**
DF1	**GPIOXX: XX for MPFS095T / MPFS160T / MPFS250T differs from MPFS025T**
DF2	**GPIOXX: XX differs for MPFS025T / MPFS095T / MPFS160T / MPFS250T**
DF3	**HSIOXX: XX differs for MPFS025T / MPFS095T / MPFS160T / MPFS250T**

Attention: Consider the I/O Glitch issues in document DS60001681A!

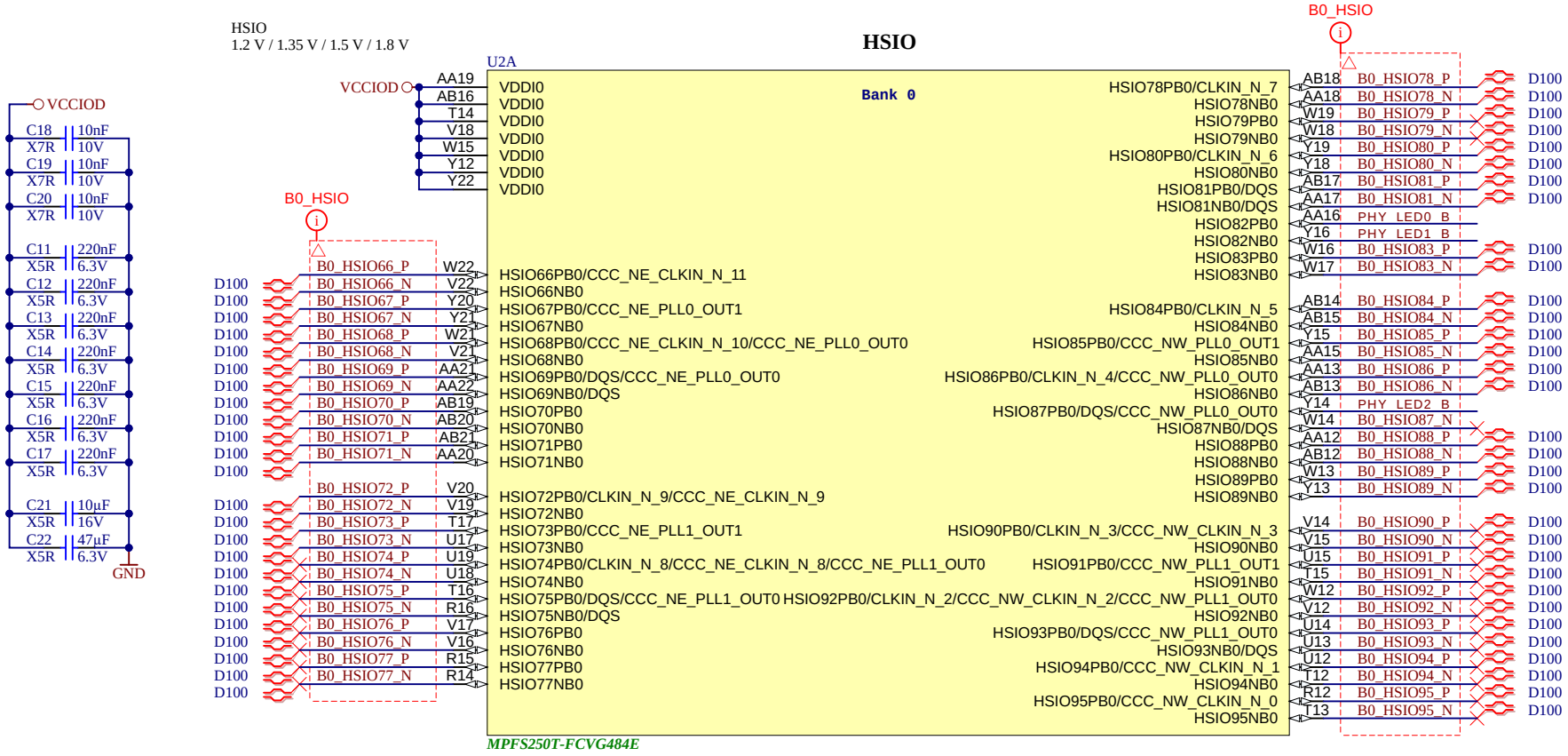
trenz electronic

Title: TEM0007 - B2B_Connector		
A4	Number: TEM0007 CHE11-A	Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH	Page 3 of 17
Filename: B2B_Connector.SchDoc		



trenz electronic	Title: TEM0007 - CPLD		
A4	Number: TEM0007 CHE11-A		Rev. 01
Date: 21.06.2022	Copyright: Trenz Electronic GmbH		Page 4 of 17
Filename: CPLD.SchDoc			

Attention:
1.) Consider the I/O Glitch issues in document DS60001681A!
2.) Using LVDS in HSIO bank needs an externally 100 Ohm resistor according to DS60001681A!



HSIOXX: XX differs for MPFS250T / MPFS095T / MPFS160T / MPFS025T

trenz electronic	Title: TEM0007 - FPGA1	
A4	Number: TEM0007 CHE11-A	Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH	Page 5 of 17
	Filename: FPGA1.SchDoc	

Attention: Consider the I/O Glitch issues in document DS60001681A!

GPIO
1.2 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V

GPIO

U2B

Bank 1

VCCIOB_SW
VDDAUX1

MPFS250T-FCVG484E

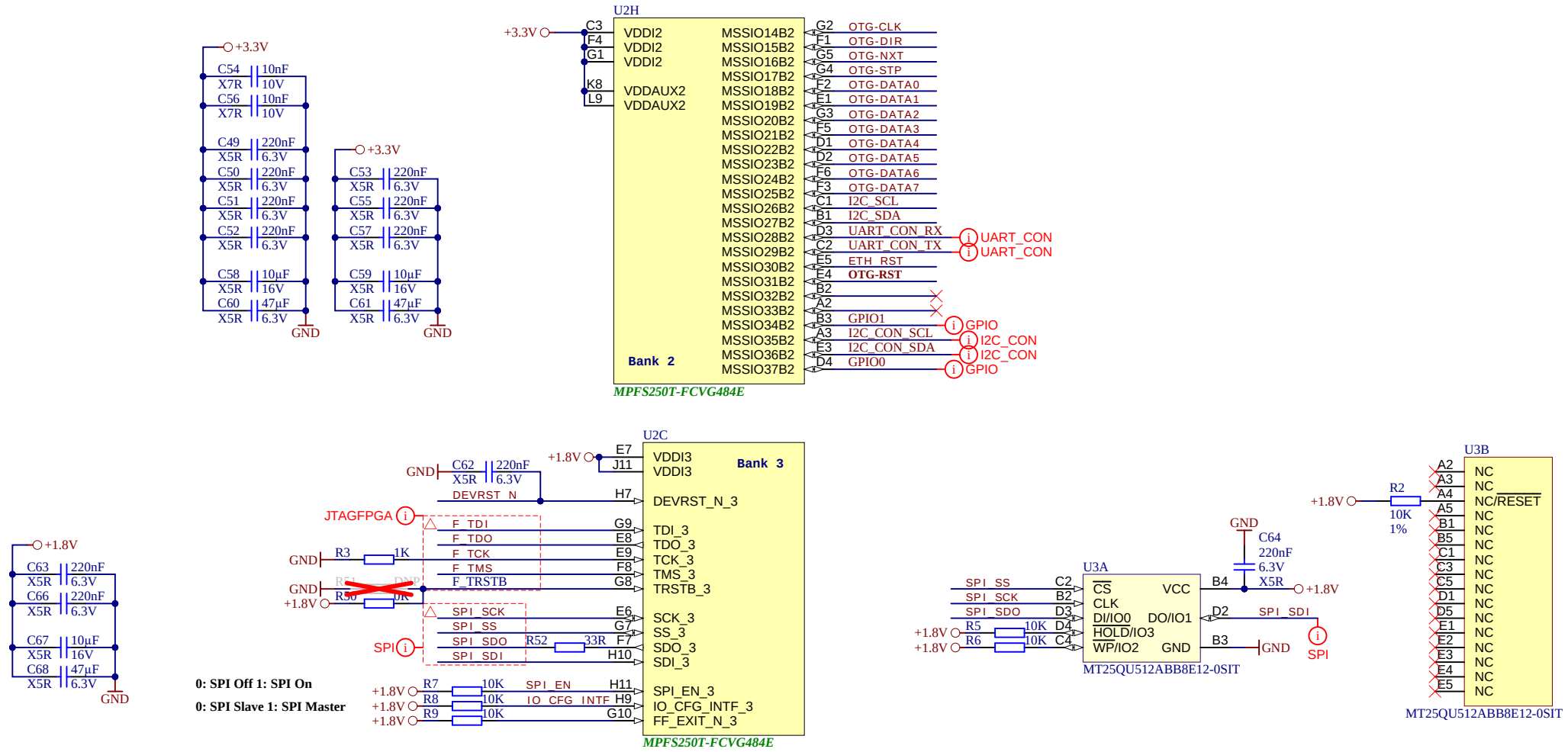
FPGA SoC Notes:

NC	**Signals are not connected for MPFS025T**
NC1	**Signals are not connected for MPFS025T and GPIOXX: XX differs for MPFS095T / MPFS160T / MPFS250T**
DF1	**GPIOXX: XX for MPFS095T / MPFS160T / MPFS250T differs from MPFS025T**
DF2	**GPIOXX: XX differs for MPFS025T / MPFS095T / MPFS160T / MPFS250T**

trenz electronic

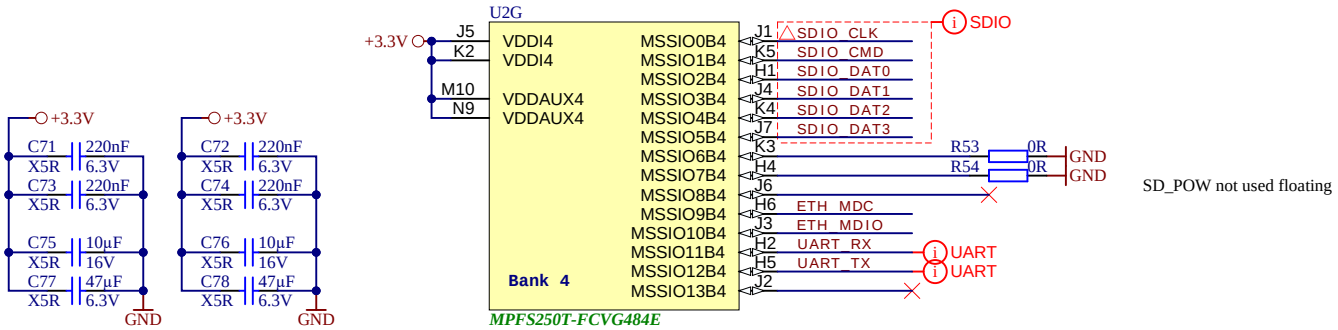
Title: TEM0007 - FPGA2			
A4	Number: TEM0007 CHE11-A		Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH		Page 6 of 17
Filename: FPGA2.SchDoc			

Attention: Consider the I/O Glitch issues in document DS60001681A!



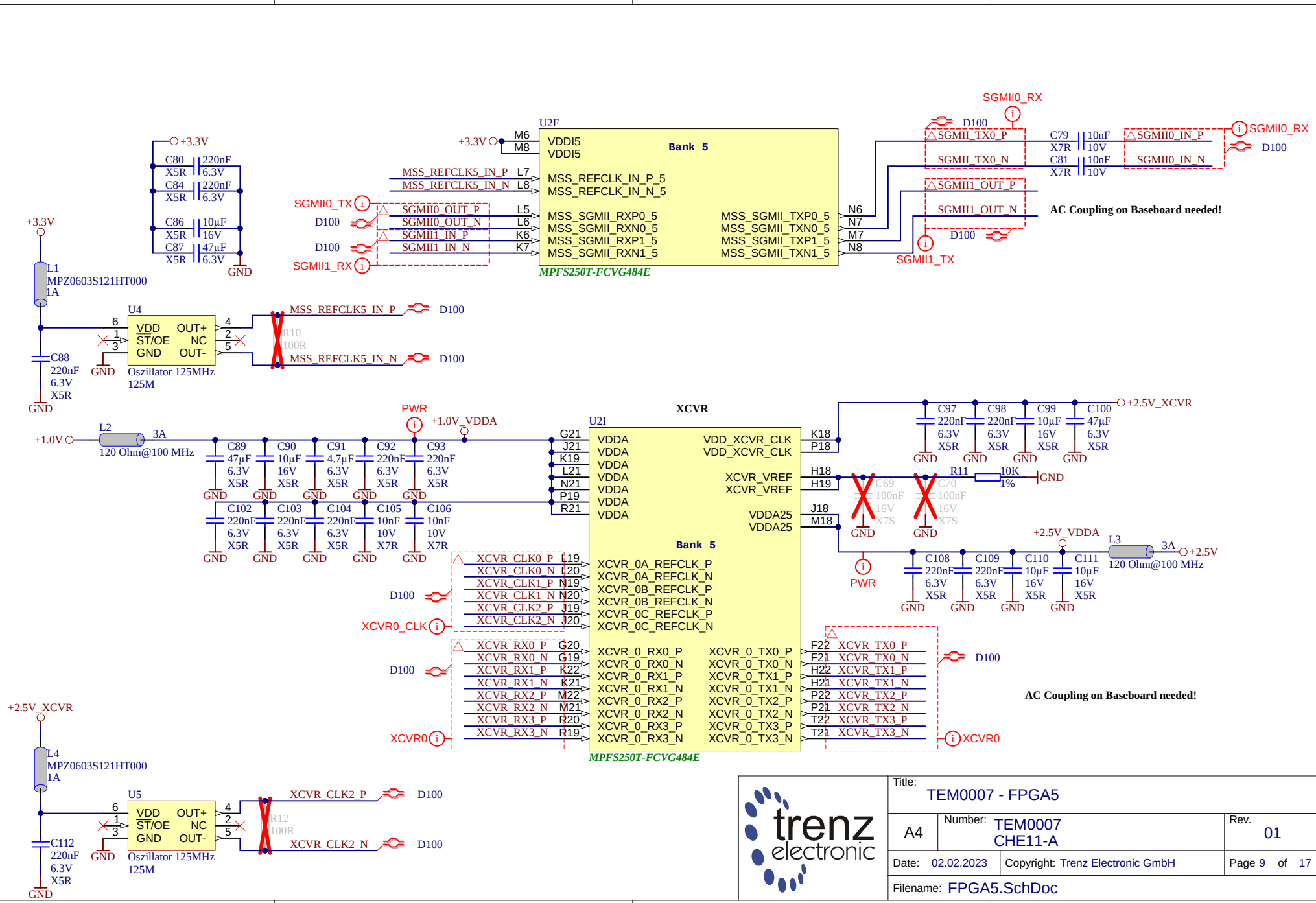
trenz electronic	Title: TEM0007 - FPGA3		
A4	Number: TEM0007 CHE11-A		Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH		Page 7 of 17
Filename: FPGA3.SchDoc			

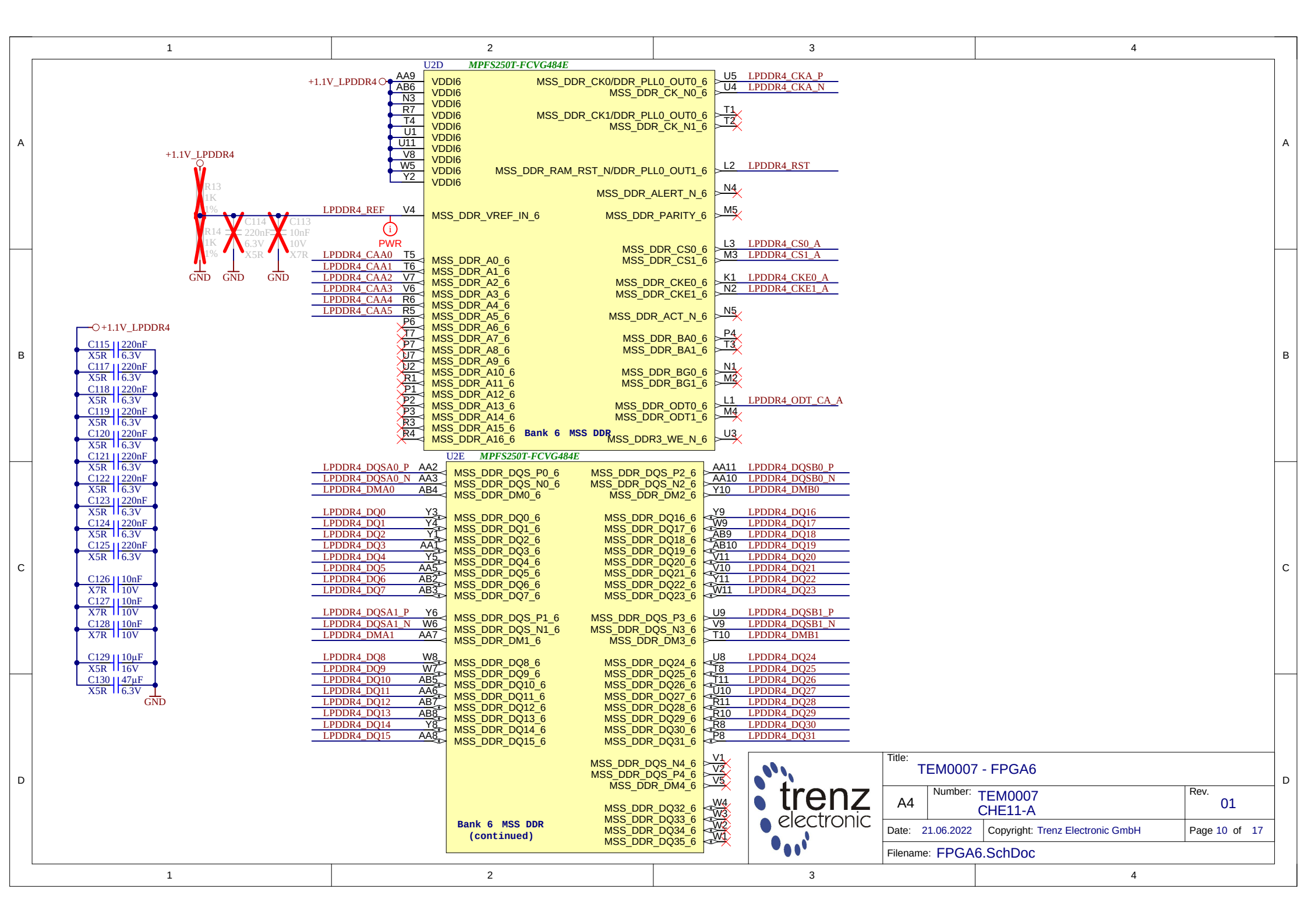
Attention: Consider the I/O Glitch issues in document DS60001681A!

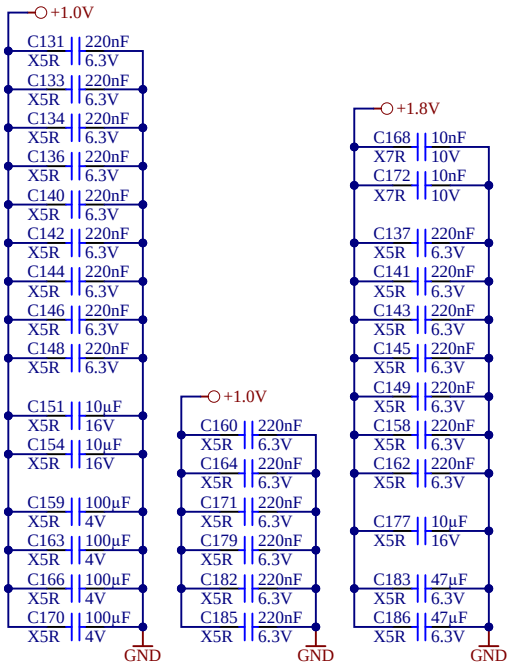


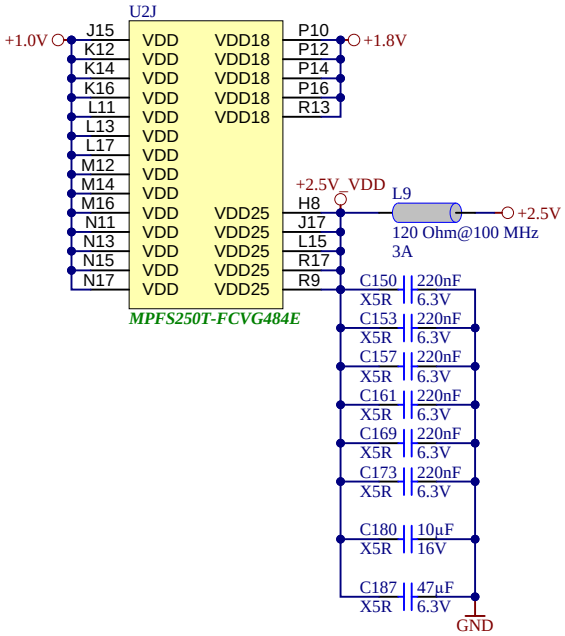
SD_POW not used floating

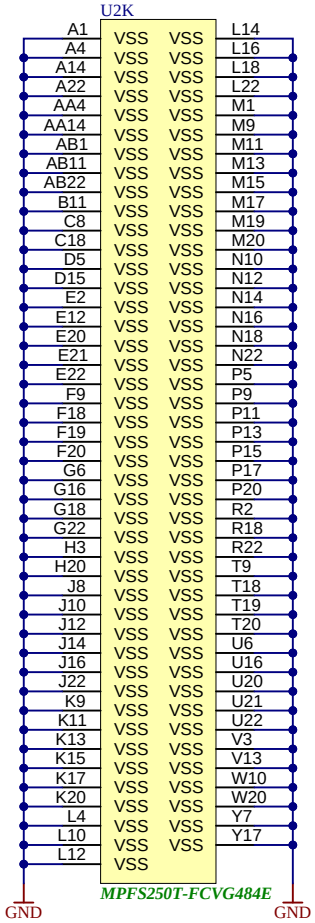
trenz electronic	Title: TEM0007 - FPGA4		
A4	Number: TEM0007 CHE11-A		Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH		Page 8 of 17
Filename: FPGA4.SchDoc			


U2F
MPFS250T-FCVG484E
Bank 5
SGMII0_RX
SGMII0_TX
SGMII1_RX
SGMII1_TX
AC Coupling on Baseboard needed!
XCVR
U2I
MPFS250T-FCVG484E
Bank 5
XCVR0_CLK
XCVR0
AC Coupling on Baseboard needed!
U4
Oszillator 125MHz
125M
U5
Oszillator 125MHz
125M
L1
MPZ0603S121HT000
1A
L2
120 Ohm@100 MHz
3A
L3
120 Ohm@100 MHz
3A
L4
MPZ0603S121HT000
1A
+3.3V
+1.0V
+1.0V_VDDA
+2.5V_XCVR
+2.5V_VDDA
+2.5V
GND
PWR
D100
MSS_REFCLK5_IN_P
MSS_REFCLK5_IN_N
XCVR_CLK2_P
XCVR_CLK2_N
R10
100R
R12
100R
R11
10K
1%
C69
100nF
16V
X7S
C70
100nF
16V
X7S
trenz electronic
Title: TEM0007 - FPGA5
A4
Number: TEM0007 CHE11-A
Rev. 01
Date: 02.02.2023
Copyright: Trenz Electronic GmbH
Page 9 of 17
Filename: FPGA5.SchDoc


U2D
MPFS250T-FCVG484E
+1.1V_LPDDR4
VDDI6
MSS_DDR_CK0/DDR_PLL0_OUT0_6
MSS_DDR_CK_N0_6
MSS_DDR_CK1/DDR_PLL0_OUT0_6
MSS_DDR_CK_N1_6
MSS_DDR_RAM_RST_N/DDR_PLL0_OUT1_6
MSS_DDR_ALERT_N_6
MSS_DDR_VREF_IN_6
MSS_DDR_PARITY_6
MSS_DDR_CS0_6
MSS_DDR_CS1_6
MSS_DDR_CKE0_6
MSS_DDR_CKE1_6
MSS_DDR_ACT_N_6
MSS_DDR_BA0_6
MSS_DDR_BA1_6
MSS_DDR_BG0_6
MSS_DDR_BG1_6
MSS_DDR_ODT0_6
MSS_DDR_ODT1_6
MSS_DDR3_WE_N_6
MSS_DDR_A0_6
MSS_DDR_A1_6
MSS_DDR_A2_6
MSS_DDR_A3_6
MSS_DDR_A4_6
MSS_DDR_A5_6
MSS_DDR_A6_6
MSS_DDR_A7_6
MSS_DDR_A8_6
MSS_DDR_A9_6
MSS_DDR_A10_6
MSS_DDR_A11_6
MSS_DDR_A12_6
MSS_DDR_A13_6
MSS_DDR_A14_6
MSS_DDR_A15_6
MSS_DDR_A16_6
Bank 6 MSS DDR
LPDDR4_CKA_P
LPDDR4_CKA_N
LPDDR4_RST
LPDDR4_CS0_A
LPDDR4_CS1_A
LPDDR4_CKE0_A
LPDDR4_CKE1_A
LPDDR4_ODT_CA_A
LPDDR4_REF
LPDDR4_CAA0
LPDDR4_CAA1
LPDDR4_CAA2
LPDDR4_CAA3
LPDDR4_CAA4
LPDDR4_CAA5
PWR
R13 1K 1%
R14 1K 1%
C114 220nF 6.3V X5R
C113 10nF 10V X7R
GND
U2E
MPFS250T-FCVG484E
MSS_DDR_DQS_P0_6
MSS_DDR_DQS_N0_6
MSS_DDR_DM0_6
MSS_DDR_DQS_P1_6
MSS_DDR_DQS_N1_6
MSS_DDR_DM1_6
MSS_DDR_DQS_P2_6
MSS_DDR_DQS_N2_6
MSS_DDR_DM2_6
MSS_DDR_DQS_P3_6
MSS_DDR_DQS_N3_6
MSS_DDR_DM3_6
MSS_DDR_DQS_N4_6
MSS_DDR_DQS_P4_6
MSS_DDR_DM4_6
MSS_DDR_DQ0_6
MSS_DDR_DQ1_6
MSS_DDR_DQ2_6
MSS_DDR_DQ3_6
MSS_DDR_DQ4_6
MSS_DDR_DQ5_6
MSS_DDR_DQ6_6
MSS_DDR_DQ7_6
MSS_DDR_DQ8_6
MSS_DDR_DQ9_6
MSS_DDR_DQ10_6
MSS_DDR_DQ11_6
MSS_DDR_DQ12_6
MSS_DDR_DQ13_6
MSS_DDR_DQ14_6
MSS_DDR_DQ15_6
MSS_DDR_DQ16_6
MSS_DDR_DQ17_6
MSS_DDR_DQ18_6
MSS_DDR_DQ19_6
MSS_DDR_DQ20_6
MSS_DDR_DQ21_6
MSS_DDR_DQ22_6
MSS_DDR_DQ23_6
MSS_DDR_DQ24_6
MSS_DDR_DQ25_6
MSS_DDR_DQ26_6
MSS_DDR_DQ27_6
MSS_DDR_DQ28_6
MSS_DDR_DQ29_6
MSS_DDR_DQ30_6
MSS_DDR_DQ31_6
MSS_DDR_DQ32_6
MSS_DDR_DQ33_6
MSS_DDR_DQ34_6
MSS_DDR_DQ35_6
Bank 6 MSS DDR (continued)
LPDDR4_DQSA0_P
LPDDR4_DQSA0_N
LPDDR4_DMA0
LPDDR4_DQSA1_P
LPDDR4_DQSA1_N
LPDDR4_DMA1
LPDDR4_DQSB0_P
LPDDR4_DQSB0_N
LPDDR4_DMB0
LPDDR4_DQSB1_P
LPDDR4_DQSB1_N
LPDDR4_DMB1
LPDDR4_DQ0
LPDDR4_DQ1
LPDDR4_DQ2
LPDDR4_DQ3
LPDDR4_DQ4
LPDDR4_DQ5
LPDDR4_DQ6
LPDDR4_DQ7
LPDDR4_DQ8
LPDDR4_DQ9
LPDDR4_DQ10
LPDDR4_DQ11
LPDDR4_DQ12
LPDDR4_DQ13
LPDDR4_DQ14
LPDDR4_DQ15
LPDDR4_DQ16
LPDDR4_DQ17
LPDDR4_DQ18
LPDDR4_DQ19
LPDDR4_DQ20
LPDDR4_DQ21
LPDDR4_DQ22
LPDDR4_DQ23
LPDDR4_DQ24
LPDDR4_DQ25
LPDDR4_DQ26
LPDDR4_DQ27
LPDDR4_DQ28
LPDDR4_DQ29
LPDDR4_DQ30
LPDDR4_DQ31
+1.1V_LPDDR4
C115 220nF X5R 6.3V
C117 220nF X5R 6.3V
C118 220nF X5R 6.3V
C119 220nF X5R 6.3V
C120 220nF X5R 6.3V
C121 220nF X5R 6.3V
C122 220nF X5R 6.3V
C123 220nF X5R 6.3V
C124 220nF X5R 6.3V
C125 220nF X5R 6.3V
C126 10nF X7R 10V
C127 10nF X7R 10V
C128 10nF X7R 10V
C129 10µF X5R 16V
C130 47µF X5R 6.3V
GND
trenz electronic
Title: TEM0007 - FPGA6
A4
Number: TEM0007 CHE11-A
Rev. 01
Date: 21.06.2022
Copyright: Trenz Electronic GmbH
Page 10 of 17
Filename: FPGA6.SchDoc







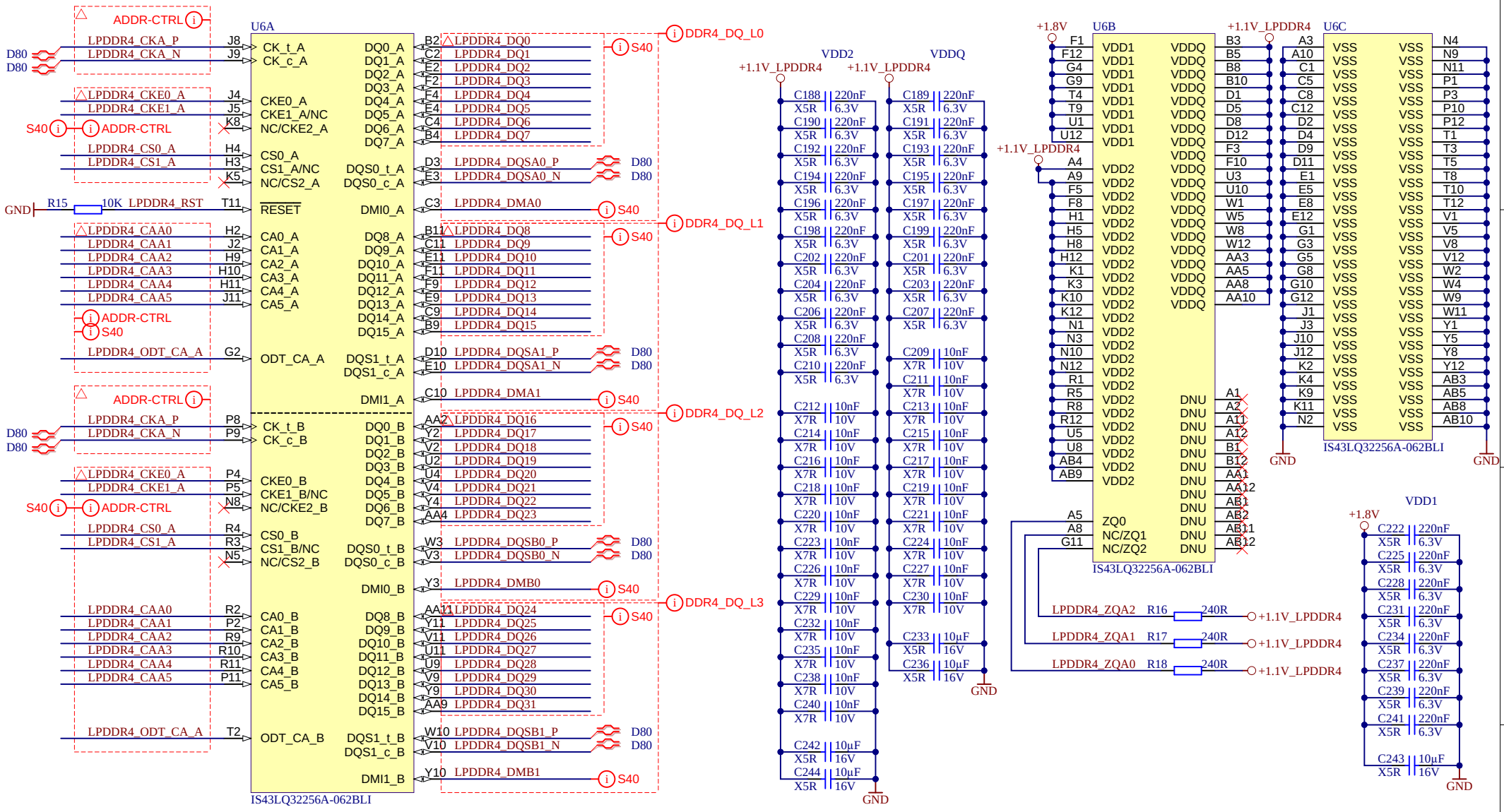
Both VDDA and VDD_XCVR_CLK supplies must be powered when any of the transceivers are used. VDD_XCVR_CLK must power on within the I/O calibration time (as specified for the device in Libero). VDDA and VDD_XCVR_CLK must both then remain powered during operation. If VDDA needs to be powered down, VDD_XCVR_CLK must also be powered down. There is no required sequence for powering up or down VDDA and VDD_XCVR_CLK.

There are no sequencing requirements for the power supplies. However, VDDI3 and must be valid at same time as the main supplies. The other I/O supplies (VDDI, VDDAUX) have no effect on power-up of FPGA fabric (that is, the fabric still powers up even if the I/O supplies of some I/O banks remain powered off).

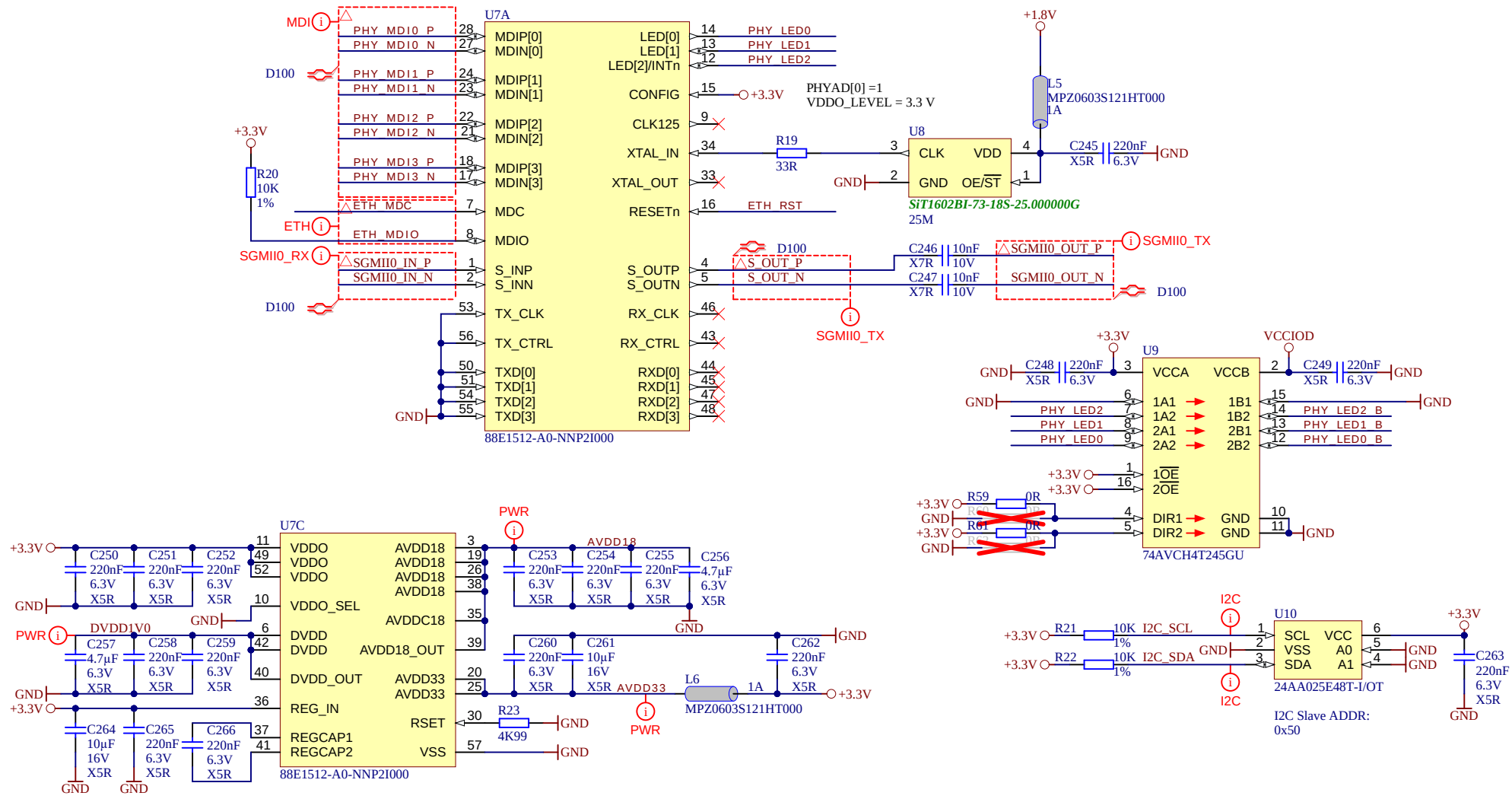
VDD - For fabric core and transceiver/PCIe blocks.
VDD18 - For fabric programming and RC oscillators.
VDD25 - For corner phase-locked loop (PLLs) and on-chip non-volatile memory (sNVM).
VDDIx - For I/O banks.
VDDAUXx - For GPIO and HSIO banks.
VDDA - For transceiver.
VDDA25 - For transceiver PLLs.
VDD_XCVR_CLK - For transceiver reference clock input buffers.

trenz electronic

Title: TEM0007 - FPGA_PWR		
A4	Number: TEM0007 CHE11-A	Rev. 01
Date: 21.06.2022	Copyright: Trenz Electronic GmbH	Page 11 of 17
Filename: FPGA_PWR.SchDoc		

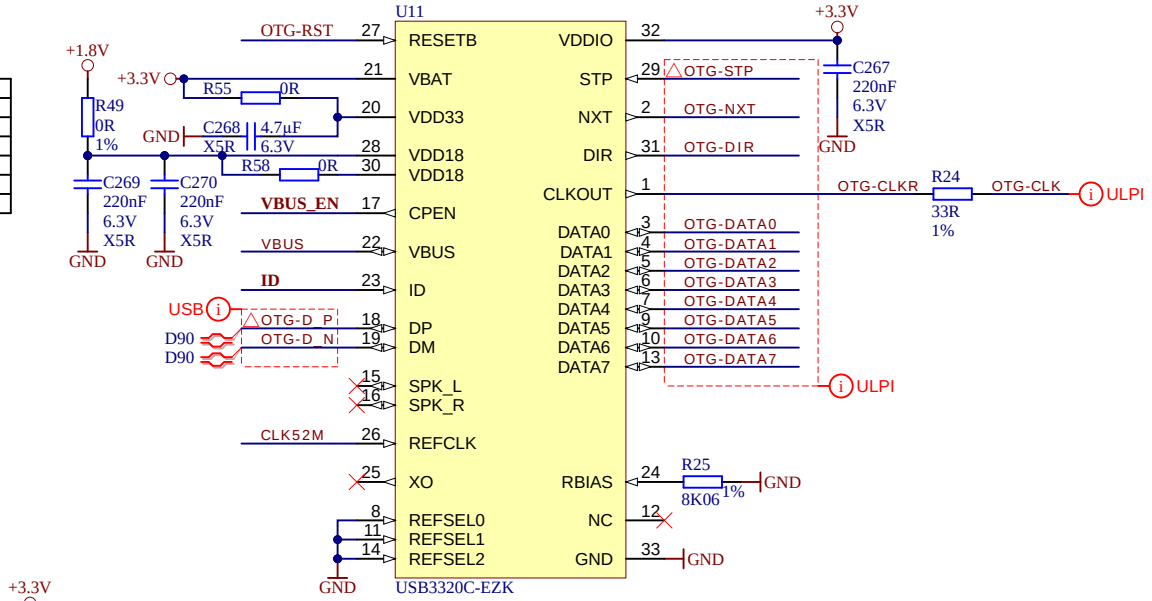


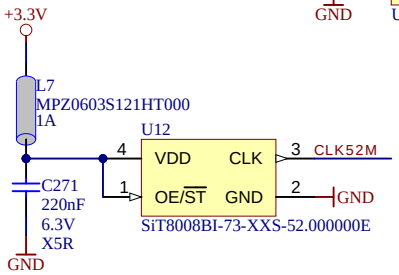
trenz electronic	Title: TEM0007 - LPDDR4		
	A4	Number: TEM0007 CHE11-A	Rev. 01
	Date: 21.06.2022	Copyright: Trenz Electronic GmbH	Page 12 of 17
	Filename: LPDDR4.SchDoc		



trenz electronic	Title: TEM0007 - ETH-PHY		
	A4	Number: TEM0007 CHE11-A	Rev. 01
	Date: 02.02.2023	Copyright: Trenz Electronic GmbH	Page 13 of 17
	Filename: ETH-PHY.SchDoc		

	USB3320:	USB3340:
R49	0R	DNP
R55	0R	DNP
R58	0R	DNP
C268	4.7 uF	1.0 uF
C269	0.1 uF	1.0 uF
C270	0.1 uF	1.0 uF



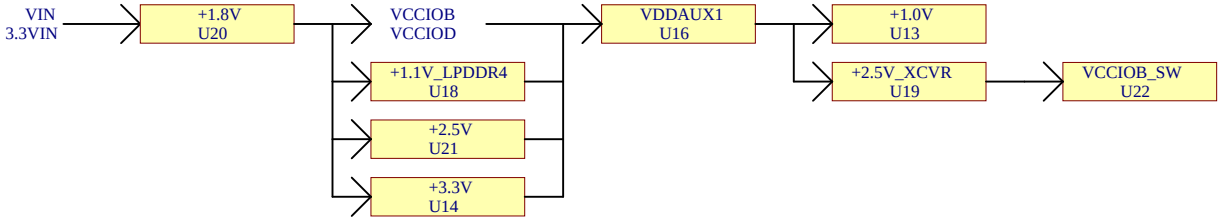


trenz electronic

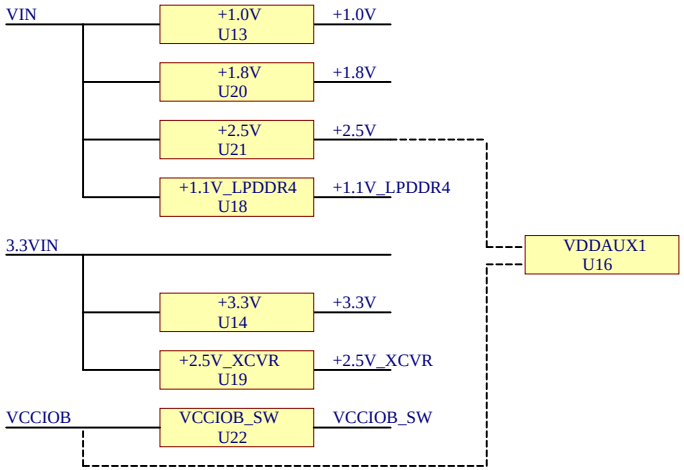
Title: TEM0007 - USB-PHY		
A4	Number: TEM0007 CHE11-A	Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH	Page 14 of 17
Filename: USB-PHY.SchDoc		

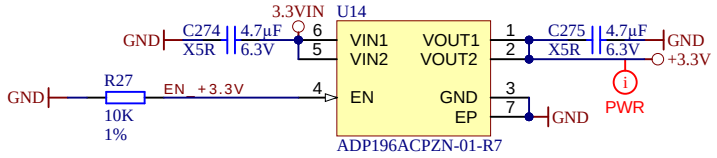
Recommended Power Supply Sequencing

The final power sequende depends on the CPLD.

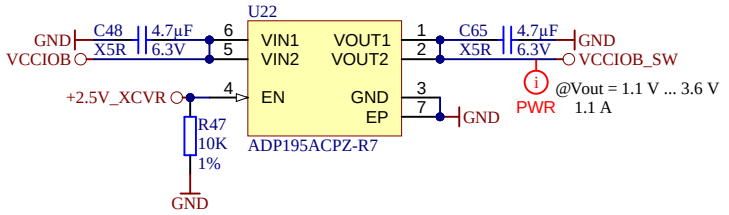


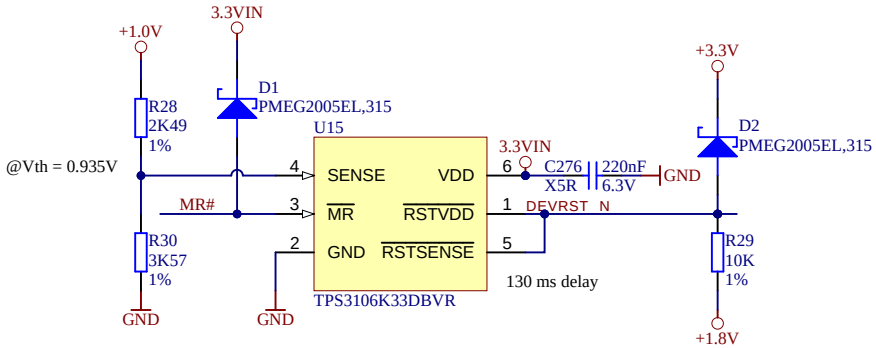
Power Supply Structure

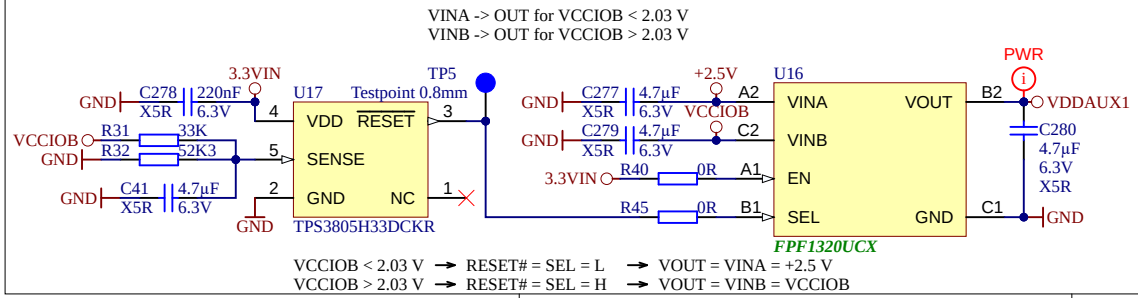




Needed for IO Glitch Prevention!

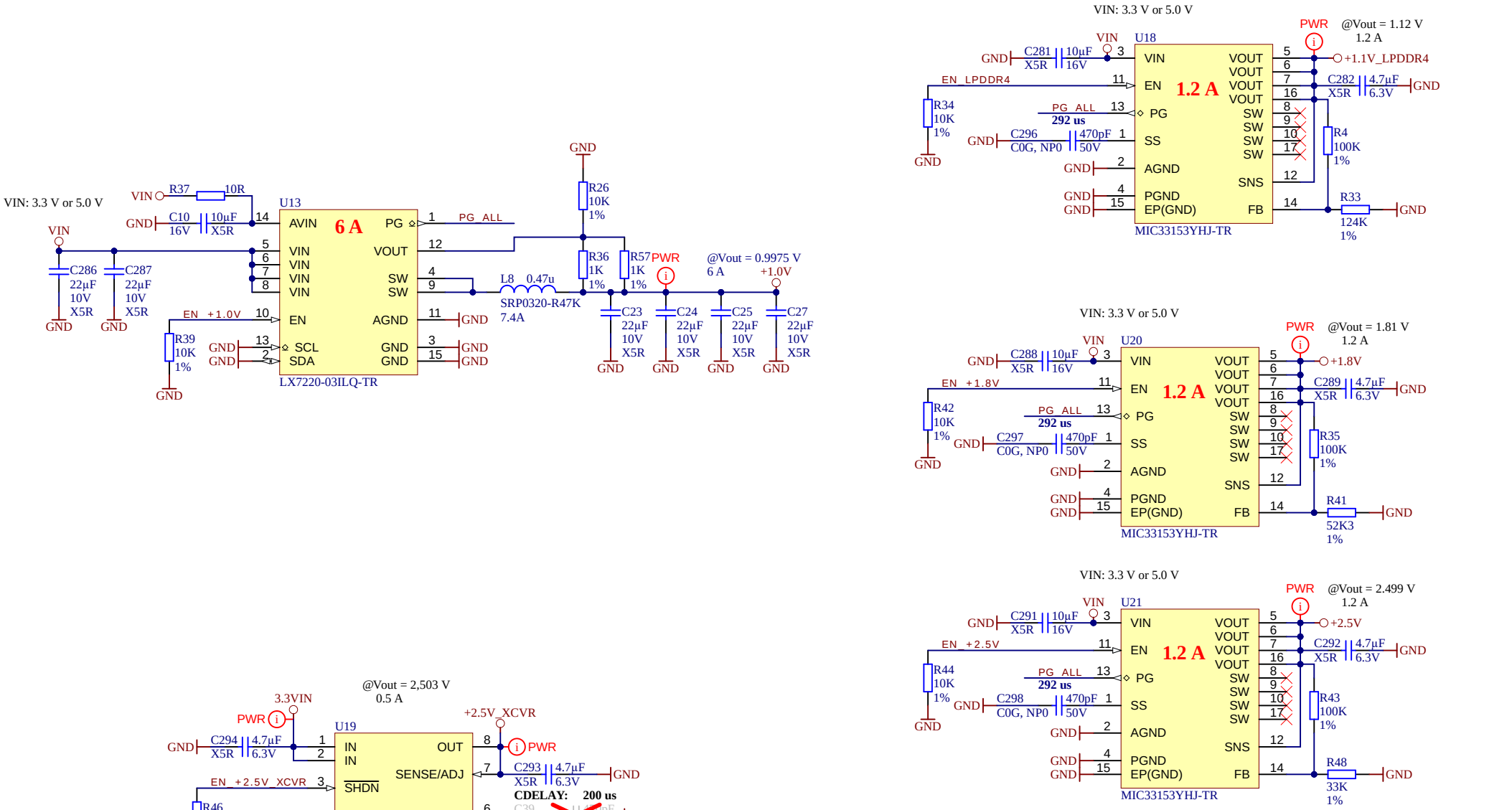






trenz electronic

Title: TEM0007 - POWER1		
A4	Number: TEM0007 CHE11-A	Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH	Page 15 of 17
Filename: POWER1.SchDoc		



trenz electronic

Title: TEM0007 - POWER2		
A4	Number: TEM0007 CHE11-A	Rev. 01
Date: 02.02.2023	Copyright: Trenz Electronic GmbH	Page 16 of 17
Filename: POWER2.SchDoc		

REV	DATE	Description	
-05		Initial revision	ED
	2023-09-04	1. Changed power switch U16 from FPF1321BUCX to FPF1320UCX. 2. Updated revision history.	ED

trenz electronic	Title: TEM0007 - Revision Changes List		
	A4	Number: TEM0007 CHE11-A	Rev. 01
	Date: 2021-10-22	Copyright: Trenz Electronic GmbH	Page 17 of 17
	Drawn by:	Filename: Revision Changes.SchDoc	