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U_J1
J1.SchDoc



U_DDR3
DDR3-RAM.SchDoc



QSPI_MicroSD
QSPI_MicroSD.SchDoc



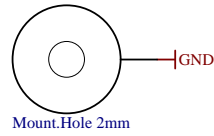
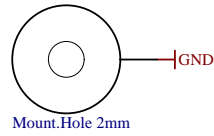
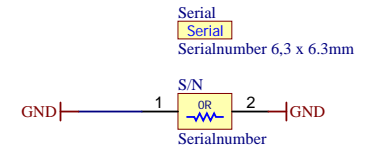
U_ZYNQ
ZYNQ.SchDoc



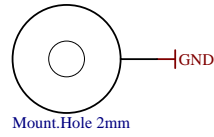
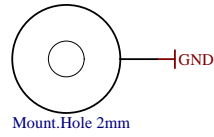
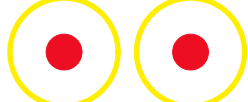
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ETH-PHY.SchDoc



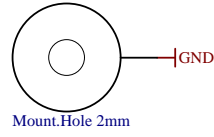
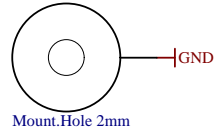
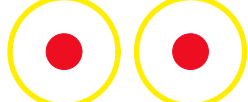
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POWER.SchDoc



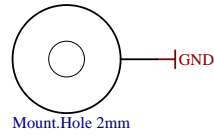
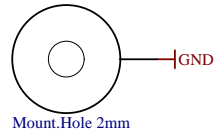
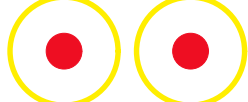
FIDU-DOT - small FIDU-DOT - small



PM1 PM2
FIDU-DOT - small FIDU-DOT - small



PM3 PM4
FIDU-DOT - small FIDU-DOT - small



PM5

PM6



Title: TE0724		
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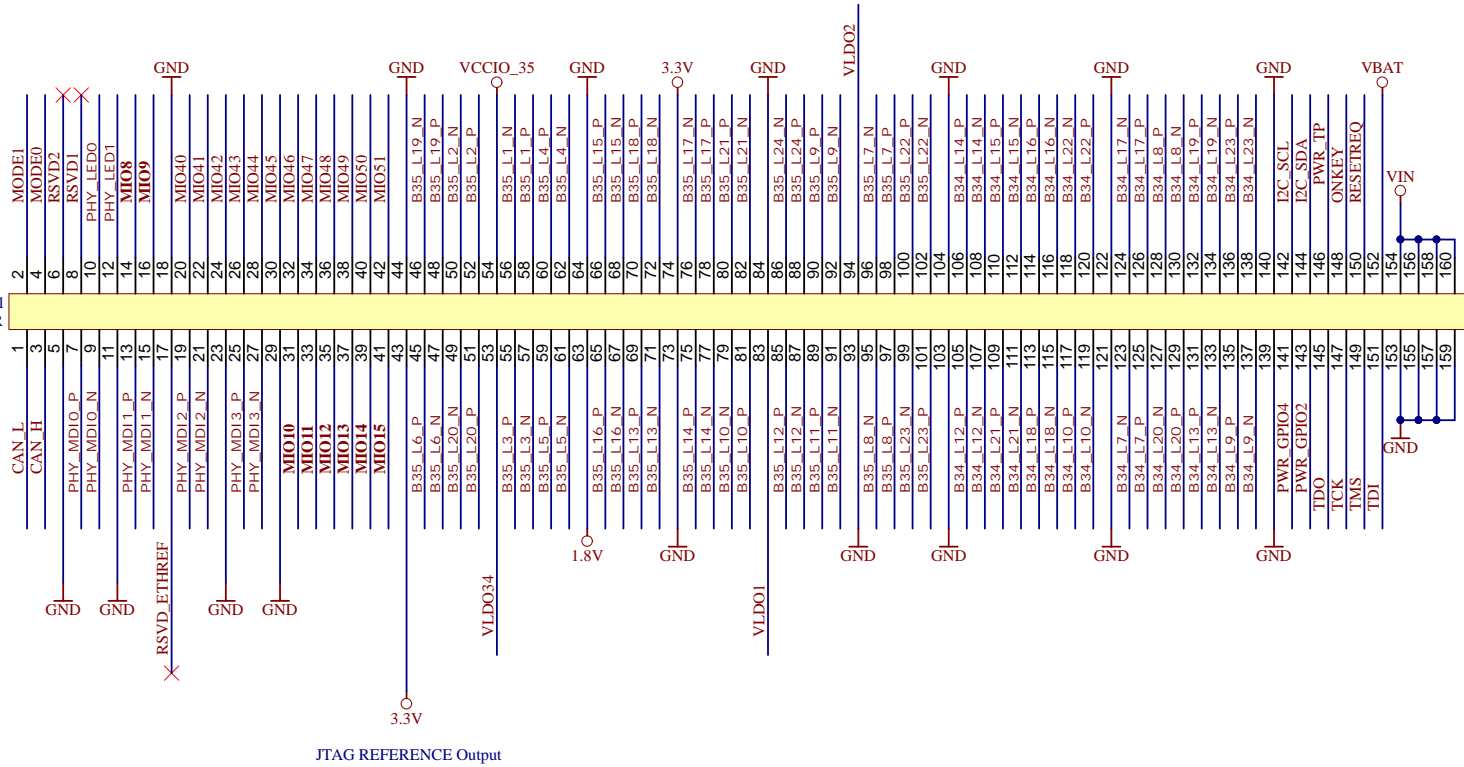
C

D

D

MIO0 - 8 I/O 3.3V
 MIO1 - 12 I/O 1.8V
 B34 - 16 I/O 3.3V
 B35 - 48 I/O Variable

ST5-80-1.50-L-D-P-TR J1



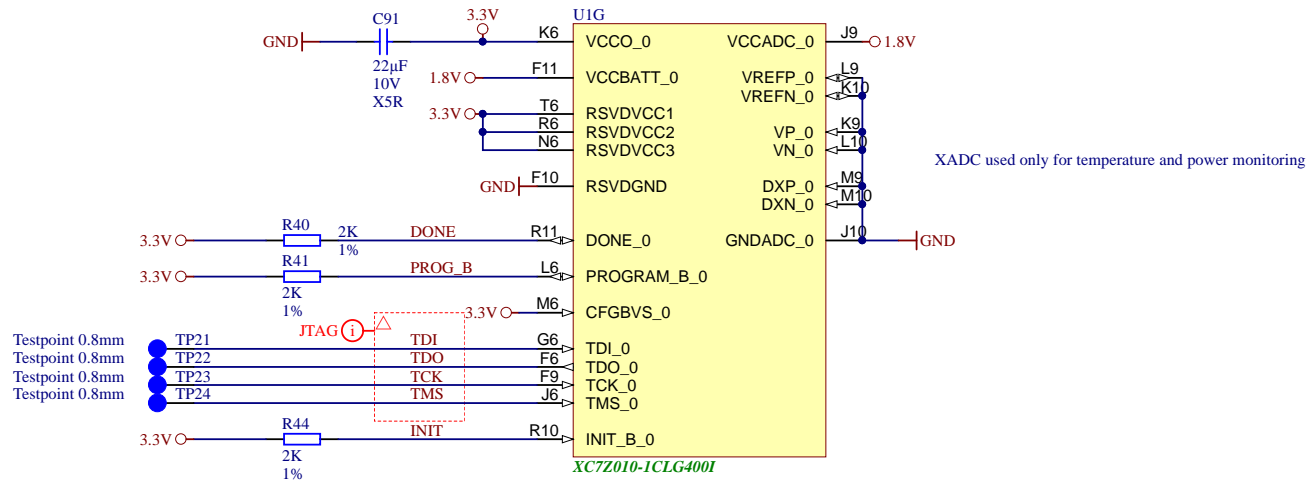
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	A4	Number: TE0724 10-11
	Date: 2017-05-30	Copyright: Trenz Electronic GmbH / TT
	Filename: J1.SchDoc	Rev. 02
		Page2 of 16

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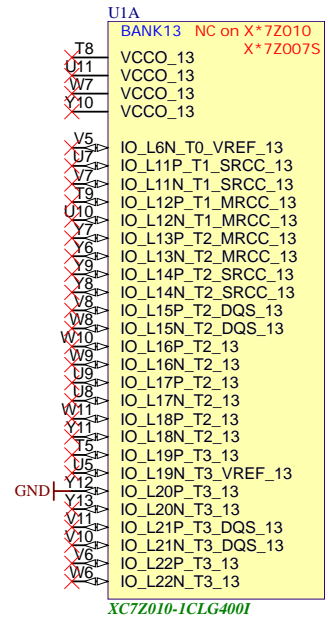
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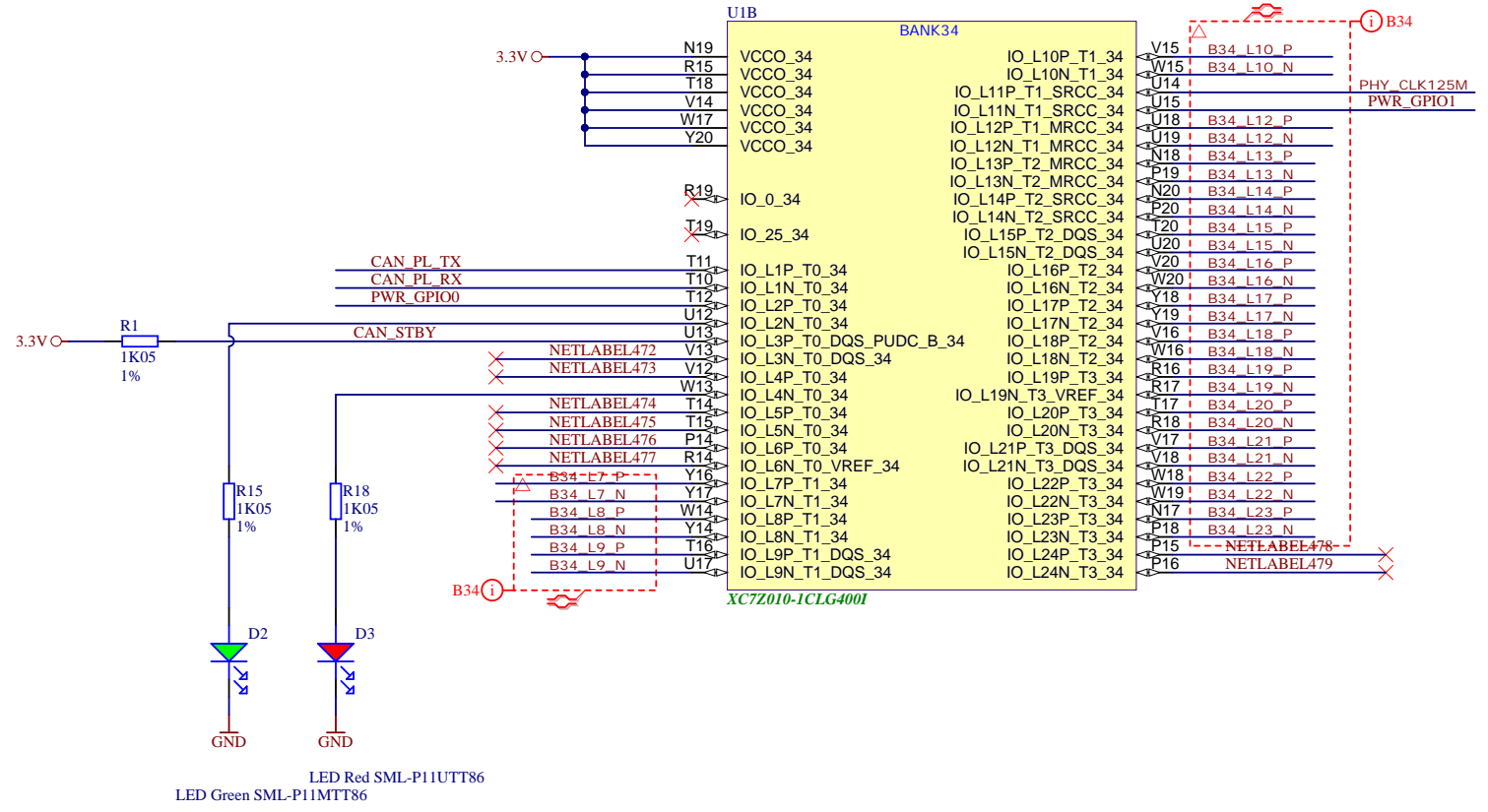
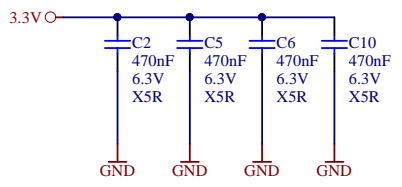
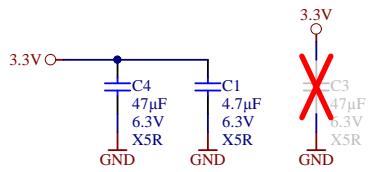
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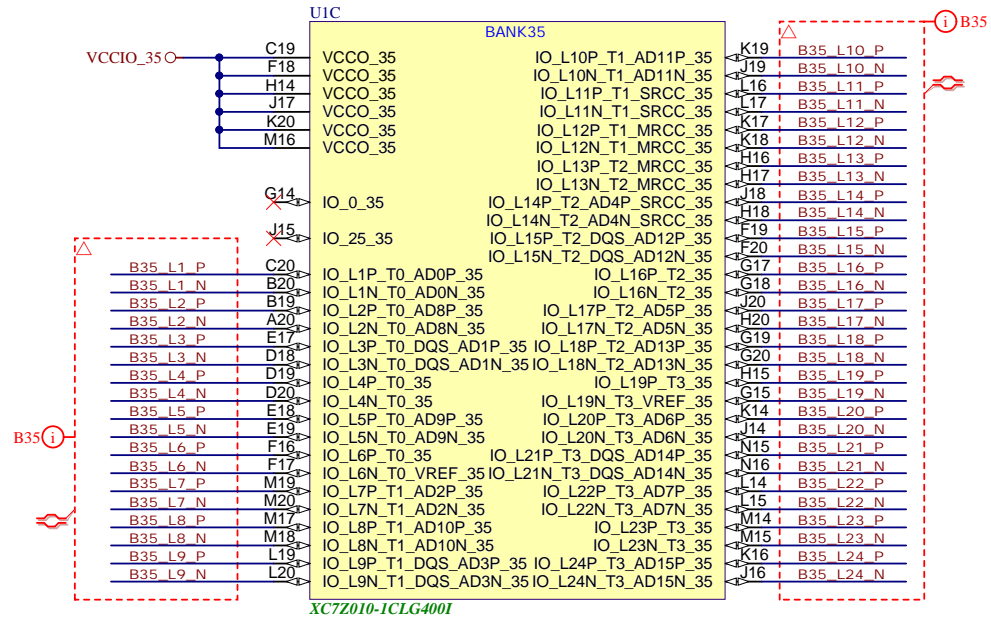
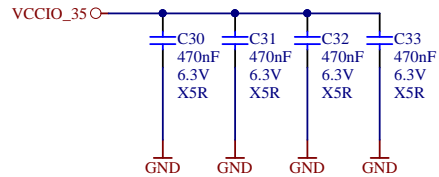
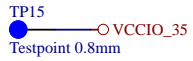
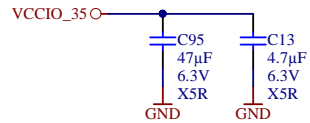

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	A4	Number: TE0724 10-11	Rev. 02
	Date: 2017-05-30	Copyright: Trenz Electronic GmbH / TT	Page3 of 16
	Filename: ZYNQ_MISC.SchDoc		



	Title: TE0724 - Zynq_B13		
	A4	Number: TE0724 10-11	Rev. 02
	Date: 2017-05-30	Copyright: Trenz Electronic GmbH / TT	Page4 of 16
	Filename: B13.SchDoc		



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		A4	Number: TE0724 10-11
Date: 2017-05-30		Copyright: Trenz Electronic GmbH / TT	
Filename: B34.SchDoc		Page5 of 16	

Title: TE0724 - Zynq_B35		
A4	Number: TE0724 10-11	Rev. 02
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U_B13
B13.SchDoc



U_B500
MIO_B500.SchDoc



U_B501
MIO_B501.SchDoc



U_PS_DDR
PS-DDR.SchDoc



U_MISC
ZYNQ_MISC.SchDoc



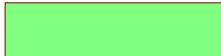
U_B34
B34.SchDoc



U_ZYNQ_POWER
ZYNQ_POWER.SchDoc



U_B35
B35.SchDoc



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Title: TE0724 - Zynq		
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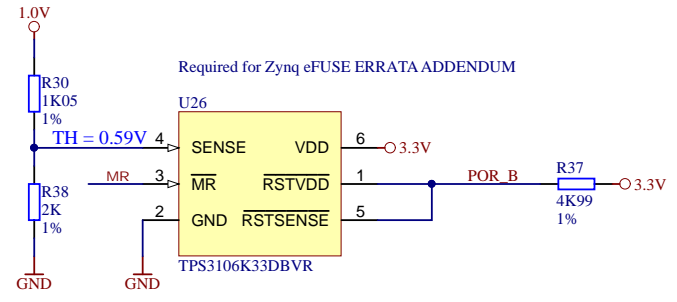
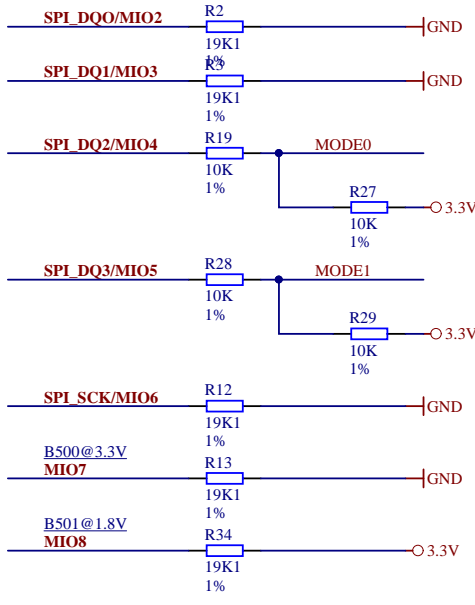
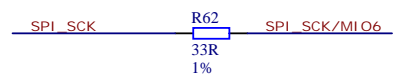
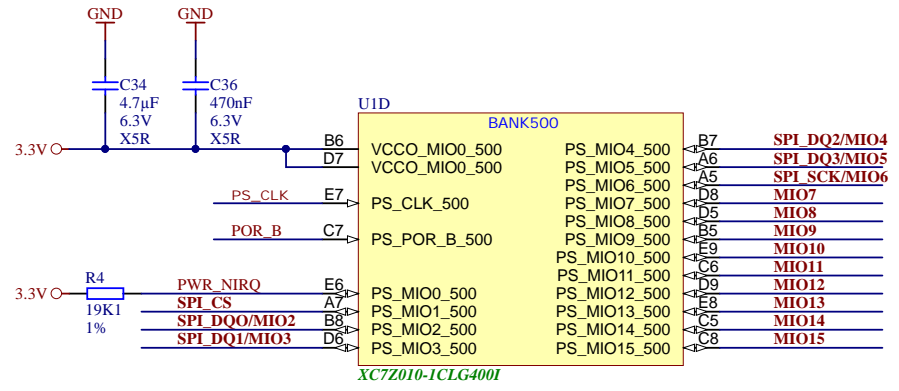
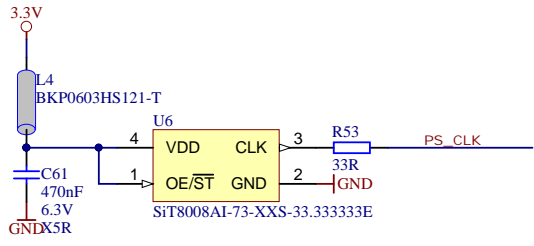
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Required for Zynq eFUSE ERRATA ADDENDUM



Title: TE0724 - Zynq_MIO_B500		
A4	Number: TE0724 10-11	Rev. 02
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Filename: MIO_B500.SchDoc		

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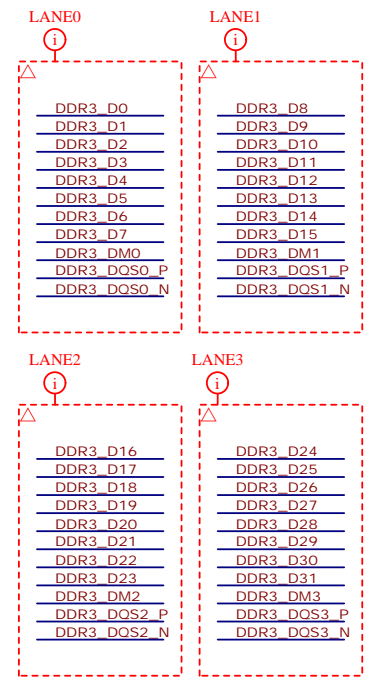
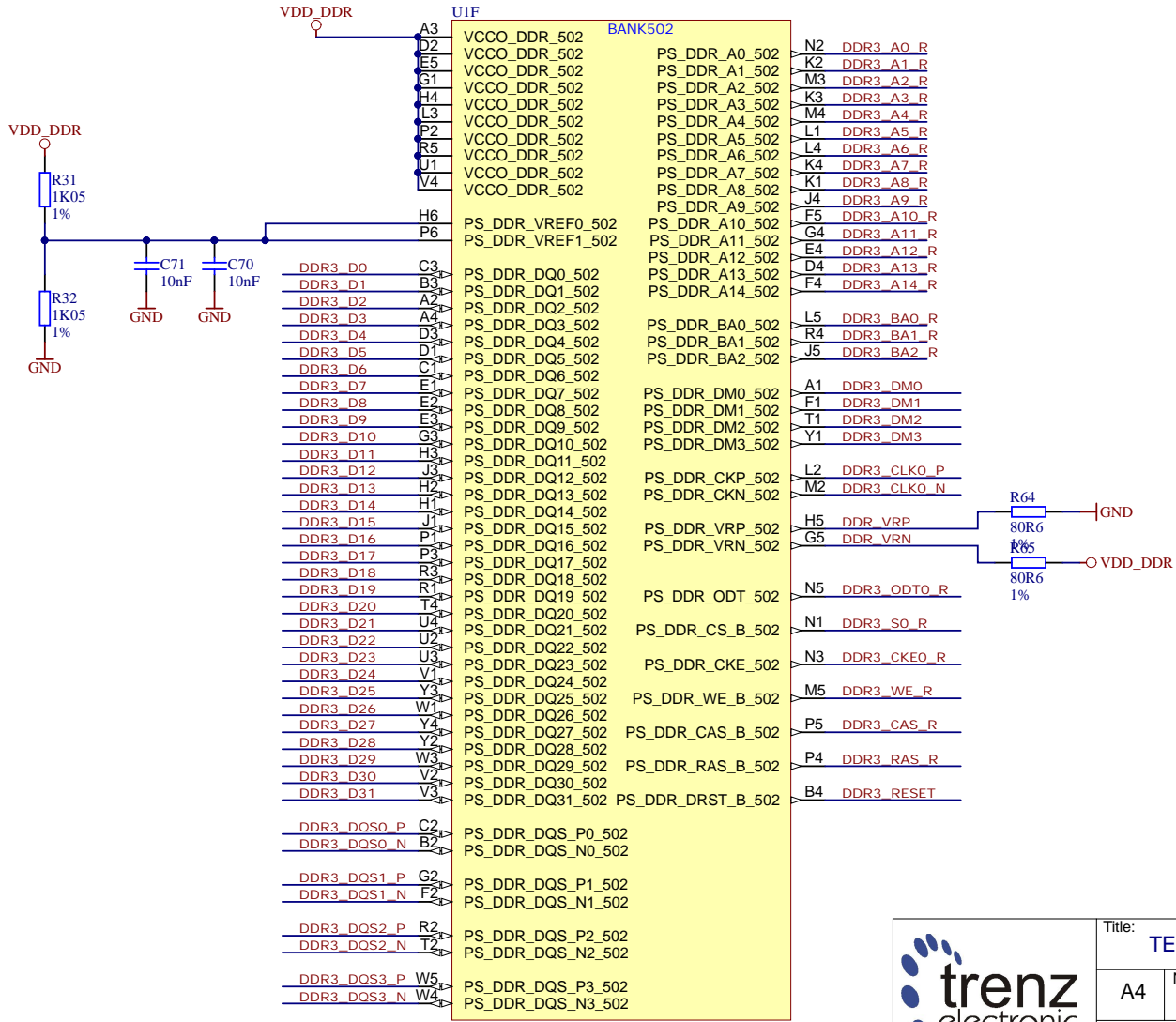
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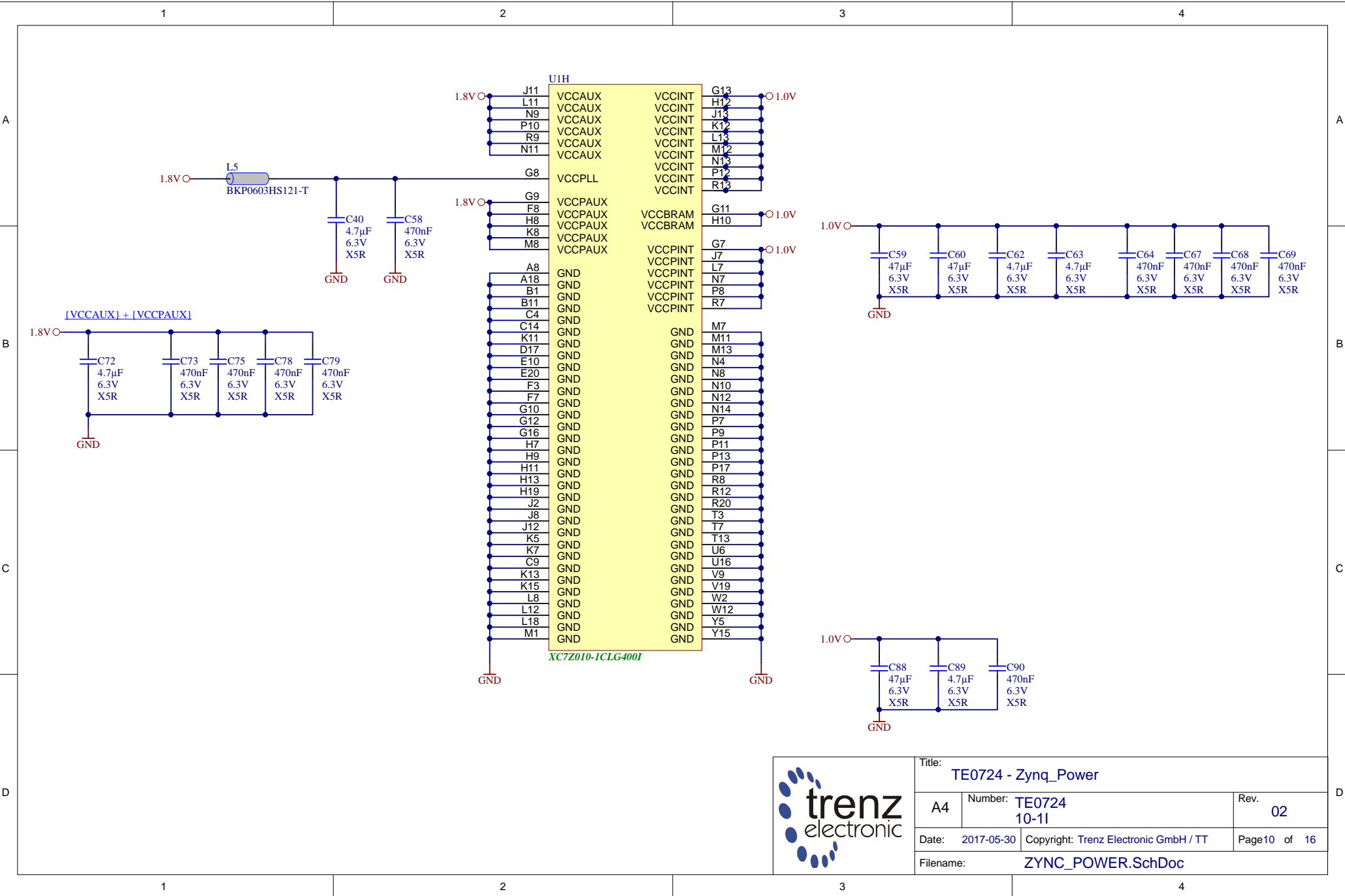
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Date: 2017-05-30		Copyright: Trenz Electronic GmbH / TT	
Filename: PS-DDR.SchDoc		Page9 of 16	

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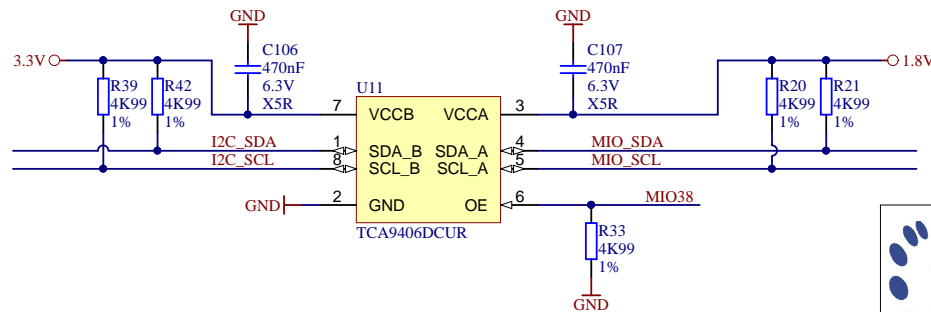
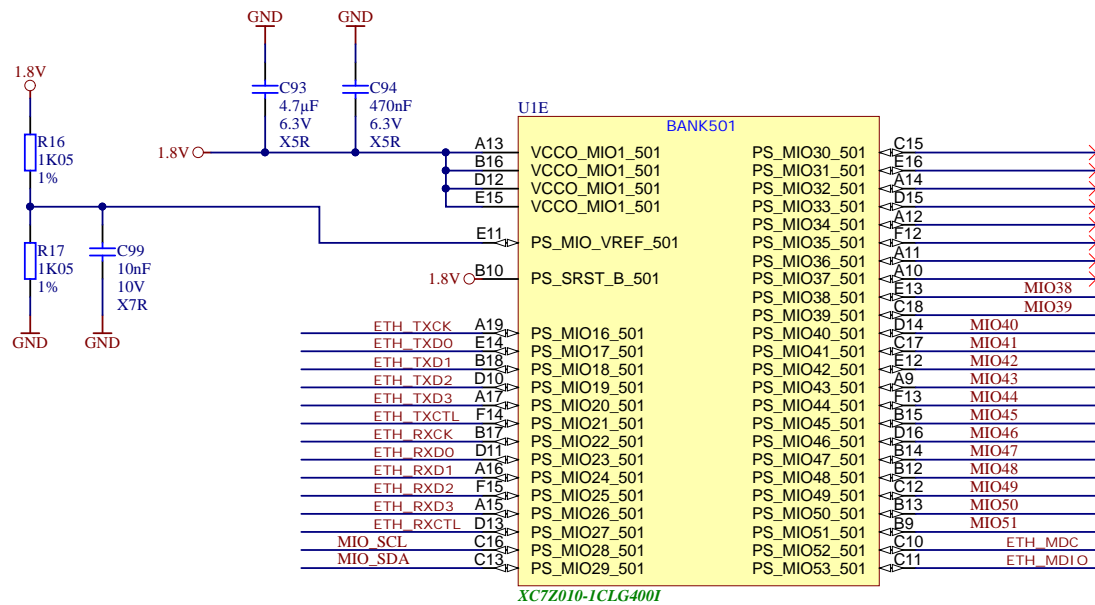
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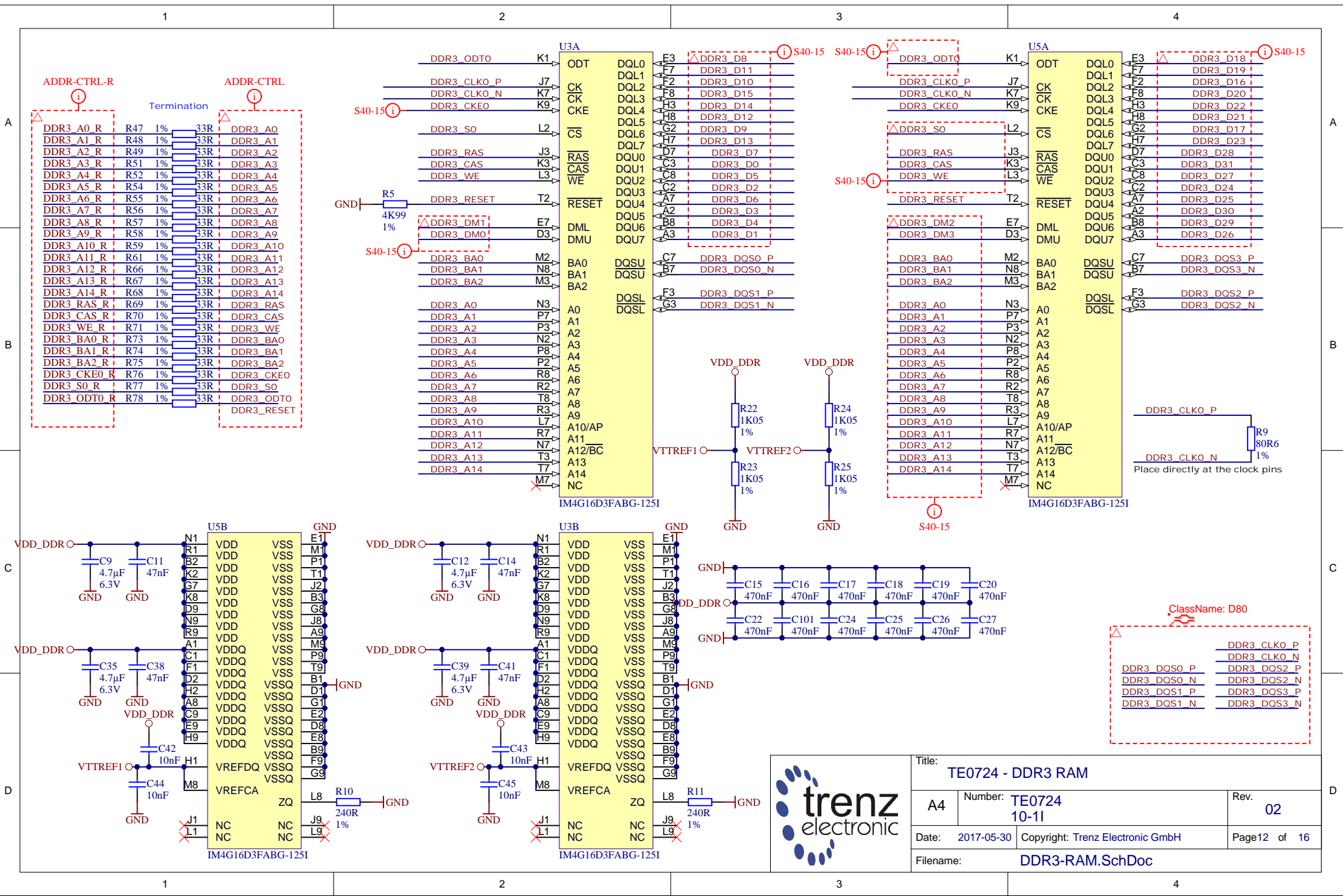
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Date: 2017-05-30	Copyright: Trenz Electronic GmbH / TT	Page10 of 16
Filename: ZYNC_POWER.SchDoc		

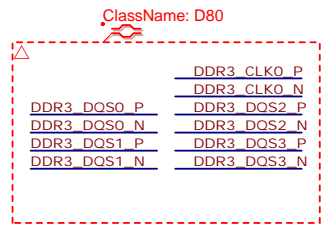


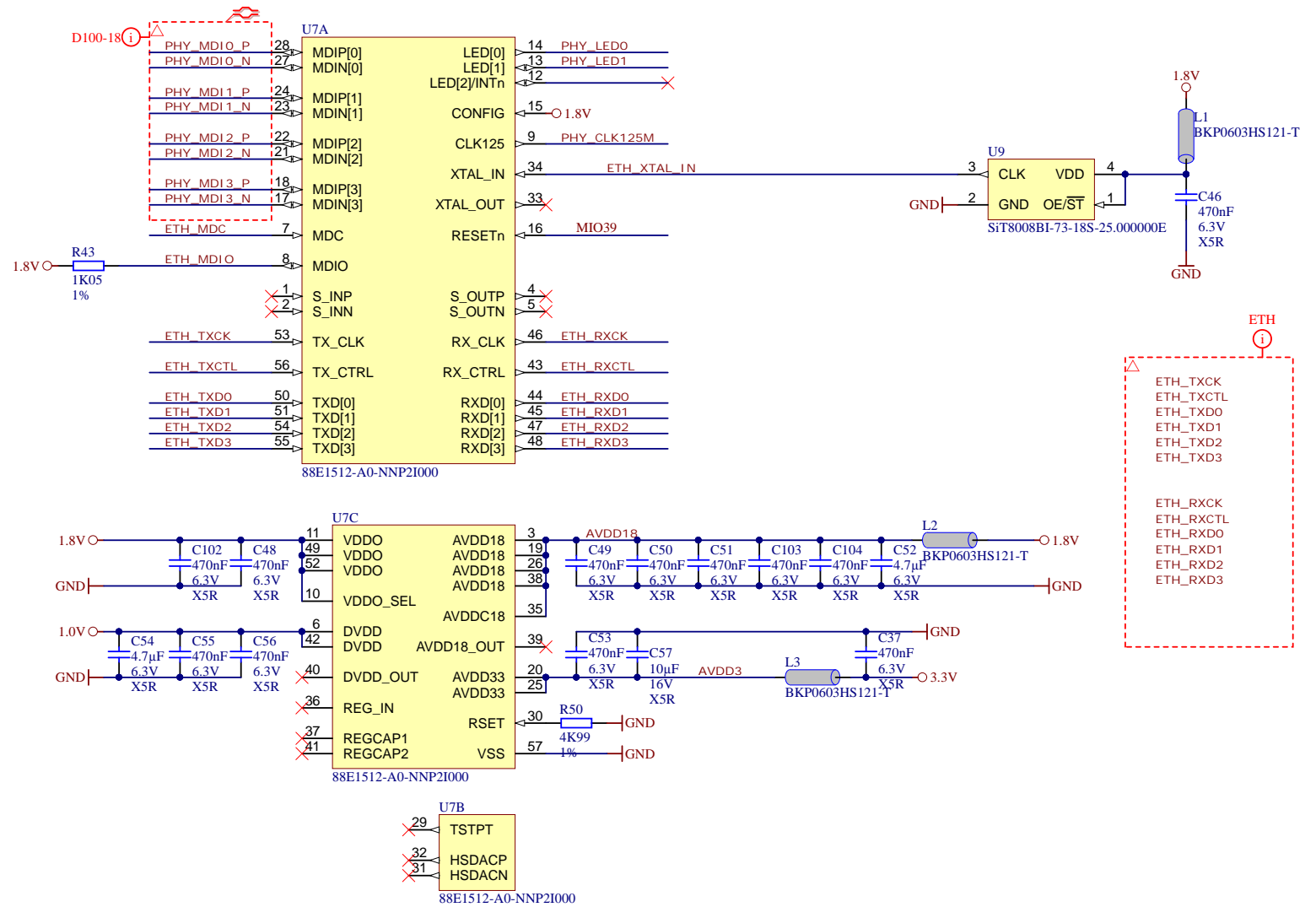
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Date: 2017-05-30	Copyright: Trenz Electronic GmbH / TT	Page 11 of 16
Filename: MIO_B501.SchDoc		



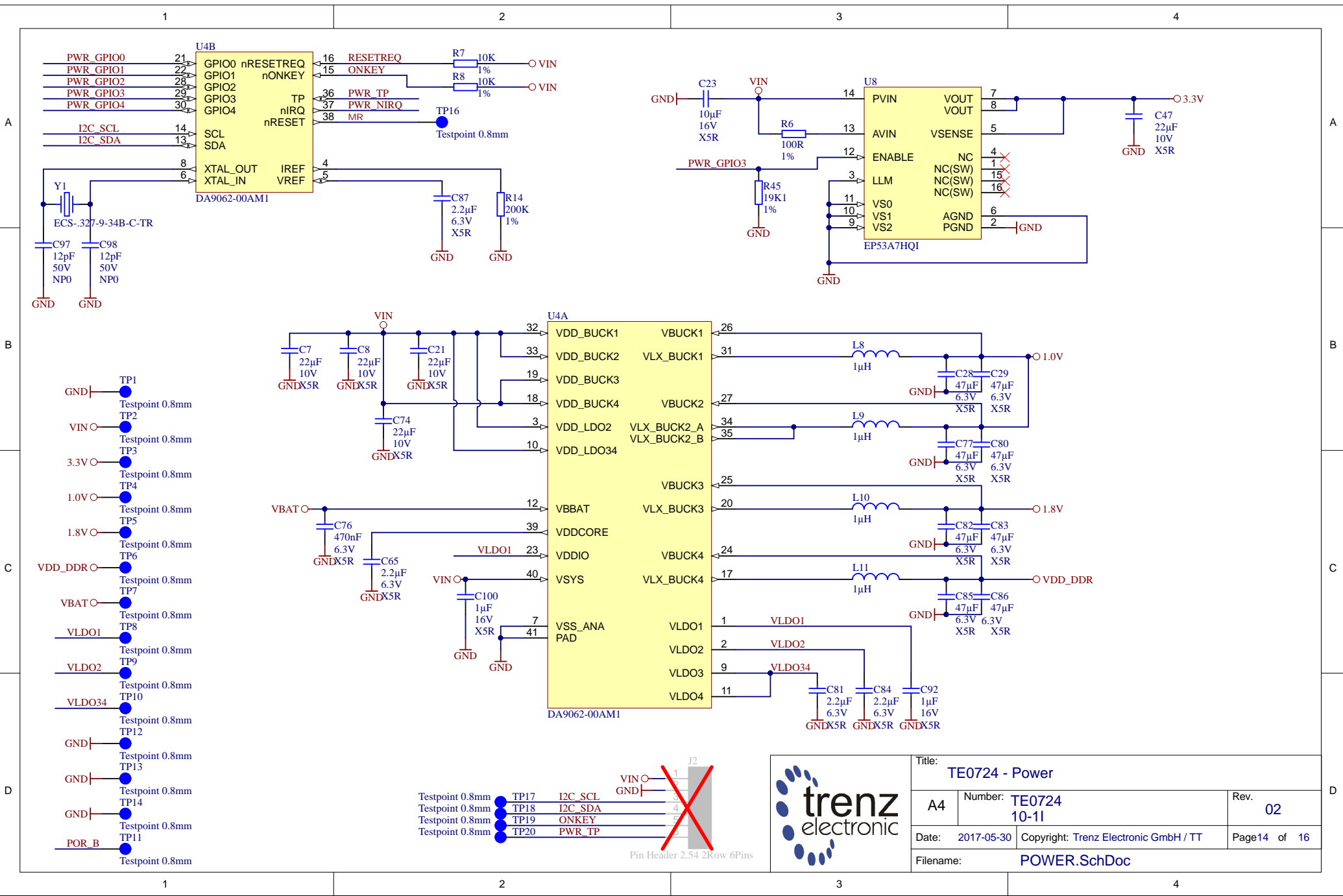
trenz electronic

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Date: 2017-05-30	Copyright: Trenz Electronic GmbH	Page 12 of 16
Filename: DDR3-RAM.SchDoc		



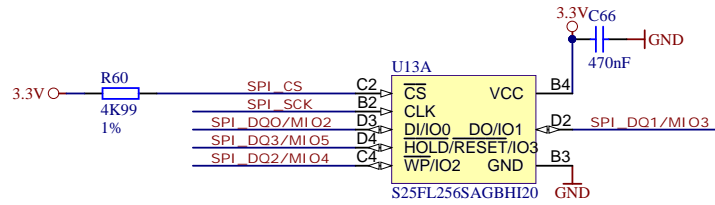


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Date: 2017-05-30	Copyright: Trenz Electronic GmbH / TT	Page13 of 16
Filename: ETH-PHY.SchDoc		

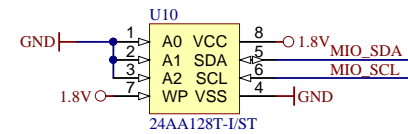
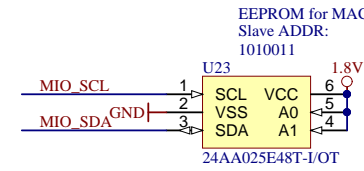


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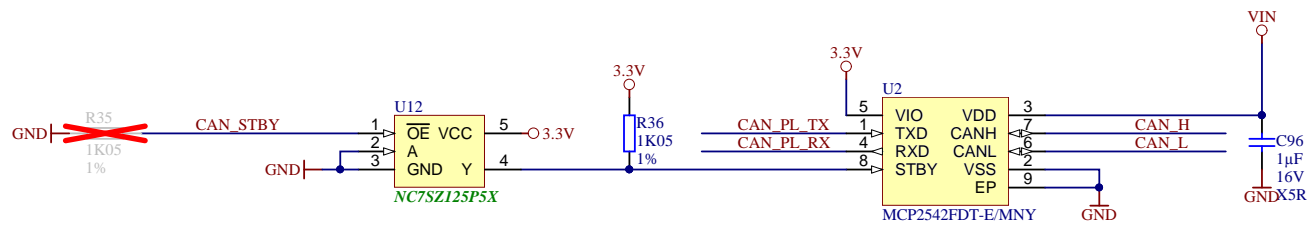
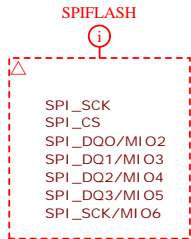
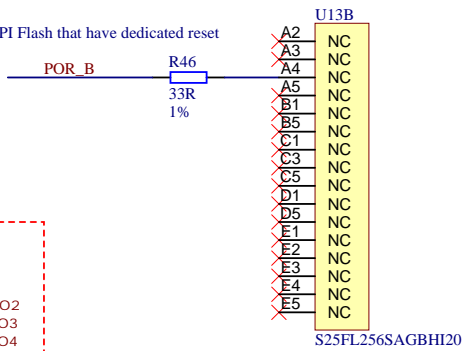
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A4	Number: TE0724 10-11	Rev. 02
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Filename: POWER.SchDoc		



Optional EEPROM Memories



OPTIONAL for SPI Flash that have dedicated reset



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REV. 02:

- 1) New I2C translator U11: TCA9406DCUR
- 2) Fixed boot mode connection. Mode0 pulled-up by R27 and Mode 1 pulled-up by R33
- 3) Green LED D3 replaced to Red LED
- 4) C91 changed from 47 to 22uF
- 5) C3 not fitted
- 6) C105 deleted, C47 replaced from 10 to 22uF (EP53A7HQI output capacitor)
- 7) PWR_GPIO3 (EP53A7HQI enable) pulled down by R45 (19.1 kOhm)
- 8) DONE, INIT, PROG_B pulled-up to 3.3V
- 9) Added testpoints: JTAG, PMIC (I2C, ONKEY, TP)
- 10) J2 changed to 2 row 6-pin header. To J2 added ONKEY, PWR_TP, VIN
- 11) Mounting holes changed from 2mm to 2.2mm

REV.02A:

- 1) PCB revision: all vias are epoxy filled and copper capped. No mask openings on vias. No electrical changes

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Title: TE0724		
A4	Number: TE0724 10-11	Rev. 02
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Filename: Revision changes.SchDoc		