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Schematics and other handouts serve for informational purposes only!

	Title: TE0724		
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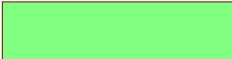
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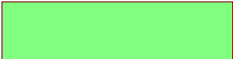
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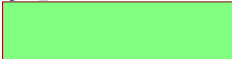
U_J1
J1.SchDoc




U_DDR3
DDR3-RAM.SchDoc




QSPI_MicroSD
QSPI_MicroSD.SchDoc




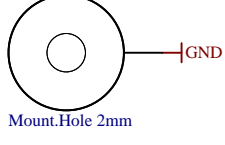
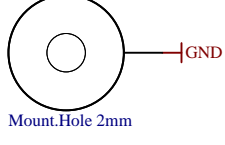
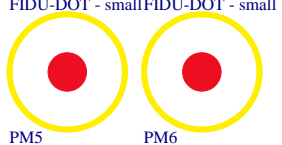
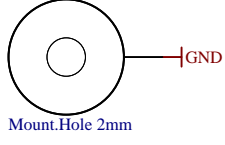
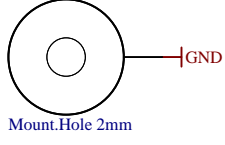
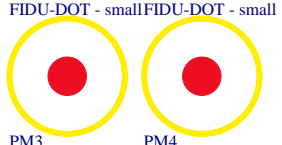
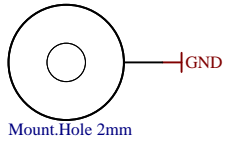
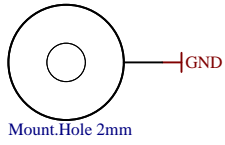
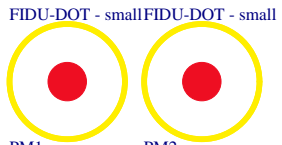
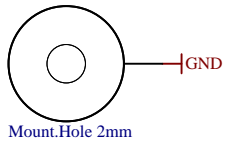
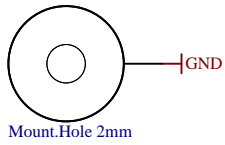
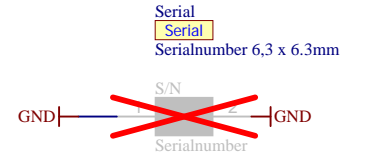
U_ZYNQ
ZYNQ.SchDoc



U_ETH_PHY
ETH-PHY.SchDoc



U_POWER
POWER.SchDoc

Design drawn by:	MR
Checked by:	IG
Assembly variant:	41133-A
Created by:	VT
Modified by:	MR
Modified at:	2020-09-04



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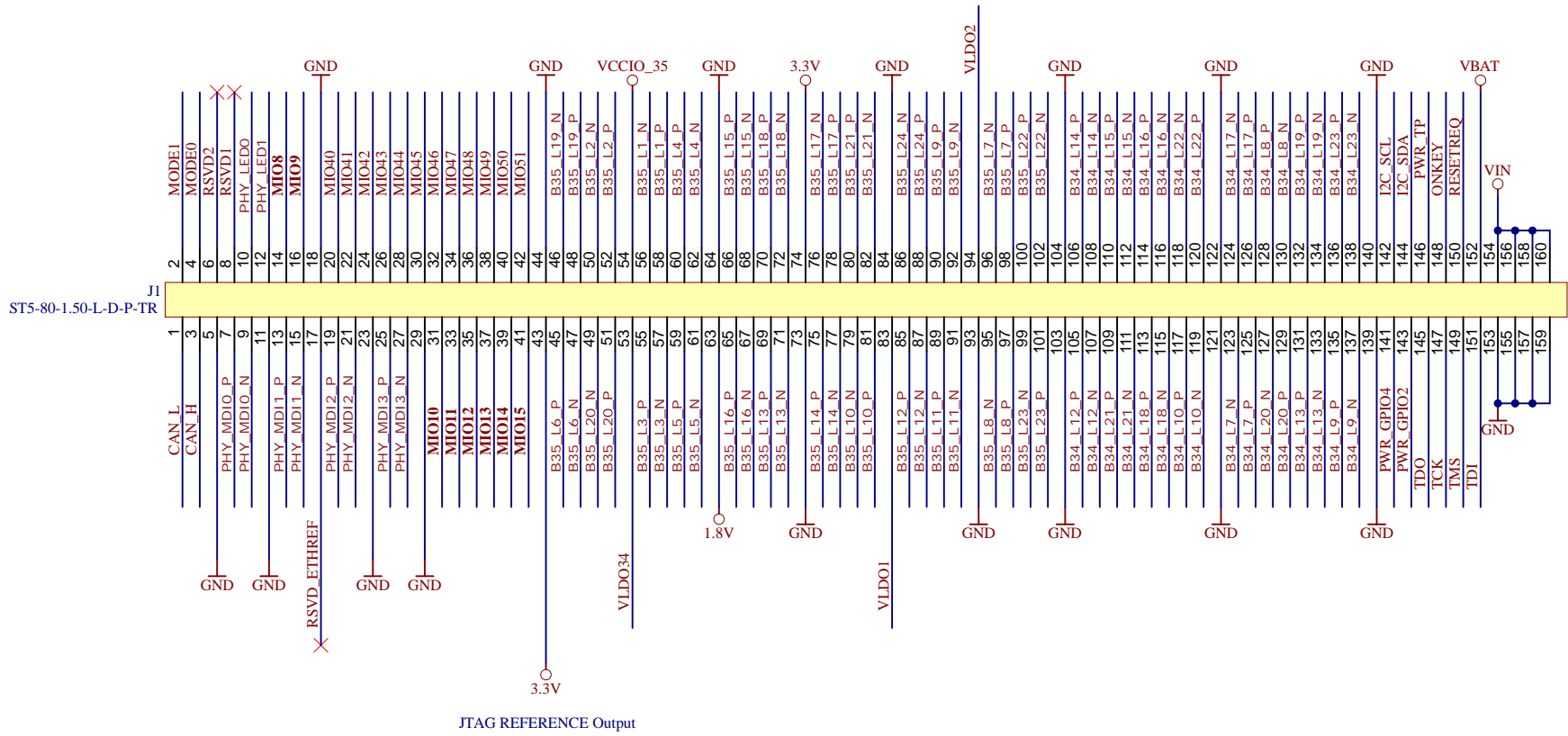
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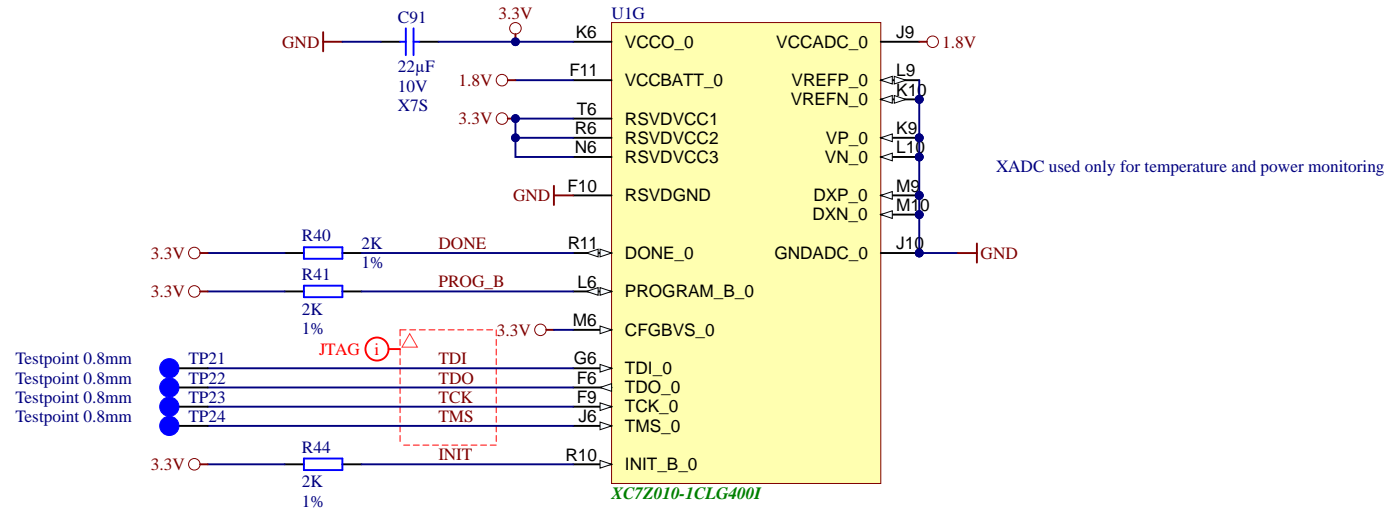
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MIO0 - 8 I/O 3.3V
 MIO1 - 12 I/O 1.8V
 B34 - 32 I/O 3.3V
 B35 - 24 LVDS or 48 I/O Variable

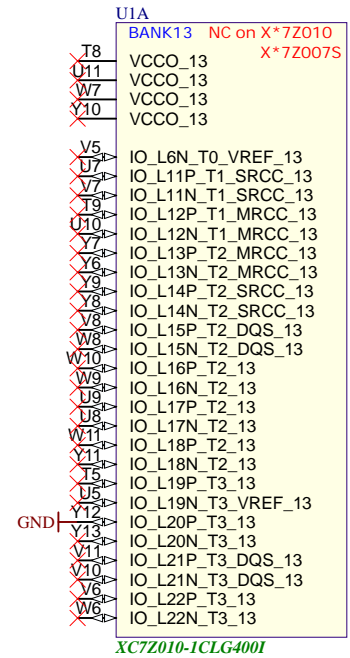




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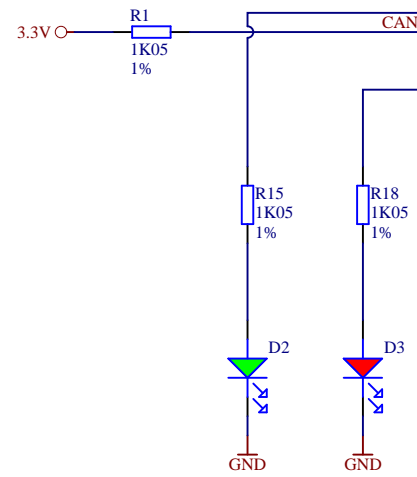
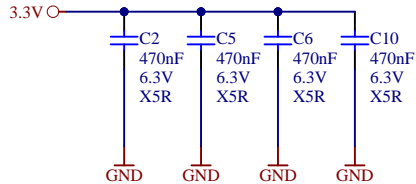
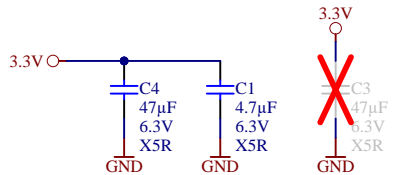
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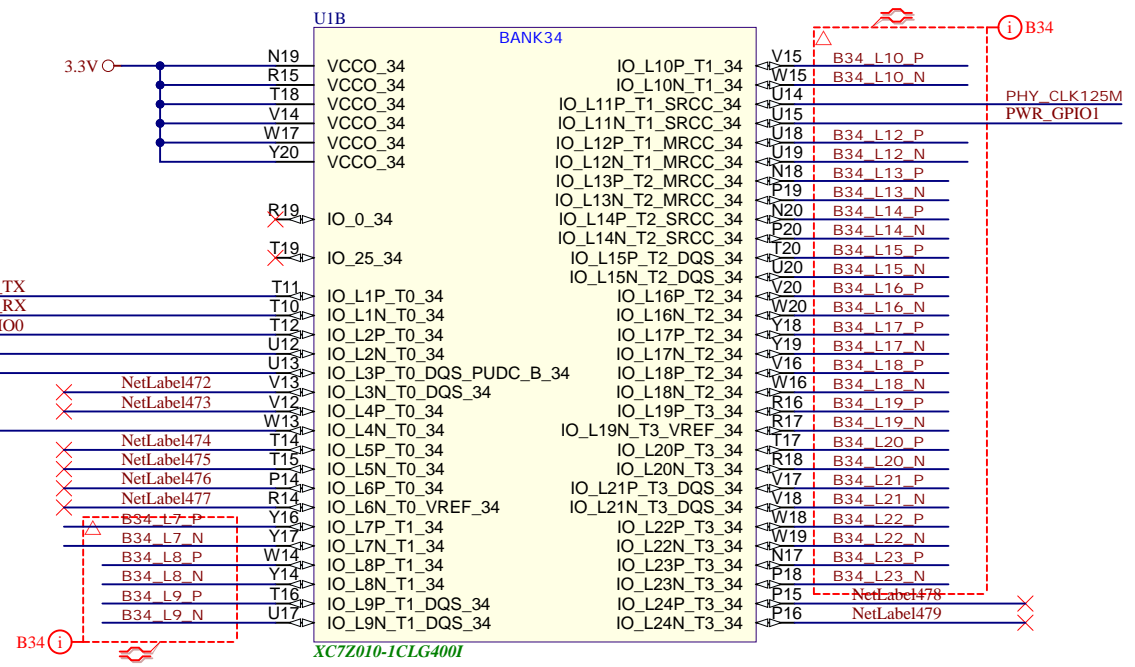
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Filename: ZYNQ_MISC.SchDoc		



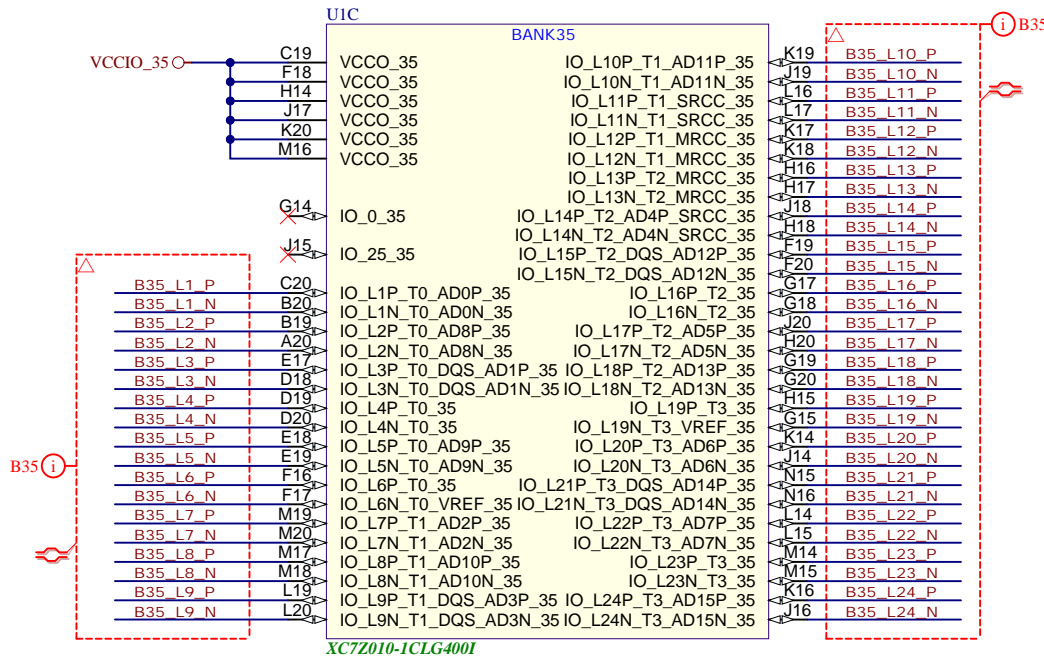
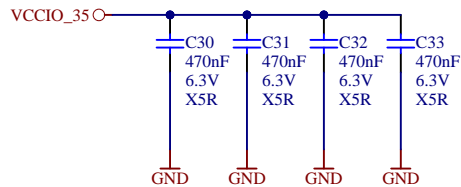
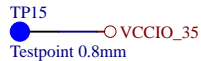
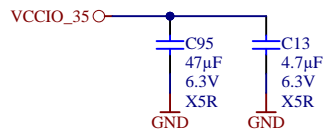
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	Filename: B13.SchDoc		



LED Red SML-P11UTT86
LED Green SML-P11MTT86



Title: TE0724 - Zynq_B34		
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A

A

U_B13
B13.SchDoc



U_B500
MIO_B500.SchDoc



U_B501
MIO_B501.SchDoc



U_PS_DDR
PS-DDR.SchDoc



U_MISC
ZYNQ_MISC.SchDoc



U_B34
B34.SchDoc



U_ZYNQ_POWER
ZYNQ_POWER.SchDoc



U_B35
B35.SchDoc



B


B

C

C

D

D

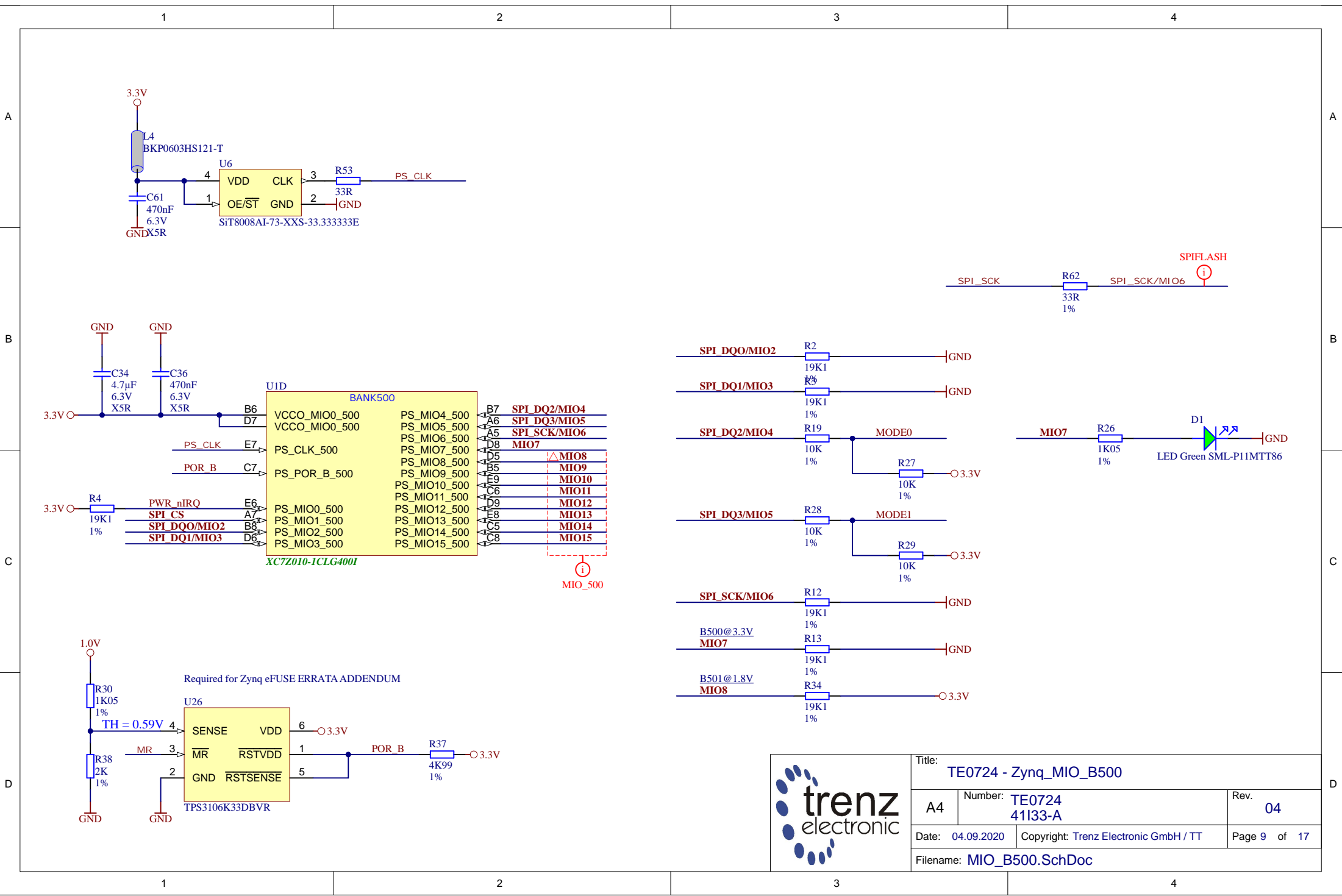
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Date: 21.08.2020		Copyright: Trenz Electronic GmbH / TT	
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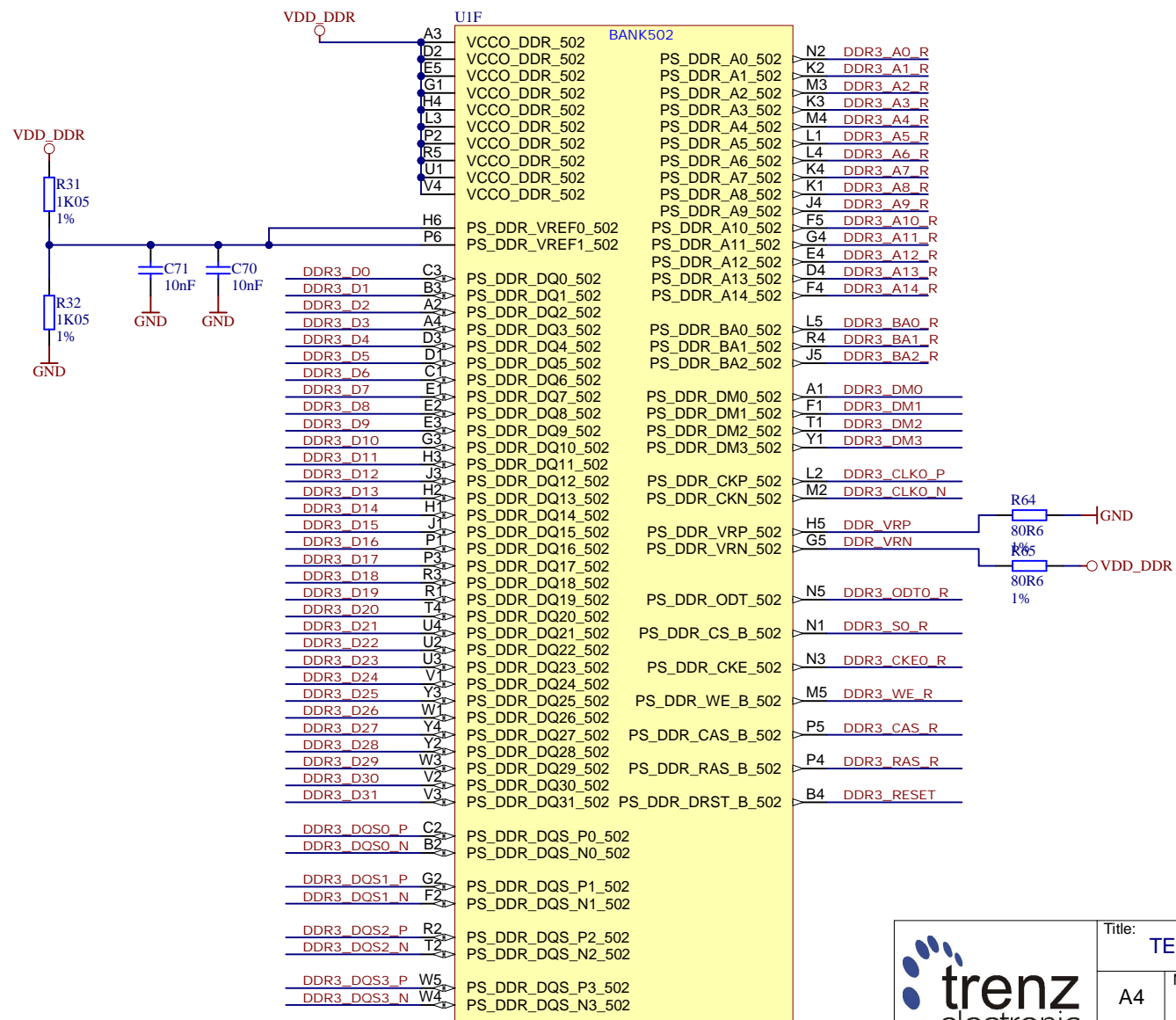
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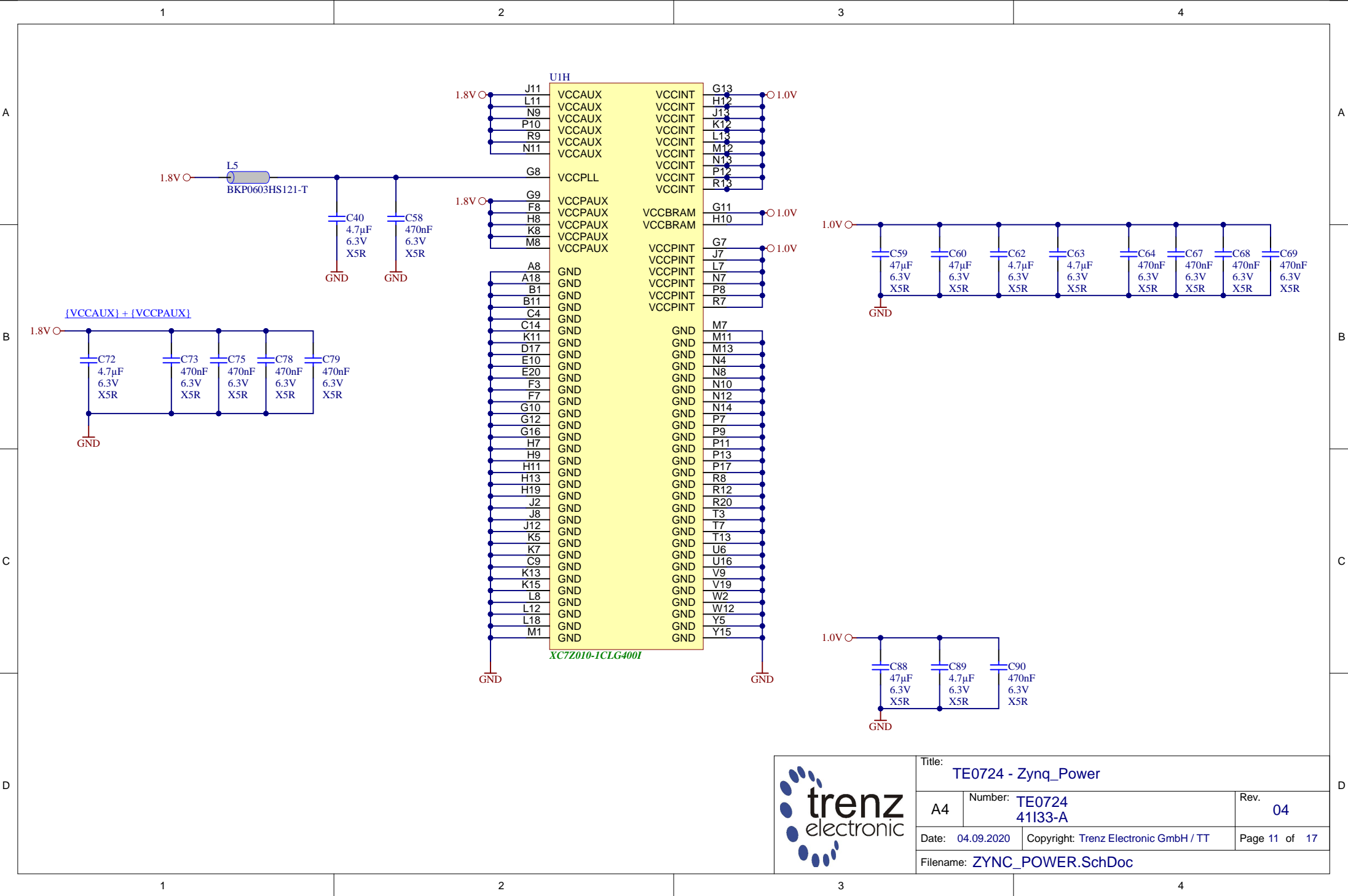
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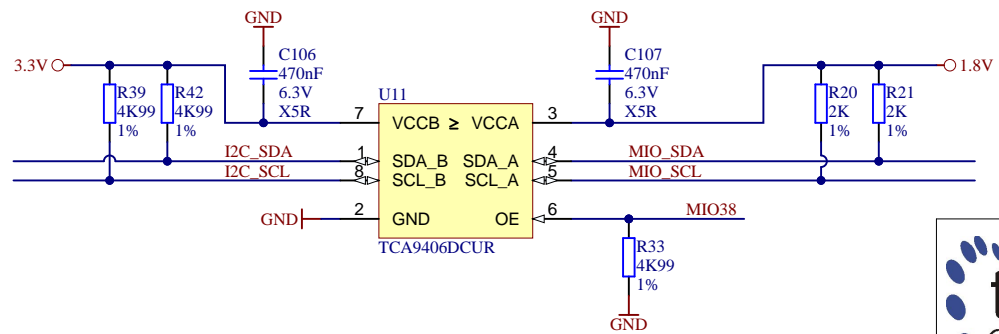
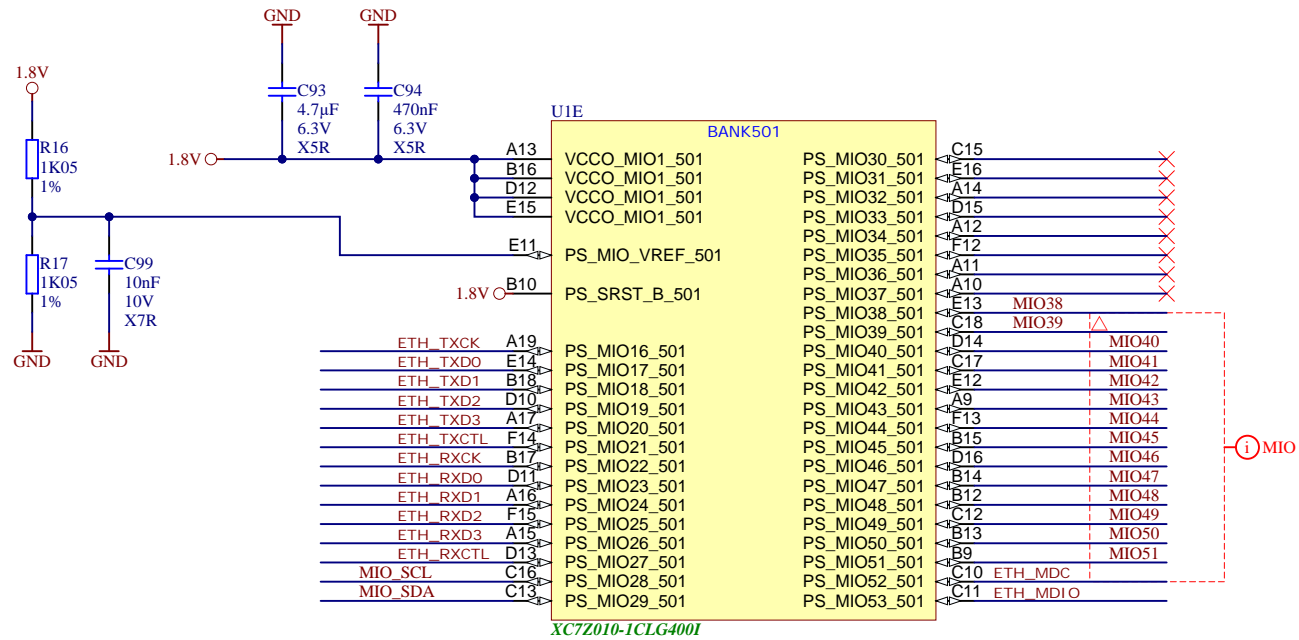

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Title: TE0724 - Zynq_PS_DDR		
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A

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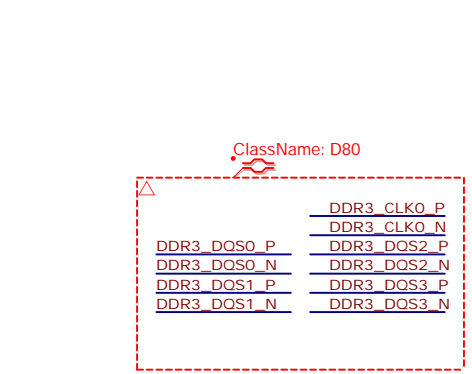
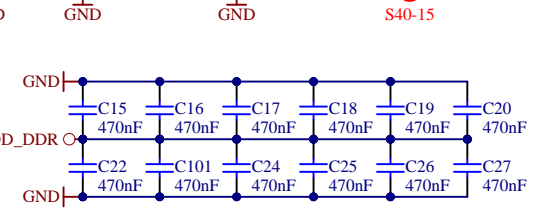
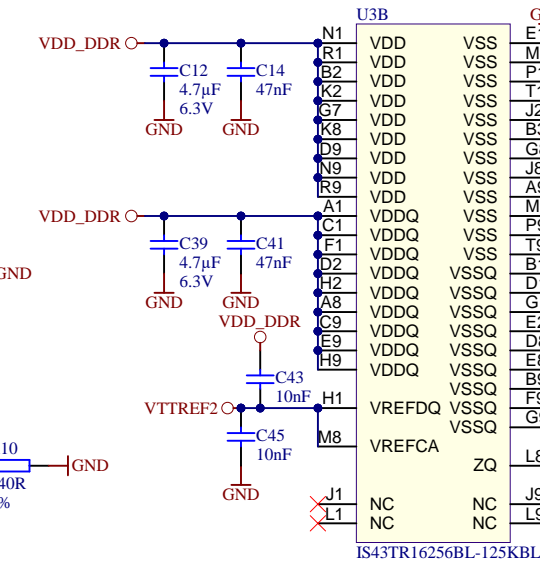
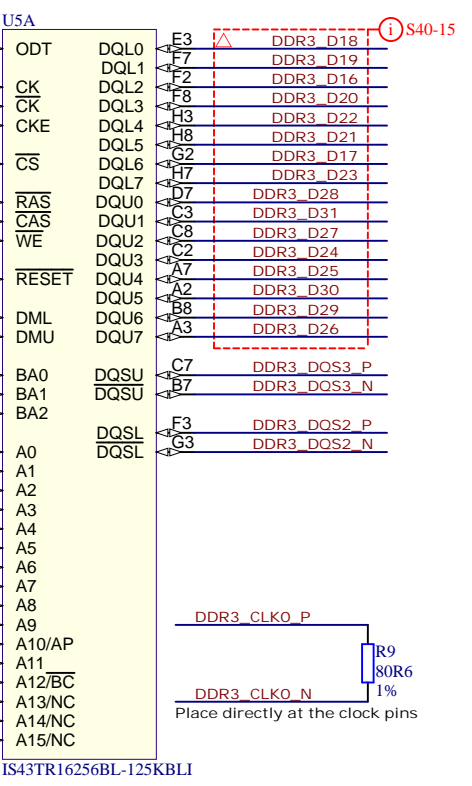
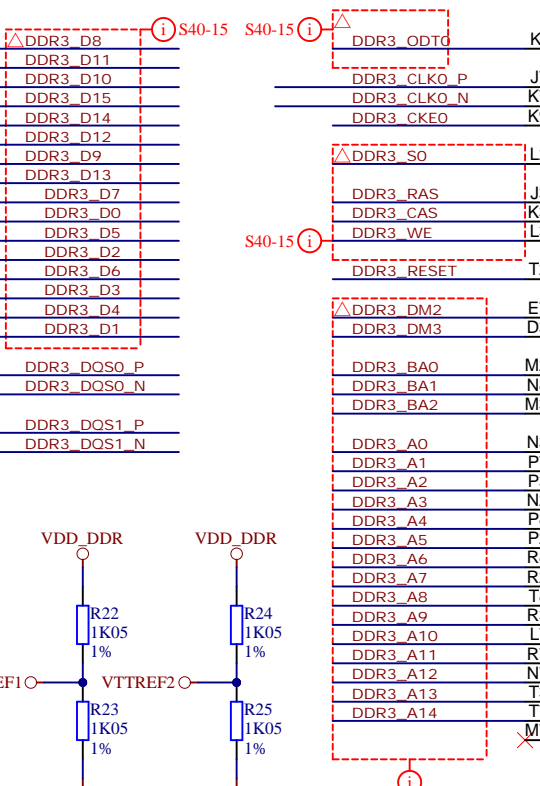
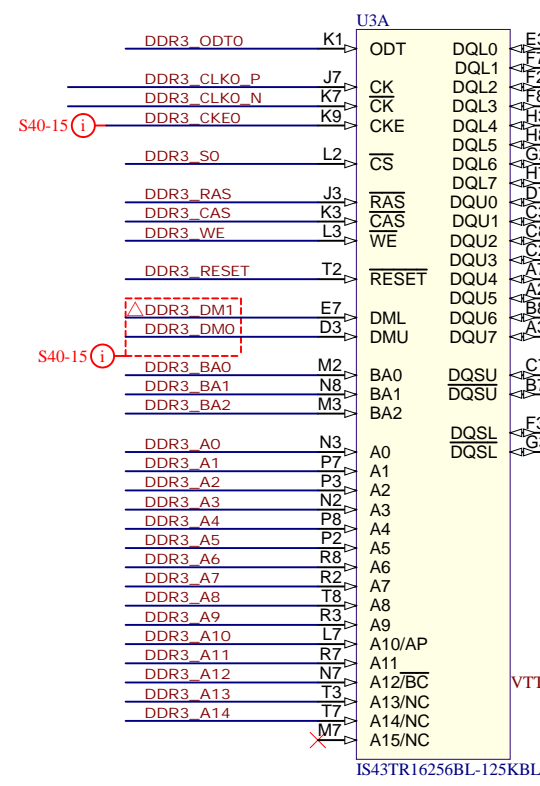
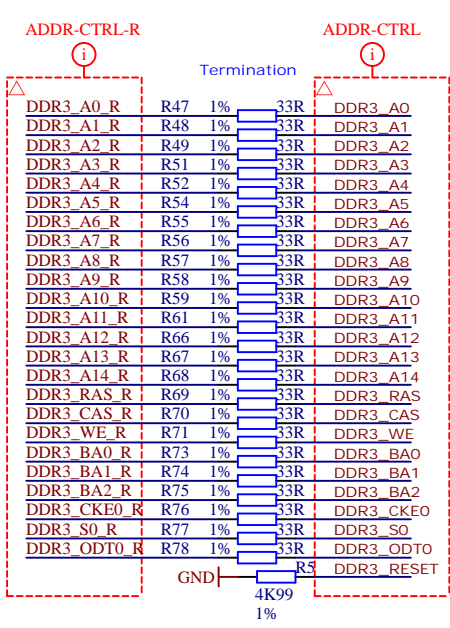
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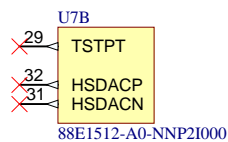
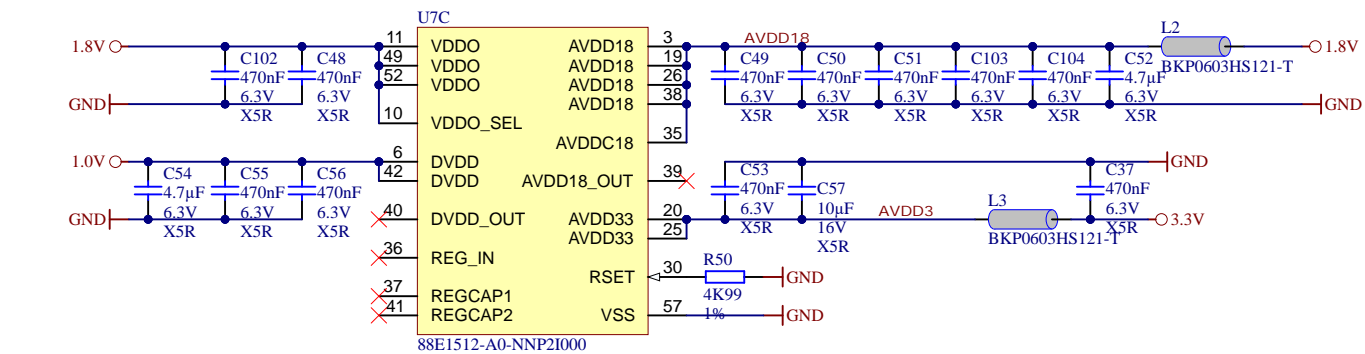
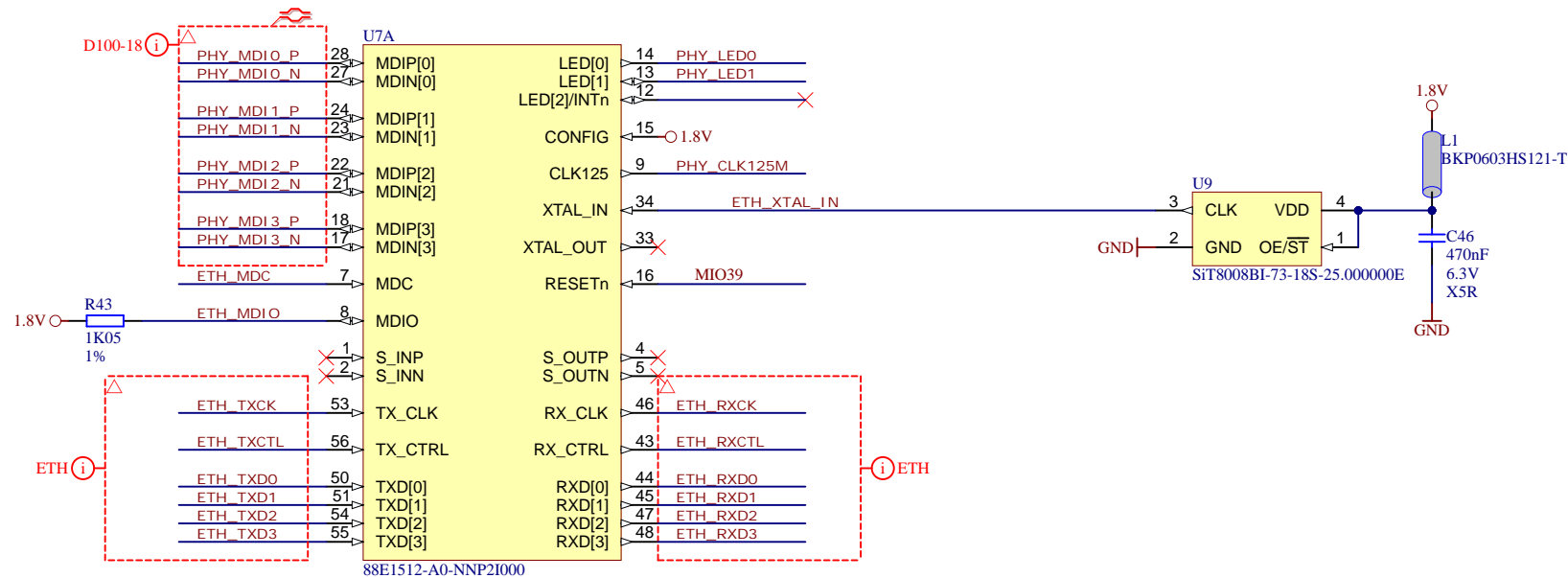
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D



Title: TE0724 - DDR3 RAM		
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A

A

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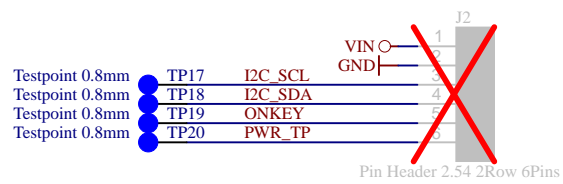
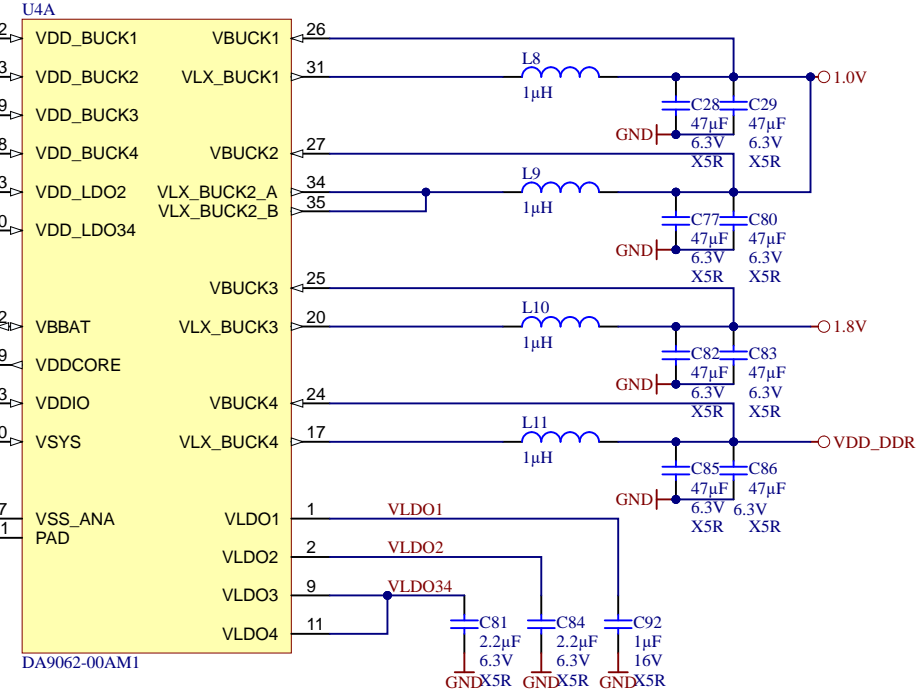
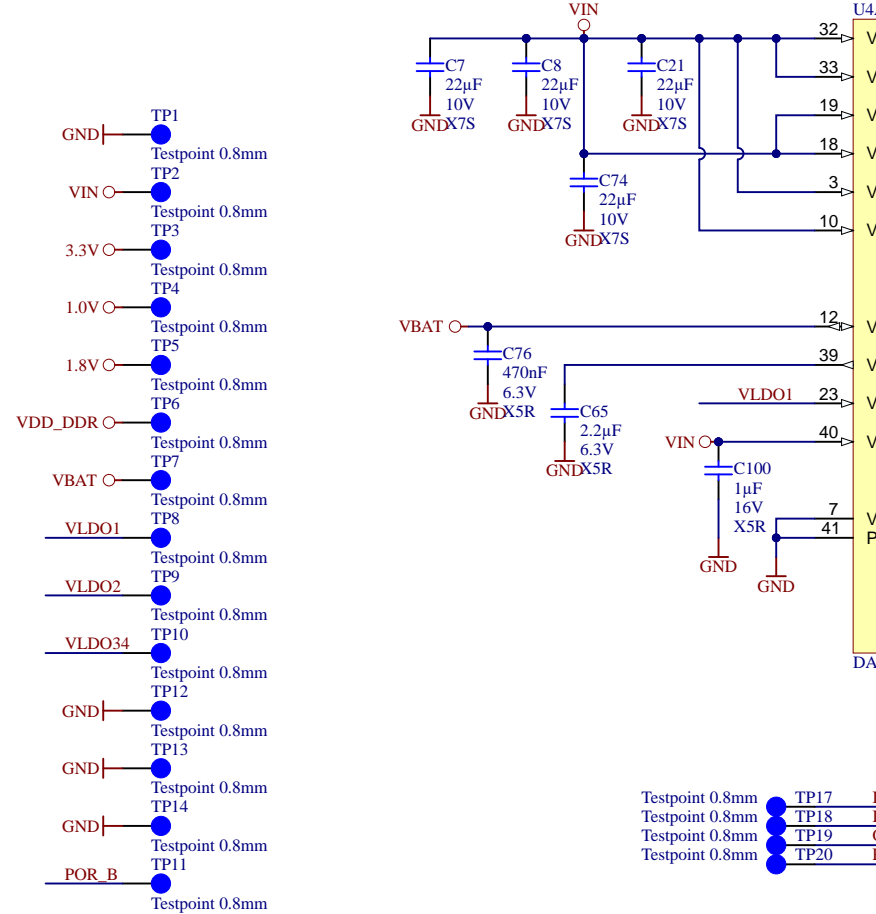
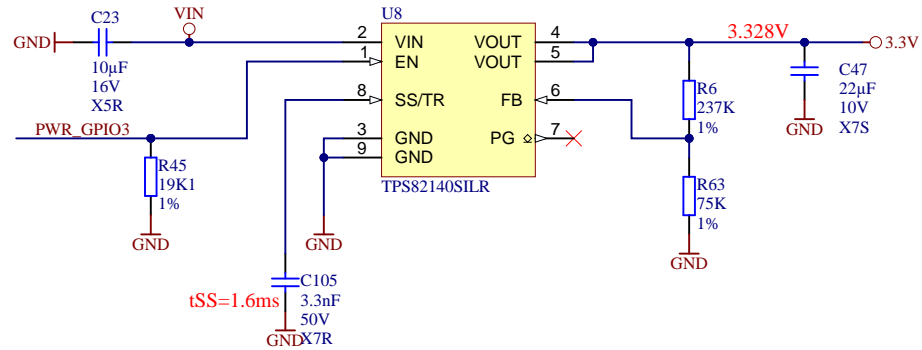
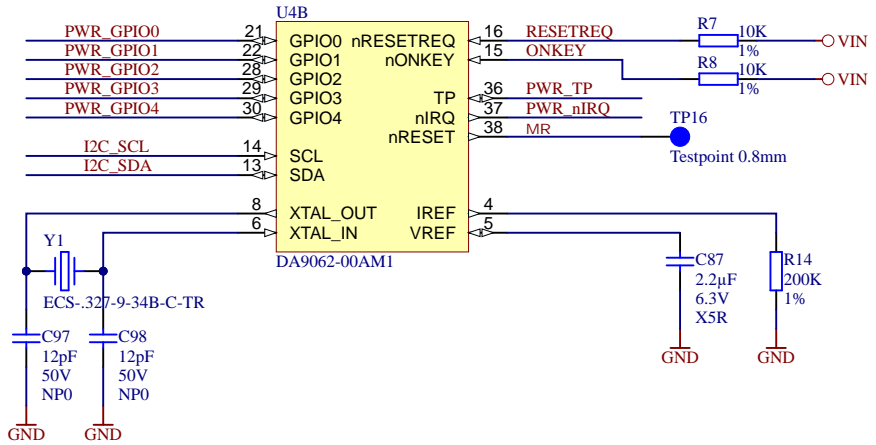
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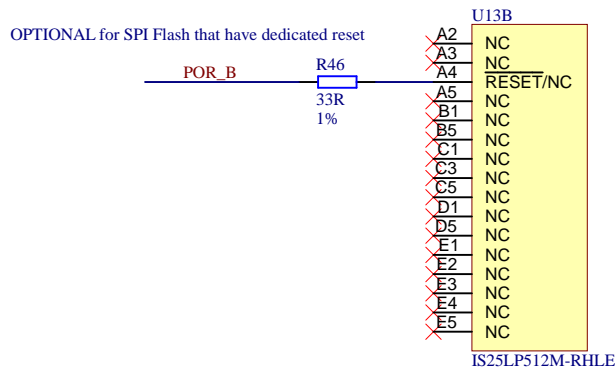
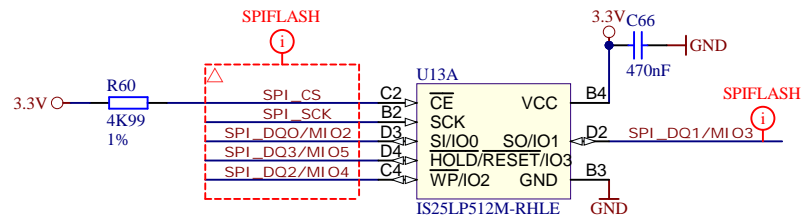
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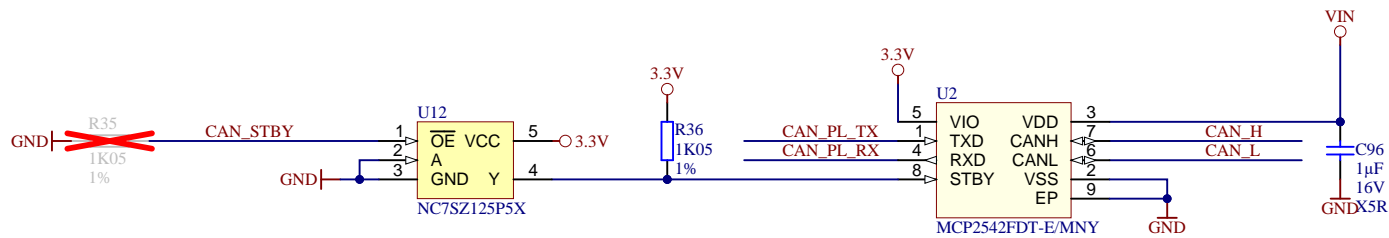
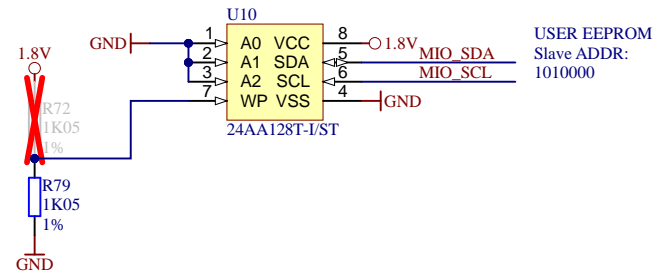
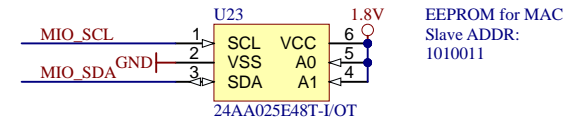
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3

4



Optional EEPROM Memories



		Title: TE0724 - QSPI MicroSD	
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REV02

- 1) New I2C translator U11: TCA9406DCUR
- 2) Fixed boot mode connection. Mode0 pulled-up by R27 and Mode 1 pulled-up by R33
- 3) Green LED D3 replaced to Red LED
- 4) C91 changed from 47 to 22uF
- 5) C3 not fitted
- 6) C105 deleted, C47 replaced from 10 to 22uF (EP53A7HQI output capacitor)
- 7) PWR_GPIO3 (EP53A7HQI enable) pulled down by R45 (19.1 kOhm)
- 8) DONE, INIT, PROG_B pulled-up to 3.3V
- 9) Added testpoints: JTAG, PMIC (I2C, ONKEY, TP)
- 10) J2 changed to 2 row 6-pin header. To J2 added ONKEY, PWR_TP, VIN
- 11) Mounting holes changed from 2mm to 2.2mm

REV02A

- 1) PCB revision: all vias are epoxy filled and copper capped. No mask openings on vias. No electrical changes

REV03


- 1) Replace DCDC U8 by TPS82140

21.02.2020 MR

- 2) update from Lib (Sch symbol of I2C levelshifter corrected)

REV04

- 1) Replaced I2C pullups by 2K R20 and R21.
- 2) Connected WP (pin 7) of EEPROM (U10) via R79 to GND, alternative R72 can be assembled for write protection.
- 3) Changed C7, C8, C21, C47, C74, C91 to same size X7S.
- 4) Moved following components slightly away from FPGA: C28, C29, C77, C80, R2, R12, R18, R43, R47, R51, R54, R57, R62, L8, L9.
- 5) Replaced DDR3 from IM4G16D3FABG-125I to IS43TR16256BL-125KBLI
- 6) Replaced Flash from S25FL256SAGBH120 to IS25LP512M-RHLE
- 7) Set S/N to not fitted.
- 8) Added legal notices for Trenz modules.
- 9) Full update from Library.

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