

1

2

3

4

A

A

B

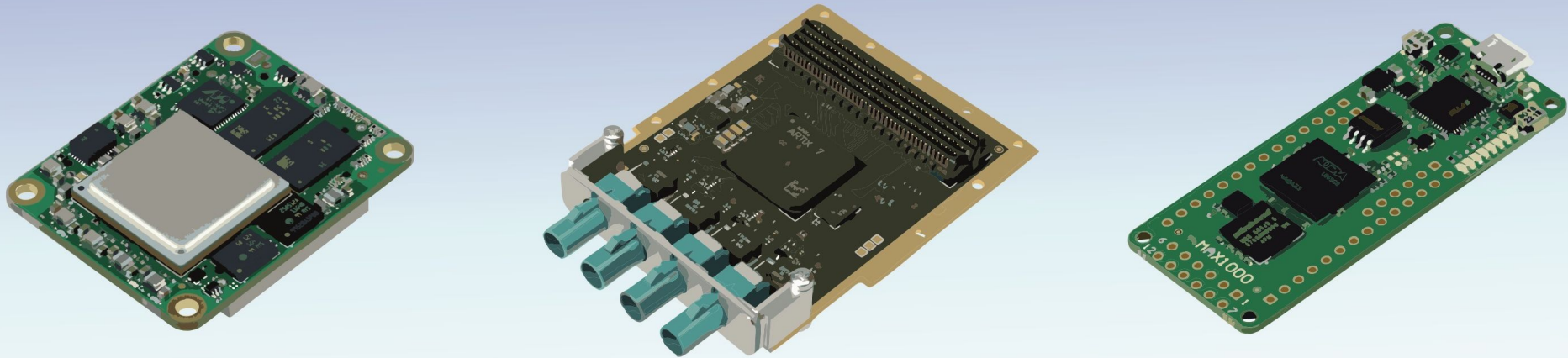
B

C

C

D


D



Regarding the usage of our schematics and alike documentation for Trenz module TE0724.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0724 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: TE0724		
	A4	Number: TE0724 61133-A	Rev. 04
	Date: 2020-08-21	Copyright: Trenz Electronic GmbH / TT	Page 1 of 17
	Filename: Legal Notices Modules.SchDoc		

1

2

3

4

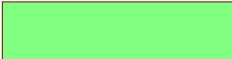
1

2

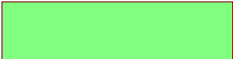
3

4

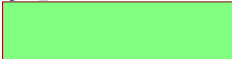
U_J1
J1.SchDoc




U_DDR3
DDR3-RAM.SchDoc




QSPI_MicroSD
QSPI_MicroSD.SchDoc




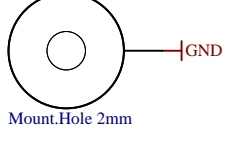
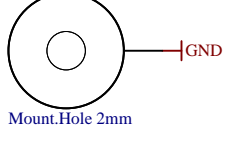
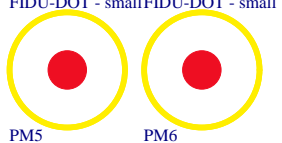
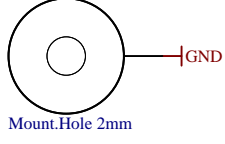
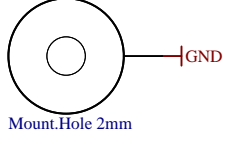
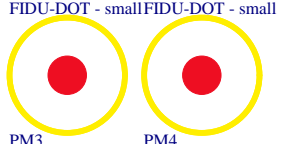
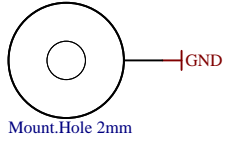
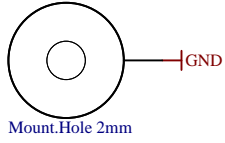
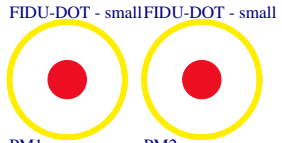
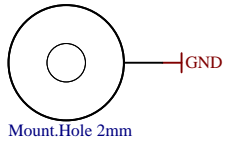
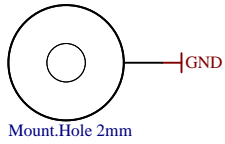
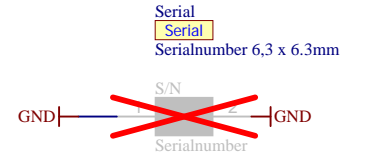
U_ZYNQ
ZYNQ.SchDoc



U_ETH_PHY
ETH-PHY.SchDoc



U_POWER
POWER.SchDoc

Design drawn by:	MR
Checked by:	IG
Assembly variant:	61133-A
Created by:	VT
Modified by:	MR
Modified at:	2020-09-04



Title: TE0724		
A4	Number: TE0724 61133-A	Rev. 04
Date: 04.09.2020	Copyright: Trenz Electronic GmbH / TT	Page 2 of 17
Filename: TE0724.SchDoc		

1

2

3

4

1

2

3

4

A

A

B

B

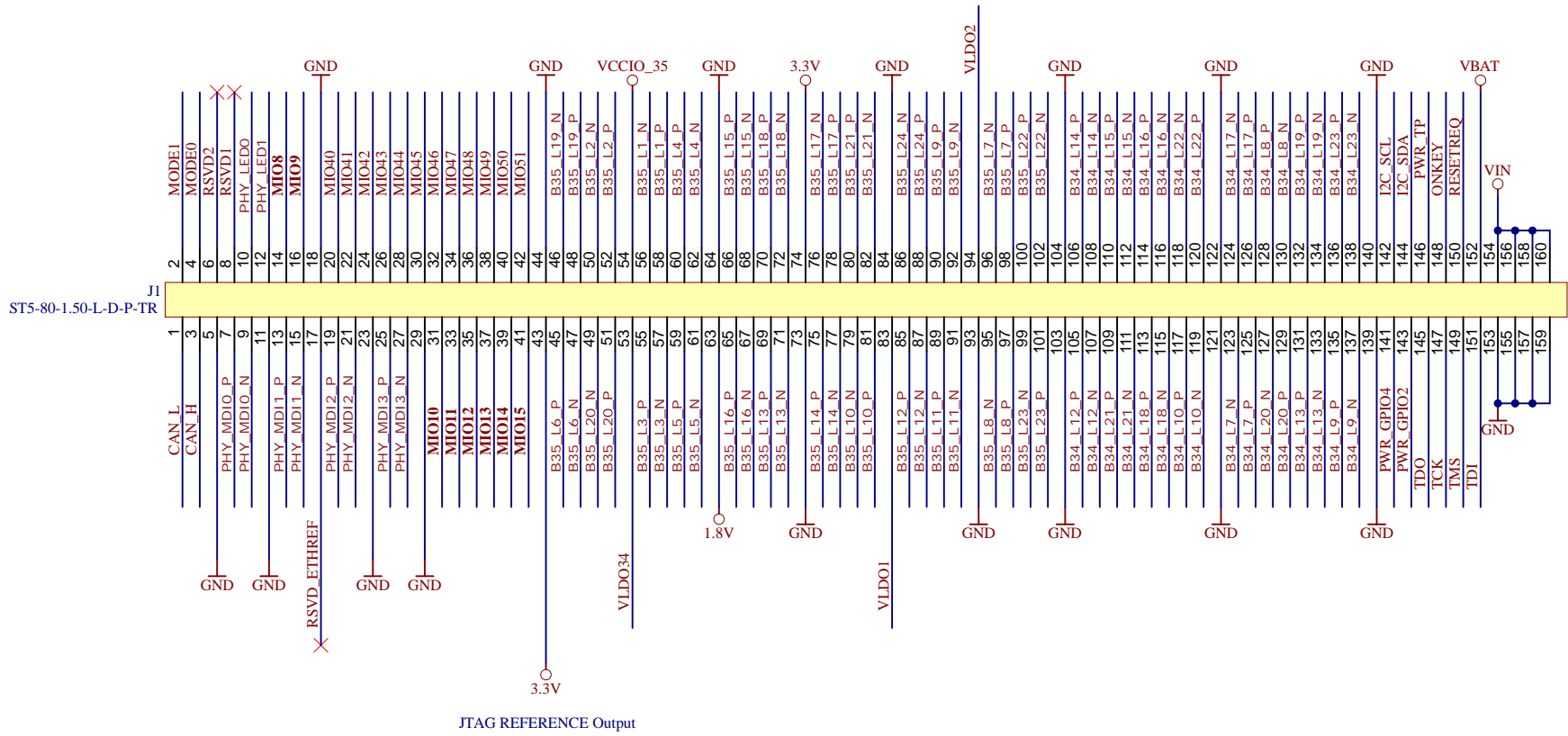
C

C

D

D

MIO0 - 8 I/O 3.3V
 MIO1 - 12 I/O 1.8V
 B34 - 32 I/O 3.3V
 B35 - 24 LVDS or 48 I/O Variable




Title: TE0724 - B2B connectors J1

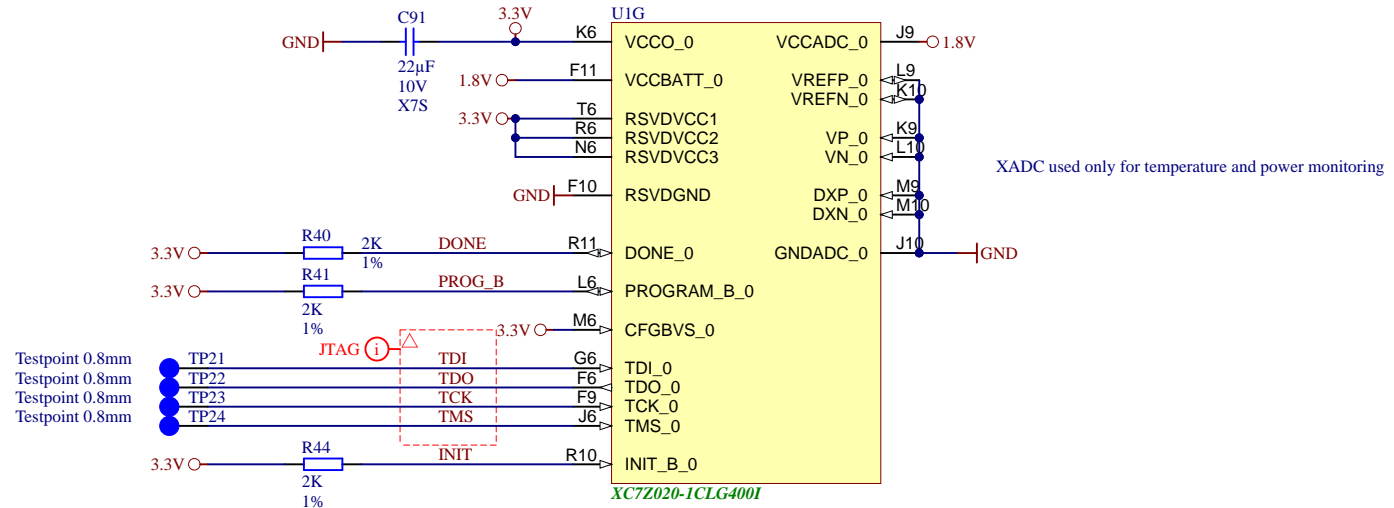
A4	Number: TE0724 61133-A	Rev. 04
Date: 04.09.2020	Copyright: Trenz Electronic GmbH / TT	Page 3 of 17
Filename: J1.SchDoc		


1

2

3

4



		Title: TE0724 - Zynq_MISC	
		A4	Number: TE0724 61133-A
Date: 04.09.2020		Copyright: Trenz Electronic GmbH / TT	
Page 4 of 17			
Filename: ZYNQ_MISC.SchDoc			

1

2

3

4

A

A

B

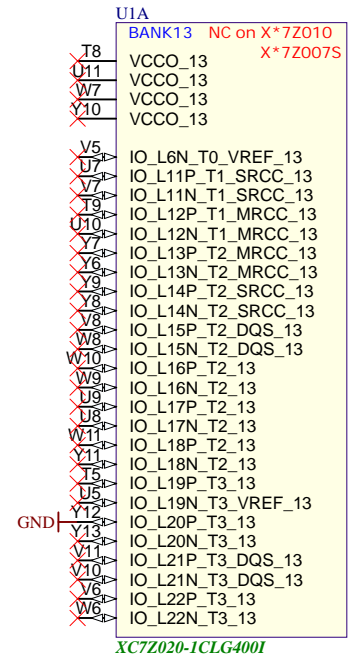
B


C

C

D

D



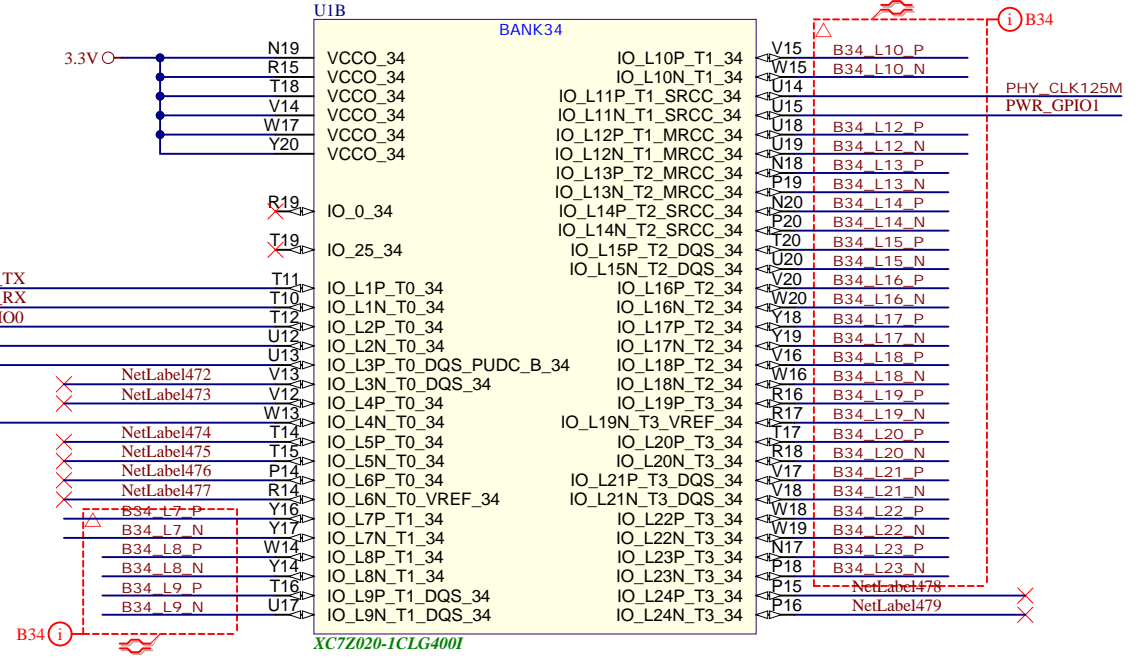
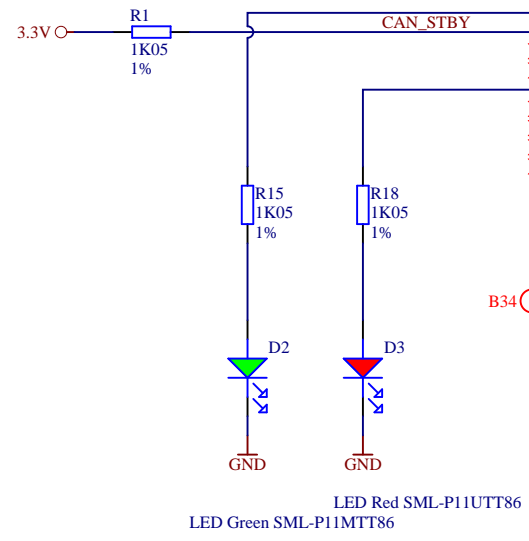
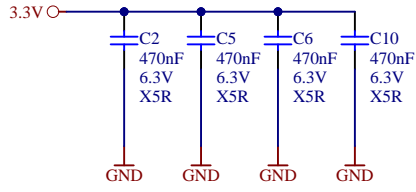
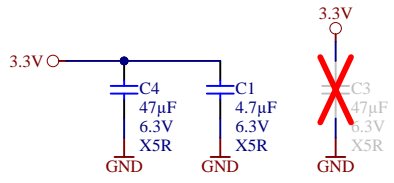
			Title: TE0724 - Zynq_B13	
			A4	Number: TE0724 61133-A
Date: 04.09.2020		Copyright: Trenz Electronic GmbH / TT		Page 5 of 17
Filename: B13.SchDoc				

1

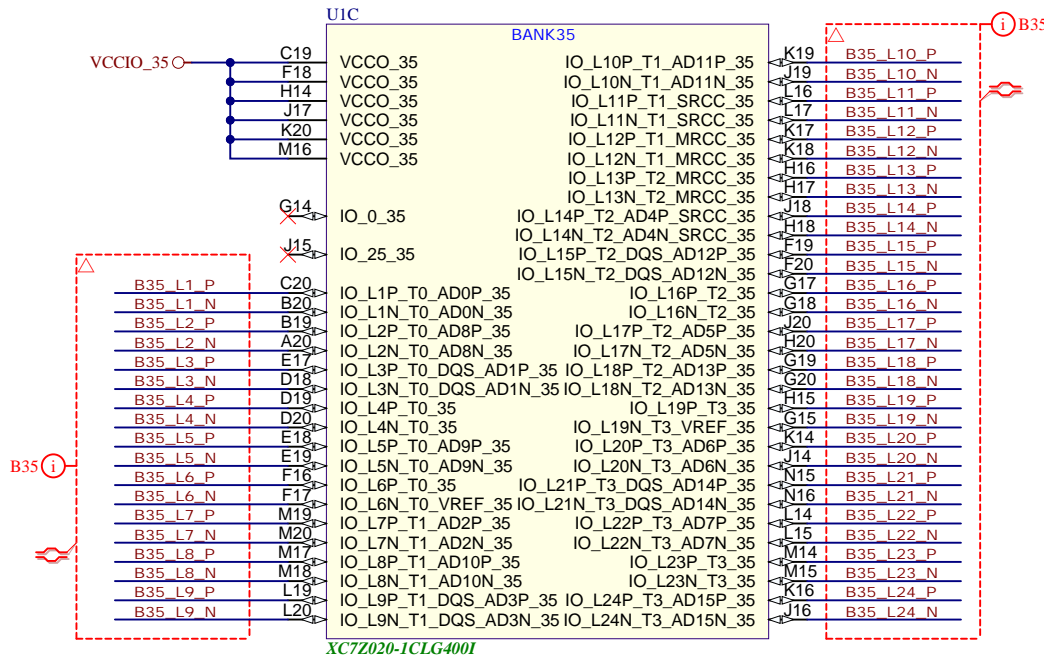
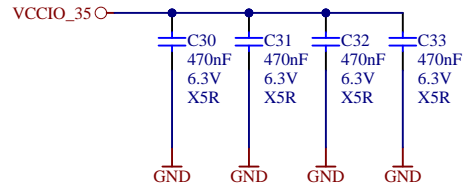
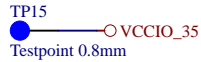
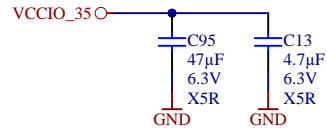
2

3

4



Title: TE0724 - Zynq_B34		
A4	Number: TE0724 61133-A	Rev. 04
Date: 04.09.2020	Copyright: Trenz Electronic GmbH / TT	Page 6 of 17
Filename: B34.SchDoc		



Title: TE0724 - Zynq_B35		
A4	Number: TE0724 61133-A	Rev. 04
Date: 04.09.2020	Copyright: Trenz Electronic GmbH / TT	Page 7 of 17
Filename: B35.SchDoc		

1

2

3

4

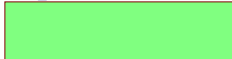
A

A

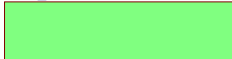
U_B13
B13.SchDoc



U_B500
MIO_B500.SchDoc



U_B501
MIO_B501.SchDoc



U_PS_DDR
PS-DDR.SchDoc



U_MISC
ZYNQ_MISC.SchDoc



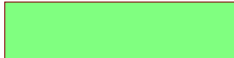
U_B34
B34.SchDoc



U_ZYNQ_POWER
ZYNQ_POWER.SchDoc



U_B35
B35.SchDoc



B

B

C

C

D

D



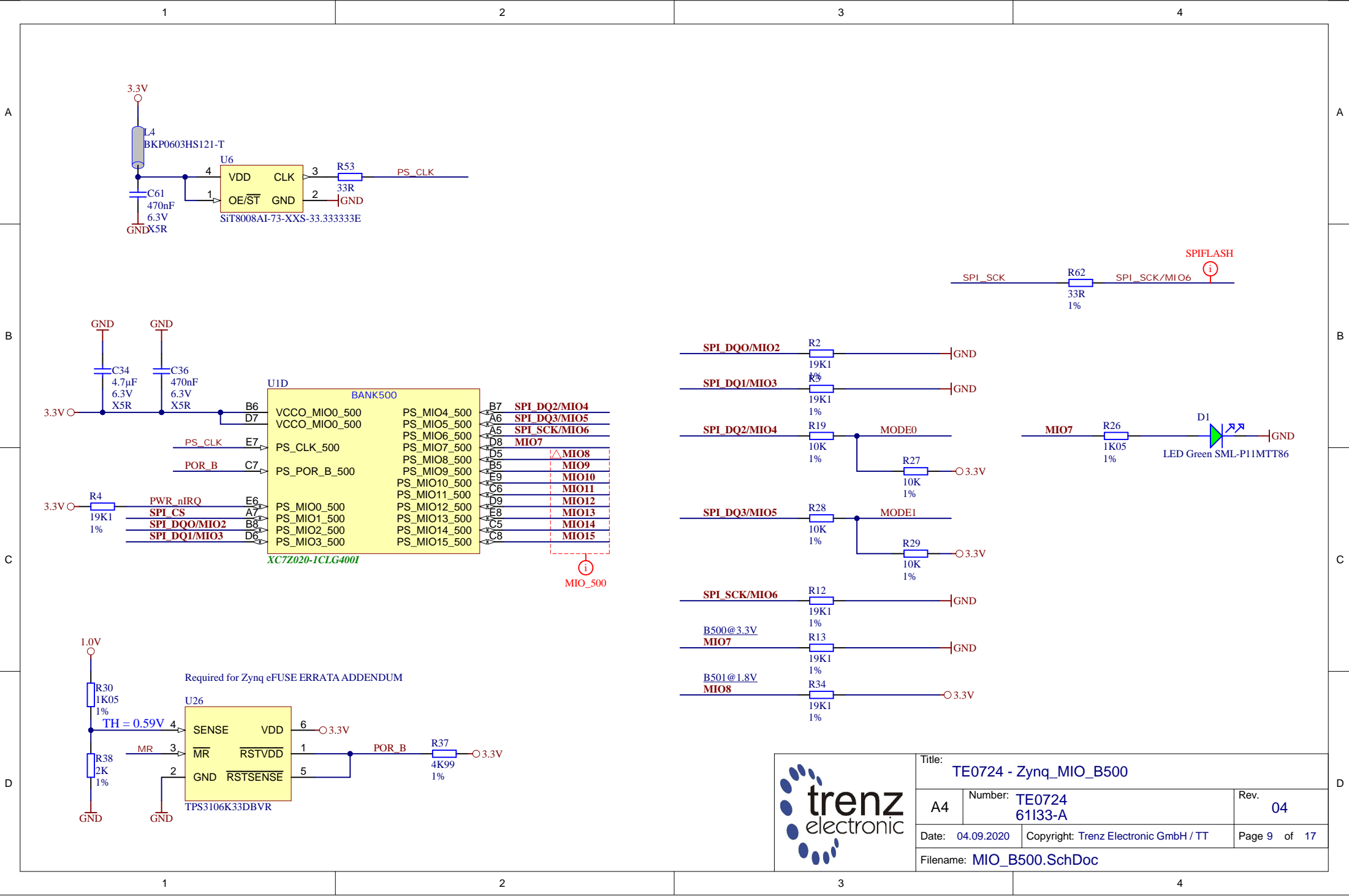
Title: TE0724 - Zynq		
A4	Number: TE0724 61133-A	Rev. 04
Date: 21.08.2020	Copyright: Trenz Electronic GmbH / TT	Page 8 of 17
Filename: ZYNQ.SchDoc		


1

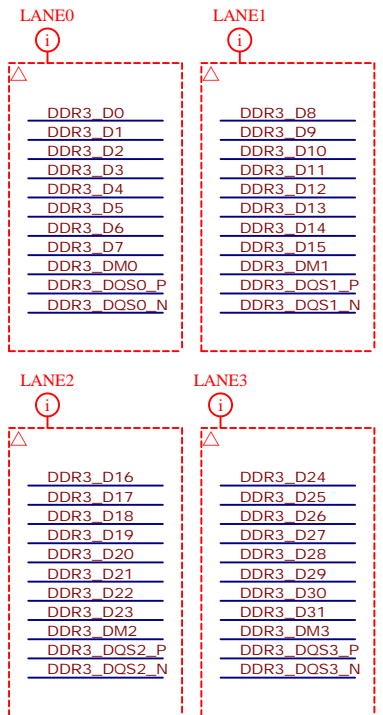
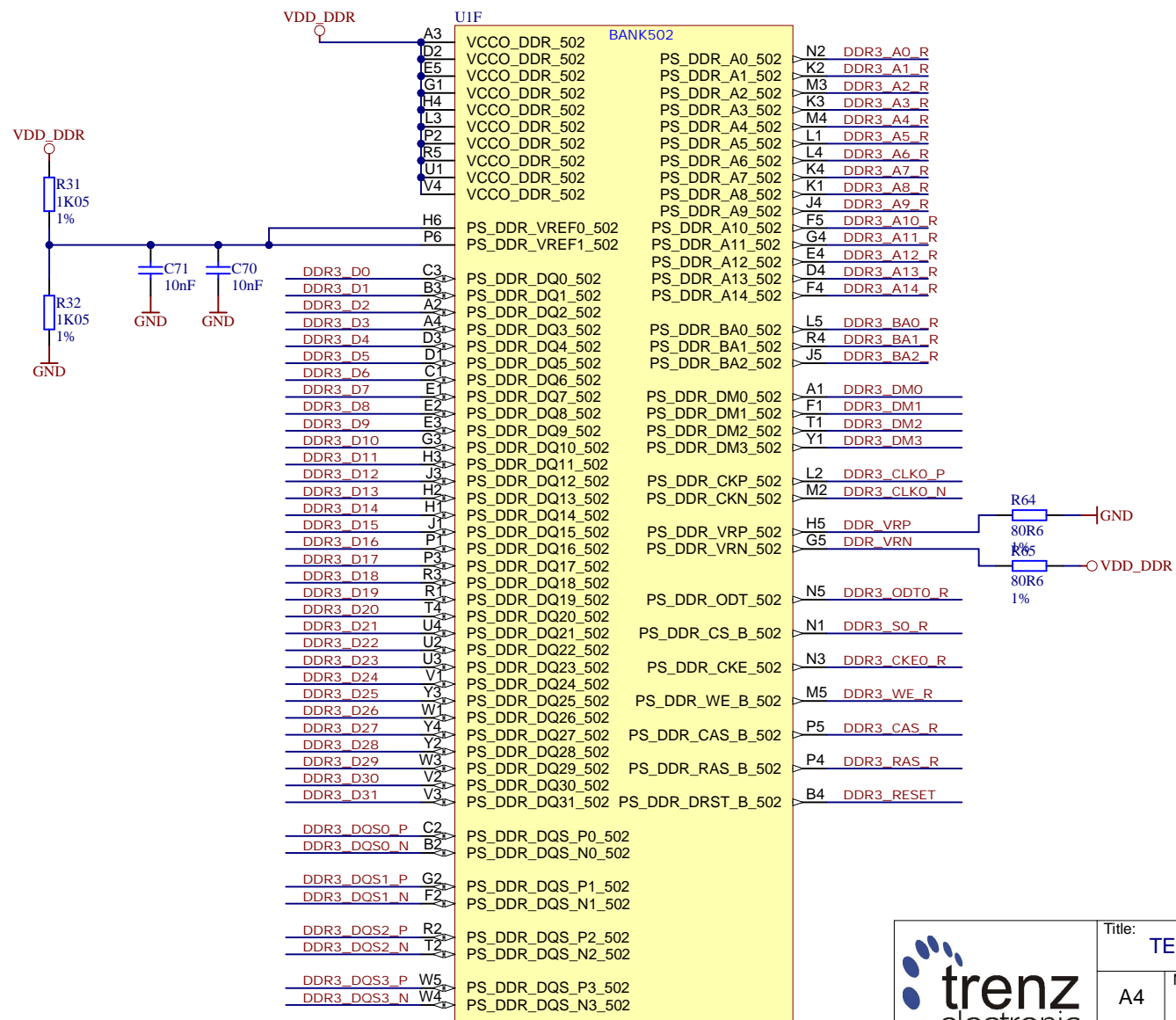
2


3

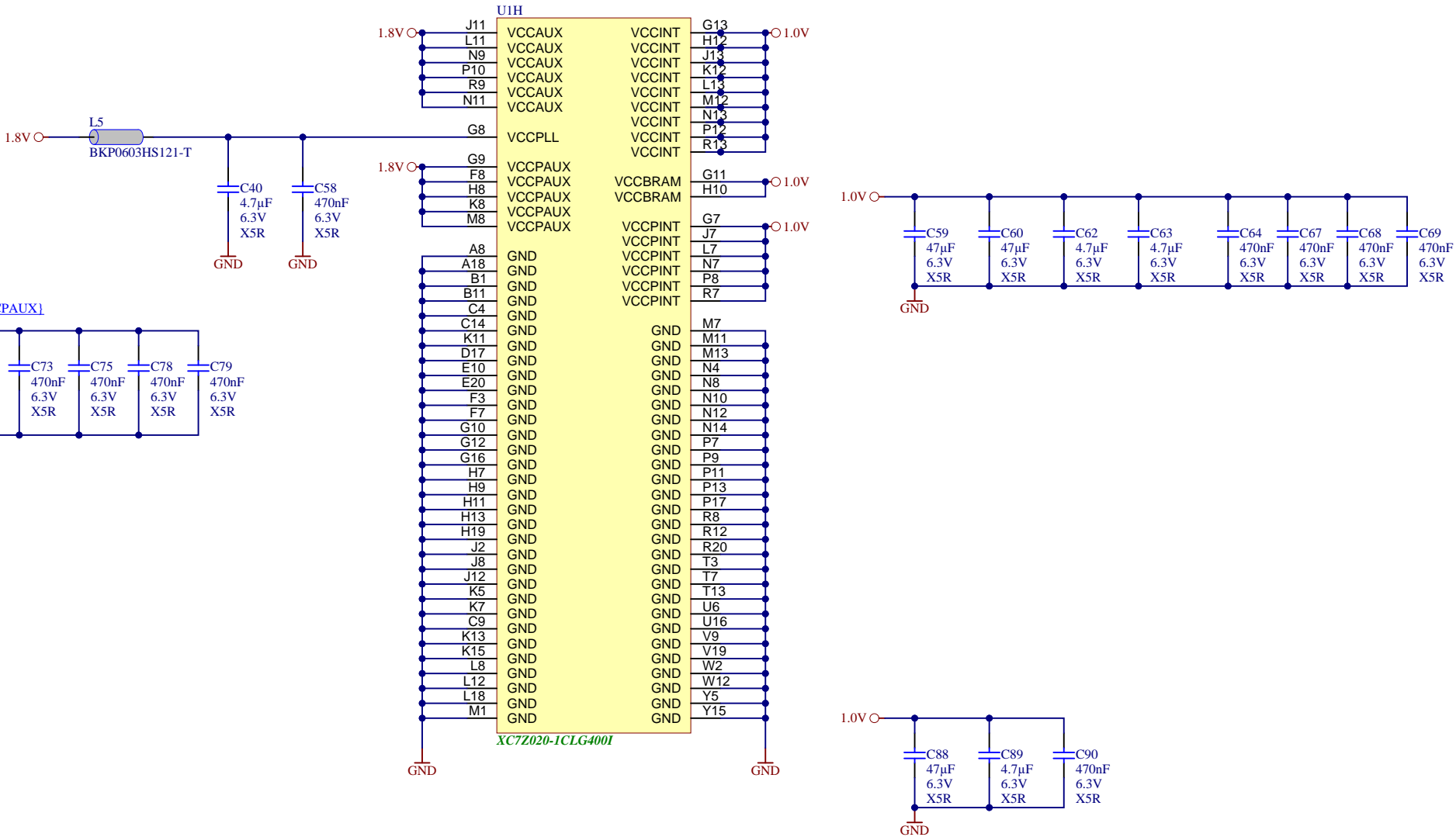
4



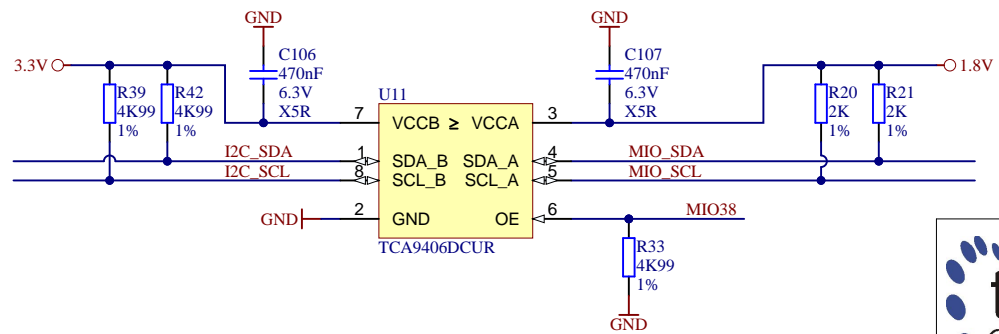
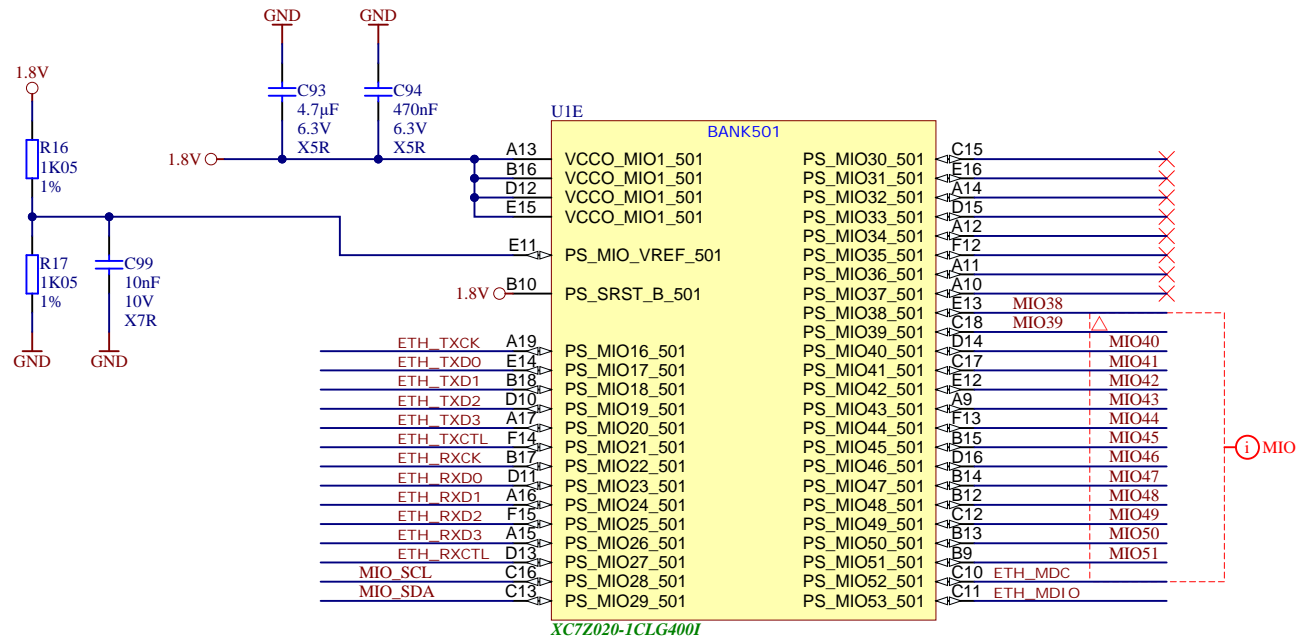
			Title: TE0724 - Zynq_MIO_B500	
			A4	Number: TE0724 61133-A
Date: 04.09.2020		Copyright: Trenz Electronic GmbH / TT		Page 9 of 17
Filename: MIO_B500.SchDoc				




		Title: TE0724 - Zynq_PS_DDR	
		A4	Number: TE0724 61133-A
Date: 04.09.2020		Copyright: Trenz Electronic GmbH / TT	
Filename: PS-DDR.SchDoc		Page 10 of 17	



Title: TE0724 - Zynq_Power		
A4	Number: TE0724 61133-A	Rev. 04
Date: 04.09.2020	Copyright: Trenz Electronic GmbH / TT	Page 11 of 17
Filename: ZYNC_POWER.SchDoc		



			Title: TE0724 - Zynq_MIO_B501	
			A4	Number: TE0724 61133-A
Date: 04.09.2020		Copyright: Trenz Electronic GmbH / TT		Page 12 of 17
Filename: MIO_B501.SchDoc				

A

B

C

D

A

B

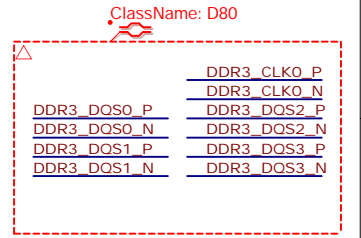
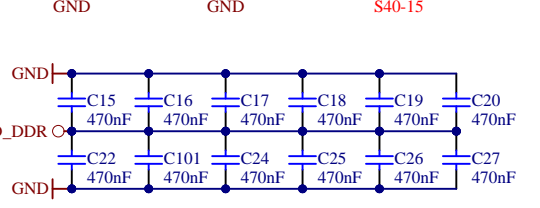
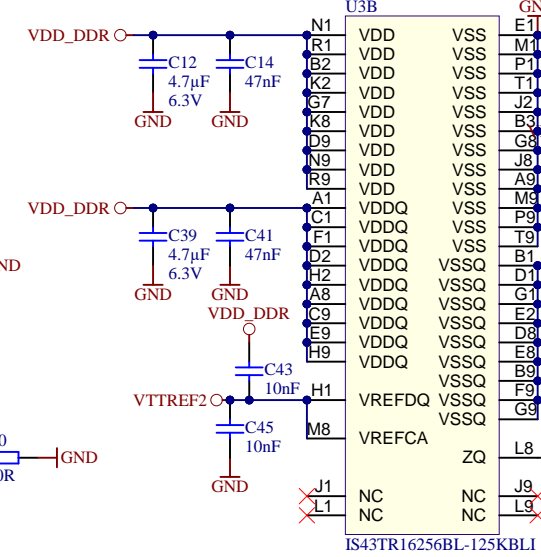
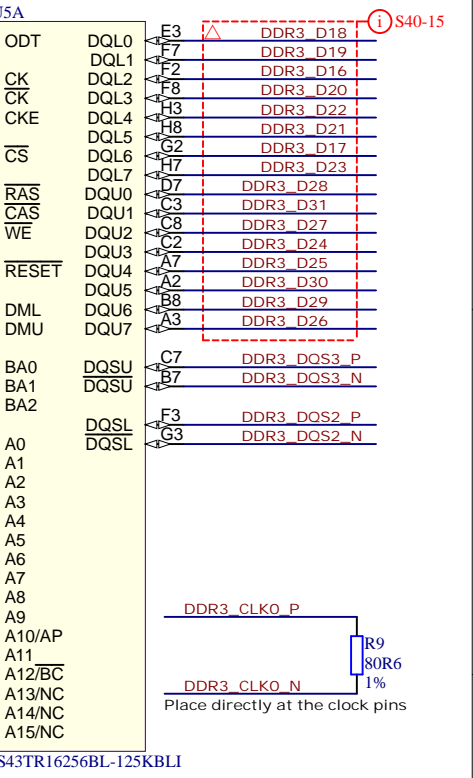
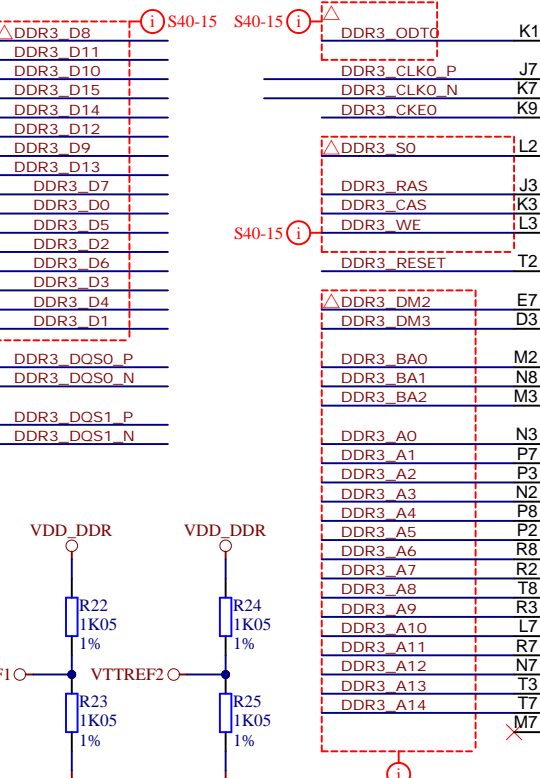
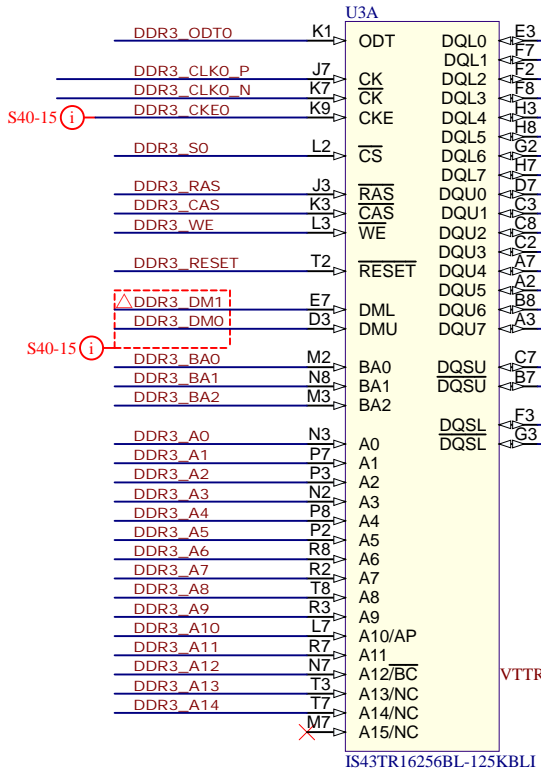
C

D

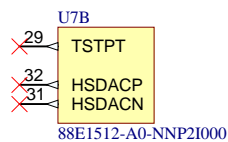
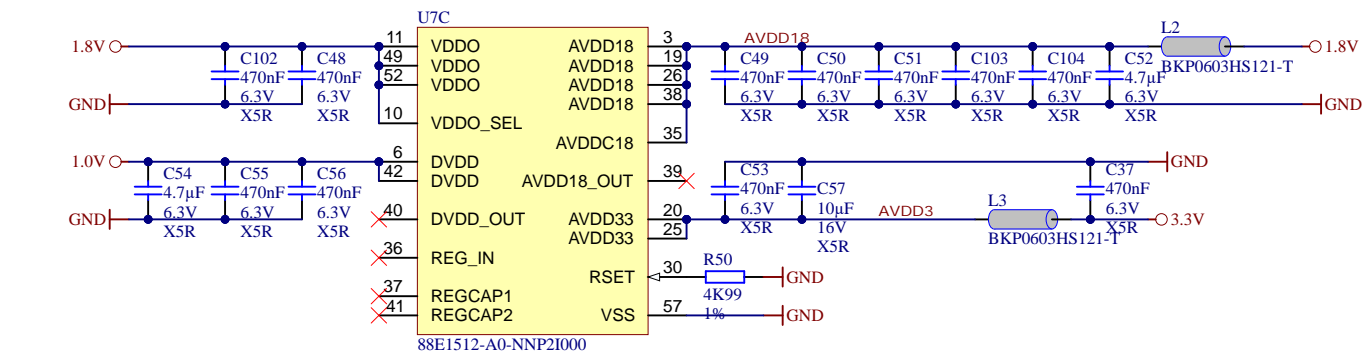
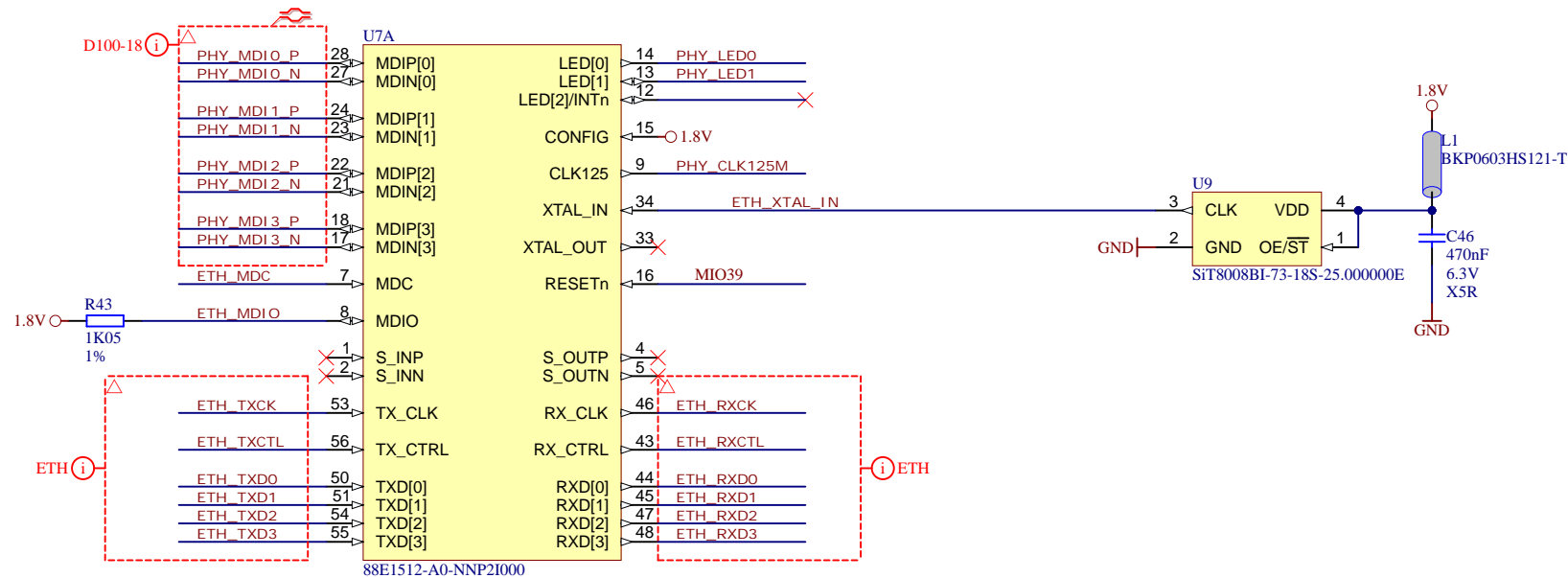
ADDR-CTRL-R ADDR-CTRL


Termination

DDR3_A0_R	R47	1%	33R	DDR3_A0
DDR3_A1_R	R48	1%	33R	DDR3_A1
DDR3_A2_R	R49	1%	33R	DDR3_A2
DDR3_A3_R	R51	1%	33R	DDR3_A3
DDR3_A4_R	R52	1%	33R	DDR3_A4
DDR3_A5_R	R54	1%	33R	DDR3_A5
DDR3_A6_R	R55	1%	33R	DDR3_A6
DDR3_A7_R	R56	1%	33R	DDR3_A7
DDR3_A8_R	R57	1%	33R	DDR3_A8
DDR3_A9_R	R58	1%	33R	DDR3_A9
DDR3_A10_R	R59	1%	33R	DDR3_A10
DDR3_A11_R	R61	1%	33R	DDR3_A11
DDR3_A12_R	R66	1%	33R	DDR3_A12
DDR3_A13_R	R67	1%	33R	DDR3_A13
DDR3_A14_R	R68	1%	33R	DDR3_A14
DDR3_RAS_R	R69	1%	33R	DDR3_RAS
DDR3_CAS_R	R70	1%	33R	DDR3_CAS
DDR3_WE_R	R71	1%	33R	DDR3_WE
DDR3_BA0_R	R73	1%	33R	DDR3_BA0
DDR3_BA1_R	R74	1%	33R	DDR3_BA1
DDR3_BA2_R	R75	1%	33R	DDR3_BA2
DDR3_CKE0_R	R76	1%	33R	DDR3_CKE0
DDR3_S0_R	R77	1%	33R	DDR3_S0
DDR3_ODT0_R	R78	1%	33R	DDR3_ODT0
	R5			DDR3_RESET
			4K99	GND
			1%	



Title: TE0724 - DDR3 RAM		
A4	Number: TE0724 61133-A	Rev. 04
Date: 2017-05-30	Copyright: Trenz Electronic GmbH	Page 13 of 17
Filename: DDR3-RAM.SchDoc		



		Title: TE0724 - ETH_PHY	
		A4	Number: TE0724 61133-A
Date: 04.09.2020		Copyright: Trenz Electronic GmbH / TT	
Filename: ETH-PHY.SchDoc			

1

2

3

4

A

A

B

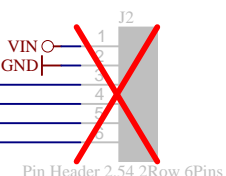
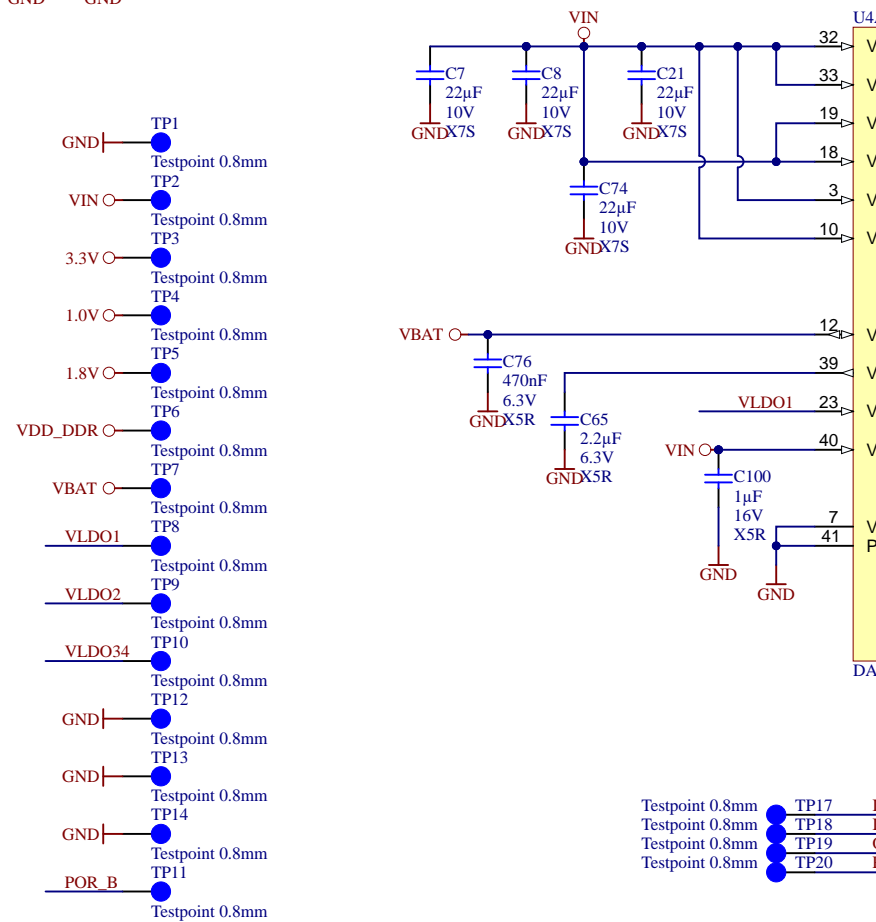
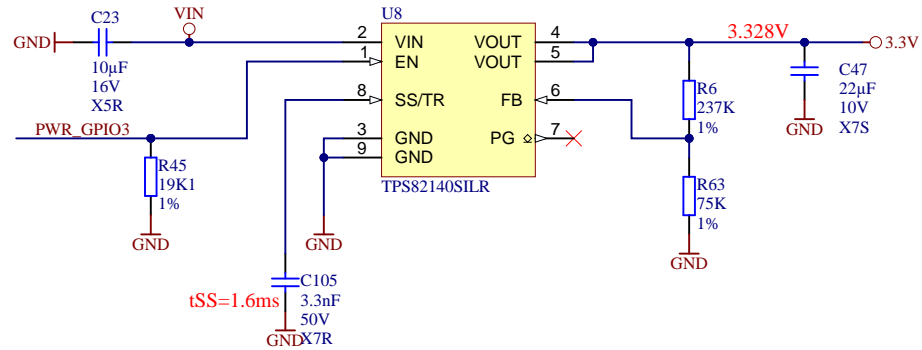
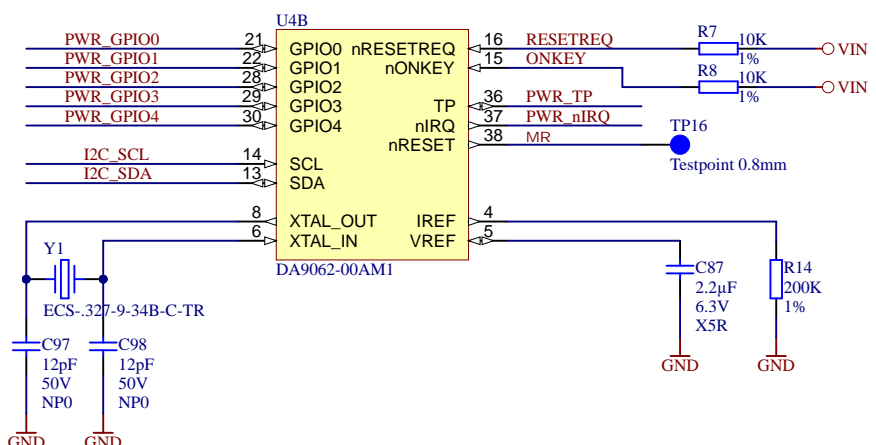
B

C

C

D

D



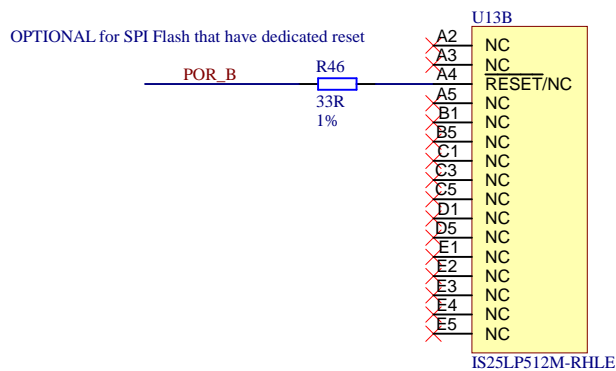
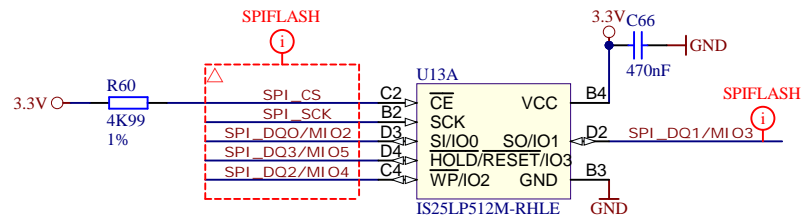
Title: TE0724 - Power		
A4	Number: TE0724 61133-A	Rev. 04
Date: 04.09.2020	Copyright: Trenz Electronic GmbH / TT	Page 15 of 17
Filename: POWER.SchDoc		

1

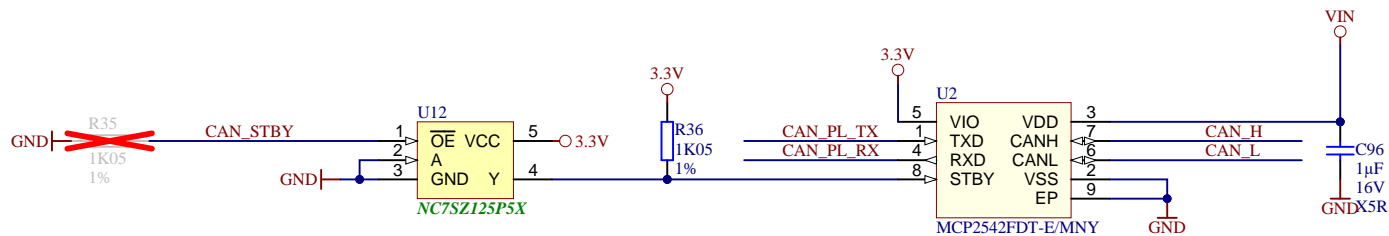
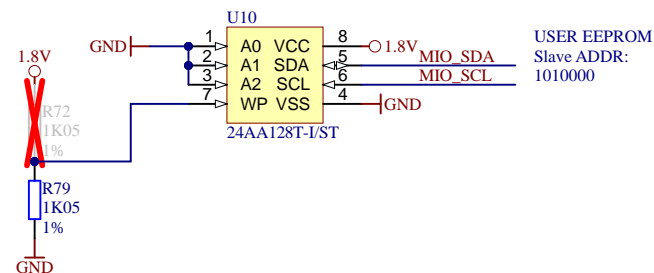
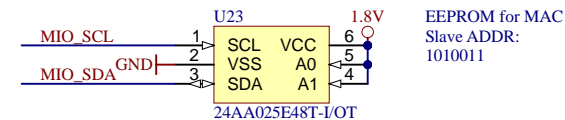
2


3

4



Optional EEPROM Memories



		Title: TE0724 - QSPI MicroSD	
		A4	Number: TE0724 61133-A
Date: 04.09.2020		Copyright: Trenz Electronic GmbH / TT	
Filename: QSPI_MicroSD.SchDoc			

REV02

- 1) New I2C translator U11: TCA9406DCUR
- 2) Fixed boot mode connection. Mode0 pulled-up by R27 and Mode 1 pulled-up by R33
- 3) Green LED D3 replaced to Red LED
- 4) C91 changed from 47 to 22uF
- 5) C3 not fitted
- 6) C105 deleted, C47 replaced from 10 to 22uF (EP53A7HQI output capacitor)
- 7) PWR_GPIO3 (EP53A7HQI enable) pulled down by R45 (19.1 kOhm)
- 8) DONE, INIT, PROG_B pulled-up to 3.3V
- 9) Added testpoints: JTAG, PMIC (I2C, ONKEY, TP)
- 10) J2 changed to 2 row 6-pin header. To J2 added ONKEY, PWR_TP, VIN
- 11) Mounting holes changed from 2mm to 2.2mm

REV02A

- 1) PCB revision: all vias are epoxy filled and copper capped. No mask openings on vias. No electrical changes

REV03


- 1) Replace DCDC U8 by TPS82140

21.02.2020 MR

- 2) update from Lib (Sch symbol of I2C levelshifter corrected)

REV04

- 1) Replaced I2C pullups by 2K R20 and R21.
- 2) Connected WP (pin 7) of EEPROM (U10) via R79 to GND, alternative R72 can be assembled for write protection.
- 3) Changed C7, C8, C21, C47, C74, C91 to same size X7S.
- 4) Moved following components slightly away from FPGA: C28, C29, C77, C80, R2, R12, R18, R43, R47, R51, R54, R57, R62, L8, L9.
- 5) Replaced DDR3 from IM4G16D3FABG-125I to IS43TR16256BL-125KBLI
- 6) Replaced Flash from S25FL256SAGBH120 to IS25LP512M-RHLE
- 7) Set S/N to not fitted.
- 8) Added legal notices for Trenz modules.
- 9) Full update from Library.

	Title: TE0724 - Revision changes		
	A4	Number: TE0724 61133-A	Rev. 04
	Date: 04.09.2020	Copyright: Trenz Electronic GmbH / TT	Page 17 of 17
	Filename: Revision changes.SchDoc		