TE0724 Test Board

Revision v.12

Exported on 2023-08-07

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0724+Test+Board

1 Table of Contents

2 Table of Figures

3 Table of Tables

4 Overview

Zynq PS Design with Linux Example and Virtual Input/Output (VIO) for Control and Monitoring with Vivado HW-Manager.
Wiki Resources page: http://trenz.org/te0724-info

4.1 Key Features

- Vitis/Vivado 2021.2.1
- PetaLinux
- SD
- ETH
- MAC from EEPROM
- I2C
- RTC
- FMeter
- FSBL to enable I2C Buffer for PMIC (RTC) and external I2C

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2022-11-16	2021.2.1	TE0724-test_board-vivado_2021.2-build_20_20221119073924.zip TE0724-test_board_nopre built-vivado_2021.2-build_20_20221119073924.zip	Manuela Strücker	• Release Vivado 2021.2.1 • script update • new assembly variants
2020-03-25	2019.2	TE0724-test_board-vivado_2019.2-build_8_20200325075929.zip TE0724-test_board_nopre built-vivado_2019.2-	John Hartfiel	• script update

Date	Vivado	Project Built	Authors	Description
		build_8_20200325075950.zip		
2020-01-30	2019.2	TE0724-test_board_nopre built-vivado_2019.2-build_4_20200130130053.zip TE0724-test_board-vivado_2019.2-build_4_20200130130040.zip	John Hartfiel	• 2019.2 update • Vitis support • FSBL changes • petalinux device tree and u-boot update
2019-13-12	2018.2	TE0724-test_board_nopre built-vivado_2018.2-build_04_20191212064015.zip TE0724-test_board-vivado_2018.2-build_04_20191212064001.zip	John Hartfiel	• bugfix IO constrains
2019-06-13	2018.2	TE0724-test_board-vivado_2018.2-build_04_20190613114927.zip TE0724-test_board_nopre built-vivado_2018.2-build_04_20190613115049.zip	Oleksandr Kiyenko, John Hartfiel	• add app to get access to EEPROM U10
2019-02-04	2018.2	TE0724-test_board-vivado_2018.2-build_04_2019020	John Hartfiel	• Important Board Part File Update

Date	Vivado	Project Built	Authors	Description
		4111543.zip TE0724-test_board_nopre built-vivado_2018.2-build_04_20190204111557.zip		• change DDR3 to DDR3 Low Power
2018-08-29	2018.2	TE0724-test_board_nopre built-vivado_2018.2-build_03_20180830170634.zip TE0724-test_board-vivado_2018.2-build_03_20180830170621.zip	John Hartfiel	• initial release

Table 1: Design Revision History

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Xilinx Software	Incompatibility of board files for ZynqMP with eMMC activated for Vivado versions below/equal to 2021.2 and 2021.2.1 patch, see Xilinx Forum Request[1]	use corresponding board files for the Vivado versions	--
EEPROM U10 is not writeable	WP is fix on on PCB Revisions, which	PCB can be patched, send request to Trenz	---

1 https://support.xilinx.com/s/feed/0D54U00005Wbon6SAB?language=en_US

Issues	Description	Workaround	To be fixed version
	shipped before 2019-06-13	Electronic support	

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2021.2.1	needed Vivado is included into Vitis installation
PetaLinux	2021.2	needed

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[2]

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0724-02-10-1I	10_1i_1gb	REV02	1GB	32MB	NA	NA	NA

2 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0724-02-20-1	20_1i_1gb	REV02	1GB	32MB	NA	NA	NA
TE0724-02-20-1IC1	20_1i_1gb	REV02	1GB	32MB	NA	NA	NA
TE0724-03-10-1I	10_1i_1gb	REV03	1GB	32MB	NA	NA	NA
TE0724-03-20-1	20_1i_1gb	REV03	1GB	32MB	NA	NA	NA
TE0724-03-20-1IC1	20_1i_1gb	REV03	1GB	32MB	NA	NA	NA
TE0724-04-41I32-A	10_1i_1gb	REV04	1GB	32MB	NA	NA	NA
TE0724-04-41I33-A*	10_1i_1gb	REV04	1GB	64MB	NA	NA	NA
TE0724-04-41I33-AZ	10_1i_1gb	REV04	1GB	64MB	NA	NA	NA
TE0724-04-61I32-A	20_1i_1gb	REV04	1GB	32MB	NA	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0724-04-61I32-AZ	20_1i_1gb	REV04	1GB	32MB	NA	NA	NA
TE0724-04-61I33-AC	20_1i_1gb	REV04	1GB	64MB	NA	NA	NA
TE0724-04-S001	10_1i_1gb	REV04	1GB	64MB	NA	NA	CAO
TE0724-04-S003	10_1i_1gb	REV04	1GB	64MB	NA	NA	CAO
TE0724-04-S004	10_1i_1gb	REV04	1GB	64MB	NA	NA	CAO
TE0724-04-S005	10_1i_1gb	REV04	1GB	64MB	NA	NA	CAO

Table 4: Hardware Modules
*used as reference

Design supports following carriers:

Carrier Model	Notes
TEB0724	

Table 5: Hardware Carrier
*used as reference

Additional HW Requirements:

Additional Hardware	Notes

Table 6: Additional Hardware
*used as reference

4.5 Content

For general structure and of the reference design, see Project Delivery - Xilinx devices[3]

4.5.1 Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

Table 7: Design sources

4.5.2 Additional Sources

3 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices

Type	Location	Notes
init.sh	<project folder>\misc\sd	Additional Initialization Script for Linux

Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Boot Script-File	*.scr	Distro Boot Script file
DebugProbes-File	*.ltx	Definition File for Vivado/ Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Device Tree	*.dts	Device tree (2 possible, one for u-boot and one for linux)
Hardware-Platform -Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File

File	File-Extension	Description
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebult content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0724 "Test Board" Reference Design[4]

4 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x6/TE0724/Reference_Design/2021.2/test_board

5 Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- AMD Development Tools[5]
- Vivado Projects - TE Reference Design[6]
- Project Delivery.[7]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

> ⚠ **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[8]

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
------------------------Set design
paths----------------------------
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
------------------------------------------------------------
--------
-------------------------TE Reference
Design---------------------------
------------------------------------------------------------
--------
-- (0)  Module selection guide, project creation...prebuilt
export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
```

5 https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDevelopmentTools-XilinxSoftware-BasicUserGuides
6 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices
8 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality

```
-- (x)  Exit Batch (nothing is done!)
----
Select (ex.:'0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
   - optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"

     ⚠ Note: Select correct one, see also Vivado Board Part Flow[9]

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "\prebuilt\hardware\")

```
\prebuilt\hardware\")">
TE::hw_build_design -export_prebuilt
```

ⓘ Using Vivado GUI is the same, except file export to prebuilt folder.

5. Create and configure your PetaLinux project with exported .xsa-file, see PetaLinux KICKstart[10]
   - use TE Template from "<project folder>\os\petalinux"
   - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>" . **Note:** HW Export from Vivado GUI creates another path as default workspace.
   - The build images are located in the "<plnx-proj-root>/images/linux" directory
6. Configure the **boot.scr** file as needed, see Distro Boot with Boot.scr[11]
7. Copy PetaLinux build image files to prebuilt folder
   - copy **u-boot.elf**, **u-boot.dtb, system.dtb**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

     ⓘ "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

8. Generate Programming Files with Vitis

run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or
 start with TE Scripts on Vivado TCL)
```

9 https://wiki.trenz-electronic.de/display/PD/Vivado+Board+Part+Flow
10 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
11 https://wiki.trenz-electronic.de/display/PD/Distro+Boot+with+Boot.scr

TCL scripts generate also platform project, this must be done manually in case GUI is used. See Vitis[12]

12 https://wiki.trenz-electronic.de/display/PD/Vitis

6 Launch

6.1 Programming

> ⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.
> Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging[13]

6.1.1 Get prebuilt boot binaries

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select Create and open delivery binary folder

   > ⓘ Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

6.1.2 QSPI-Boot mode

Option for **Boot.bin** on QSPI Flash and **image.ub** and **boot.scr** on **SD** or **USB**.

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

   run on Vivado TCL (Script programs BOOT.bin on QSPI flash)

   ```
   TE::pr_program_flash -swapp u-boot
   TE::pr_program_flash -swapp hello_te0724 (optional)
   ```

3. Copy **image.ub** and **boot.scr** on **SD** or **USB**
   - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder,see: Get prebuilt boot binaries(see page 19)
   - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
4. Set Boot Mode to **QSPI-Boot** and insert **SD** or **USB** card.
   - Depends on Carrier, see carrier TRM.

13 https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDevelopmentTools-XilinxSoftwareProgrammingandDebugging

6.1.3 SD

1. Copy **image.ub**, **boot.src** and **Boot.bin** on **SD**
   - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder, see: Get prebuilt boot binaries(see page 19)
   - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
2. Set Boot Mode to SD-Boot.
   - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

6.1.4 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section Programming(see page 19)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card or QSPI as Boot Mode (Depends on used programming variant)

   Note: See TRM of the Carrier, which is used.

   Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.
   The boot options described above describe the common boot processes for this hardware; other boot options are possible.
   For more information see Distro Boot with Boot.scr[14]

4. Power On PCB
   boot process

   1. Zynq Boot ROM loads FSBL from SD/QSPI into OCM,

   2. FSBL init the PS, programs the PL using the bitstream and loads U-boot from SD/QSPI into DDR,

   3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

6.2.1 Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. Select COM Port

   Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)

14 https://wiki.trenz-electronic.de/display/PD/Distro+Boot+with+Boot.scr

2. Linux Console:

```
# password default disabled with 2021.2 petalinux release
petalinux login: root
Password: root
```

> Note: Wait until Linux boot finished

3. You can use Linux shell now.

```
I2C
    i2cdetect -l        (Shows a list of the available I2C
buses)
    i2cdetect -y -r 0   (check I2C 0 Bus)
RTC
    dmesg | grep rtc    (RTC check)
ETH0
    udhcpc              (ETH0 check)
GPIO
    gpiodetect          (list all gpiochips present on the
system)
    gpioget `gpiofind "MIO51_J9-6"`     (read value of
specified GPIO)
    gpioset `gpiofind "MIO9_D8"`=1      (set value of
specified GPIO)
```

4. Option Features
    - Webserver to get access to Zynq
        - insert IP on web browser to start web interface
    - init.sh scripts
        - add init.sh script on SD, content will be load automatically on startup (template included in "<project folder>\misc\SD")

6.2.2 Vivado HW Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder)

- Control:
    - CAN_STBY[0:0] CAN Standby control
    - LED_RG[1:0] module LED control
    - TEB0724_ULED[5:0] TEB0724 LED control
- Monitoring:
    - vio_TEB0724_BUTTON_S24[1:0] TEB0724 Button S2 and S4
    - vio_PWR__GPIO01[1:0] PMIC GPIO
    - fm_PHY_CLK125M[31:0] PHY Clock 125MHz
    - labtools_fmeter_0_update FMeter Update

7 System Design - Vivado

7.1 Block Design

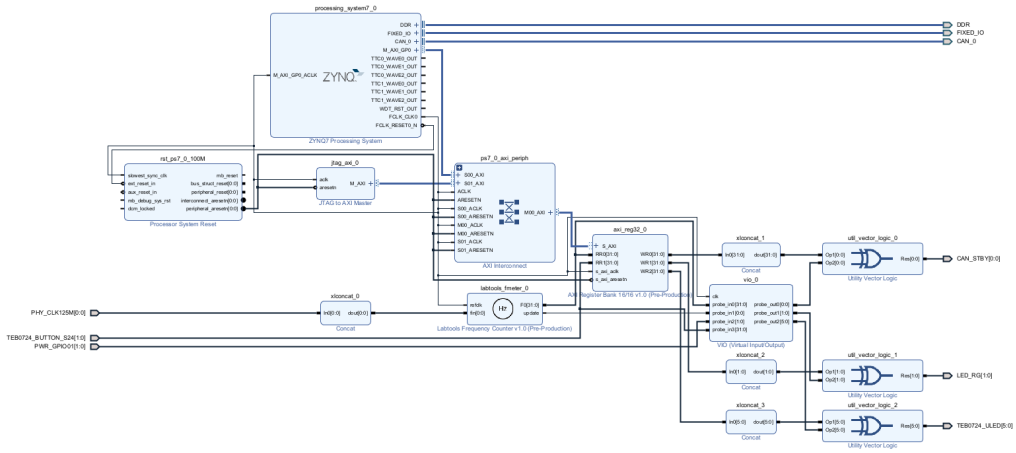

Figure 1: Block Design

7.1.1 PS Interfaces

Type	Note
DDR	
QSPI	MIO
ETH0	MIO
SD0	MIO
UART1	MIO
I2C1	MIO
CAN0	EMIO
GPIO	MIO
TTC0..1	EMIO

Type	Note
WDT	EMIO

Table 10: PS Interfaces

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen_common.xdc

```
#
# Common BITGEN related settings for TE0724 SoM
#
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property CFGBVS VCCO [current_design]
```

7.2.2 Design specific constrain

_i_io.xdc

```
# can
set_property PACKAGE_PIN T11 [get_ports CAN_0_tx]
set_property IOSTANDARD LVCMOS33 [get_ports CAN_0_tx]
set_property PACKAGE_PIN T10 [get_ports CAN_0_rx]
set_property IOSTANDARD LVCMOS33 [get_ports CAN_0_rx]
set_property PACKAGE_PIN U13 [get_ports {CAN_STBY[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {CAN_STBY[0]}]
# led
set_property PACKAGE_PIN U12 [get_ports {LED_RG[0]}]
set_property PACKAGE_PIN W13 [get_ports {LED_RG[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {LED_RG[*]}]
# CLK
set_property PACKAGE_PIN U14 [get_ports {PHY_CLK125M[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {PHY_CLK125M[0]}]
# PWR GPIO
set_property PACKAGE_PIN T12 [get_ports {PWR_GPIO01[0]}]
set_property PACKAGE_PIN U15 [get_ports {PWR_GPIO01[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {PWR_GPIO01[*]}]
# TEB0724 Button
set_property PACKAGE_PIN Y19 [get_ports {TEB0724_BUTTON_S24[0]}]
set_property PACKAGE_PIN Y18 [get_ports {TEB0724_BUTTON_S24[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {TEB0724_BUTTON_S24[*]
}]
```

```
# TEB0724 LED
set_property PACKAGE_PIN P18 [get_ports {TEB0724_ULED[0]}]
set_property PACKAGE_PIN N17 [get_ports {TEB0724_ULED[1]}]
set_property PACKAGE_PIN R17 [get_ports {TEB0724_ULED[2]}]
set_property PACKAGE_PIN R16 [get_ports {TEB0724_ULED[3]}]
set_property PACKAGE_PIN Y14 [get_ports {TEB0724_ULED[4]}]
set_property PACKAGE_PIN W14 [get_ports {TEB0724_ULED[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {TEB0724_ULED[*]}]
```

8 Software Design - Vitis

For Vitis project creation, follow instructions from:

Vitis[15]

8.1 Application

Template location: "<project folder>\sw_lib\sw_apps\"

8.1.1 zynq_fsbl

TE modified 2021.2 FSBL

General:

- Modified Files: main.c, fsbl_hooks.h/.c (search for 'TE Mod' on source code)
- Add Files: te_fsbl_hooks.h/.c (for hooks and board)
- General Changes:
    - Display FSBL Banner and Device ID

Module Specific:

- Add Files: all TE Files start with te_*
    - enable I2C Buffer over MIO38, needed for RTC and external I2C

8.1.2 zynq_fsbl_flash

TE modified 2021.2 FSBL

General:

- Modified Files: main.c
- General Changes:
    - Display FSBL Banner
    - Set FSBL Boot Mode to JTAG
    - Disable Memory initialisation

8.1.3 hello_te0724

Hello TE0724 is a Xilinx Hello World example as endless loop instead of one console output.

8.1.4 u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

15 https://wiki.trenz-electronic.de/display/PD/Vitis

9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart[16]

9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- MAC from eeprom together with device tree settings:
  - CONFIG_SUBSYSTEM_ETHERNET_PS7_ETHERNET_0_MAC=""
- add new flash partition for bootscr and sizing:
  - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART0_SIZE=0xA00000
  - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART2_SIZE=0x1400000
  - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART3_NAME="bootscr"
  - CONFIG_SUBSYSTEM_FLASH_PSU_QSPI_0_BANKLESS_PART3_SIZE=0x40000

9.2 U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- MAC from eeprom together with device tree settings:
  - CONFIG_ENV_OVERWRITE=y
- Boot Modes:
  - CONFIG_QSPI_BOOT=y
  - CONFIG_SD_BOOT=y
  - # CONFIG_ENV_IS_IN_NAND is not set
  - CONFIG_BOOT_SCRIPT_OFFSET=0x1E20000

Change platform-top.h:

```
#include <configs/zynq-common.h>
#no changes
```

9.3 Device Tree

project-spec\meta-user\recipes-bsp\device-tree\files\system-user.dtsi

```
/include/ "system-conf.dtsi"
```

16 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart

```
/*-------------------------- default ---------------------*/

/*--------------------------- GPIO -----------------------*/
&gpio0 {
   gpio-line-names =
       "MIO0_PWR"    , ""            , ""            , ""
     , ""            ,
       ""            , ""            , "MIO7"        , ""
     , "MIO9_D8"     ,
       "MIO10_J7-5"  , "MIO11_J7-6"  , "MIO12_J7-7"  ,
"MIO13_J7-8"    , "MIO14_J7-9"  ,
       "MIO15_J7-10" , ""            , ""            , ""
     , ""            ,
       ""            , ""            , ""            , ""
     , ""            ,
       ""            , ""            , ""            , ""
     , ""            ,
       "MIO30_nC"    , "MIO31_nC"    , "MIO32_nC"    , "MIO33_nC"
    , "MIO34_nC"    ,
       "MIO35_nC"    , "MIO36_nC"    , "MIO37_nC"    ,
"MIO38_TCA-OE"  , ""            ,
       ""            , ""            , ""            , ""
     , ""            ,
       ""            , "MIO46_J9-4"  , ""            , ""
     , ""            ,
       "MIO50_J9-5"  , "MIO51_J9-6"  , ""            , ""
     ;
};

/*--------------------------- QSPI -----------------------*/
&qspi {
    is-dual = <0>;
    num-cs = <1>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    spi-rx-bus-width = <4>;
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
        spi-rx-bus-width = <4>;
    };
};

/*-------------------------- ETH PHY ---------------------*/
&gem0 {
    phy-handle = <&phy0>;

    nvmem-cells = <&eth0_addr>;
    nvmem-cell-names = "mac-address";

        phy0: phy@0 {
            device_type = "ethernet-phy";
```

```
            reg = <1>;
        };
};

/*---------------------------- I2C -----------------------*/
&i2c1 {

  //pmic
  pmic0: da9062@58 {
    compatible = "dlg,da9062";
    reg = <0x58>;
    interrupt-parent = <&gpio0>;
    interrupts = <0 8>;
    interrupt-controller;
    rtc {
        compatible = "dlg,da9062-rtc";
    };
  };

  //MAC EEPROM
  eeprom: eeprom@53 {
    compatible = "microchip,24aa025", "atmel,24c02";
    reg = <0x53>;

    #address-cells = <1>;
    #size-cells = <1>;
    eth0_addr: eth-mac-addr@FA {
      reg = <0xFA 0x06>;
    };

  };

 //user EEPROM
  eeprom50: eeprom@50 {
    compatible = "microchip,24aa128", "atmel,24c128";
    reg = <0x50>;
  };

};
```

9.4 Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_REGMAP_IRQ=y
- # CONFIG_DA9062_THERMAL is not set
- # CONFIG_DA9062_WATCHDOG is not set
- CONFIG_MFD_DA9062=y
- # CONFIG_REGULATOR_DA9062 is not set
- CONFIG_RTC_DRV_DA9063=y

9.5 Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- For web server app:
  - CONFIG_busybox-httpd=y
- For additional test tools only:
  - CONFIG_i2c-tools=y
  - CONFIG_packagegroup-petalinux-utils=y (util-linux,cpufrequtils,bridge-utils,mtd-utils,usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)
- For use of libgpiod-tools (gpiodetect, gpioset, gpioget, ...) together with device tree settings:
  - CONFIG_libgpiod-tools=y

Add in <project folder>\os\petalinux\project-spec\meta-user\conf\user-rootfsconfig

```
CONFIG_libgpiod-tools
```

9.6 Applications

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps\"

9.6.1 startup

Script App to load init.sh from SD Card if available.

9.6.2 webfwu

Webserver application suitable for Zynq access. Need busybox-httpd

10 Additional Software

No additional software is needed.

11 Appx. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2022-11-21	v.12 (see page 6)	Manuela Strücker[17]	• Release Vivado 2021.2.1 • script update • new assembly variants
2020-03-25	v.10	John Hartfiel	• script update
2020-01-30	v.9	John Hartfiel	• Release 2019.2 • document style update
2019-12-12	v.8	John Hartfiel	• Bugfix IO constrains
2019-06-13	v.7	John Hartfiel	• Update Design Files • Notes U10 access
2019-02-04	v.6	John Hartfiel	• Update Design Files
2018-08-30	v.5	John Hartfiel	• 2018.2 release
--	all	John Hartfiel[18] , Manuela Strücker[19]	--

Table 11: Document change history.

17 https://wiki.trenz-electronic.de/display/~m.struecker
18 https://wiki.trenz-electronic.de/display/~j.hartfiel
19 https://wiki.trenz-electronic.de/display/~m.struecker

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11.3 Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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2019-06-07

20 http://guidance.echa.europa.eu/
21 https://echa.europa.eu/candidate-list-table
22 http://www.echa.europa.eu/