TEBF0808 CPLD

Revision v.13

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Online version of this document:

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4 Overview

Firmware for PCB-Master CPLD with designator U17. Use first CPLD Device in Chain: LCMX02-1200HC.

Firmware for PCB-Slave CPLD with designator U39. Use second CPLD Device in Chain: LCMX02-1200HC.

There are 3 different Firmware variants available:

1. (Default): SCM_07A_default.jed/SCS_07A_default.jed
2. (optional): SCM_07B_powerdown_disabled.jed/SCS_07B_powerdown_disabled.jed - Power down Sequencing is disabled (See Note Power Managment).
3. (optional): SCM_07C_msdboot_disabled.jed/SCS_07C_msdboot_disabled.jed - CD Pin of MicroSD will not influence boot Mode (mircoSD can be used as Filesystem and system Boots from QSPI)

4.1 Feature Summary

- Power Management (Slave CPLD)
- Reset Management (both)
- CPLD JTAG (both)
- FMC JTAG / PJTAG (Master CPLD)
- FMC VADJ Power (Master CPLD)
- Boot Mode (Slave CPLD)
- PCIe (Slave CPLD)
- SD (both)
- UART SoC (Slave CPLD)
- UART (Debug) (Master CPLD)
- CAN (Master CPLD)
- USB (Master CPLD)
- DisplayPort (Master CPLD)
- SFP (Master CPLD)
- I2C (Master CPLD)
- LEDs (both)
- RGPIO (both)

4.2 Firmware Revision and supported PCB Revision

See Document Change History

5 Product Specification

5.1 Port Description

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
C_T1		24	3V3SB	/ currently_not_used	U17	NC
C_T2		26	3V3SB	/ currently_not_used	U17	NC
C_T3		25	3V3SB	/ currently_not_used	U17	NC
C_TCK	in	131	3V3SB	JTAG J28 (XMOD2) / FMC JTAG	U17	
C_TDI	in	136	3V3SB	JTAG J28 (XMOD2) / FMC JTAG	U17	
C_TDO1 / C_TDO	out	137	3V3SB	JTAG J28 (XMOD2) / FMC JTAG	U17	
C_TMS	in	130	3V3SB	JTAG J28 (XMOD2) / FMC JTAG	U17	
CAN_FAULT		106	3V3SB	CAN	U17	
CAN_RX	in	107	3V3SB	CAN	U17	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
CAN_S	out	105	3V3SB	CAN	U17	
CAN_TX	out	104	3V3SB	CAN	U17	
CLK_125MHz / PHY_CLK	in	70	1.8V	/ currently_not_used	U17	
CON_NTRST / JTAG_TRST	in	117	3V3SB	JTAG, Connector J30	U17	
CON_RTCK / JTAG_RTCK	out	125	3V3SB	JTAG, Connector J30	U17	
CON_sRST / JTAG_SRST	in	127	3V3SB	JTAG, Connector J30	U17	
CON_TCK / JTAG_TCK	in	122	3V3SB	JTAG, Connector J30	U17	
CON_TDI / JTAG_TDI	in	119	3V3SB	JTAG, Connector J30	U17	
CON_TDO / JTAG_TDO	out	126	3V3SB	JTAG, Connector J30	U17	
CON_TMS / JTAG_TMS	in	121	3V3SB	JTAG, Connector J30	U17	
DIR_T1		23	3V3SB	/ currently_not_used	U17	NC
DIR_T2		28	3V3SB	/ currently_not_used	U17	NC

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
DIR_T3		27	3V3SB	/ currently_not_used	U17	NC
DP_AUX_DE / DP_DE	out	92	3V3SB	Display Port	U17	
DP_AUX_RX / DP_RX	in	91	3V3SB	Display Port	U17	
DP_AUX_TX / DP_TX	out	93	3V3SB	Display Port	U17	
DP_EN	out	77	3V3SB	Display Port	U17	
DP_TX_HPD / DP_HPD	in	94	3V3SB	Display Port	U17	
ETH_RST	out	62	1.8V	ETH Reset	U17	
EX_IO1		112	3V3SB	/ currently_not_used	U17	
EX_IO2		113	3V3SB	/ currently_not_used	U17	
EX_IO3		114	3V3SB	/ currently_not_used	U17	
EX_IO4		115	3V3SB	/ currently_not_used	U17	
F2_EN		19	3V3SB	/ currently_not_used	U17	NC

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
F2PWM		20	3V3SB	/ currently_not_used	U17	NC
F2SENSE		21	3V3SB	/ currently_not_used	U17	NC
FMC_CLK_DIR / FMC_CLKDIR	in	73	3V3SB	FMC	U17	
FMC_TCK	out	95	3V3SB	FMC	U17	
FMC_TDI	out	96	3V3SB	FMC	U17	
FMC_TDO	in	97	3V3SB	FMC	U17	
FMC_TMS	out	98	3V3SB	FMC	U17	
FMC_VID0	out	139	3V3SB	FMC	U17	
FMC_VID1	out	140	3V3SB	FMC	U17	
FMC_VID2	out	141	3V3SB	FMC	U17	
GND		84	3V3SB	REV03 unconnected / currently_not_used	U17	USB_TRST, other USB HUB
HDIO_SC10 / SC10	out	60	1.8V	FPGA / DP_RX or 'Z'	U17	
HDIO_SC11 / SC11	in	59	1.8V	FPGA / DP_DE	U17	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
HDIO_SC12 / SC12	out	58	1.8V	FPGA / DP_HPD	U17	
HDIO_SC13 / SC13	out	57	1.8V	FPGA / RGPIO TX	U17	
HDIO_SC14 / SC14	in	56	1.8V	FPGA / RGPIO RX	U17	
HDIO_SC15 / SC15	in	55	1.8V	FPGA / RGPIO CLK	U17	
HDIO_SC16 / SC16	in	54	1.8V	FPGA / CAN_S	U17	
HDIO_SC17 / SC17	in	52	1.8V	FPGA / XMOD LED	U17	
HDIO_SC18 / SC18	in	68	1.8V	FPGA / CAN_TX	U17	
HDIO_SC19 / SC19	out	69	1.8V	FPGA / CAN_RX	U17	
I2C_RST	out	61	1.8V	I2C	U17	
JTAGENB		120	3V3SB	external Pin for CPLD Firmware Update	U17	
LED_1A / JLED1	out	109	3V3SB	USB3.0 LED Jellow	U17	
LED_2A / JLED2A	out	111	3V3SB	USB3.0 LED Green/ Orange	U17	
LED_2B / JLED2B	out	110	3V3SB	USB3.0 LED Green/ Orange	U17	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
MIO26	out	41	1.8V	MIO / PJTAG	U17	
MIO27	out	40	1.8V	MIO / PJTAG	U17	
MIO28	in	39	1.8V	MIO / PJTAG	U17	
MIO29	out	38	1.8V	MIO / PJTAG	U17	
OCLK_EN / OSC_EN	out	74	3V3SB	Programmable Oscillator U45	U17	
PHY_CONFIG	out	65	1.8V	ETH PHY	U17	
PHY_LED0	in	67	1.8V	ETH PHY	U17	
PHY_LED1	in	86	3V3SB	ETH PHY	U17	
PHY_LED2	in	85	3V3SB	ETH PHY	U17	
SC_CLK0 / CLK0	in	76	3V3SB	/ currently_not_used	U17	
SC_CLK1 / CLK1	in	75	3V3SB	/ currently_not_used	U17	
SC_IO0 / X0	out	50	1.8V	MTS dummy	U17	
SC_IO1 / X1	in	49	1.8V	internal cpld RGPIO CLK	U17	
SC_IO2 / X2	out	48	1.8V	internal cpld RGPIO TX	U17	
SC_IO3 / X3	in	47	1.8V	internal cpld RGPIO RX	U17	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
SC_IO4 / X4	out	45	1.8V	SD WP to slave cpld	U17	
SC_IO5 / X5	in	44	1.8V	STM dummy	U17	
SC_IO6 / X6	out	43	1.8V	/ currently_not_used	U17	
SC_IO7 / X7	out	42	1.8V	/ currently_not_used	U17	
SC_IO8 / X8	in	22	3V3SB	internal cpld RGPIO available(1.8V on)	U17	
SC_SCL / SCL	in	14	3V3SB	I2C Mux U27 / currently_not_used	U17	
SC_SDA / SDA	in	13	3V3SB	I2C Mux U27 / currently_not_used	U17	
SC2_SW3 / SW3	in	6	3V3SB	DIP-Switch S5-3	U17	
SC2_SW4 / SW4	in	5	3V3SB	DIP-Switch S5-4	U17	
SD_WP	in	100	3V3SB	MMC SD WP	U17	
SFP_LED1 / SFP_LED0	out	81	3V3SB	SFP	U17	
SFP_LED2 / SFP_LED1	out	82	3V3SB	SFP	U17	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
SFP_LED3 / SFP_LED2	out	78	3V3SB	SFP	U17	
SFP_LED4 / SFP_LED3	out	83	3V3SB	SFP	U17	
SFP1_LOS		32	3V3SB	SFP / currently_not_used	U17	
SFP1_TX_DIS	out	33	3V3SB	SFP	U17	
SFP2_LOS		35	3V3SB	SFP / currently_not_used	U17	
SFP2_TX_DIS	out	34	3V3SB	SFP	U17	
STAT_LED0 / LED0	out	99	3V3SB	LED D4 Green	U17	
STAT_LED1 / LED1	out	128	3V3SB	LED D1 Red	U17	
USB0_RST / USB_TRST		71	1.8V	USB (U9) PHY Reset	U17	
USBH_LED_G3		11	3V3SB	USB Hub (U4) / currently_not_used	U17	
USBH_LED_G4		12	3V3SB	USB Hub (U4) / currently_not_used	U17	
USBH_LED_SS1		9	3V3SB	USB Hub (U4) / currently_not_used	U17	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
USBH_LED_SS2		133	3V3SB	USB Hub (U4) / currently_not_used	U17	
USBH_LED_SS3		132	3V3SB	USB Hub (U4) / currently_not_used	U17	
USBH_LED_SS4		138	3V3SB	USB Hub (U4) / currently_not_used	U17	
USBH_MODE0	out	142	3V3SB	USB Hub (U4)	U17	
USBH_MODE1	out	143	3V3SB	USB Hub (U4)	U17	
USBH_RST	out	10	3V3SB	USB Hub (U4)	U17	
XMOD1_A / XMOD_TXD	out	3	3V3SB	J28 (XMOD 2 UART)	U17	
XMOD1_B / XMOD_RXD	in	2	3V3SB	J28 (XMOD 2 UART)	U17	
XMOD1_E / XMOD_E	out	4	3V3SB	J28 (XMOD 2 LED)	U17	
XMOD1_G / XMOD_G	out	1	3V3SB	J28 (XMOD 2 Button)	U17	
1.8V_EN / EN_1V8	out	106	3V3SB	Enable 1.8V Power	U39	
5V_EN / EN_5V	out	115	3V3SB	Enable 5V Power, can be permanently enabled by S4-4	U39	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
C_TCK		131	3V3SB	JTAG J28 (XMOD2) / currently_not_used	U39	
C_TDO	out	137	3V3SB	JTAG J28 (XMOD2)	U39	
C_TDO1 / C_TDI	in	136	3V3SB	JTAG J28 (XMOD2)	U39	
C_TMS		130	3V3SB	JTAG J28 (XMOD2) / currently_not_used	U39	
CLK_A / AUD_CLK	out	1	1.8V	AUDIO U3 CLK	U39	
CLK_CPLD / MEMS_CLKIN	in	128	3V3SB	U25 24,576MHz	U39	
DONE	in	67	1.8V	PS Done	U39	
EN_DDR	out	86	3V3SB	Enable Module DDR Power	U39	
EN_FMC / FMC_EN	out	104	3V3SB	FMC	U39	
EN_FPD	out	81	3V3SB	Enable Module PS FPD Power	U39	
EN_GT_L	out	77	3V3SB	Enable Module GT Power	U39	
EN_GT_R	out	93	3V3SB	Enable Module GT Power	U39	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
EN_LPD	out	84	3V3SB	Enable Module PS LPD Power	U39	
EN_PL	out	95	3V3SB	Enable Module PL Power	U39	
EN_PLL_PWR	out	78	3V3SB	Enable Module SI5345 Power	U39	
EN_PSGT / EN_PSGTR	out	75	3V3SB	Enable Module PS GT Power	U39	
ERR_OUT / ERROR	in	70	1.8V	Module PS Error Out / Status	U39	
ERR_STATUS / ERR_STAT	in	69	1.8V	Module PS Error Status	U39	
F1PWM	out	121	3V3SB	FAN1	U39	
F1SENSE	in	125	3V3SB	FAN1	U39	
FAN_FMC_EN / FMC_FAN_EN		132	3V3SB	FMC FAN	U39	
FMC_PG_C2M	out	141	3V3SB	FMC PG	U39	
HD_LED_N / HDLED_N	out	112	3V3SB	J10 HD LED	U39	
HD_LED_P / HDLED_P	out	110	3V3SB	J10 HD LED	U39	
HDIO_SC0 / SC0	in	32	1.8V	FPGA IO / forward to HD_LED_P / HDLED_P	U39	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
HDIO_SC1 / SC1	in	33	1.8V	/ currently_not_used	U39	
HDIO_SC2 / SC2	in	34	1.8V	/ currently_not_used	U39	
HDIO_SC3		35	1.8V	/ currently_not_used	U39	
HDIO_SC4		25	1.8V	/ currently_not_used	U39	
HDIO_SC5 / SC5	out	26	1.8V	FPGA IO / RGPIO	U39	
HDIO_SC6 / SC6	in	27	1.8V	FPGA IO / RGPIO CLK	U39	
HDIO_SC7 / SC7	in	28	1.8V	.FPGA IO / RGPIO	U39	
I2C_SCL / SCL	in	50	1.8V	I2C / currently_not_used	U39	
I2C_SDA / SDA	in	52	1.8V	I2C / currently_not_used	U39	
INIT_B / INIT	in	68	1.8V	Module PS Init_B	U39	
JTAGENB		120	3V3SB	external Pin for CPLD Firmware Update	U39	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
LP_GOOD / PG_LPD	in	83	3V3SB	Module LP Power Good	U39	
MIO24		38	1.8V	MIO / currently_not_used	U39	
MIO25		39	1.8V	MIO / currently_not_used	U39	
MIO30	in	48	1.8V	MIO / USB Reset	U39	
MIO31	in	49	1.8V	MIO / PCIe Reset	U39	
MIO32		40	1.8V	MIO / currently_not_used	U39	
MIO33		41	1.8V	MIO / currently_not_used	U39	
MIO34		42	1.8V	MIO / currently_not_used	U39	
MIO35		43	1.8V	MIO / currently_not_used	U39	
MIO36		44	1.8V	MIO / currently_not_used	U39	
MIO37		45	1.8V	MIO / currently_not_used	U39	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
MIO40	in	54	1.8V	MIO	U39	
MIO41		55	1.8V	MIO / currently_not_used	U39	
MIO42	out	60	1.8V	MIO	U39	
MIO43	in	61	1.8V	MIO	U39	
MIO44		47	1.8V	MIO	U39	
MOD_EN	out	119	3V3SB	Enable Main Module Power 3.3V	U39	
MODE0	out	6	1.8V	Module Boot Mode	U39	
MODE1	out	9	1.8V	Module Boot Mode	U39	
MODE2	out	10	1.8V	Module Boot Mode	U39	
MODE3	out	11	1.8V	Module Boot Mode	U39	
MR / MRESETn	out	92	3V3SB	Module PS Power Reset	U39	
PCI_SFP_EN	out	76	3V3SB	SFP	U39	
PER_EN	out	117	3V3SB	Enable 3.3V power	U39	
PERST / PERSTn	out	139	3V3SB	PCIE Resetn	U39	
PG_DDR	in	91	3V3SB	Module Power Good	U39	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
PG_FPD	in	85	3V3SB	Module Power Good	U39	
PG_GT_L	in	96	3V3SB	Module Power Good	U39	
PG_GT_R	in	94	3V3SB	Module Power Good	U39	
PG_PL	in	82	3V3SB	Module Power Good	U39	
PG_PLL_1V8 / PG_PLL	in	73	3V3SB	Module Power Good	U39	
PG_PSGT	in	74	3V3SB	Module Power Good	U39	
PLL_LOLn / PLL_LOL	in	58	1.8V	Module PLL / currently_not_used	U39	
PLL_RST / PLL_RSTn	out	56	1.8V	Module PLL Reset	U39	
PLL_SEL0	out	57	1.8V	Module PLL	U39	
PLL_SEL1	out	59	1.8V	Module PLL	U39	
POK_1V8	in	107	3V3SB	Carrier Power Good	U39	
POK_FMC	in	99	3V3SB	FMC Power Good	U39	
PROG_B	OUT	71	1.8V	Module PS_PROG_B	U39	
PSON	out	105	3V3SB	ATX J20 PS_ON_N	U39	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
PWR_BTN	in	113	3V3SB	Power Button S1 or J10	U39	
PWRLED_N / LED_N	out	111	3V3SB	J10 PWR	U39	
PWRLED_P / LED_P	out	109	3V3SB	J10 PWR	U39	
PWROK	in	100	3V3SB	ATX J20 PWROK	U39	
RST_BTN	in	114	3V3SB	Reset Button S2 or J10	U39	
S_1		127	3V3SB	BEEPER / currently_not_used	U39	
SC_IO0 / X0	in	12	1.8V	MTS dummy	U39	
SC_IO1 / X1	out	13	1.8V	internal cpld RGPIO CLK	U39	
SC_IO2 / X2	in	14	1.8V	internal cpld RGPIO RX	U39	
SC_IO3 / X3	out	20	1.8V	internal cpld RGPIO TX	U39	
SC_IO4 / X4	in	21	1.8V	MMC SD WP from master	U39	
SC_IO5 / X5	out	22	1.8V	STM dummy	U39	
SC_IO6 / X6	in	23	1.8V	/ currently_not_used	U39	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
SC_IO7 / X7	in	24	1.8V	/ currently_not_used	U39	
SC_IO8 / X8	out	126	3V3SB	internal cpld RGPIO available(1.8V on)	U39	
SC2_SW1 / SW1	in	133	3V3SB	S5-1 / Boot Mode Selection	U39	
SC2_SW2 / SW2	in	138	3V3SB	S5-2 / Boot Mode Selection	U39	
SD_A_EN	out	140	3V3SB	Micro SD	U39	
SD_B_EN	out	122	3V3SB	MMC SD	U39	
SD_CD / SD_CD_OUT	out	65	1.8V	SD Card detect to FPGA	U39	
SD_CD_B	in	143	3V3SB	MMC SD CD	U39	
SD_CD_S	in	142	3V3SB	Micro SD CD	U39	
SEL_SD / SD_SEL	out	62	1.8V	SD select (Mirco or MMC)	U39	
SRST_B / SRSTn	out	19	1.8V	Module PS_SRST_B	U39	
STAT_LED2 / LED2	out	98	3V3SB	LED D6 Green	U39	

Name / opt. VHD Name	Direction	Pin	Bank Power	Description	CPLD	PCB REV02 Exception
STAT_LED3 / LED3	out	97	3V3SB	LED D7 Red	U39	
XMOD2_A / XMOD_TXD	out	5	1.8V	J12 (XMOD 1 UART)	U39	
XMOD2_B / XMOD_RXD	in	4	1.8V	J12 (XMOD 1 UART)	U39	
XMOD2_E / XMOD_LED	out	3	1.8V	J12 (XMOD 1 LED)	U39	
XMOD2_G / XMOD_BTN	in	2	1.8V	J12 (XMOD 1 Button)	U39	

5.2 Functional Description

5.2.1 JTAG

JTAGENB set carrier board CPLD into the chain for firmware update. For Update set DIP S4-3 to ON.

5.2.2 Power

FMC VADJ is handled on master CPLD.

DIP	Positon	Description
S5-4	ON	1.8V
S5-4	OFF	1.2V

Power on and off sequencing is done with slave CPLD.

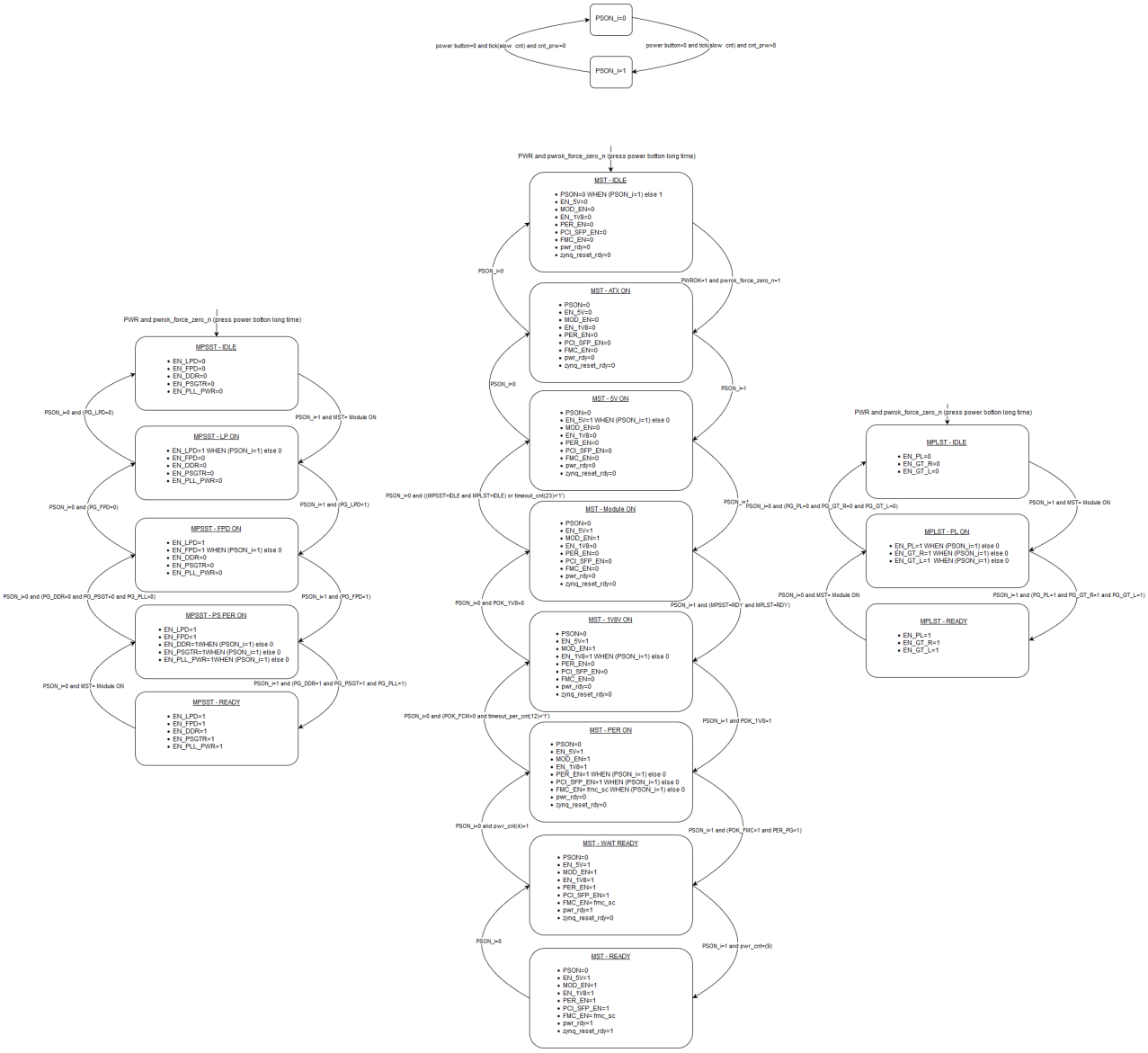

Figure 1: Power On/OFF Sequencing

Note: Power downs sequencing above can be disabled with second optional CPLD Firmware:

1. Configure Firmware version SCM_07B_powerdown_disabled.jed/SCS_07B_powerdown_disabled.jed
2. Add Jumper to J10-6 and J10-8 instead of Enclousure Button
3. Module will be powered and boot on with Main power supply.

5.2.3 Reset

Power, Zynq reset and PCIe is handle on Slave CPLD

USB, I2C Reset is handled on Master CPLD

Type	controlled by
PCie	Power On Reset_N(pwr_rdy), MIO31

Type	controlled by
USB(PHY+HUB)	Power On Reset_N(pwr_rdy), MIO30
Modul PLL	Power On Reset_N(pwr_rdy)
PS_POR_B	Reset Button (hold long time ~3s), zynq_reset_ready
PS_SRST_B	Reset Button (hold short time ~1s), zynq_reset_ready
FMC_FAN_EN	Power On Reset_N(pwr_rdy)
I2C_RST	Power On Reset_N(pwr_rdy)
ETH_RST	Power On Reset_N(pwr_rdy)

5.2.4 JTAG

CPLD JTAG only needed for CPLD Firmware update.

FMC and CPLD JTAG is accessable over XMOD2(J28).

S4-3	
ON	CPLD Access on both CPLD
OFF	FMC JTAG Access

PJTAG on connector J17 is routed over Master CPLD to MIO26..29.

Signal	Connection
JTAG_TCK	MIO26
JTAG_RTCK	JTAG_TCK
JTAG_TDI	MIO27
JTAG_TDO	MIO28

Signal	Connection
JTAG_TMS	MIO29
JTAG_SRST	not usedconnected only to FPGA RGPIO
JTAG_TRST	not used, connected only to FPGA RGPIO

5.2.5 Boot Mode

Boot Mode is handled on Slave CPLD.

S5-1	S5-2	Description
ON	ON	Default, boot from SD/microSD or SPI Flash if no SD is detected
OFF	ON	Boot from eMMC
ON	OFF	Boot mode PJTAG0
OFF	OFF	Boot mode main JTAG

Note: There is a second CPLD Variant available, where microSD will not change the boot mode.

1. Configure Firmware version SCM_07C_msdboot_disabled.jed/SCS_07C_msdboot_disabled.jed
2. Boot mode will be still QSPI,when microSD is insered.

5.2.6 PCIe

PCIe is handled on Slave CPLD.

Signal	Connection
PERSTn	Power On reset and MIO31

5.2.7 SD

SD is mainly handled on Slave CPLD

SD Signal	Description
SD_SEL	CD Pin form microSD selects the SD Card, microSD has higher priority
CD (MIO45)	mircoSD and SD Card detect
WP(MIO44)	0 when miroSD is used else SD card detect (forrward over Master CPLD)

5.2.8 UART SoC

SoC(ZynqMP) is accessible over XMOD1(J12) and connected to ZynqMP over Slave CPLD

Signal	Description
XMOD_TXD	ZynqMP TX(MIO43), when PWR Ready else 1
XMOD_RXD	to ZynqMP RX(MIO42), when PWR Ready else 1

5.2.9 UART (Debug)

Simple Firmware Debug UART is accessible over XMOD2(28) over Master CPLD

Firmware Versions and some statistics can be displayed over second XMOD:

- Included since CPLD Firmware Update to REV07
- UART Speed is 115200
- Press XMOD Button to see output, otherwise RX/TX are loop backed

Signal	Description
XMOD_TXD	Debug output, when XMOD Button is pressed else RX loopback
XMOD_RXD	Debug input(currently no function), when XMOD Button is pressed else TX loopback

5.2.10 CAN

CAN is handled mainly on Master CPLD

Signal	Description
CAN_TX	SC18(FPGA LOC depends on module)
CAN_RX	SC19(FPGA LOC depends on module)
CAN_S	SC16(FPGA LOC depends on module)
CAN_FAULT	Monitoring over RGPIO only

5.2.11 USB

USB Reset is handled mainly on Master CPLD

Signal	Description
USB_RST	Power On Reset and MIO30 (over slave CPLD)
USBH_RST	Power On Reset and MIO30 (over slave CPLD)
USBH_MODE0	const 1
USBH_MODE1	const 1

5.2.12 DisplayPort

DisplayPort is handled on Master CPLD

Signal	Description
DP_EN	not Power On Reset
DP_RX	to SC10 when SC11 is 0 else Z
DP_TX	SX10
DP_DE	SC11
DP_HPD	SC12

5.2.13 SFP

ETH Reset is handled on Master CPLD

Signal	Description
SFP1_TX_DIS	const 0 (Enabled)
SFP2_TX_DIS	const 0 (Enabled)

5.2.14 I2C

I2C MUX is handled on Master CPLD

Signal	Description
I2C_RST	Power On Reset

5.2.15 ETH

ETH Reset is handled on Master CPLD

Signal	Description
ETH_RST	Power On Reset
PHY_CONFIG	const 1

5.2.16 LEDs

LEDs are handled on both CPLDs.

They used different Blink Sequence to indicate all state:

******** (slow blinking)	~0,7 Hz	continuous blinking, like SFP LEDs or Enclosure HD LED when board is powered down
******** (fast blinking)	~5,8 Hz	continuous blinking, like D6 LED or Enclosure Power LED when board is powered down

*****ooo	~0,7 Hz, duty cycle 5/8	5 times fast blink with a break
****oooo	~0,7 Hz, duty cycle 4/8	4 times fast blink with a break
***ooooo	~0,7 Hz, duty cycle 3/8	3 times fast blink with a break
**oooooo	~0,7 Hz, duty cycle 2/8	2 times fast blink with a break
*ooooooo	~0,7 Hz, duty cycle 1/8	1 times fast blink with a break
ON	---	LED ON
OFF	---	LED OFF

<table>
<tr><th>Designator</th><th>Color</th><th>Usage</th><th>Description</th></tr>
<tr><td>D7</td><td>Red</td><td>status</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>PS POR Reset pressed long time (or whole system is powered off)</td><td>ON</td></tr>
<tr><td>2</td><td>PS Soft Reset pressed short time</td><td>OFF</td></tr>
<tr><td>3</td><td>SD Boot</td><td>*ooooooo</td></tr>
<tr><td>4</td><td>QSPI Boot</td><td>**ooooooo</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Designator</th><th>Color</th><th>Usage</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>5</td><td>eMMC Boot</td><td>***ooooo</td></tr>
<tr><td>6</td><td>PJTAG Boot</td><td>****oooo</td></tr>
<tr><td>7</td><td>JTAG Boot</td><td>*****ooo</td></tr>
<tr><td>8</td><td>Error</td><td>******** (fast blinking)</td></tr>
</table>
</td></tr>
<tr><td>D6</td><td>Green</td><td>status</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power OFF</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>PG_LPD low</td><td>*****ooo</td></tr>
<tr><td>3</td><td>PG_FPD low</td><td>****oooo</td></tr>
<tr><td>4</td><td>PG_PL low</td><td>***ooooo</td></tr>
</table>
</td></tr>
</table>

Designator	Color	Usage	Description

Priority	Description	Blink sequencing
5	PG_DDR low or PG_PSGT low or PG_PLL low or PG_GT_L low or PG_GT_R low	**oooooo
6	POK_1V8 low or POK_FMC low or perihpery_pg low or (Main Power State Machine Ready and FMC Sanity check low)	*ooooooo
7	Main Power State Machine Ready	OFF
8	ERROR some power failed, see XMOD LEDs	ON

<table>
<tr><th>Designator</th><th>Color</th><th>Usage</th><th>Description</th></tr>
<tr><td>J10 Power LED</td><td>Blue (symbol light bulb)</td><td>status/user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>power button pressed long time forced power down</td><td>******* (fast blinking)</td></tr>
<tr><td>2</td><td>Main Power State Machine Idle and Power of State is off</td><td>******* (slow blinking)</td></tr>
<tr><td>3</td><td>power button pressed short time power to power on/ off</td><td>*****ooo</td></tr>
<tr><td>4</td><td>PS reset button pressed long time</td><td>****oooo</td></tr>
<tr><td>5</td><td>PS reset button pressed short time</td><td>***ooooo</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Designator</th><th>Color</th><th>Usage</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>6</td><td>power down sequencing is running</td><td>**ooooo</td></tr>
<tr><td>7</td><td>whole system hold into reset</td><td>*ooooo</td></tr>
<tr><td>8</td><td>MIO40</td><td>User Defined</td></tr>
</table>
</td></tr>
<tr><td>J10 HD LED</td><td>Red (symbol drive)</td><td>status/user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>PS Init is low</td><td>********
(fast blinking)</td></tr>
<tr><td>2</td><td>PS Error High</td><td>*****ooo</td></tr>
<tr><td>3</td><td>PS Error Status High</td><td>****oooo</td></tr>
<tr><td>4</td><td>SOC Done low</td><td>***ooooo</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Designator</th><th>Color</th><th>Usage</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>5</td><td>SC0</td><td>User Defined</td></tr>
</table>
</td></tr>
<tr><td>XMOD1 D4</td><td>Red</td><td>status</td><td>
<table>
<tr><th>Priority</th><th>XMOD Button</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Pressed</td><td>power button pressed long time forced power down</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>Pressed</td><td>Main Power State Machine Idle and Power of State is power down sequencing</td><td>*****ooo</td></tr>
<tr><td>3</td><td>Pressed</td><td>PS reset button</td><td>****oooo</td></tr>
</table>
</td></tr>
</table>

Designator	Color	Usage	Description
			<table><tr><th>Priority</th><th>XMOD Button</th><th>Description</th><th>Blink sequencing</th></tr><tr><td></td><td></td><td>pressed</td><td></td></tr><tr><td>4</td><td>Pressed</td><td>Power button pressed short time power on/off</td><td>***ooooo</td></tr><tr><td>5</td><td>Pressed</td><td>Power of State is power down sequencing</td><td>**oooooo</td></tr><tr><td>6</td><td>Pressed</td><td>System hold into reset</td><td>*oooooo</td></tr><tr><td>7</td><td>Pressed</td><td>PS Init low</td><td>ON</td></tr><tr><td>1</td><td>Unpressed</td><td>Problem with other CPLD, FMC is disabled</td><td>******** (fast blinking)</td></tr></table>

Designator	Color	Usage	Description

Priority	XMOD Button	Description	Blink sequencing
2	Unpressed	Main Power State Machine Wait Ready ON/OFF	******ooo
3	Unpressed	Main Power State Machine 3.3V and VADJ ON/OFF	******oooo
4	Unpressed	power not ready (power reset)	**oooooo
5	Unpressed	zynq reset	*oooooooo
7	Unpressed	PS Init low	ON
x	Pressed/Unp	all fine	OFF

<table>
<tr><th>Designator</th><th>Color</th><th>Usage</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>Priority</th><th>XMOD Button</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td></td><td>ressed</td><td></td><td></td></tr>
</table>
</td></tr>
<tr><td>XMOD2 D4</td><td>Red</td><td>status/user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>SC17</td><td>User Defined</td></tr>
</table>
</td></tr>
<tr><td>SFP D1</td><td>Red</td><td>status/user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Designator</th><th>Color</th><th>Usage</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>3</td><td>RGPIO(0), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr>
<tr><td>4</td><td>--</td><td>OFF</td></tr>
</table>
</td></tr>
<tr><td>SFP D8</td><td>Green</td><td>status/user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>RGPIO(1), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr>
<tr><td>4</td><td>--</td><td>OFF</td></tr>
</table>
</td></tr>
<tr><td>D17 - USB HUB LED (Suspend)</td><td>Green</td><td>status</td><td>ON, no USB connected, OFF, USB connected</td></tr>
</table>

<table>
<tr><th>Designator</th><th>Color</th><th>Usage</th><th>Description</th></tr>
<tr><td>SFP D9</td><td>Red</td><td>status/user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>RGPIO(2), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr>
<tr><td>4</td><td>--</td><td>OFF</td></tr>
</table>
</td></tr>
<tr><td>SFP D10</td><td>Green</td><td>status/user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Designator</th><th>Color</th><th>Usage</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>3</td><td>RGPIO(3), when RGPIO Enabled over FPGA</td><td>User Defined</td></tr>
<tr><td>4</td><td>--</td><td>OFF</td></tr>
</table>
</td></tr>
<tr><td>ETH J7</td><td>Yellow</td><td>status</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>ETH PHY LED</td><td>(not PHY_LED 0)</td></tr>
</table>
</td></tr>
<tr><td>ETH J7</td><td>Green/Orange</td><td>status</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>Power On Reset</td><td>******** (slow blinking)</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Designator</th><th>Color</th><th>Usage</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>2</td><td>PS Init low</td><td>******** (fast blinking)</td></tr>
<tr><td>3</td><td>ETH PHY LED</td><td>(PHY_LED1)</td></tr>
</table>
</td></tr>
<tr><td>D4</td><td>Green</td><td>status/user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>1.8V disabled, inter CPLD RGPIO is disabled</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>1.8V enabled, inter CPLD RGPIO is disabled</td><td>*****ooo</td></tr>
<tr><td>3</td><td>Power On Reset</td><td>****oooo</td></tr>
<tr><td>4</td><td>USB Reset</td><td>***ooooo</td></tr>
<tr><td>5</td><td>RGPIO(4), when RGPIO Enabled</td><td>User Defined</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Designator</th><th>Color</th><th>Usage</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td></td><td>over FPGA</td><td></td></tr>
<tr><td>6</td><td>all fine</td><td>*ooooooo</td></tr>
</table>
</td></tr>
<tr><td>D5</td><td>Red</td><td>status/user</td><td>
<table>
<tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr>
<tr><td>1</td><td>1.8V disabled, inter CPLD RGPIO is disabled</td><td>******** (fast blinking)</td></tr>
<tr><td>2</td><td>1.8V enabled, inter CPLD RGPIO is disabled</td><td>*****ooo</td></tr>
<tr><td>3</td><td>Power On Reset</td><td>****oooo</td></tr>
<tr><td>4</td><td>PCie Reset</td><td>***ooooo</td></tr>
<tr><td>5</td><td>RGPIO(4), when RGPIO Enabled</td><td>User Defined</td></tr>
</table>
</td></tr>
</table>

Designator	Color	Usage	Description
			<table><tr><th>Priority</th><th>Description</th><th>Blink sequencing</th></tr><tr><td></td><td>over FPGA</td><td></td></tr><tr><td>6</td><td>all fine</td><td>*oooooo</td></tr></table>

5.2.17 RGPIO

There are 3 RGPIO interfaces, one InterCPLD RGPIO, and one from every CPLD to SoC.

InterCPLD RGPIO handles:

Signal	Description
Reset Button (SW)	for monitoring only
PS POR	for monitoring only
PS ERR Stat	for monitoring only
PS ERR	for monitoring only
PS Init	for monitoring only
PCIe Reset	for monitoring only
USB Reset	for USB Reset and monitoring
Power On Reset	for Power On Reset and monitoring
inter FPGA	Data from Slave RGPIO to Master RGPIO (for test only)

Master CPLD-SoC RGPIO (accesseble via SoC):

Signal	Description
FPGA Read (23)	JTAG_SRST
FPGA Read (22)	JTAG_TRST
FPGA Read (21)	FMC_CLKDIR
FPGA Read (20)	SD_WP
FPGA Read (19)	unused 0
FPGA Read (18)	SW4
FPGA Read (17)	SW3
FPGA Read (16)	XMOD_G
FPGA Read (15 dt 13)	PHY LEDs
FPGA Read (12)	CAN_FAULT
FPGA Read (11 dt 8)	current RGPIO Mux
FPGA Read (7 dt 0)	Data depends on MUX: 0 – Data(7dt0) from Slave CPLD-SoC RGPIO 1 – POR Statistic 2 – PS RST Statistic 3 – PS POR Statistic 4 – PS Init Statistic 5 – PS ERR Statistic

Signal	Description
	6 PS ERR Stat Statistic 7 PCie RST Statistic 8 USB RST Statistic
FPGA Write (23 dt 12)	unused
FPGA Write (11 dt 8)	RGPIO Mux, see FPGA Read (7 dt 0) , when RGIO active
FPGA Write (7 dt 6)	unused
FPGA Write (5 dt 0)	Diverse LED controll(see LED description) , when RGIO active

Slave CPLD-SoC RGPIO (accesseble via SoC):

Signal	Description
FPGA Read (23)	PLL_LOL
FPGA Read (22)	PG_PLL
FPGA Read (21)	PG_PL
FPGA Read (20)	PWROK and pwrok_force_zero_n
FPGA Read (19)	fmc_sanity_check
FPGA Read (18)	POK_FMC
FPGA Read (17)	PG_GT_R
FPGA Read (16)	PG_GT_L
FPGA Read (15)	PG_PSGT

Signal	Description
FPGA Read (14)	PG_FPD
FPGA Read (13)	PG_DDR
FPGA Read (12)	PG_LPD
FPGA Read (11 dt 8)	current Boot Mode
FPGA Read (7)	ERR_STAT
FPGA Read (6)	ERROR
FPGA Read (5)	SD_CD_B
FPGA Read (4)	SD_CD_S
FPGA Read (3)	unused const 1
FPGA Read (2)	XMOD_BTN
FPGA Read (1)	SW2
FPGA Read (0)	SW1
FPGA Write (23 dt 8)	unused
FPGA Write (7dt 0)	Readable over Master CPLD-SoC RGPIO, when RGIO active

6 Appx. A: Change History and Legal Notices

6.1 Revision Changes

Master	Slave

CPLD REV06 to REV07
• complete rework
• add inter CPLD RGPIO
• new LED debugging sequencing
• simple UART output with Revision Number and some statistic on second XMOD
CPLD REV05 to REV06
• BUGFIX: renamed SC19 to SC17
• Connect FMC JTAG to XMOD2 JTAG
• Connect PJTAG0 (MIO29..26) to JTAG Pin Header J30
• Connect CAN to PL
• RGPIO Pin changes
CPLD REV04 to REV05
• SD WP
• XMOD LED access over PL
Older Revision (PCB REV03) to CPLD REV04
• Fix USB HUB Mode default state over RGPIO
• Invert JLED2B over RGPIO
Older Revision (PCB REV02) to CPLD REV04
• Add all functionality from older Revision (PCB REV03)
	CPLD REV06 to REV07
	• complete rework
	• add variants (power up and SD)multi-functions for buttons
	• power on and power downs sequencing
	  • module complete disable on power down
	  • power on sequencing
	  • power down sequencing --> can be forced with power button (hold longer)
	• Soft PS or PS POR Reset on Reset button (hold longer for PS POR Reset)
	• add inter CPLD RGPIO
	• new SoC RGPIO Pinout
	• removed reboot for pcie initialization
	• new LED debugging sequencing
	• Disabled UART on power down state
	• bugfix WP pin for microSD slot
	• removed PCIe Reboot.
	CPLD REV05 to REV06
	• LED Status changes of LED D2 D3 and HD_LED, XMOD LED
	• extended Power Management
	CPLD REV04 to REV05
	• PS reboot via FSBL over MIO30 (need for proper PCI initialization on first power on without press Reset Button)
	• SD Boot from micoSD only if switch S5-1/-2 is selected to ON
	• RGPIO connection
	• Add SD WP to FPGA
	• Power, Rest Button debounced
	• direct LED access via MIO and PL
	Older Revision (PCB REV03) to CPLD REV04
	• Bugfix: PCIe Reset Pin location.
	• Bugfix: Swapping HDLED and PWRLED location.
	• Bugfix: MEMS_CLKIN Pin location.
	• Add XMOD 1 LED
	Older Revision (PCB REV02) to CPLD REV04
	• Add all functionality from older Revision (PCB REV03)

6.2 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
2019-05-06	v.13 (see page 6)	REV07	REV03,REV04 *	@ John Hartfiel[1]	• REV07 finished (Firmware released on 2019-05-06) • *please write to Trenz Electronic support for PCB REV02
2017-06-07	v.1[2]			@ John Hartfiel[3]	• Initial release (combine Master and Slave CPLD description)
	All			@ John Hartfiel[4]	

6.3 Legal Notices

6.4 Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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1 https://wiki.trenz-electronic.de/display/~j.hartfiel
2 https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=31229214
3 https://wiki.trenz-electronic.de/display/~j.hartfiel
4 https://wiki.trenz-electronic.de/display/~j.hartfiel

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6.10 REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH[5]. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List[6] are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA)[7].

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

5 http://guidance.echa.europa.eu/
6 https://echa.europa.eu/candidate-list-table
7 http://www.echa.europa.eu/

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

2019-06-07

7 TEBF0808 CPLD Archive

7.1 TEBF0808 Master CPLD

Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/SC-CPLD-Firmware

7.1.1 Overview

Firmware for PCB-Master CPLD with designator U17. First CPLD Device in Chain: LCMX02-1200HC

Feature Summary

- FMC VADJ Power
- JTAG / FMC JTAG / PJTAG
- RESET/Enable Management
- LED
- RGPIO
- SD
- CAN
- USB
- DisplayPort

Firmware Revision and supported PCB Revision

See Document Change History

7.1.2 Product Specification

Port Description

Schematic /Souce Code Name	Direction	Pin	Description	PCB REV2 Exception
C_T1		24	/ currently_not_used	NC
C_T2		26	/ currently_not_used	NC
C_T3		25	/ currently_not_used	NC
C_TCK	in	131	JTAG J28 (XMOD2) / FMC JTAG	

Schematic /Souce Code Name	Direction	Pin	Description	PCB REV2 Exception
C_TDI	in	136	JTAG J28 (XMOD2) / FMC JTAG	
C_TDO	out	137	JTAG J28 (XMOD2) / FMC JTAG	
C_TMS	in	130	JTAG J28 (XMOD2) / FMC JTAG	
CAN_FAULT	in	106	CAN	
CAN_RX	in	107	CAN	
CAN_S	out	105	CAN	
CAN_TX	out	104	CAN	
CLK_125MHZ / PHY_CLK	in	70	/ currently_not_used	
CON_NTRST		117	/ currently_not_used	
CON_RTCK / JTAG_RTCK	out	125	JTAG, Connector J30	
CON_SRST / JTAG_SRST	in	127	JTAG, Connector J30	
CON_TCK / JTAG_TCK	in	122	JTAG, Connector J30 / PJTAG0	
CON_TDI / JTAG_TDI	in	119	JTAG, Connector J30 / PJTAG0	

Schematic /Souce Code Name	Direction	Pin	Description	PCB REV2 Exception
CON_TDO / JTAG_TDO	out	126	JTAG, Connector J30 / PJTAG0	
CON_TMS / JTAG_TMS	in	121	JTAG, Connector J30 / PJTAG0	
DIR_T1		23	/ currently_not_used	NC
DIR_T2		28	/ currently_not_used	NC
DIR_T3		27	/ currently_not_used	NC
DP_AUX_DE / DP_DE	out	92	Display Port	
DP_AUX_RX / DP_RX	in	91	Display Port	
DP_AUX_TX / DP_TX	out	93	Display Port	
DP_EN	out	77	Display Port	
DP_TX_HPD / DP_HDP	in	94	Display Port	
ETH_RST	out	62	Ethernet	
EX_IO1		112	PMOD / currently_not_used	
EX_IO2		113	PMOD / currently_not_used	
EX_IO3		114	PMOD / currently_not_used	

Schematic /Souce Code Name	Direction	Pin	Description	PCB REV2 Exception
EX_IO4		115	PMOD / currently_not_used	
F2_EN		19	FAN J35 / currently_not_used	NC
F2PWM		20	FAN J35 / currently_not_used	NC
F2SENSE		21	FAN J35 / currently_not_used	NC
FMC_CLK_DIR	in	73	FMC	
FMC_TCK	out	95	FMC	
FMC_TDI	out	96	FMC	
FMC_TDO	in	97	FMC	
FMC_TMS	out	98	FMC	
FMC_VID0	out	139	FMC VADJ Power Selection	
FMC_VID1	out	140	FMC VADJ Power Selection	
FMC_VID2	out	141	FMC VADJ Power Selection	
GND		84	REV03 unconnected / currently_not_used	USB_TRST, other USB HUB
HDIO_SC10 / SC10	inout	60	FPGA / DP_RX or 'Z'	
HDIO_SC11 / SC11	in	59	FPGA / DP_DE	
HDIO_SC12 / SC12	out	58	FPGA / DP_HPD	
HDIO_SC13 / SC13	out	57	FPGA / RGPIO TX	

Schematic /Souce Code Name	Direction	Pin	Description	PCB REV2 Exception
HDIO_SC14 / SC14	in	56	FPGA / RGPIO RX	
HDIO_SC15 / SC15	in	55	FPGA / RGPIO CLK	
HDIO_SC16 / SC16	in	54	FPGA / CAN_S	
HDIO_SC17 / SC17	in	52	FPGA / XMOD LED	
HDIO_SC18 / SC18	in	68	FPGA / CAN_TX	
HDIO_SC19 / SC19	out	69	FPGA / CAN_RX	
I2C_RST	out	61	I2C	
JTAGENB		120	external Pin for CPLD Firmware Update	
LED_1A / JLED1	out	109	USB3.0 LED Jellow	
LED_2A / JLED2A	out	111	USB3.0 LED Green/Orange	
LED_2B / JLED2B	out	110	USB3.0 LED Green/Orange	
MIO26	in	41	MIO / PJTAG	
MIO27	in	40	MIO / PJTAG	
MIO28	in	39	MIO / PJTAG	
MIO29	in	38	MIO / PJTAG	
OCLK_EN / OSC_EN	out	74	Programmable Oscillator U45	
PHY_CONFIG	out	65	ETH PHY	

Schematic /Souce Code Name	Direction	Pin	Description	PCB REV2 Exception
PHY_LED0	in	67	ETH PHY	
PHY_LED1	in	86	ETH PHY	
PHY_LED2	in	85	ETH PHY	
SC_CLK0 / CLK0	in	76	/ currently_not_used	SC_CLK_P
SC_CLK1 / CLK1	in	75	/ currently_not_used	SC_CLK_N
SC_IO0 / X0	in	50	Master-Slave SC-Communication / Power Reset	
SC_IO1 / X1	in	49	Master-Slave SC-Communication / Power Reset	
SC_IO2 / X2	in	48	Master-Slave SC-Communication / currently_not_used	
SC_IO3 / X3	in	47	Master-Slave SC-Communication / currently_not_used	
SC_IO4 / X4	out	45	Master-Slave SC-Communication / SD WP to Slave CPLD	
SC_IO5 / X5	out	44	Master-Slave SC-Communication / currently_not_used	
SC_IO6 / X6	out	43	Master-Slave SC-Communication / Sanity check to other CPLD (FMC VADJ Enable)	
SC_IO7 / X7	out	42	Master-Slave SC-Communication / Sanity check to other CPLD (FMC VADJ Enable)	
SC_IO8		22	Master-Slave SC-Communication / currently_not_used	NC

Schematic /Souce Code Name	Direction	Pin	Description	PCB REV2 Exception
SC_SCL / SCL	in	14	I2C Mux U27 / currently_not_used	
SC_SDA / SDA	in	13	I2C Mux U27 / currently_not_used	
SC2_SW3 / SW3	in	6	DIP-Switch S5-3	
SC2_SW4 / SW4	in	5	DIP-Switch S5-4	
SD_WP	in	100	MMC SD	
SFP_LED1 / SFP_LED0	out	81	SFP	
SFP_LED2 / SFP_LED1	out	82	SFP	
SFP_LED3 / SFP_LED2	out	78	SFP	
SFP_LED4 / SFP_LED3	out	83	SFP	
SFP1_LOS		32	SFP / currently_not_used	NC, controlled by FPGA
SFP1_TX_DIS	out	33	SFP	NC, controlled by FPGA
SFP2_LOS		35	SFP / currently_not_used	NC, controlled by FPGA
SFP2_TX_DIS	out	34	SFP	NC, controlled by FPGA
STAT_LED0 / LED0		99	LED D4 Green	

Schematic /Souce Code Name	Direction	Pin	Description	PCB REV2 Exception
STAT_LED1 / LED1		128	LED D1 Red	
USB0_RST / USB_RST	out	71	USB (U9) PHY Reset	USB PHY and HUB Reset
USBH_LED_G3		11	USB Hub (U4) / currently_not_used	NC, other USB HUB
USBH_LED_G4		12	USB Hub (U4) / currently_not_used	NC, other USB HUB
USBH_LED_SS1		9	USB Hub (U4) / currently_not_used	NC, other USB HUB
USBH_LED_SS2 / dummy	out	133	USB Hub (U4) Dummy Signal / currently_not_used	NC, other USB HUB
USBH_LED_SS3		132	USB Hub (U4) / currently_not_used	NC, other USB HUB
USBH_LED_SS4		138	USB Hub (U4) / currently_not_used	NC, other USB HUB
USBH_MODE0	out	142	USB Hub (U4)	NC, other USB HUB
USBH_MODE1	out	143	USB Hub (U4)	NC, other USB HUB
USBH_RST	out	10	USB Hub (U4)	NC, other USB HUB
XMOD1_A		3	J28 (XMOD 2) / currently_not_used	
XMOD1_B		2	J28 (XMOD 2) / currently_not_used	

Schematic /Souce Code Name	Direction	Pin	Description	PCB REV2 Exception
XMOD1_E /XMOD_E	out	4	J28 (XMOD 2 LED)	
XMOD1_G / XMOD_G	in	1	J28 (XMOD 2 Button)	

Functional Description

JTAG

JTAGENB set carrier board CPLD into the chain for firmware update. For Update set DIP S4-3 to ON.

FMC JTAG is connected to XMOD2 JTAG. Set DIP S4-3 to OFF for FMC access.

PJTAG (MIO29..26) is connected to JTAF Pinheader J30.

Power

FMC VADJ is 1.8V if S5-4 is ON else 1.2V.

Reset

Main Reset is send by Slave CPLD via X0, X1 Pins.

USB PHY hold ~0,6s after Main Reset or XMOD_G Reset or inv.RGPIO Bus Pin 0 (if active).

USB HUB hold ~0,25s after Main Reset or XMOD_G Reset or inv. RGPIO Bus Pin 0 (if active). Long delay is a BUGFIX: is currently need to start Linux before Reset is disabled.

I2C Reset is Main Reset or inv. RGPIO Bus Pin 2 (if active).

ETH Reset is Main Reset or inv. RGPIO Bus Pin 3 (if active).

Enable

FMC VADJ Enable is set from Slave CPLD via Saity Check (X6, X7).

SFP1 and SFP2 are always enabled.

Oscillator U45 is enabled

USB

USB Hub Device Operation Mode (USBH_MODEx Pins) are set to internal ROM configuration. Can be controlled by RGPIO Bus Pin 4 and 5.

ETH

PHY Address is 1.

Display Port

SC10 is controlled by DP_RX when SC11 is zero else high impedance state. DP_TX controlled by SC10 and DP_DE controlled by SC11.SC12 is controlled by DP_HPD.

CAN

CAN_TX soured by SC18.

SC19 sourced by CAN_RX.

CAN_S sourced by S16.

SD

SD WP is forwarded to Slave CPLD.

RGPIO

RGPIO Pin to FPGA	Value
0	SW3
1	SW4
2	SD_WP
3	XMOD_G
4	'0'
5	'0'
6	'0'
7	'0'
8	CAN_FAULT
9	PHY_LED0
10	PHY_LED1
11	PHY_LED2

RGPIO Pin to FPGA	Value
12	FMC_TDO
13	FMC_CLKDIR
14	JTAG_TRST
15	JTAG_SRST
16	'0'
17	'0'
18	'0'
19	DP_HPD
20	SDA
21	SCL
22-23	unused zero
24-27	reserved
28-31	Interface detection

RGPIO Pin from FPGA	Value
0	not USB_RST
1	not USBH_RST
2	not I2C_RST
3	not ETH_RST
4	not USBH_MODE0

RGPIO Pin from FPGA	Value
5	not USBH_MODE1
6	LED0
7	LED1
8	SFP_LED0
9	SFP_LED1
10	SFP_LED2
11	SFP_LED3
12	JLED1
13	JLED2A
14	JLED2B
15-23	unused
24-27	reserved
28-31	Interface detection

LED

Name	Description
LED0 D4 Green	RGPIO (6) when active else USB HUB RSTN
LED1 D1 Red	RGPIO (7) when active else Main Reset from Slave CPLD
SFP_LED0 Red	RGPIO (8) when active else blinking when PCB power is on and reset Button is pressed else off

Name	Description
SFP_LED1 Green	RGPIO (9) when active else blinking when PCB power is on and reset Button is pressed else off
SFP_LED2 Red	RGPIO (10) when active else blinking when PCB power is on and reset Button is pressed else off
SFP_LED3 Green	RGPIO (11) when active else blinking when PCB power is on and reset Button is pressed else off
JLED1 Yellow	RGPIO (12) when active else blinking when PCB power is on and reset Button is pressed else not PHY_LED0 when X1 is zero else off
JLED2A Green	RGPIO (13) when active else blinking when PCB power is on and reset Button is pressed else not PHY_LED1 when X1 is zero else on
JLED2B Orange	RGPIO (14) when active else blinking when PCB power is on and reset Button is pressed else off
XMOD_E Red	Blinking when Main Power Reset else SC17

*Blinking: ~1,5Hz

7.1.3 Appx. A: Change History

Revision Changes

CPLD REV05 to REV06

- BUGFIX: renamed SC19 to SC17
- Connect FMC JTAG to XMOD2 JTAG
- Connect PJTAG0 (MIO29..26) to JTAG Pin Header J30
- Connect CAN to PL
- RGPIO Pin changes

CPLD REV04 to REV05

- SD WP
- XMOD LED access over PL

Older Revision (PCB REV03) to CPLD REV04

- Fix USB HUB Mode default state over RGPIO
- Invert JLED2B over RGPIO

Older Revision (PCB REV02) to CPLD REV04

- Add all functionality from older Revision (PCB REV03)

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
2017-11-02	v.27 (see page 54) Unbekanntes Makro: 'metadata'	REV06	(REV02 Special Firmware!), REV03,REV04	@ John Hartfiel[8]	• small Update Pinout Table
2017-10-18	v.25	REV06	(REV02 Special Firmware!), REV03,REV04	John Hartfiel[9]	• Revision 06 finished
2017-06-20	v.23	REV05	(REV02 Special Firmware!), REV03,REV04	John Hartfiel[10]	• Document Bugfix, XMOD LED is connected to SC17
2017-06-12	v.22	REV05	(REV02 Special Firmware!), REV03,REV04	John Hartfiel[11]	• Port description update
2017-06-09	v.21	REV05	(REV02 Special Firmware!), REV03,REV04	John Hartfiel[12]	• Revision 05 finished
2017-06-08	v.17 (see page 54)	REV04	(REV02 Special Firmware!), REV03,REV04	John Hartfiel[13]	• document style update

8 https://wiki.trenz-electronic.de/display/~j.hartfiel
9 https://wiki.trenz-electronic.de/display/%7Ej.hartfiel
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Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
2017-03-10	v.15 (see page 54)	REV04	(REV02 Special Firmware!), REV03,REV04	John Hartfiel[14]	• Revision 04 finished
2016-12-14	v.1	---		@ John Hartfiel[15]	• Initial release
	All			@ John Hartfiel[16]	

7.1.4 Appx. B: Legal Notices

Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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REACH, RoHS and WEEE

REACH

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17 http://guidance.echa.europa.eu/
18 https://echa.europa.eu/candidate-list-table
19 http://www.echa.europa.eu/

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2019-06-07

7.2 TEBF0808 Slave CPLD

Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/SC-CPLD-Firmware

7.2.1 Overview

Firmware for PCB-Slave CPLD with designator U39. Second CPLD Device in Chain: LCMX02-1200HC

Feature Summary

- Power Management
- Reset Management
- Boot Mode
- LEDs
- RGPIO
- SD Selection
- UART

Firmware Revision and supported PCB Revision

See Document Change History

7.2.2 Product Specification

Port Description

Name / opt. VHD Name	Direction	Pin	Description
1.8V_EN / EN_1V8	out	106	Power
5V_EN / EN_5V	out	115	Enable 5V, can be permanently enabled by S4-4
C_TCK		131	JTAG J28 (XMOD2) / internal currently_not_used

Name / opt. VHD Name	Direction	Pin	Description
C_TDO		137	JTAG J28 (XMOD2) / internal currently_not_used
C_TDO1		136	JTAG J28 (XMOD2) / internal currently_not_used
C_TMS		130	JTAG J28 (XMOD2) / internal currently_not_used
CLK_A / AUD_CLK	out	1	AUDIO U3 CLK
CLK_CPLD / MEMS_CLKIN	in	128	U25 24,576MHz
DONE	in	67	PS Done
EN_DDR	out	86	Enable DDR Power
EN_FMC / FMC_EN	out	104	FMC
EN_FPD	out	81	Enable PS FPD Power
EN_GT_L	out	77	Enable GT Power
EN_GT_R	out	93	Enable GT Power
EN_LPD	out	84	Enable PS LPL Power
EN_PL	out	95	Enable PL Power
EN_PLL_PWR	out	78	Enable SI5345 Power
EN_PSGT / EN_PSGTR	out	75	Enable PS GT Power
ERR_OUT / ERROR	in	70	PS Error Out / Status / readable via RGIO

Name / opt. VHD Name	Direction	Pin	Description
ERR_STATUS / ERROR_STAT	in	69	PS Error Status / Status / readable via RGIO
F1PWM	out	121	FAN1
F1SENSE	in	125	FAN1
FAN_FMC_EN / FMC_FAN_EN	out	132	FMC FAN
FMC_PG_C2M	out	141	FMC PG
HD_LED_N / HDLED_N	out	112	J10 HD LED
HD_LED_P / HDLED_P	out	110	J10 HD LED
HDIO_SC0 / SC0	in	32	FPGA IO / forward to HD_LED_P / HDLED_P
HDIO_SC1 / SC1	in	33	FPGA IO / currently_not_used
HDIO_SC2 / SC2	in	34	FPGA IO / currently_not_used
HDIO_SC3 / SC3	out	35	FPGA IO / currently_not_used
HDIO_SC4 / SC4	out	25	FPGA IO / currently_not_used
HDIO_SC5 / SC5	out	26	FPGA IO / RGPIO
HDIO_SC6 / SC6	in	27	FPGA IO / RGPIO CLK
HDIO_SC7 / SC7	in	28	FPGA IO / RGPIO
I2C_SCL / SCL	in	50	I2C / currently_not_used

Name / opt. VHD Name	Direction	Pin	Description
I2C_SDA / SCA	in	52	I2C / currently_not_used
INIT_B / INIT	in	68	PS init B
JTAGENB		120	external Pin for CPLD Firmware Update
LP_GOOD / PG_LPD	in	83	LP Power Good
MIO24		38	MIO / currently_not_used
MIO25		39	MIO / currently_not_used
MIO30	in	48	MIO / force reboot after FSBL-PLL config for PCIe
MIO31	in	49	MIO / PCIe reset
MIO32		40	MIO / currently_not_used
MIO33		41	MIO / currently_not_used
MIO34		42	MIO / currently_not_used
MIO35		43	MIO / currently_not_used
MIO36		44	MIO / currently_not_used
MIO37		45	MIO / currently_not_used
MIO40	in	54	MIO / forwarded to PWRLED_P / LED_P
MIO41		55	MIO / currently_not_used
MIO42	out	60	FPGA UART RX
MIO43	in	61	FPGA UART TX

Name / opt. VHD Name	Direction	Pin	Description
MIO44	out	47	MIO / SD_WP to FPGA
MOD_EN	out	119	Module Power 3.3V Enable
MODE0	out	6	Boot Mode
MODE1	out	9	Boot Mode
MODE2	out	10	Boot Mode
MODE3	out	11	Boot Mode
MR / MRESETn	out	92	PS Reset
PCI_SFP_EN	out	76	SFP
PER_EN	out	117	Baseboard Power 3.3V Enable
PERST / PERSTn	out	139	PCIE Resetn
PG_DDR	in	91	Power Good / Status / readable via RGIO
PG_FPD	in	85	Power Good / Status / readable via RGIO
PG_GT_L	in	96	Power Good / Status / readable via RGIO
PG_GT_R	in	94	Power Good / Status / readable via RGIO
PG_PL	in	82	Power Good / Status / readable via RGIO
PG_PLL_1V8 / PG_PLL	in	73	Power Good / Status / readable via RGIO
PG_PSGT	in	74	Power Good / Status / readable via RGIO

Name / opt. VHD Name	Direction	Pin	Description
PLL_LOLN / PLL_LOL	in	58	Module U5 Si5345 / readable via RGIO / currently_not_used
PLL_RST / PLL_RSTn	out	56	Module U5 Si5345
PLL_SEL0	out	57	Module U5 Si5345
PLL_SEL1	out	59	Module U5 Si5345
POK_1V8	in	107	Power
POK_FMC	in	99	FMC Power/ readable via RGIO
PROG_B	inout	71	PS_PROG_B
PSON	out	105	ATX J20 PS_ON_N
PWR_BTN	in	113	Power Button S1 or J10
PWRLED_N / LED_N	out	111	J10 PWR
PWRLED_P / LED_P	out	109	J10 PWR
PWROK	in	100	ATX J20 PWROK / readable via RGIO
RST_BTN	in	114	Reset Button S2 or J10
S_1		127	Beeper/ currently_not_used
SC_IO0 / X0	out	12	Master-Slave SC-Communication / Power Reset

Name / opt. VHD Name	Direction	Pin	Description
SC_IO1 / X1	out	13	Master-Slave SC-Communication / Power Reset
SC_IO2 / X2	out	14	Master-Slave SC-Communication / currently_not_used
SC_IO3 / X3	out	20	Master-Slave SC-Communication / currently_not_used
SC_IO4 / X4	in	21	Master-Slave SC-Communication /MMC SD WP
SC_IO5 / X5	in	22	Master-Slave SC-Communication / currently_not_used
SC_IO6 / X6	in	23	Master-Slave SC-Communication / Sanity check from other CPLD (FMC VADJ Enable)
SC_IO7 / X7	in	24	Master-Slave SC-Communication / Sanity check from other CPLD (FMC VADJ Enable)
SC_IO8 / dummy		126	/ currently_not_used / ! not available on PCB REV2 !
SC2_SW1	in	133	S5-1 / Boot Mode Selection / readable via RGIO
SC2_SW2	in	138	S5-2 / Boot Mode Selection / readable via RGIO
SD_A_EN	out	140	Micro SD
SD_B_EN	out	122	MMC SD
SD_CD / SD_CD_OUT	out	65	SD Card detect to FPGA
SD_CD_B	in	143	MMC SD / readable via RGIO

Name / opt. VHD Name	Direction	Pin	Description
SD_CD_S	in	142	Micro SD / readable via RGIO
SEL_SD / SD_SEL	out	62	Select SD
SRST_B / SRSTn	out	19	PS_SRST_B
STAT_LED2 / LED2	out	98	LED D6 Green
STAT_LED3 / LED3	out	97	LED D7 Red
XMOD2_A / XMOD_TXD	out	5	J12 (XMOD 1)
XMOD2_B / XMOD_RXD	in	4	J12 (XMOD 1)
XMOD2_E / XMOD_LED	out	3	J12 (XMOD 1)
XMOD2_G / XMOD_BTN	in	2	J12 (XMOD 1) / readable via RGIO

Functional Description

JTAG

JTAGENB set carrier board CPLD into the chain for firmware update. For Update set DIP S4-3 to ON.

Power

PSON signal will be enabled/disabled after delay, when Power Button is pressed. Power Button is debounced.

Stage	Power Enable Signal	Enable Power domain	Note
1	PSON	ATX PSON (12V from ATX power supply)	Signal will be enabled/ disabled after delay, when Power Button is pressed.Power Button is debounced.

Stage	Power Enable Signal	Enable Power domain	Note
2	PWROK(ATX Power)	5V_EN (5V)	Note 1: If S4-4 is on, 5V is always on. S4-4 must be on, if TEBF0808 is used with external 12V instead of ATX Power. Note 2: CPLD Pullup is used for PWROK to works without external 12V only.
2	PWROK	MOD_EN (Module 3.3V), EN_LPD, EN_FPD, EN_PL	Module B2B connector Main Power and enables
3	PG_FPD	EN_DDR, EN_PLL_PWR, EN_PSGTR	Module periphery power
3	PG_PL	EN_GT_R, EN_GT_L	Module periphery power
4	PG_FPD and PG_PL	PER_EN(Periphery 3.3V), EN_1V8(Periphery 1.8V), PCI_SFP_EN (PCIe and SFP)	Carrier periphery power
4	PWROK and PG_FPD and PG_PL and PSON and Master CPLD status	FMC_EN (FMC VADJ)	FMC VADJ
5	PWROK and PG_FPD and PG_PL and PSON and POK_FMC(VADJ)	FMC_PG_C2M	FMC supply power status to FMC connector

Note: Power Status is visible on LEDs, see LED section

⚠ TE0808 module is not completely powered off with power button, if 12V power jack (J25) is used for power supply. 12V Power ON/OFF is only with ATX power supply usable.

Enable

SD's will be enabled by PWROK and PG_FPD and PG_PL and PSON;.

FMC_FAN_EN will be enabled by PWROK and PG_FPD and PG_PL and PSON_i or RGPIO (11) controlled, when active. F1PWM is constant on.

Reset

Power Button is debounced.

Reset will be also set via modified FSBL, if PCIe is detected.

Name	Description
PLL_RSTn	not RGPIO (0) when active else '1'
SRSTn	'1'
MRESETn	RST_BTN and PWROK and PG_FPD and PG_PL and PSON and "PS reboot via FSBL"
PERSTn	not RGPIO (1) and MIO31 when active else rst_btn_i and MIO31
Master CPLD Reset	PWROK and PG_FPD and PG_PL and PSON and Reset Button over CPLD interconnect.
PS reboot via FSBL	Reboot possible over FSBL over MIO30 (need for proper PCI initialization on first power on without press Reset Button)

Note: Reset Status is visible on LEDs, see LED section

Boot Mode

S5-1	S5-2	Description
ON	ON	Default, boot from SD/microSD or SPI Flash if no SD is detected
OFF	ON	Boot from eMMC
ON	OFF	Boot mode PJTAG0
OFF	OFF	Boot mode main JTAG

Note: Boot Mode Status is visible on LEDs, see LED section

UART

XMOD_TXD is sourced by MIO43 and MIO42 by XMOD_RXD.

Module SI5345

Module U5 Selection Pins are constant zero.

SD Card

SD Card selection is done via Micro SD Card detection.

SD WP is forwarded to ZynqMP from Master CPLD.

RGPIO

RGPIO Pin to FPGA	Value
0	SW1
1	SW2
2	XMOD_BTN
3	Force FSBL reboot done
4	SD_CD_S
5	SD_CD_B
6	Error
7	ERR_STAT
11-8	Boot Mode
12	PG_LPD
13	PG_DDR
14	PG_FPD
15	PG_PSGT

RGPIO Pin to FPGA	Value
16	PG_GT_L
17	PG_GT_R
18	POK_FMC
19	DET_POWROK
20	PWROK
21	PG_PL
22	PG_PLL
23	PLL_LOL
24-27	reserved
28-31	Interface detection

RGPIO Pin from FPGA	Value
0	PLL_RSTn
1	PERSTn
2	FMC_FAN_EN
7	LED_N
8	LED_P
9	HDLED_N
10	HDLED_P
12-23	unused

RGPIO Pin from FPGA	Value
24-27	reserved
28-31	Interface detection

LED

LED2 D6 Green (near FAN1 connector on PCB)		
Power Flags	**Blink Sequence**	**Comment**
PWROK	********	ATX Power failed or PCB is powered off
PG_LPD	*****ooo	Module Low Power Domain failed
PG_FPD	****oooo	Module Full Power Domain failed
PG_PL	***ooooo	Module PL Power Domain failed
POK_1V8 or POK_FMC	**oooooo	Carrier 1V8 or FMC VADJ Power Domain failed
PG_DDR='0' or PG_GT_L='0' or PG_GT_R='0' or PG_PSGT='0' or PG_PLL='0'	*ooooooo	Module DDR, PL GT, PS GT or PLL Power Domain failed
	OFF	All Ready

LED3 D7 Red (near FAN1 connector on PCB)		
Bode Mode	**Blink Sequence**	**Comment**
Error	********	ERROR

LED3 D7 Red (near FAN1 connector on PCB)		
Bode Mode	**Blink Sequence**	**Comment**
JTAG	*****ooo	JTAG
PJTAG0	****oooo	Boot Mode is set to PJTAG0
eMMC	***ooooo	Boot Mode is set to eMMC
SPI Boot	**oooooo	Boot Mode is set to QSPI
SD Boot	*ooooooo	Boot Mode is set to SD
	ON	Reset is on

XMOD LED Red (XMOD1 on J12 with green dot)		
Status	**Blink Sequence**	**Comment**
PS_INIT_B	********	Indicates the PS is not initialized after a power-on reset (POR).
PS_ERROR_OUT	*****ooo	The PS_ERROR_OUT signal is asserted for accidental loss of power, an error, or an exception in the PMU.
DONE	ON or OFF	Indicates the PL configuration is completed (LED is OFF).

LED_P/N (BLUE Power LED on enclosure)		
Status/ User	**Blink Sequence**	**Comment**
Power	******** (slow blink)	Indicate board is powered off.
RGPIO controlled	User Defined	RGPIO 14 and 15, if RGPIO is active.

LED_P/N (BLUE Power LED on enclosure)		
Status/ User	**Blink Sequence**	**Comment**
MIO40	User Defined	MIO40, if RGPIO is deactivated

HDLED_P/N (Red HD LED on enclosure)		
Status/ User	**Blink Sequence**	**Comment**
PS_INIT_B	********	Indicates the PS is initialized after a power-on reset (POR).
PS_ERROR_OUT	*****ooo	The PS_ERROR_OUT signal is asserted for accidental loss of power, an error, or an exception in the PMU.
ERR_STAT	****oooo	The PS_ERROR_STATUS indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status.
RGPIO controlled	User Defined	RGPIO 16 and 17, if RGPIO is active
SC0	User Defined	SC0 (PL IO), if RGPIO is deactivated

Blink Frequency:

Blink Sequence	Comment
********	~5,8 Hz
*****ooo	~0,7 Hz, duty cycle 5/8
****oooo	~0,7 Hz, duty cycle 4/8
***ooooo	~0,7 Hz, duty cycle 3/8
**oooooo	~0,7 Hz, duty cycle 2/8
*ooooooo	~0,7 Hz, duty cycle 1/8

7.2.3 Appx. A: Change History

Revision Changes

CPLD REV05 to REV06

- LED Status changes of LED D2 D3 and HD_LED, XMOD LED
- extended Power Management

CPLD REV04 to REV05

- PS reboot via FSBL over MIO30 (need for proper PCI initialization on first power on without press Reset Button)
- SD Boot from micoSD only if switch S5-1/-2 is selected to ON
- RGPIO connection
- Add SD WP to FPGA
- Power, Rest Button debounced
- direct LED access via MIO and PL

Older Revision (PCB REV03) to CPLD REV04

- Bugfix: PCIe Reset Pin location.
- Bugfix: Swapping HDLED and PWRLED location.
- Bugfix: MEMS_CLKIN Pin location.
- Add XMOD 1 LED

Older Revision (PCB REV02) to CPLD REV04

- Add all functionality from older Revision (PCB REV03)

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
2018-01-17	v.39 (see page 70) Unbekanntes Makro: 'metadata'	REV06	REV02, REV03, REV04	@ John Hartfiel[20]	• typo correction
2017-11-15	v.38	REV06	REV02, REV03, REV04	John Hartfiel[21]	• Correction Boot Mode Section
2017-10-18	v.36	REV06	REV02, REV03, REV04	John Hartfiel[22]	• Revision 06 finished

20 https://wiki.trenz-electronic.de/display/~j.hartfiel
21 https://wiki.trenz-electronic.de/display/~j.hartfiel
22 https://wiki.trenz-electronic.de/display/~j.hartfiel

Date	Document Revision	CPLD Firmware Revision	Supported PCB Revision	Authors	Description
2017-06-20	v.29	REV05	REV02, REV03, @ REV04	John Hartfiel[23]	• description and style bug-fix
2017-06-09	v.28	REV05	REV02, REV03, @ REV04	John Hartfiel[24]	• Revision 05 finished
2017-06-08	v.23 (see page 70)	REV05	REV02, REV03, @ REV04	John Hartfiel[25]	• Document style update
2017-05-08	v.22 (see page 70)	REV05	REV02, REV03, @ REV04	John Hartfiel[26]	• Revision 05 working in process
2017-02-08	v.19	REV04	REV02, REV03, REV04	John Hartfiel[27]	• Revision 04 finished
2016-04-11	v.1	---		@ John Hartfiel[28]	• Initial release
	All			@ John Hartfiel[29]	

7.2.4 Appx. B: Legal Notices

Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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30 http://guidance.echa.europa.eu/
31 https://echa.europa.eu/candidate-list-table

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