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CHANGES REV01 to REV02

- 1) MAC EEPROM Address patch fixed on PCB
- 2) lib components update

A

A

B

B


C

C

D

D

Assembly variant	81C11-A
Created by	VY
Modified by	VY
Modified at	2019-07-08
SVN Version	8496

	Title: TE0745		
	A4	Number: 1 81C11-A	Rev. 02
	Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page1 of 25
	Filename: Revision Changes.SchDoc		

1

2

3

4

U_J1
J1.SchDoc

U_J2
J2.SchDoc

U_J3
J3.SchDoc

U_ZYNQ
ZYNQ.SchDoc

U_POWER
POWER.SchDoc

U_POWER_2
POWER_2.SchDoc

U_RTC
SENSOR-RTC.SchDoc

U_POWER_3
POWER_3.SchDoc

U_CLK
CLK.SchDoc

U_DDR3
DDR3-RAM.SchDoc

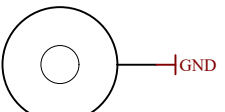
U_ETH_PHY
ETH-PHY.SchDoc

U_USB_PHY
USB-PHY.SchDoc

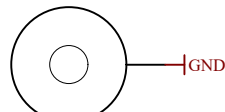
U_PowerOverview
PowerOverview.SchDoc

U_Revision Changes
Revision Changes.SchDoc

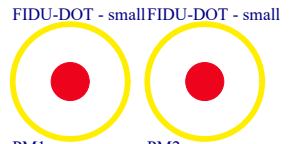
LOGO1
TE Logo PRINT Layer
LOGO PRINT



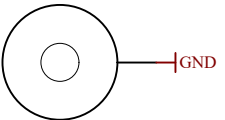
Mount.Hole 3.2mm für Unterlegscheibe



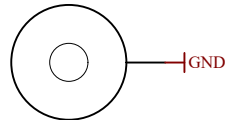
Mount.Hole 3.2mm für Unterlegscheibe



PM1 FIDU-DOT - small



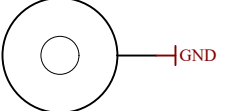
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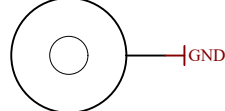
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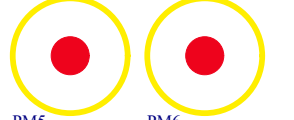
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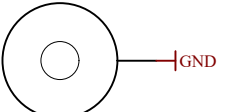
Mount.Hole 3.2mm für Unterlegscheibe



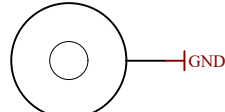
Mount.Hole 3.2mm für Unterlegscheibe



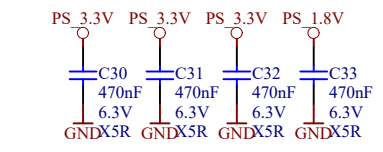
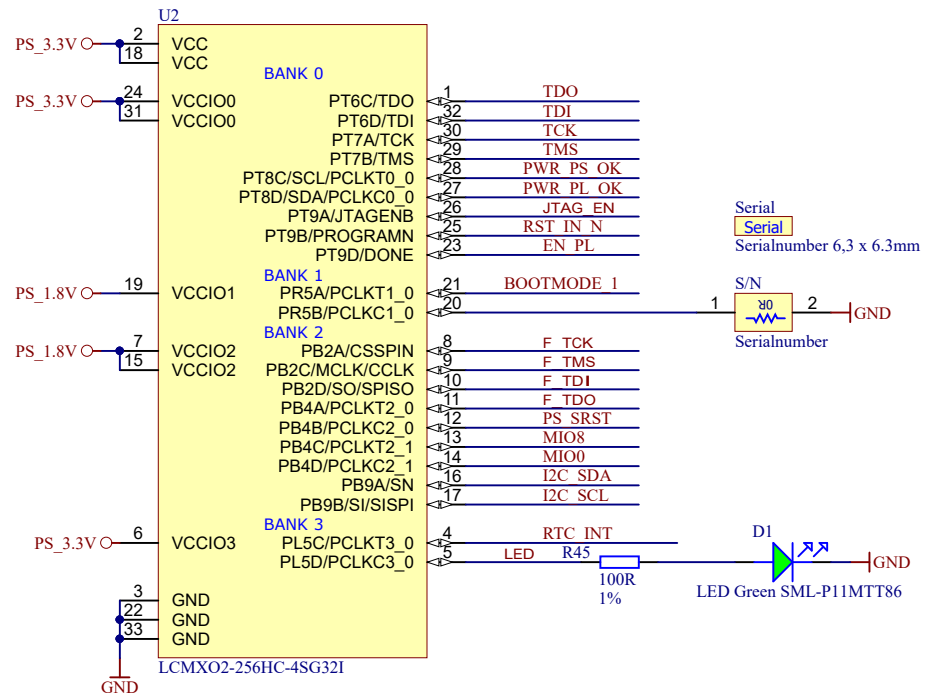
PM5 FIDU-DOT - small



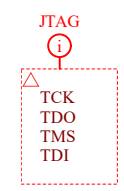
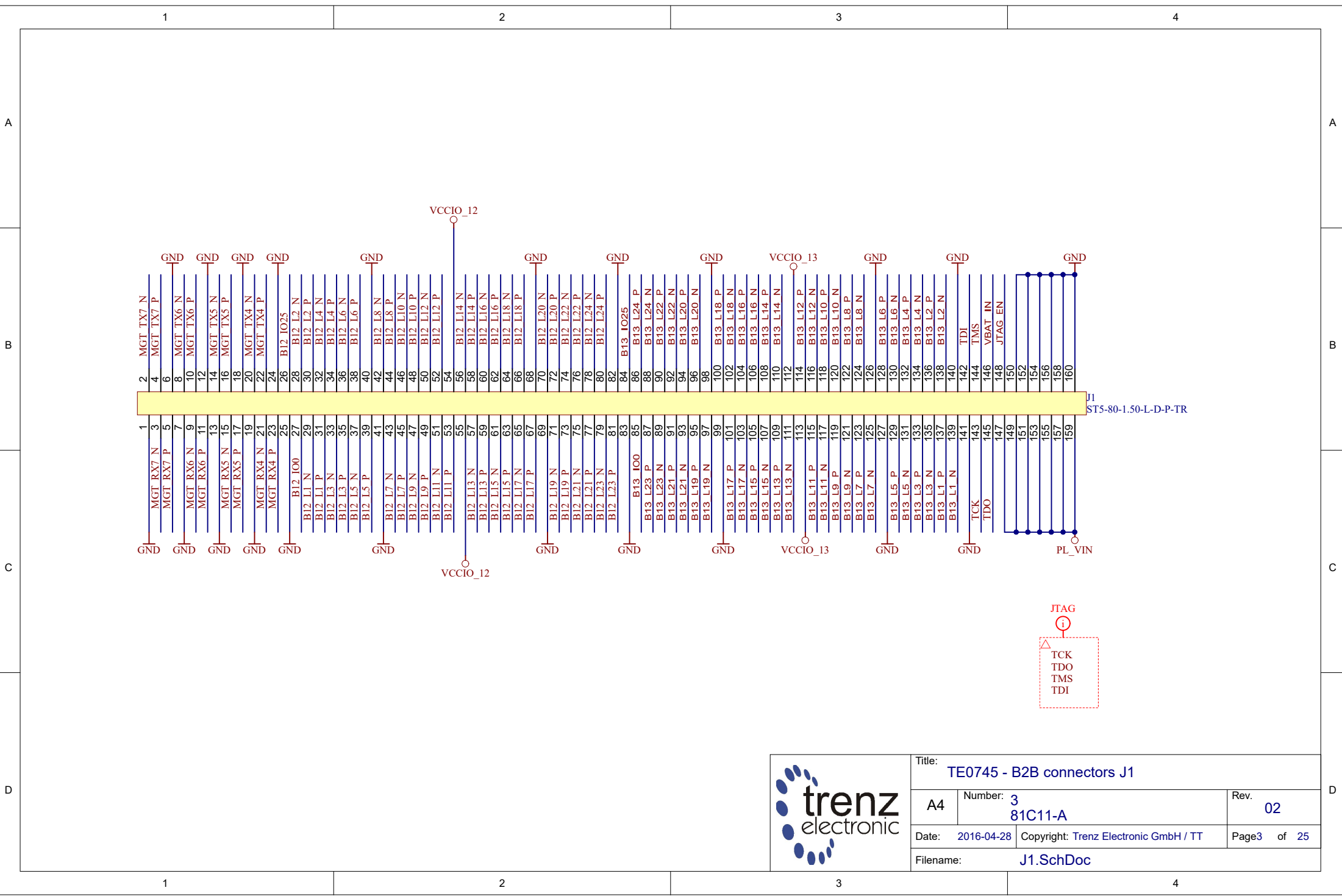
Mount.Hole 3.2mm für Unterlegscheibe




Mount.Hole 3.2mm für Unterlegscheibe



	Title: TE0745	
	A4	Number: 2 81C11-A
	Date: 2016-04-28	Rev. 02
	Copyright: Trenz Electronic GmbH / TT	Page 2 of 25
Filename: TE0745.SchDoc		

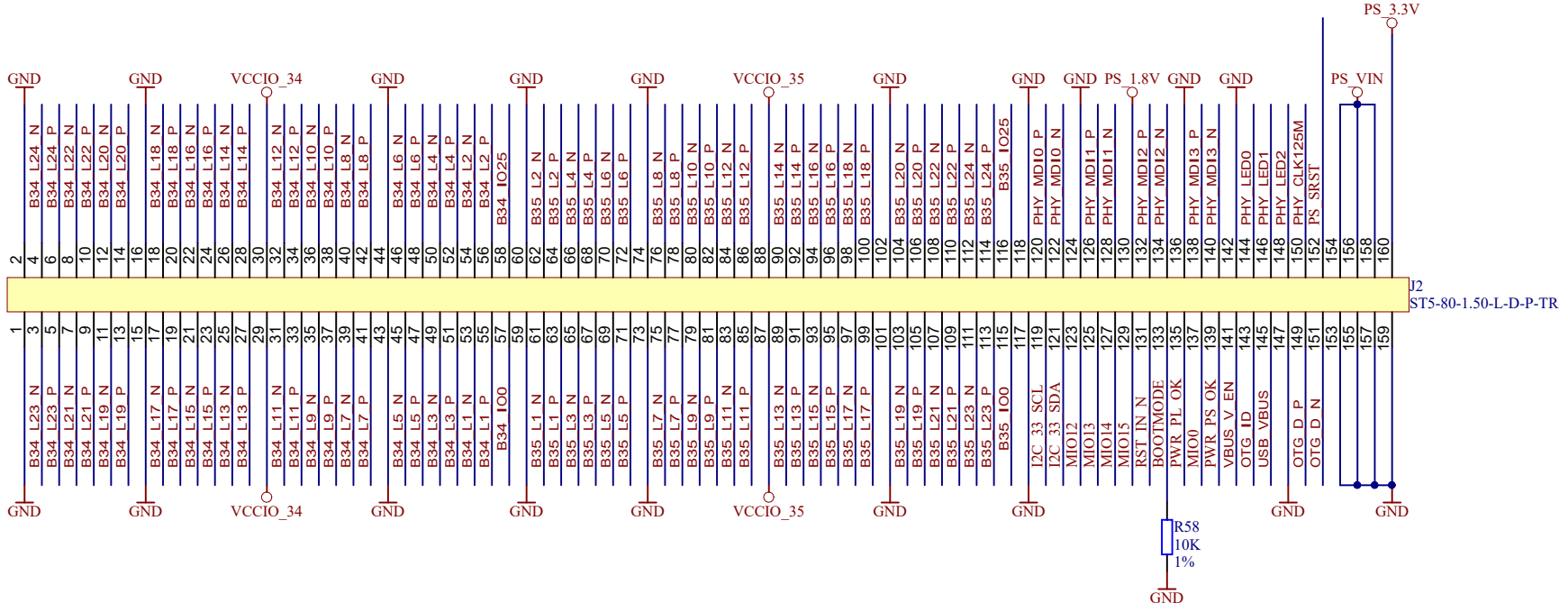


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		A4	Number: 3 81C11-A
Date: 2016-04-28		Copyright: Trenz Electronic GmbH / TT	
Date: 2016-04-28		Page 3 of 25	
Filename: J1.SchDoc			

ETH_MDI

1

- PHY_MDI1_P
- PHY_MDI1_N
- PHY_MDI3_P
- PHY_MDI3_N
- PHY_MDI0_P
- PHY_MDI0_N
- PHY_MDI2_P
- PHY_MDI2_N



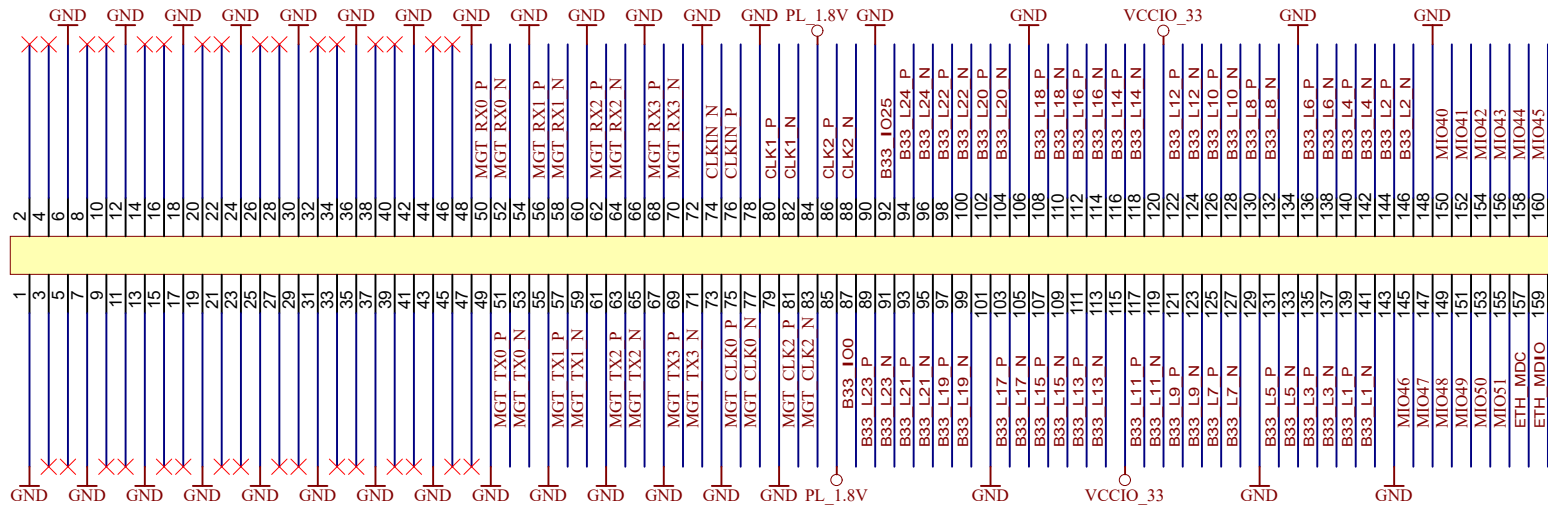
J2 ST5-80-1.50-L-D-P-TR

R58 10K 1% GND



Title: TE0745 - B2B connectors J2		
A4	Number: 4 81C11-A	Rev. 02
Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page 4 of 25
Filename: J2.SchDoc		

RESERVED for additional 8 GTX lanes



J3
ST5-80-1.50-L-D-P-TR



Title: TE0745 - B2B connectors J3		
A4	Number: 5 81C11-A	Rev. 02
Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page5 of 25
Filename: J3.SchDoc		

1

2

3

4

U_B12
B12.SchDoc



U_B500
MIO_B500.SchDoc



U_B13
B13.SchDoc



U_PS_DDR
PS-DDR.SchDoc



U_B33
B33.SchDoc



U_MISC
ZYNQ_MISC.SchDoc



U_B34
B34.SchDoc



U_ZYNQ_POWER
ZYNQ_POWER.SchDoc



U_B35
B35.SchDoc



U_FPGA_MGT
FPGA_MGT.SchDoc



A

A

B

B

C

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D


D

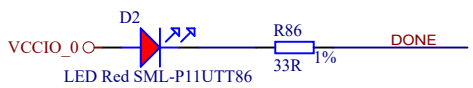
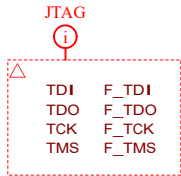
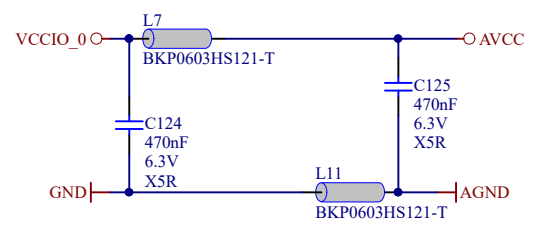
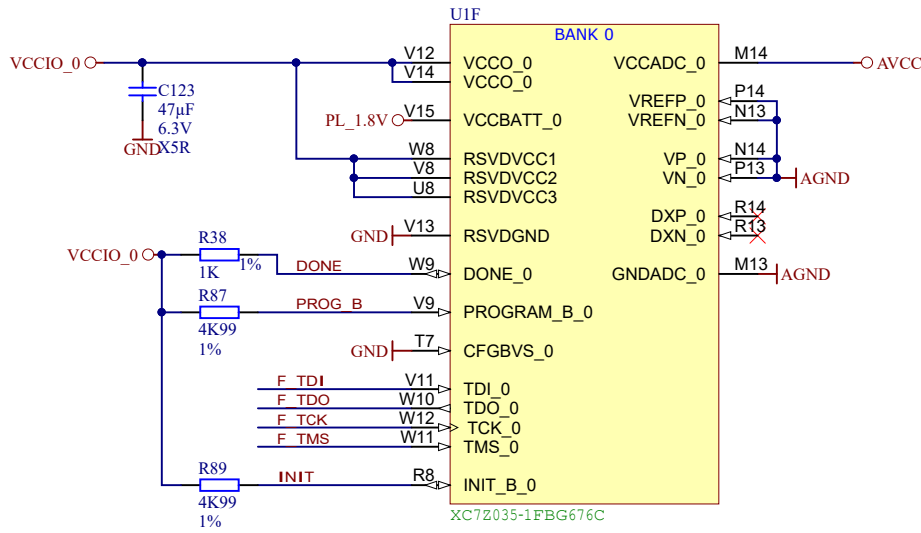
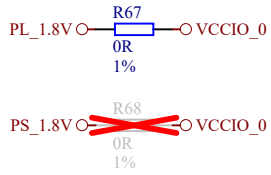
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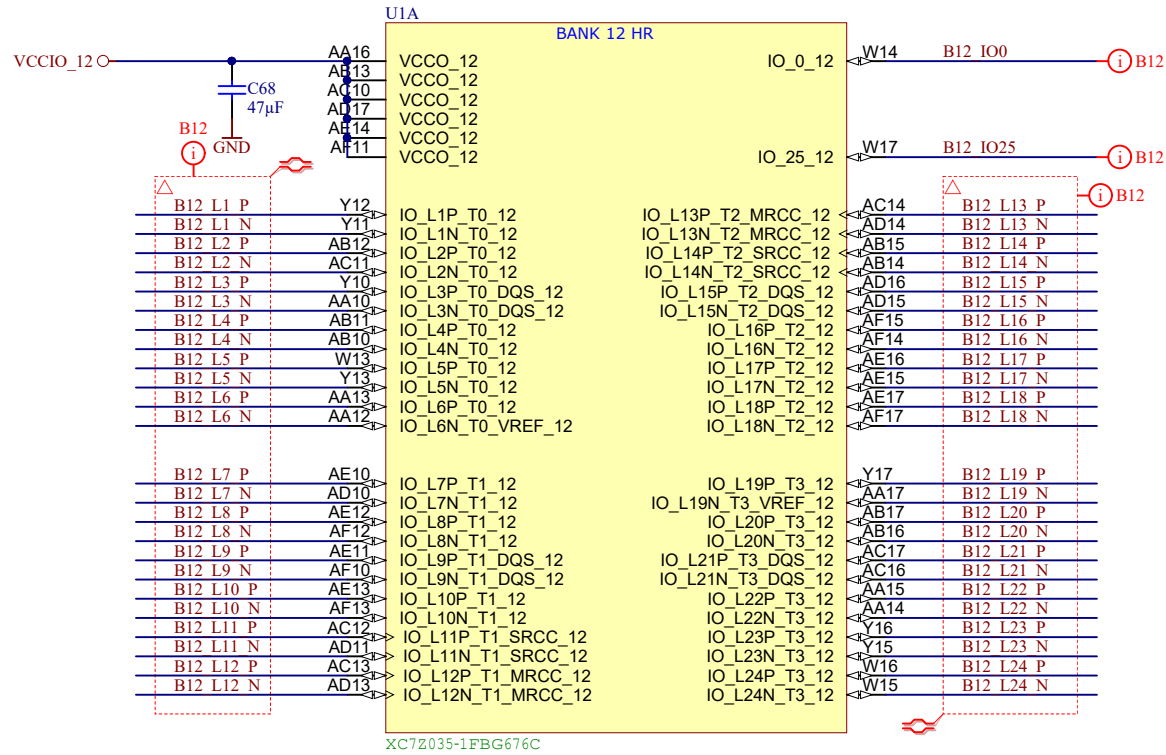
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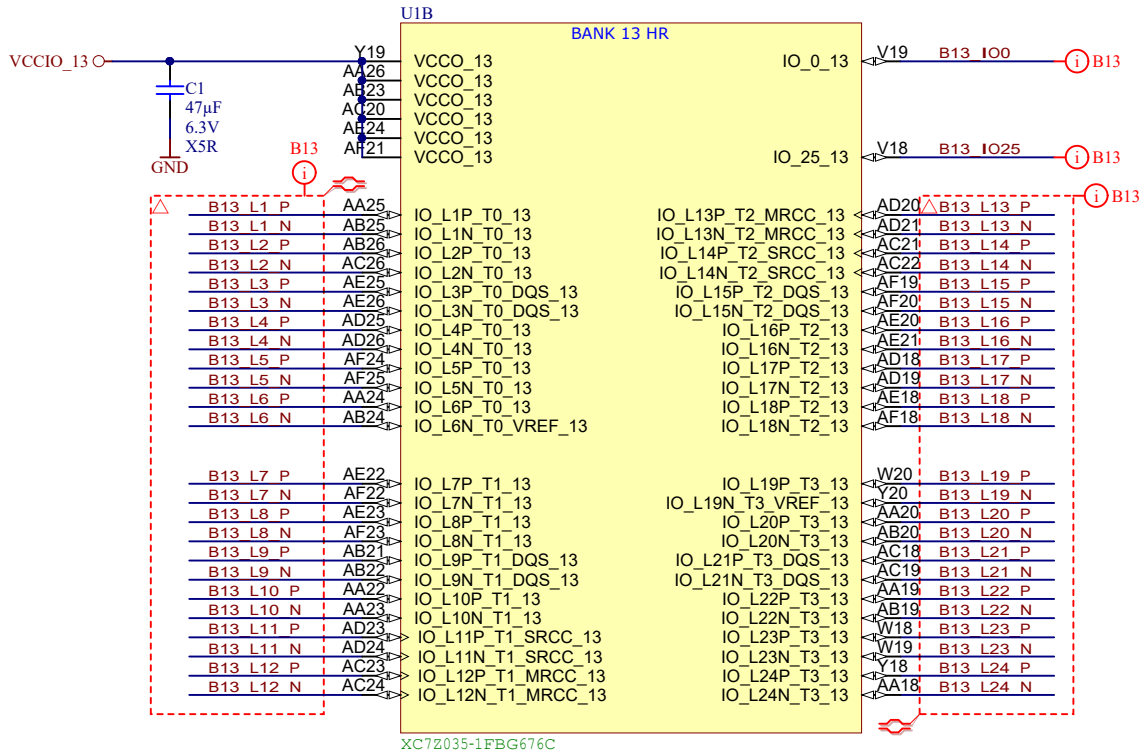
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			A4	Number: 6 81C11-A	Rev. 02
Date: 2016-04-28		Copyright: Trenz Electronic GmbH / TT		Page6 of 25	
Filename: ZYNQ.SchDoc					



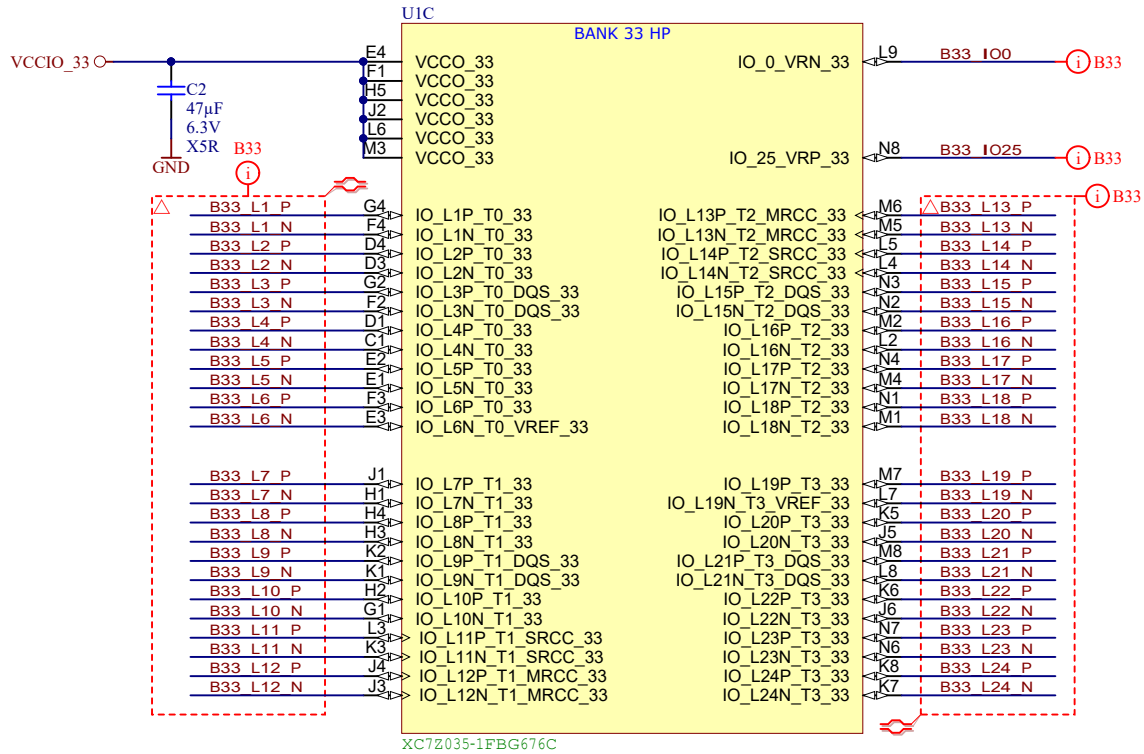
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Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page 7 of 25
Filename: ZYNQ_MISC.SchDoc		



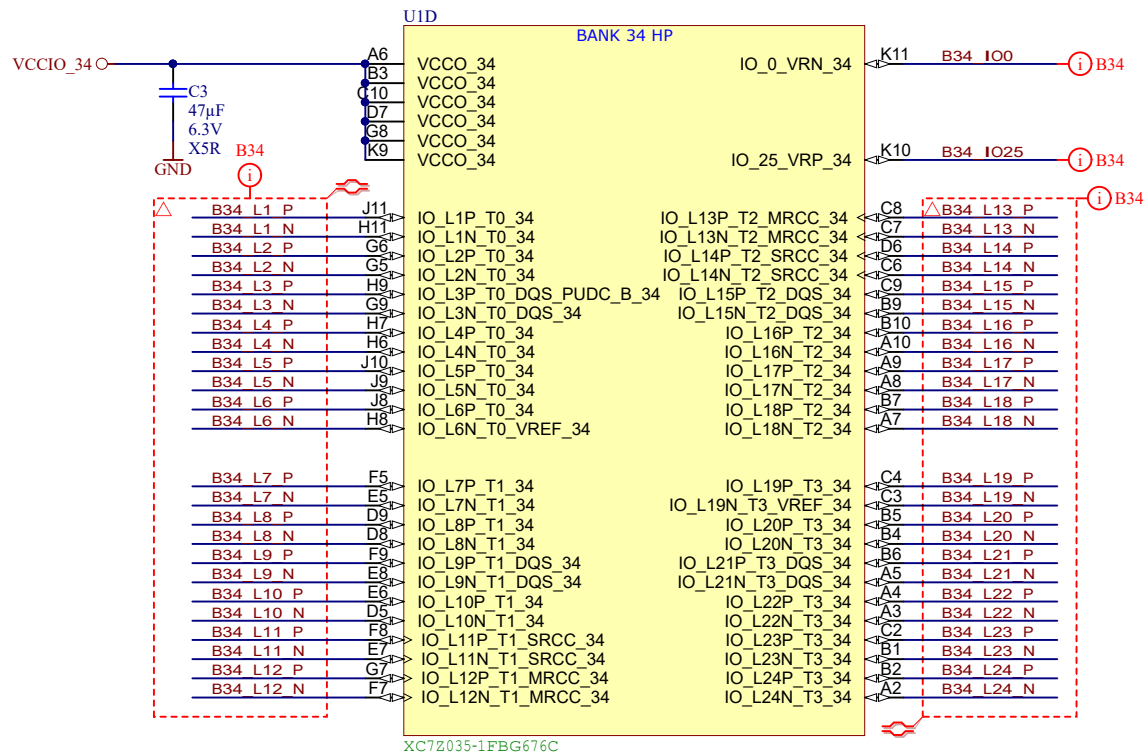
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	Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page 8 of 25
	Filename: B12.SchDoc		



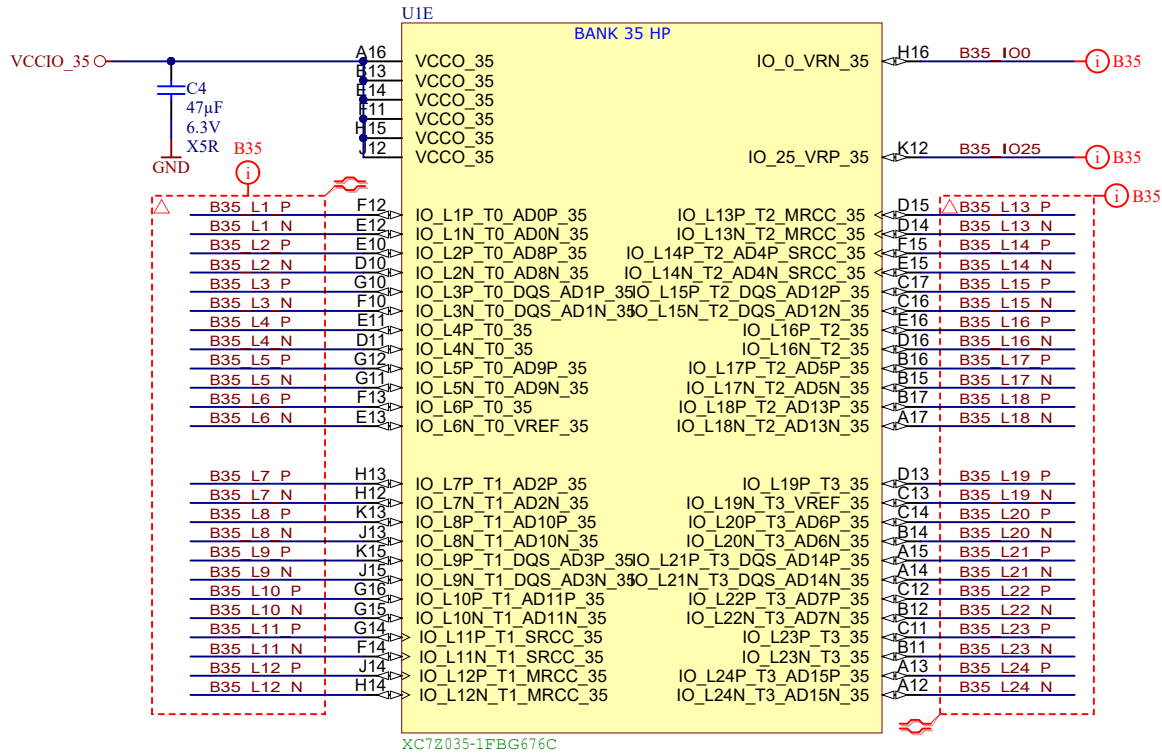
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Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page9 of 25
Filename: B13.SchDoc		



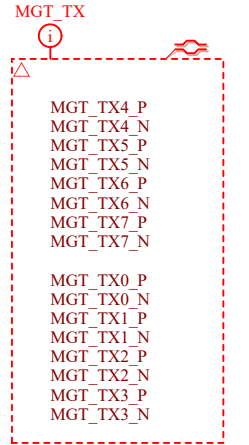
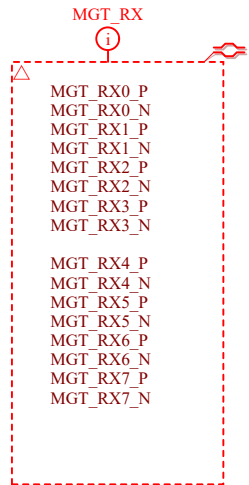
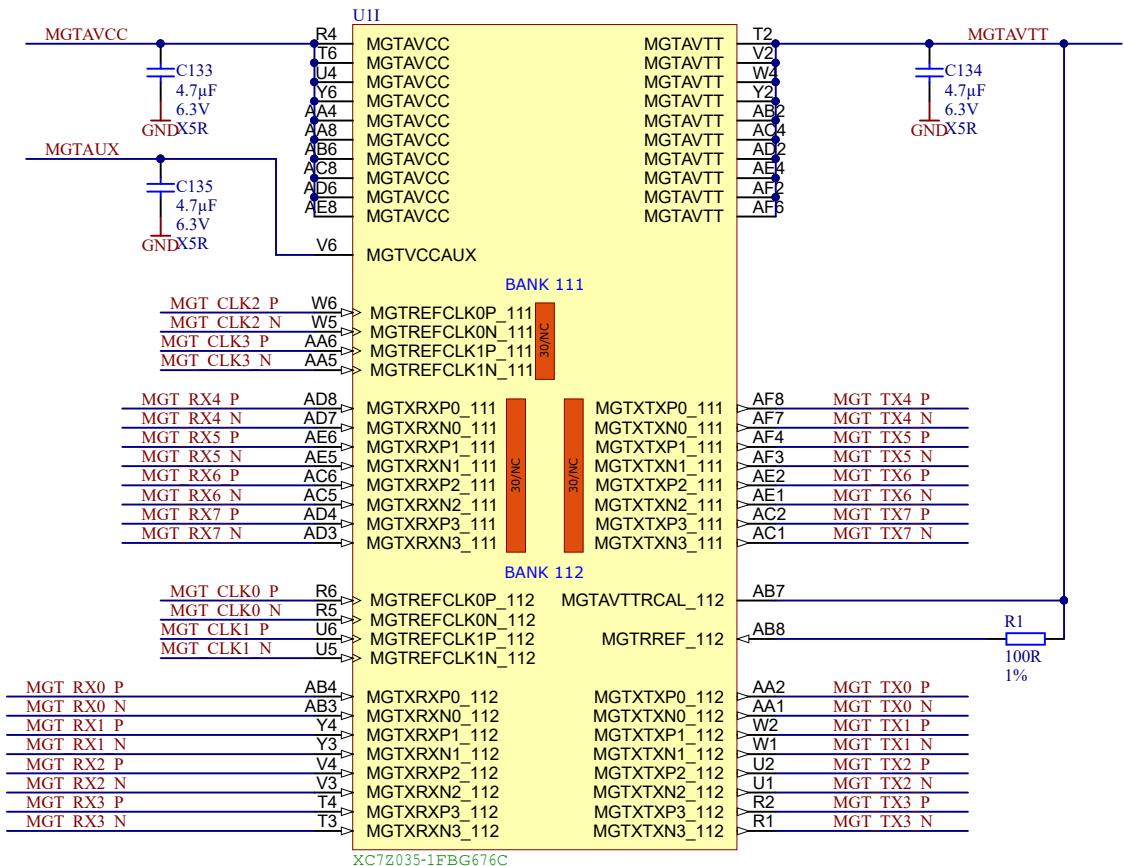
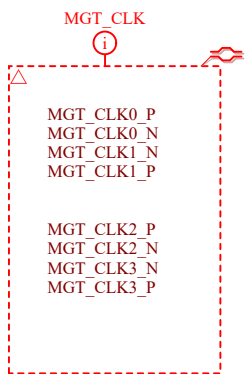

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Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page 10 of 25
Filename: B33.SchDoc		



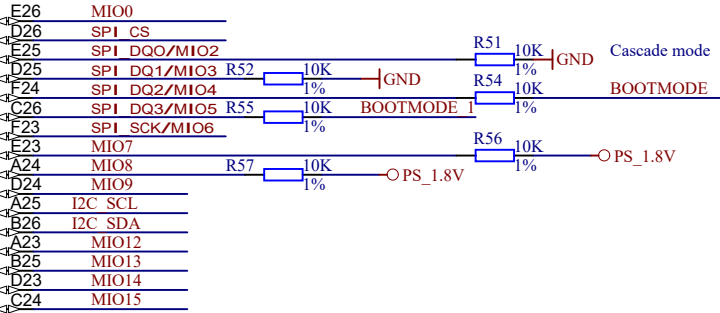
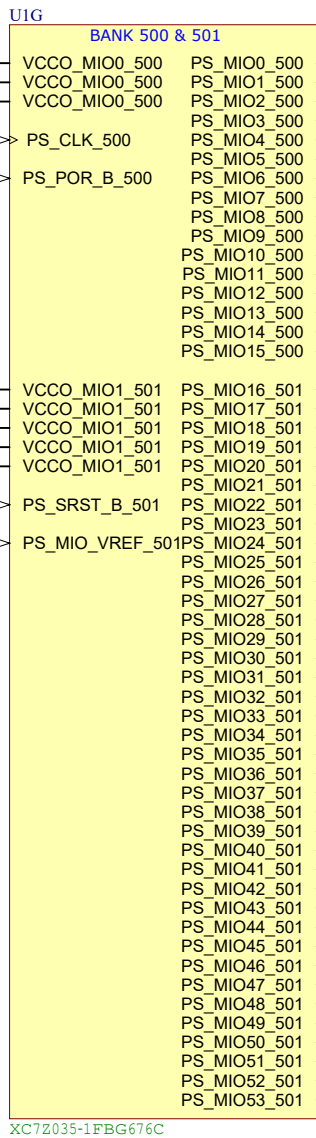
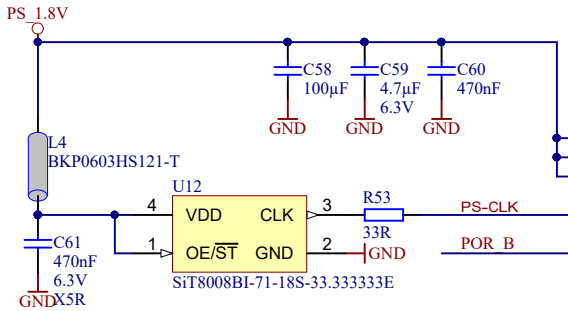
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Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page 11 of 25
Filename: B34.SchDoc		



	Title: TE0745 - Zynq_B35	
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	Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT
	Rev. 02	Page 12 of 25
Filename: B35.SchDoc		

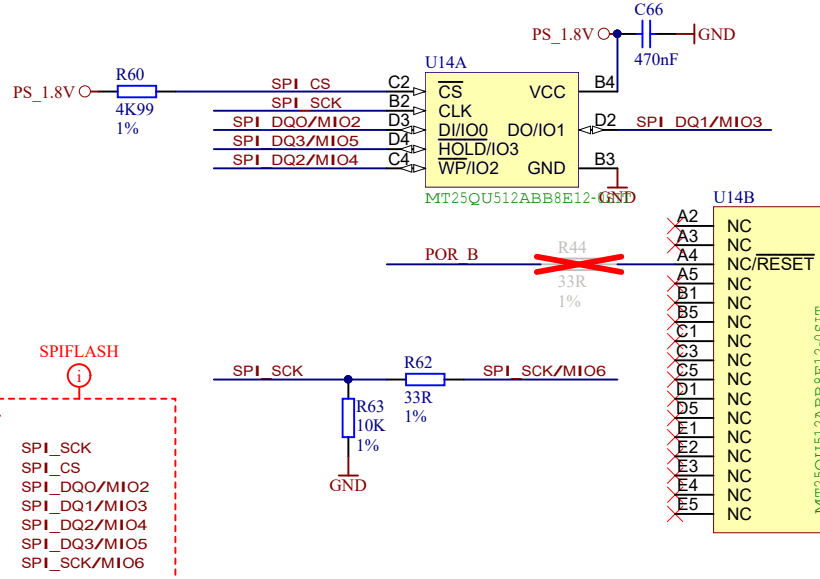
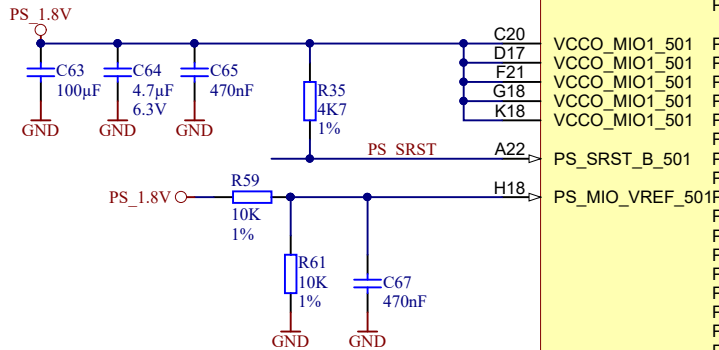



Title: TE0745 - Zynq_MGT		
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Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page 13 of 25
Filename: FPGA_MGT.SchDoc		

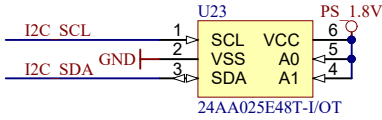


MIO Bank Voltage	MIO7 Bank0	MIO8 Bank1
2.5V, 3.3V	0	0
1.8V	1	1

BOOT MODE	MIO5 MIO4 MIO3
JTAG Boot Mode	0 0 0
NOR Boot	0 0 1
NAND	0 1 0
Quad-SPI	1 1 0
SD Card	1 1 0

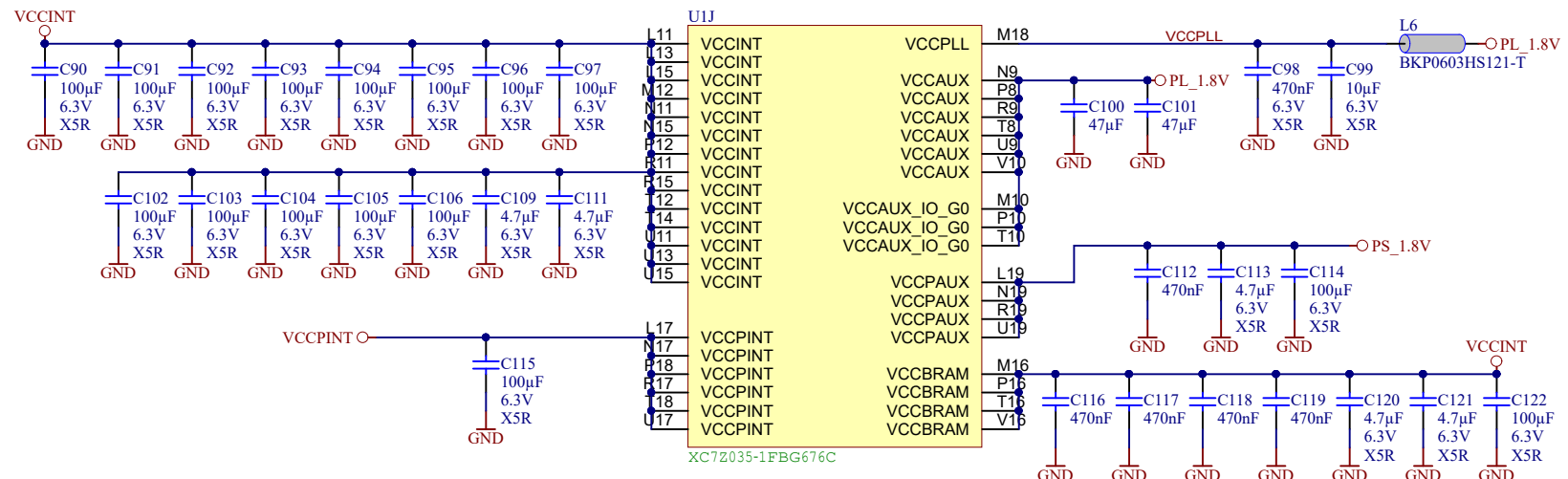
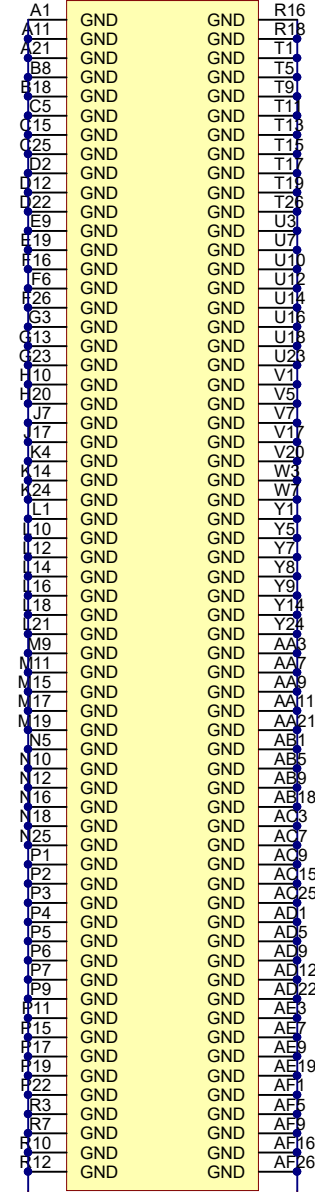


EEPROM for MAC
Slave ADDR:
1010011



Title: TE0745 - Zynq_MIO_Banks		
A4	Number: 14 81C11-A	Rev. 02
Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page 14 of 25
Filename: MIO_B500.SchDoc		

UIK



Title: TE0745 - Zynq_Power		
A4	Number: 16 81C11-A	Rev. 02
Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page 16 of 25
Filename: ZYNC_POWER.SchDoc		

A

A

B

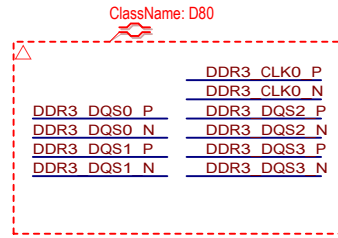
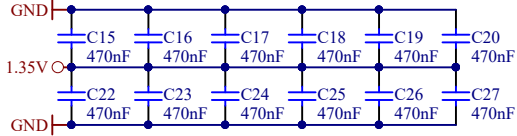
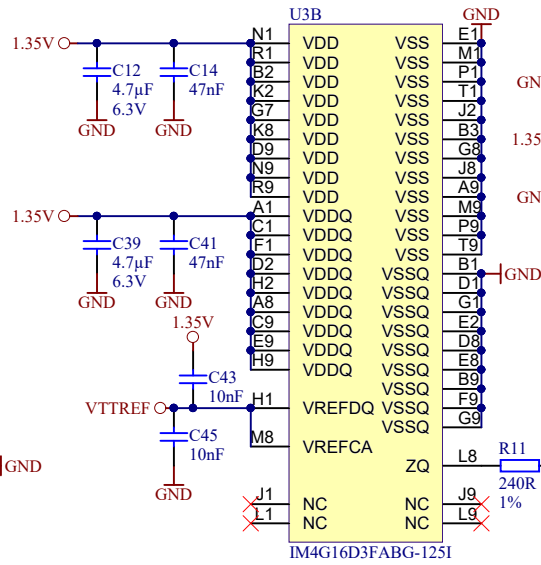
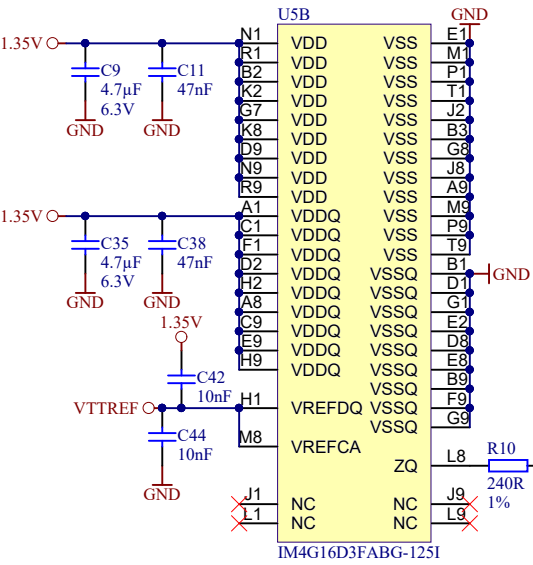
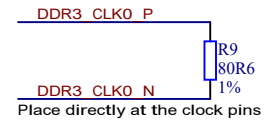
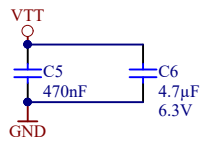
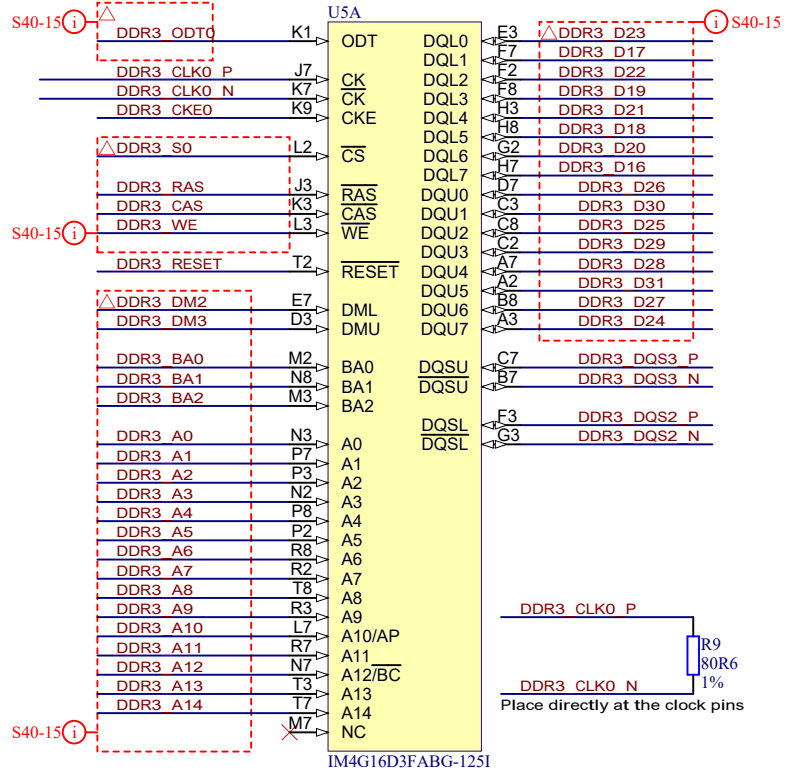
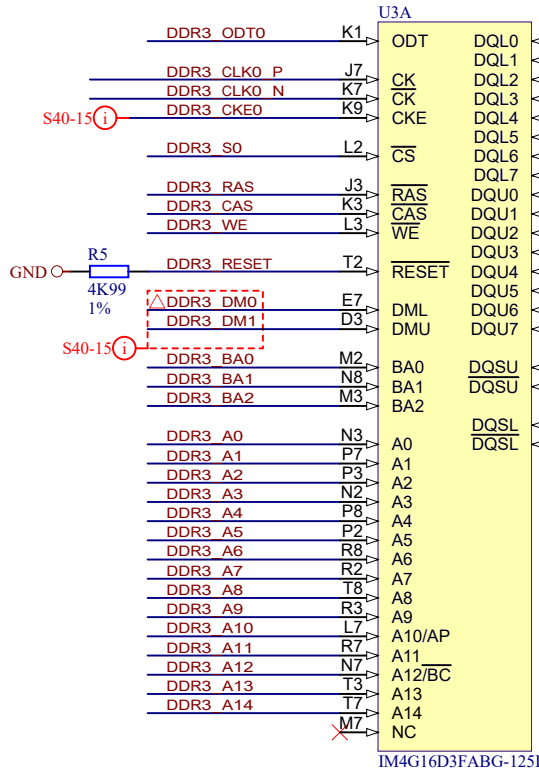
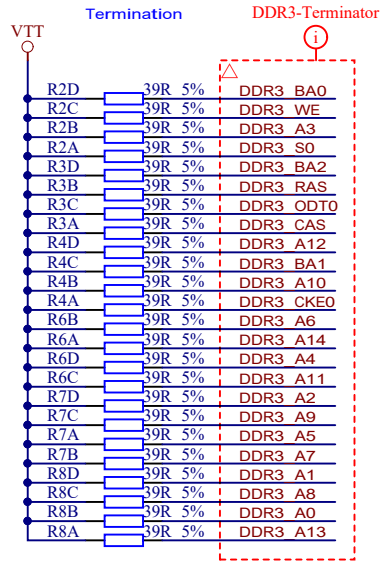
B

C

C

D

D



Title: TE0745 - DDR3 RAM		
A4	Number: 17 81C11-A	Rev. 02
Date: 2016-04-28	Copyright: Trenz Electronic GmbH	Page 17 of 25
Filename: DDR3-RAM.SchDoc		

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3

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A

A

B

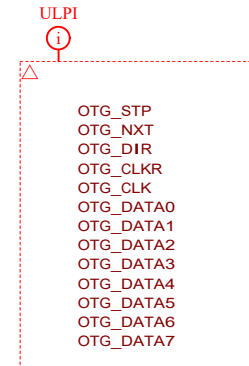
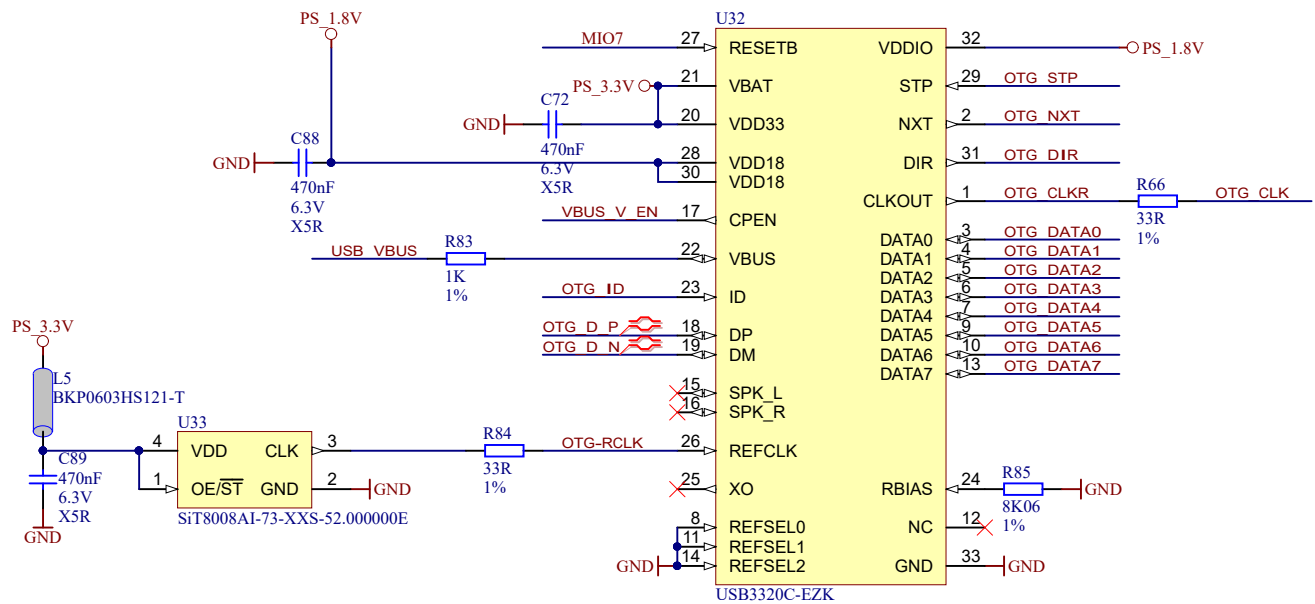
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C

C

D

D



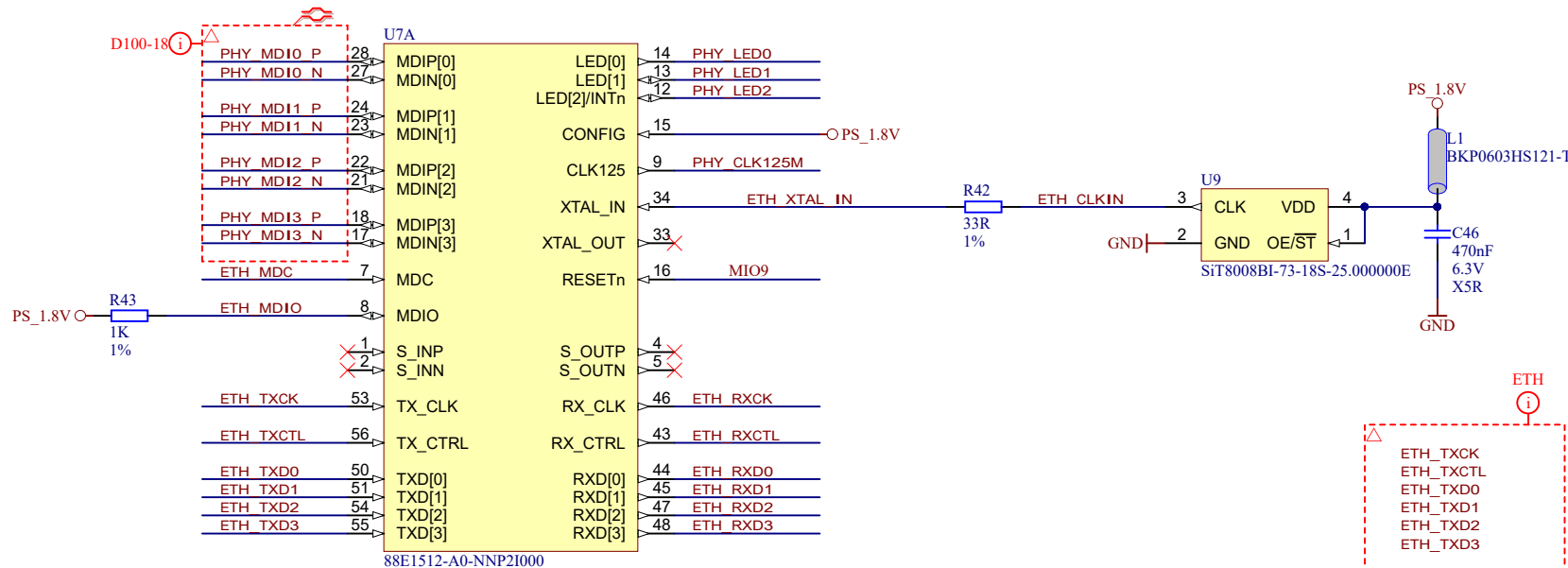
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A4	Number: 18 81C11-A	Rev. 02
Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page 18 of 25
Filename: USB-PHY.SchDoc		

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3

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A

A

B


B

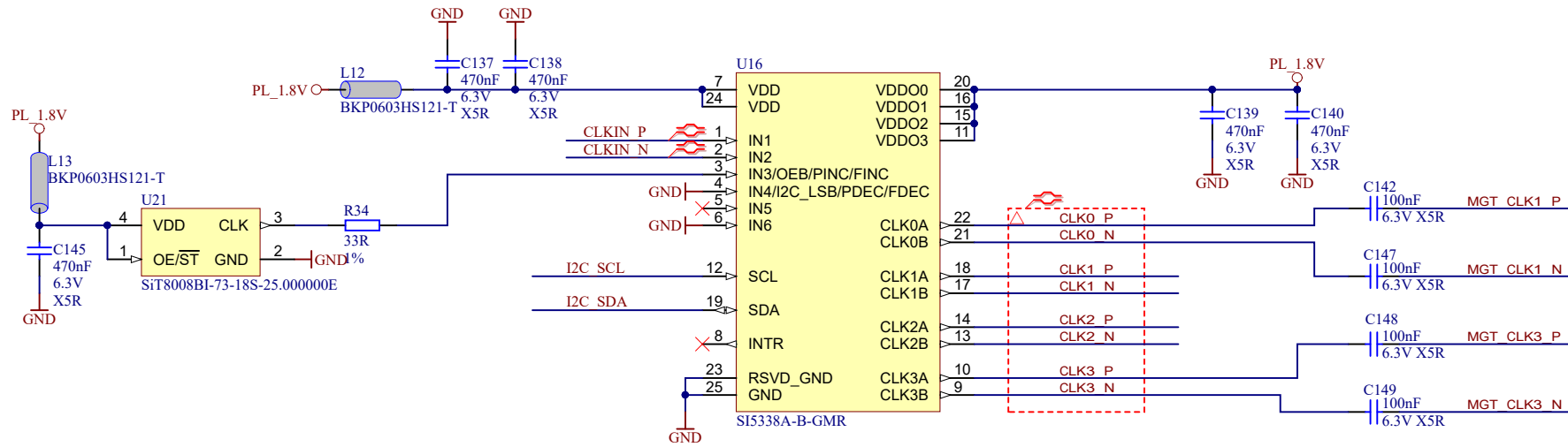
C

C


D

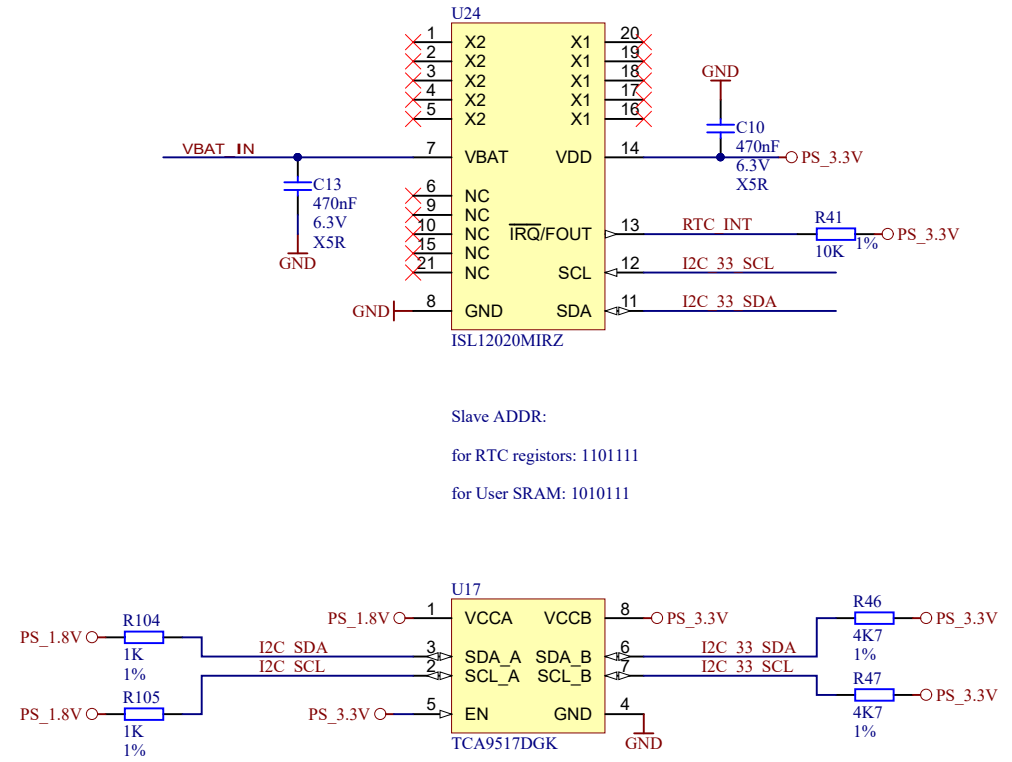
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			A4	Number: 19 81C11-A
Date: 2016-04-28		Copyright: Trenz Electronic GmbH / TT		Page 19 of 25
Filename: ETH-PHY.SchDoc				

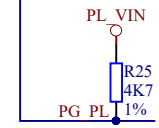
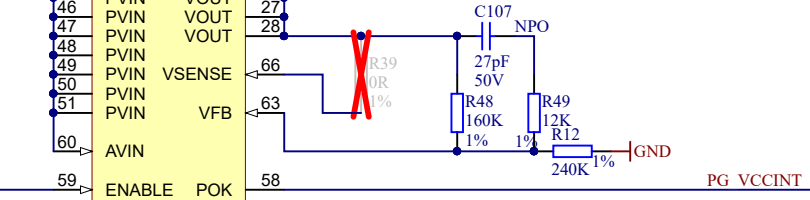
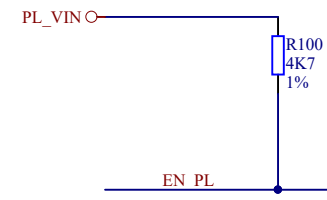
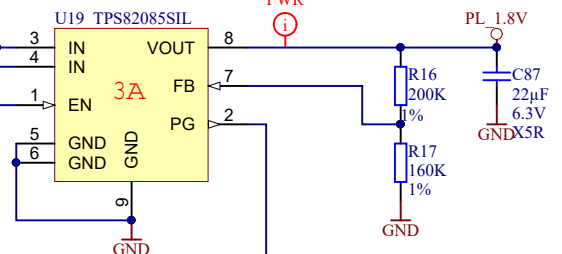
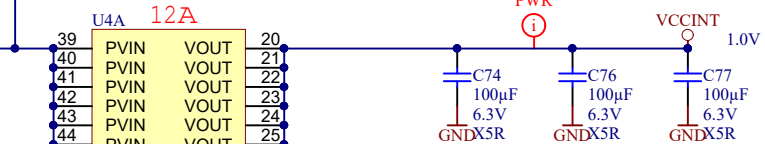
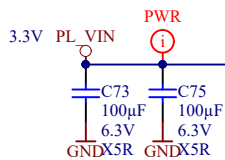


Slave ADDR:
1110000 OR 1110001

		Title: TE0745 - CLK	
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Date: 2016-04-28		Copyright: Trenz Electronic GmbH / TT	
Filename: CLK.SchDoc		Page 20 of 25	

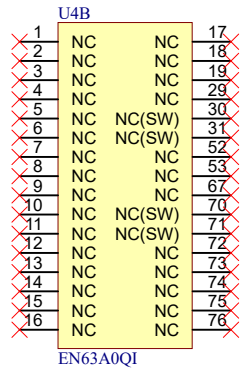
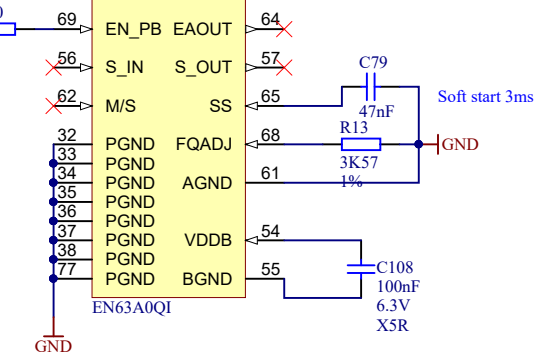


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Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page21 of 25
Filename: SENSOR-RTC.SchDoc		

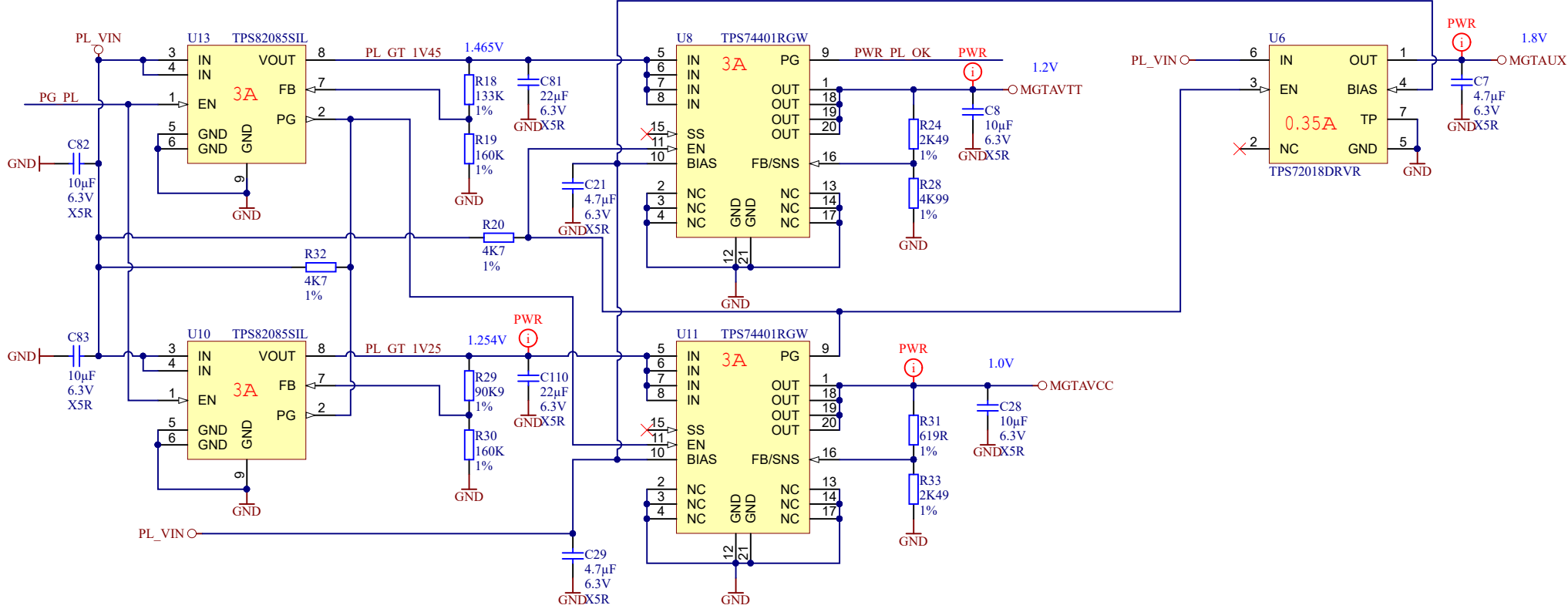


Pre-bias assembly option

R39	R40	MODE	EN63A0QI
OK	X		enable pre-bias start-up
X	OK		disable pre-bias start-up



Title: TE0745 - Power		
A4	Number: 22 81C11-A	Rev. 02
Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page 22 of 25
Filename: POWER.SchDoc		



Title: TE0745 - Power3		
A4	Number: 24 81C11-A	Rev. 02
Date: 2016-04-28	Copyright: Trenz Electronic GmbH / TT	Page24 of 25
Filename: POWER_3.SchDoc		

