



TE0745 Test Board

Revision v.15

Exported on 2024-01-25

Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0745+Test+Board>

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4 Overview

Zynq Design PS with Linux and simple frequency counter to measure MGT Reference CLK with Vivado HW-Manager.

Refer to <http://trenz.org/te0745-info> for the current online version of this manual and other available documentation.

4.1 Key Features

- Vitis/Vivado 2021.2.1
- PetaLinux
- SD
- ETH (MAC from EEPROM)
- USB
- I2C
- RTC
- FMeter
- Modified FSBL for SI5338 programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2023-04-25	2021.2.1	TE0745-test_board-vivado_2021.2-build_20_20230425125003.zip TE0745-test_board_nopre-built-vivado_2021.2-build_20_20230425125003.zip	Manuela Strücker	<ul style="list-style-type: none"> • new assembly variants
2023-02-07	2021.2.1	TE0745-test_board-vivado_2021.2-build_20_20230207205537.zip TE0745-test_board_nopre-built-vivado_2021.2-	Manuela Strücker	<ul style="list-style-type: none"> • update 2021.2 • new assembly variants • added jtag2axi for test purposes

Date	Vivado	Project Built	Authors	Description
		build_20_20230207205537.zip		
2020-03-30	2019.2	TE0745-test_board-vivado_2019.2-build_8_20200330083452.zip TE0745-test_board_noprebuilt-vivado_2019.2-build_8_20200330083503.zip	John Hartfiel	<ul style="list-style-type: none"> • 2019.2 update • FSBL rework, SI5338 Project with Clock Builder pro • device tree update • Vitis support • new assembly variants
2018-09-2019	2018.2	TE0745-test_board_noprebuilt-vivado_2018.2-build_04_20190918103545.zip TE0745-test_board-vivado_2018.2-build_04_20190918103531.zip	John Hartfiel	<ul style="list-style-type: none"> • BUGFIX in TE0745-02-45-3EA board parts
2018-11-26	2018.2	TE0745-test_board-vivado_2018.2-build_03_20181126115131.zip TE0745-test_board_noprebuilt-vivado_2018.2-build_03_20181126115320.zip	John Hartfiel	<ul style="list-style-type: none"> • Rework Board Part Files • New assembly versions • Rework BD Design • add init.sh scripts
2017-10-23	2017.2	TE0745-test_board_noprebuilt-vivado_2017.2-	John Hartfiel	<ul style="list-style-type: none"> • initial release

Date	Vivado	Project Built	Authors	Description
		build_05_2017102 3171903.zip TE0745- test_board- vivado_2017.2- build_05_2017102 3171855.zip		

Table 1: Design Revision History

4.3 Release Notes and Known Issues

Issues	Description	Workaround	To be fixed version
QSPI programming	QSPI programming is not possible in other boot modes than JTAG.	<ul style="list-style-type: none"> • use JTAG boot mode for QSPI programming • When using the carrier board TEB0745, use the optional firmware to get into JTAG boot mode. 	---

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2021.2.1	needed, Vivado is included into Vitis installation
PetaLinux	2021.2	needed

Software	Version	Note
SI ClockBuilder Pro	---	optional

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).¹

Complete List is available on "<project folder>\board_files*_board_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0745-02-30-1I	30_1i_1gb	REV02 REV01	1GB	32MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-30-2IA	30_2i_1gb	REV02 REV01	1GB	32MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-35-1C	35_1c_1gb	REV02 REV01	1GB	32MB	NA	NA	
TE0745-02-45-2I	45_2i_1gb	REV02 REV01	1GB	32MB	NA	NA	
TE0745-02-45-2IA	45_2i_1gb	REV02 REV01	1GB	64MB	NA	NA	

¹ <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0745-02-45-1C*	45_1c_1gb	REV02 REV01	1GB	32MB	NA	NA	
TE0745-02-45-1CA	45_1c_1gb	REV02 REV01	1GB	64MB	NA	NA	
TE0745-02-45-3EA	45_3e_1gb	REV02 REV01	1GB	64MB	NA	NA	
TE0745-02-93E11-A	45_3e_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-92I11-F	45_2i_ff_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-92I11-A	45_2i_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-91C11-A	45_1c_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-81C11-A	35_1c_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-72I11-A	30_2i_1gb	REV02	1GB	64MB	NA	NA	smaller FPGA has less MGTs

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0745-02-71I11-A	30_1i_1gb	REV02	1GB	64MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-71I11-AK	30_1i_1gb	REV02	1GB	64MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-71I31-A	30_1i_1gb	REV02	1GB	64MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-71I31-AK	30_1i_1gb	REV02	1GB	64MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-72I31-A	30_2i_1gb	REV02	1GB	64MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-81C31-A	35_1c_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-91C31-A	45_1c_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-92I31-A	45_2i_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-92I31-AK	45_2i_1gb	REV02	1GB	64MB	NA	NA	

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0745-02-92I31-B	45_2i_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-93E11-KA	45_3e_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-93E31-A	45_3e_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-93E31-AK	45_3e_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-S003	45_2i_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-S005	30_1i_1gb	REV02	1GB	64MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-S006	30_1i_1gb	REV02	1GB	64MB	NA	NA	smaller FPGA has less MGTs without RTC
TE0745-02-S007C1	45_2i_1gb	REV02	1GB	64MB	NA	NA	without PLL
TE0745-02-S007C2	45_2i_1gb	REV02	1GB	64MB	NA	NA	without PLL

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0745-02-S007C3	45_2i_1gb	REV02	1GB	64MB	NA	NA	without PLL
TE0745-02-S012	45_2i_1gb	REV02	1GB	64MB	NA	NA	without PLL
TE0745-02-S008	30_1i_1gb	REV02	1GB	64MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-S009	30_1i_1gb	REV02	1GB	64MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-82I31-A	35_2i_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-72I31-AZ	30_2i_1gb	REV02	1GB	64MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-S013	45_2i_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-93E31-AZ	45_3e_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-S016	45_3e_1gb	REV02	1GB	64MB	NA	NA	

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0745-02-S017	30_1i_1gb	REV02	1GB	64MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-71I31-AZ	30_1i_1gb	REV02	1GB	64MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-S018	30_1i_1gb	REV02	1GB	64MB	NA	NA	less MGT
TE0745-02-S019	45_2i_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-S020	45_2i_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-S021	45_2i_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-S022	45_2i_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-81C31-AZ	35_1c_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-91C31-AZ	45_1c_1gb	REV02	1GB	64MB	NA	NA	
TE0745-02-92I31-AZ	45_2i_1gb	REV02	1GB	64MB	NA	NA	

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0745-02-S014C1	45_2i_1gb	REV02	1GB	64MB	NA	without PLL	
TE0745-02-S014C2	45_2i_1gb	REV02	1GB	64MB	NA	without PLL	
TE0745-02-S014C3	45_2i_1gb	REV02	1GB	64MB	NA	without PLL	

Table 4: Hardware Modules

*used as reference

Design supports following carriers:

Carrier Model	Notes
TEB0745*	

Table 5: Hardware Carrier

*used as reference

Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct type
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

Table 6: Additional Hardware

*used as reference

4.5 Content

For general structure and of the reference design, see [Project Delivery - AMD devices](#)²

4.5.1 Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<project folder>\os\petalinux	PetaLinux template with current configuration

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
SI5338	<project folder>\misc\PLL\SI5338_B	SI5338 Project with current PLL Configuration
init.sh	<project folder>\misc\sd\	Additional Initialization Script for Linux

Table 8: Additional design sources

4.5.3 Prebuilt

² <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+AMD+devices>

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Boot Script-File	*.scr	Distro Boot Script file
DebugProbes-File	*.ltx	Definition File for Vivado/ Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Device Tree	*.dts	Device tree (2 possible, one for u-boot and one for linux)
Hardware-Platform-Description-File	*.xsa	Exported Vivado hardware description file for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebuilt content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0745 "test Board Reference Design"](#)³

³ https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0745/Reference_Design/2021.2/test_board

5 Design Flow

! Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- [AMD Development Tools](#)⁴
- [Vivado Projects - TE Reference Design](#)⁵
- [Project Delivery](#).⁶

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)⁷

! **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:

_create_win_setup.cmd/_create_linux_setup.sh

```
-----Set design
paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-----

-----TE Reference
Design-----
-----

-- (0)  Module selection guide, project creation...prebuilt
export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
```

⁴ <https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDDevelopmentTools-XilinxSoftware-BasicUserGuides>


⁵ <https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design>

⁶ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+AMD+devices>

⁷ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+AMD+devices#ProjectDeliveryAMDdevices-Currentlylimitationsoffunctionality>

```
----
Select (ex.: '0' for module selection guide):
```


2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.
 - optional for manual changes: Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_gui mode.cmd"

 Note: Select correct one, see also [Vivado Board Part Flow](#)⁸


4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

run on Vivado TCL (Script generates design and export files into "\prebuilt\hardware\")

```
\prebuilt\hardware\")">
TE::hw_build_design -export_prebuilt
```

 Using Vivado GUI is the same, except file export to prebuilt folder.

5. Create and configure your PetaLinux project with exported .xsa-file, see [PetaLinux KICKstart](#)⁹
 - use TE Template from "<project folder>\os\petalinux"
 - use exported .xsa file from "<project folder>\prebuilt\hardware\<short name>" .
Note: HW Export from Vivado GUI creates another path as default workspace.
 - The build images are located in the "<plnx-proj-root>/images/linux" directory
6. Configure the **boot.scr** file as needed, see [Distro Boot with Boot.scr](#)¹⁰
7. Copy PetaLinux build image files to prebuilt folder
 - copy **u-boot.elf**, **system.dtb**, **image.ub** and **boot.scr** from "<plnx-proj-root>/images/linux" to prebuilt folder

 "<project folder>\prebuilt\os\petalinux\<ddr size>" or "<project folder>\prebuilt\os\petalinux\<short name>"

8. Generate Programming Files with Vitis


run on Vivado TCL (Script generates applications and bootable files, which are defined in "test_board\sw_lib\apps_list.csv")

```
TE::sw_run_vitis -all
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or
start with TE Scripts on Vivado TCL)
```

⁸ <https://wiki.trenz-electronic.de/display/PD/Vivado+Board+Part+Flow>

⁹ <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>


¹⁰ <https://wiki.trenz-electronic.de/display/PD/Distro+Boot+with+Boot.scr>

 TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis](#)¹¹

¹¹ <https://wiki.trenz-electronic.de/display/PD/Vitis>

6 Launch


6.1 Programming

-  Check Module and Carrier TRMs for proper HW configuration before you try any design.
Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: [Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging](#)¹²

6.1.1 Get prebuilt boot binaries

1. Run `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
 - a. Select assembly version
 - b. Validate selection
 - c. Select create and open delivery binary folder

 Note: Folder "<project folder>_binaries_<Article Name>" with subfolder "boot_<app name>" for different applications will be generated

6.1.2 QSPI-Boot mode

Option for **Boot.bin** on QSPI Flash and **image.ub** and **boot.scr** on **SD** or **USB**.

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"

run on Vivado TCL (Script programs **BOOT.bin** on QSPI flash)

```
TE::pr_program_flash -swapp u-boot  
TE::pr_program_flash -swapp hello_te0745 (optional)
```

3. Copy **image.ub** and **boot.scr** on **SD** or **USB**
 - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder, see: [Get prebuilt boot binaries](#) (see page 22)
 - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
4. Set Boot Mode to **QSPI-Boot** and insert **SD** or **USB**.
 - Depends on Carrier, see carrier TRM.

¹² <https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDDevelopmentTools-XilinxSoftwareProgrammingandDebugging>

6.1.3 SD-Boot mode


1. Copy **image.ub**, **boot.scr** and **Boot.bin** on **SD**
 - use files from "<project folder>_binaries_<Article Name>\boot_linux" from generated binary folder, see: [Get prebuilt boot binaries \(see page 22\)](#)
 - or use prebuilt file location, see "<project folder>\prebuilt\file_location.txt"
2. Set Boot Mode to SD-Boot.
 - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.


6.1.4 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section [Programming \(see page 22\)](#)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)


 Note: See TRM of the Carrier, which is used.

 Starting with Petalinux version 2020.1, the industry standard "Distro-Boot" boot flow for U-Boot was introduced, which significantly expands the possibilities of the boot process and has the primary goal of making booting much more standardised and predictable.
The boot options described above describe the common boot processes for this hardware; other boot options are possible.
For more information see [Distro Boot with Boot.scr](#)¹³

4. Power On PCB
boot process
 1. Zynq Boot ROM loads FSBL from SD/QSPI into OCM,
 2. FSBL init PS, programs PL using the bitstream and loads U-boot from SD into DDR,
 3. U-boot loads Linux (**image.ub**) from SD/QSPI/... into DDR

6.2.1 Linux


1. Open Serial Console (e.g. putty)
 - Speed: 115200
 - select COM Port

 Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)

2. Linux Console:

¹³ <https://wiki.trenz-electronic.de/display/PD/Distro+Boot+with+Boot.scr>

```
# password default disabled with 2021.2 petalinux release
petalinux login: root
Password: root
```

 Note: Wait until Linux boot finished

3. You can use Linux shell now.

```
i2cdetect -y -r 0    (check I2C 0 Bus)
dmesg | grep rtc     (RTC check)
udhcpc              (ETH0 check)
lsusb               (USB2.0 check)
```

4. Option Features

- Webserver to get access to Zynq
 - insert IP on web browser to start web interface
- init.sh scripts
 - add init.sh script on SD, content will be load automatically on startup (template included in "<project folder>\misc\SD"
 - Script will enable SFP interface after linux booting, if file is copied on SD

6.2.2 Vivado HW Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder)

- Monitoring:
 - SI5338 CLKs:
 - Set radix from VIO signals to unsigned integer.
- Note:** Frequency Counter is inaccurate and displayed unit is Hz, SI5338 CLK (0 and 3) are configured to 125MHz by default.

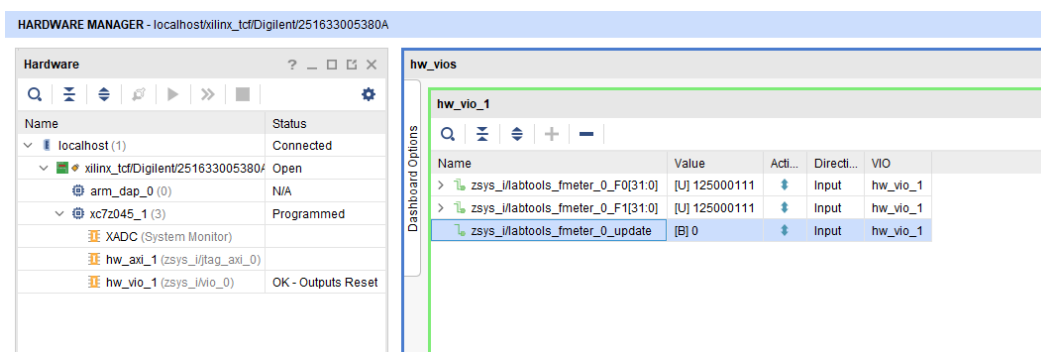


Figure 1: Vivado Hardware Manager

7 System Design - Vivado

7.1 Block Design

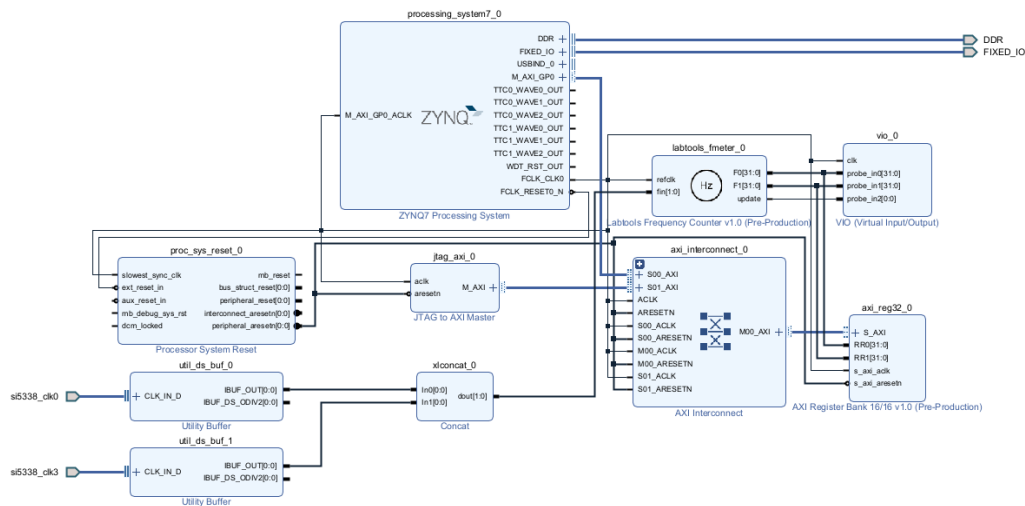


Figure 2: Block Design
*clk3 is not available on the smallest SOC (xc7z030)

7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
ETH0	MIO
USB0	MIO
SD0	MIO
UART0	MIO
I2C0	MIO

Type	Note
GPIO	MIO
ETH0 Reset	MIO
USB0 Reset	MIO
I2C0 Reset	MIO
TTC0..1	EMIO
SWDT0	EMIO

Table 10: PS Interfaces

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen_common

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 1.8 [current_design]
set_property CFGBVS GND [current_design]
```

7.2.2 Design specific constrain

_i_timing.xdc

```
set_false_path -from [get_clocks clk_fpga_0] -to [get_clocks
si5338_clk0_clk_p]
set_false_path -from [get_clocks clk_fpga_0] -to [get_clocks
si5338_clk3_clk_p]
set_false_path -from [get_clocks si5338_clk0_clk_p] -to [get_clocks
clk_fpga_0]
set_false_path -from [get_clocks si5338_clk3_clk_p] -to [get_clocks
clk_fpga_0]
```

8 Software Design - Vitis

For Vitis project creation, follow instructions from:

[Vitis](#)¹⁴

8.1 Application

Template location: "<project folder>\sw_lib\sw_apps\"

8.1.1 fsbl

TE modified 2021.2 FSBL

General:

- Modified Files: main.c, fsbl_hooks.h/.c (search for 'TE Mod' on source code)
- Add Files: te_fsbl_hooks.h/.c (for hooks and board)
- General Changes:
 - Display FSBL Banner and Device ID

Module Specific:

- Add Files: all TE Files start with te_*
 - Si5338 Configuration

8.1.2 hello_te0745

Hello TE0745 is a Xilinx Hello World example as endless loop instead of one console output.

8.1.3 u-boot

U-Boot.elf is generated with PetaLinux. Vitis is used to generate Boot.bin.

¹⁴ <https://wiki.trenz-electronic.de/display/PD/Vitis>

9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- [PetaLinux KICKstart](#)¹⁵

9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- MAC from eeprom together with uboot and device tree settings:
 - CONFIG_SUBSYSTEM_ETHERNET_PS7_ETHERNET_0_MAC=""
- add new flash partition for bootscr and sizing
 - CONFIG_SUBSYSTEM_FLASH_PS7_QSPI_0_BANKLESS_PART0_SIZE=0xA00000
 - CONFIG_SUBSYSTEM_FLASH_PS7_QSPI_0_BANKLESS_PART2_SIZE=0x1400000
 - CONFIG_SUBSYSTEM_FLASH_PS7_QSPI_0_BANKLESS_PART3_NAME="bootscr"
 - CONFIG_SUBSYSTEM_FLASH_PS7_QSPI_0_BANKLESS_PART3_SIZE=0x40000

9.2 U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- MAC from eeprom together with uboot and device tree settings:
 - CONFIG_ENV_OVERWRITE=y
- Boot Modes:
 - CONFIG_QSPI_BOOT=y
 - CONFIG_SD_BOOT=y
 - # CONFIG_ENV_IS_IN_NAND is not set
 - CONFIG_BOOT_SCRIPT_OFFSET=0x1E20000

Change platform-top.h:

```
#include <configs/zynq-common.h>
#no changes
```

9.3 Device Tree

project-spec\meta-user\recipes-bsp\device-tree\files\system-user.dtsi

```
/include/ "system-conf.dtsi"
```

```
/*----- QSPI -----*/
```

¹⁵ <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

```

&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash@0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

/*----- ETH PHY -----*/
&gem0 {
    phy-handle = <&phy0>;

    nvmem-cells = <&eth0_addr>;
    nvmem-cell-names = "mac-address";

    mdio {
        #address-cells = <1>;
        #size-cells = <0>;
        phy0: phy@1 {
            compatible = "marvell,88e1510";
            device_type = "ethernet-phy";
            reg = <1>;
        };
    };
};

/*----- USB -----*/
/{
    usb_phy0: usb_phy@0 {
        compatible = "ulpi-phy";
        #phy-cells = <0>;
        reg = <0xe0002000 0x1000>;
        view-port = <0x0170>;
        drv-vbus;
    };
};

&usb0 {
    dr_mode = "host";
    //dr_mode = "peripheral";
    usb-phy = <&usb_phy0>;
};

/*----- I2C -----*/
&i2c0 {

    rtc@6F {
        compatible = "isil,isl12022";
        reg = <0x6F>;
    };
};

```

```
//MAC EEPROM
eeprom: eeprom@53 {
    compatible = "microchip,24aa025", "atmel,24c02";
    reg = <0x53>;

    #address-cells = <1>;
    #size-cells = <1>;
    eth0_addr: eth-mac-addr@FA {
        reg = <0xFA 0x06>;
    };

};

i2cmux_SFP: i2cmux@72 {
    compatible = "nxp,pca9548";
    reg = <0x72>;

    SFP@0 {
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0>;
    };
    SFP@1 {
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <1>;
    };
    SFP@2 {
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <2>;
    };
    SFP@3 {
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <3>;
    };
    SFP@4 {
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <4>;
    };
    SFP@5 {
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <5>;
    };
    SFP@6 {
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <6>;
    };
    SFP@7 {
        #address-cells = <1>;
        #size-cells = <0>;
```

```
        reg = <7>;  
    };  
};  
  
};
```

9.4 Kernel

Start with **petalinux-config -c kernel**

Changes:

- for Real Time Clock ISL12020MIRZ
 - CONFIG_RTC_DRV_ISL12022=y

9.5 Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- For web server app:
 - CONFIG_busybox-httpd=y
- For additional test tools only:
 - CONFIG_i2c-tools=y
 - CONFIG_packagegroup-petalinux-utils=y (util-linux,cpufrequtils,bridge-utils,mtd-utils,usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)

9.6 Applications

See "<project folder>\os\petalinux\project-spec\meta-user\recipes-apps\"

9.6.1 startup

Script App to load init.sh from SD Card if available.

9.6.2 webfwu

Webserver application suitable for Zynq access. Need busybox-httpd

10 Additional Software

10.1 SI5338

File location "<project folder>\misc\PLL\Si5338_B\Si5338-*.slabtimeproj"


General documentation how you work with this project will be available on [Si5338](https://wiki.trenz-electronic.de/display/PD/Si5338)¹⁶

¹⁶ <https://wiki.trenz-electronic.de/display/PD/Si5338>

11 Appx. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
 2023-04-25	v.15 (see page 6)	Manuela Strücker ¹⁷	<ul style="list-style-type: none"> new assembly variants
2023-02-08	v.14	Manuela Strücker	<ul style="list-style-type: none"> Release 2021.2 new assembly variants added jtag2axi for test purposes
2020-03-30	v.13	John Hartfiel	<ul style="list-style-type: none"> Release 2019.2
2019-09-18	v.12	John Hartfiel	<ul style="list-style-type: none"> bugfix for TE0745-02-45-3EA
2018-12-19	v.11	John Hartfiel	<ul style="list-style-type: none"> documentation notes
2018-11-26	v.10	John Hartfiel	<ul style="list-style-type: none"> update 2018.2 documentation style update
2018-04-09	v.7	John Hartfiel	<ul style="list-style-type: none"> Typo correction
2018-02-09	v.6	John Hartfiel	<ul style="list-style-type: none"> Release 2017.2
2017-09-11	v.1	John Hartfiel	<ul style="list-style-type: none"> Initial release

¹⁷ <https://wiki.trenz-electronic.de/display/~m.struecker>

Date	Document Revision	Authors	Description
--	all	John Hartfiel ¹⁸ , Manuela Strücker ¹⁹	--

Table 11: Document change history.

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Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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¹⁸ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

¹⁹ <https://wiki.trenz-electronic.de/display/~m.struecker>

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²⁰ <http://guidance.echa.europa.eu/>

²¹ <https://echa.europa.eu/candidate-list-table>

²² <http://www.echa.europa.eu/>

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