

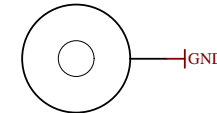
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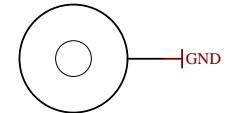
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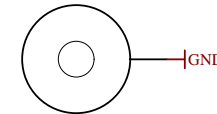
U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_DDR4-TERM DDR4-TERM.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_REV_CH Revision_Changes.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	
	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	



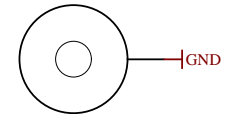
Mount.Hole 3.2mm für Unterlegscheibe



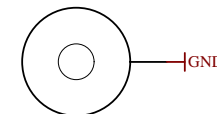
Mount.Hole 3.2mm für Unterlegscheibe



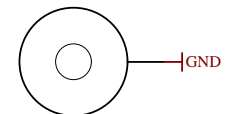
Mount.Hole 3.2mm für Unterlegscheibe



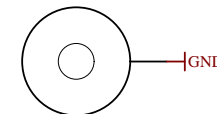
Mount.Hole 3.2mm für Unterlegscheibe



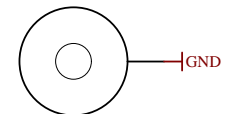
Mount.Hole 3.2mm für Unterlegscheibe



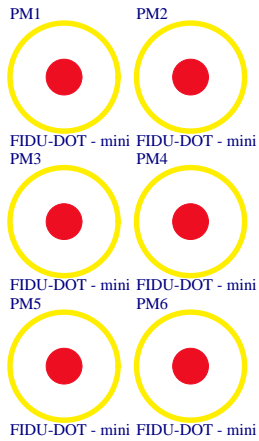
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe

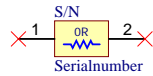


Mount.Hole 3.2mm für Unterlegscheibe



LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial
Serial
Serialnumber 6,3 x 6,3mm



Title: TE0803		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page1 of 26
Filename: TE0803.SchDoc		

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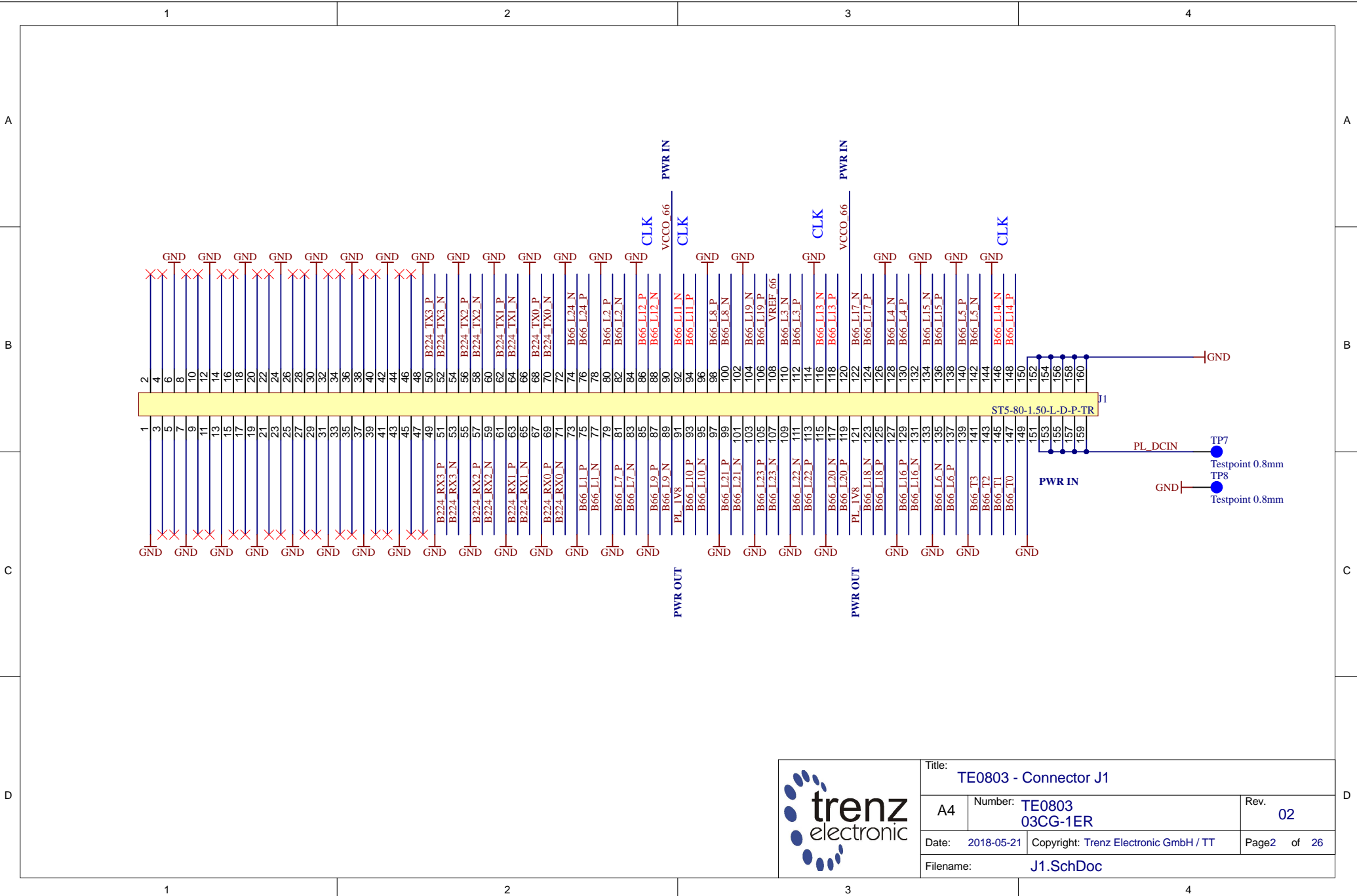

B

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Title: TE0803 - Connector J1		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page2 of 26
Filename: J1.SchDoc		

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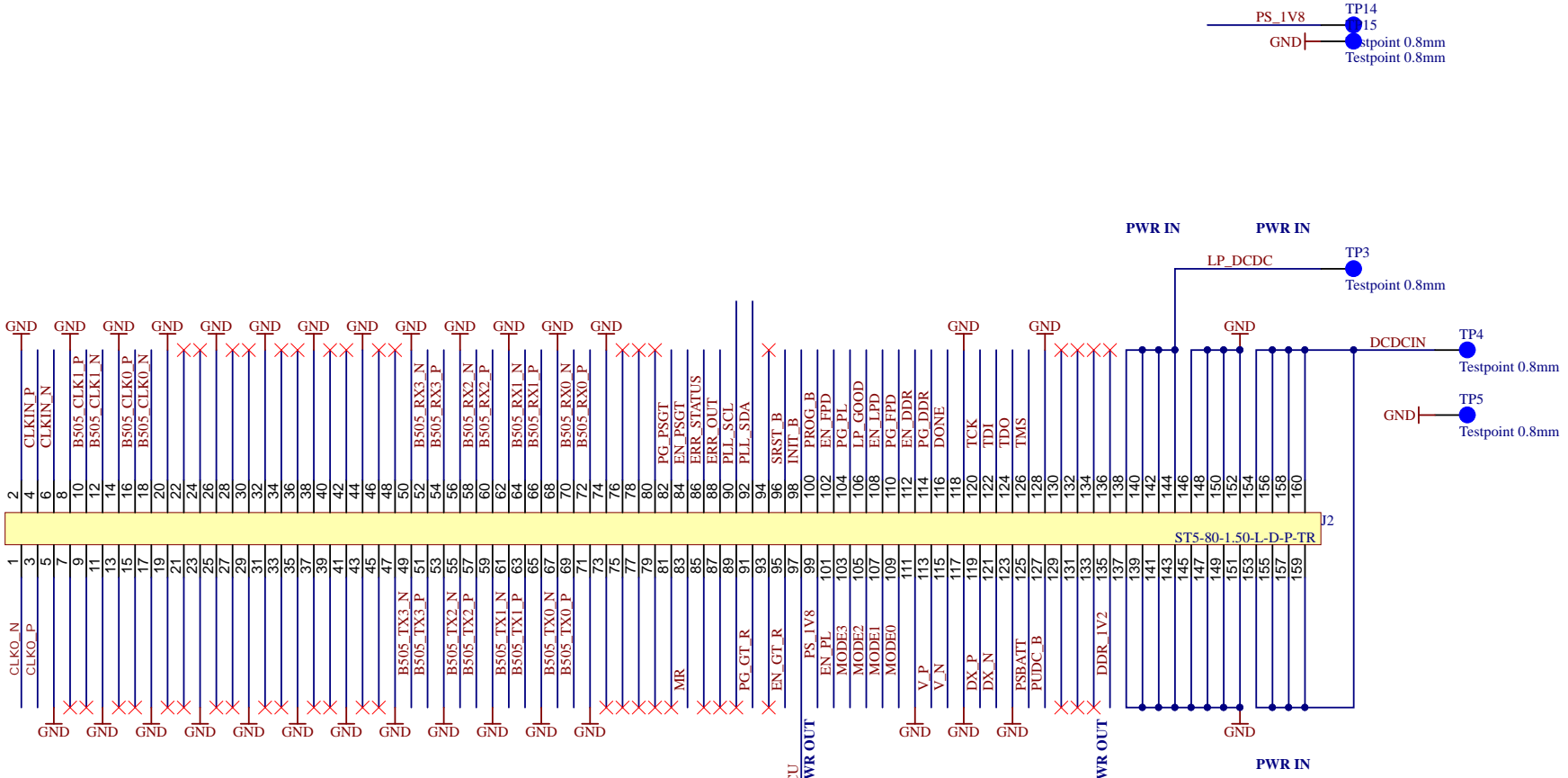
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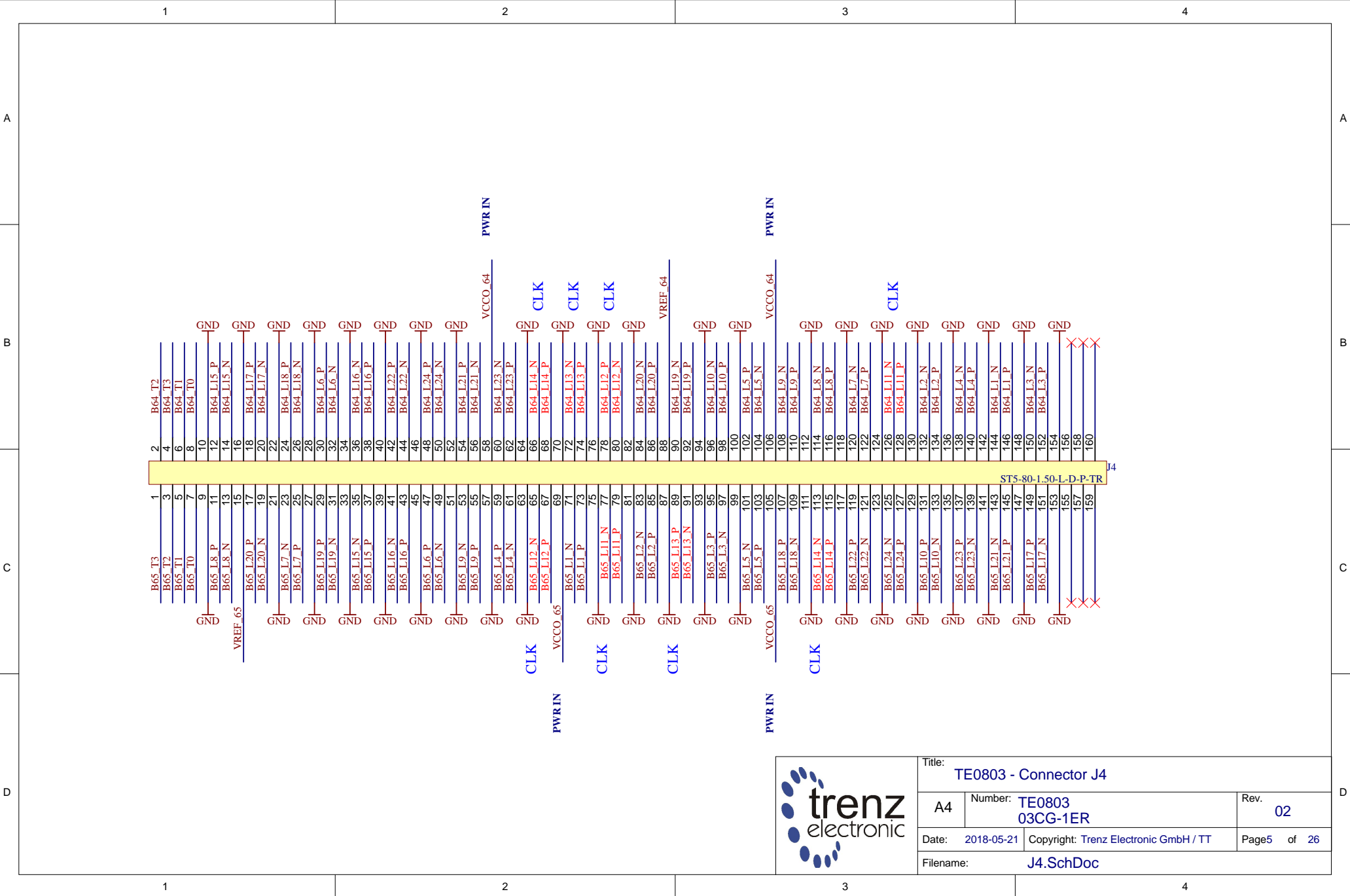
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A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page3 of 26
Filename: J2.SchDoc		

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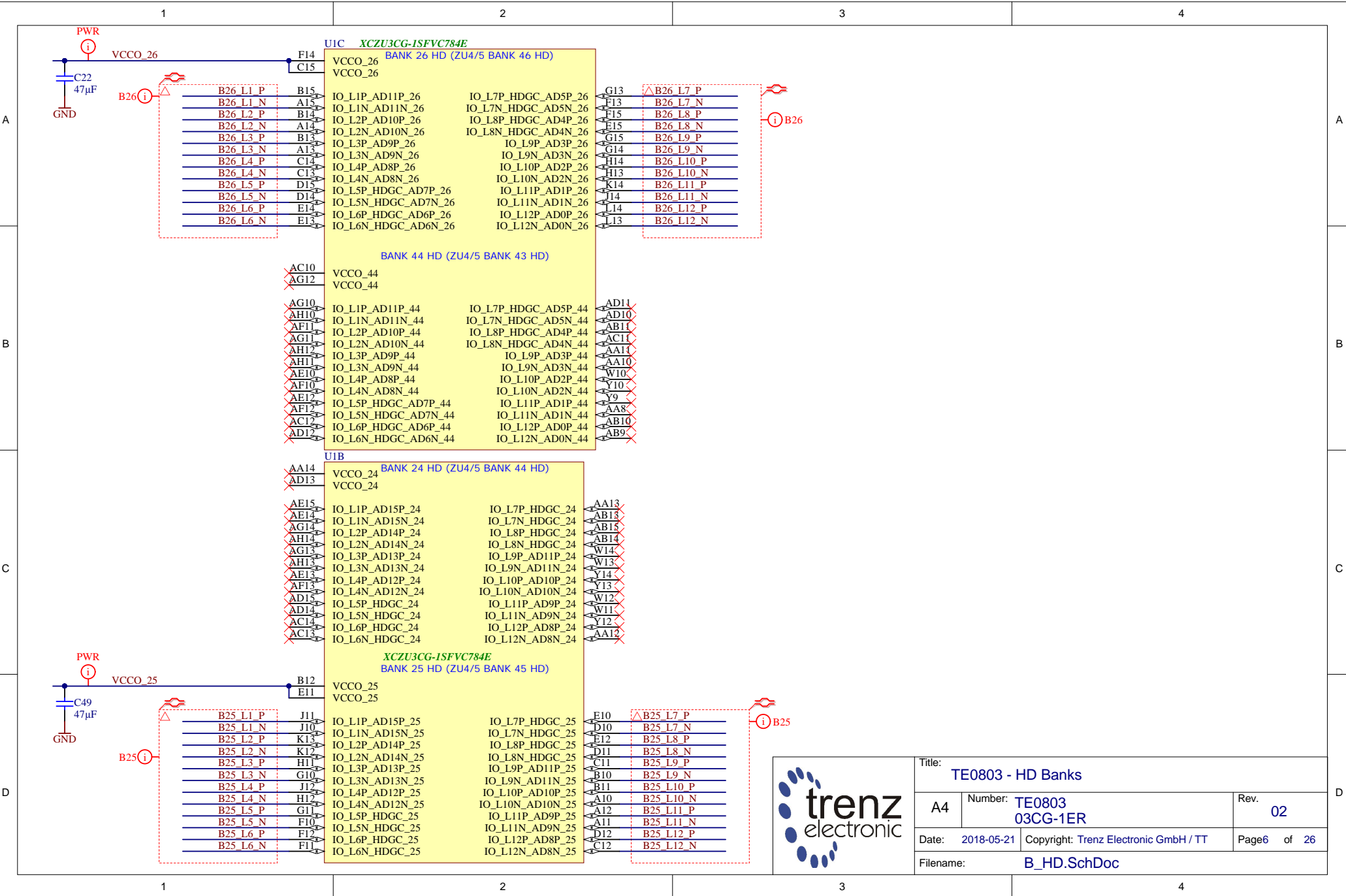
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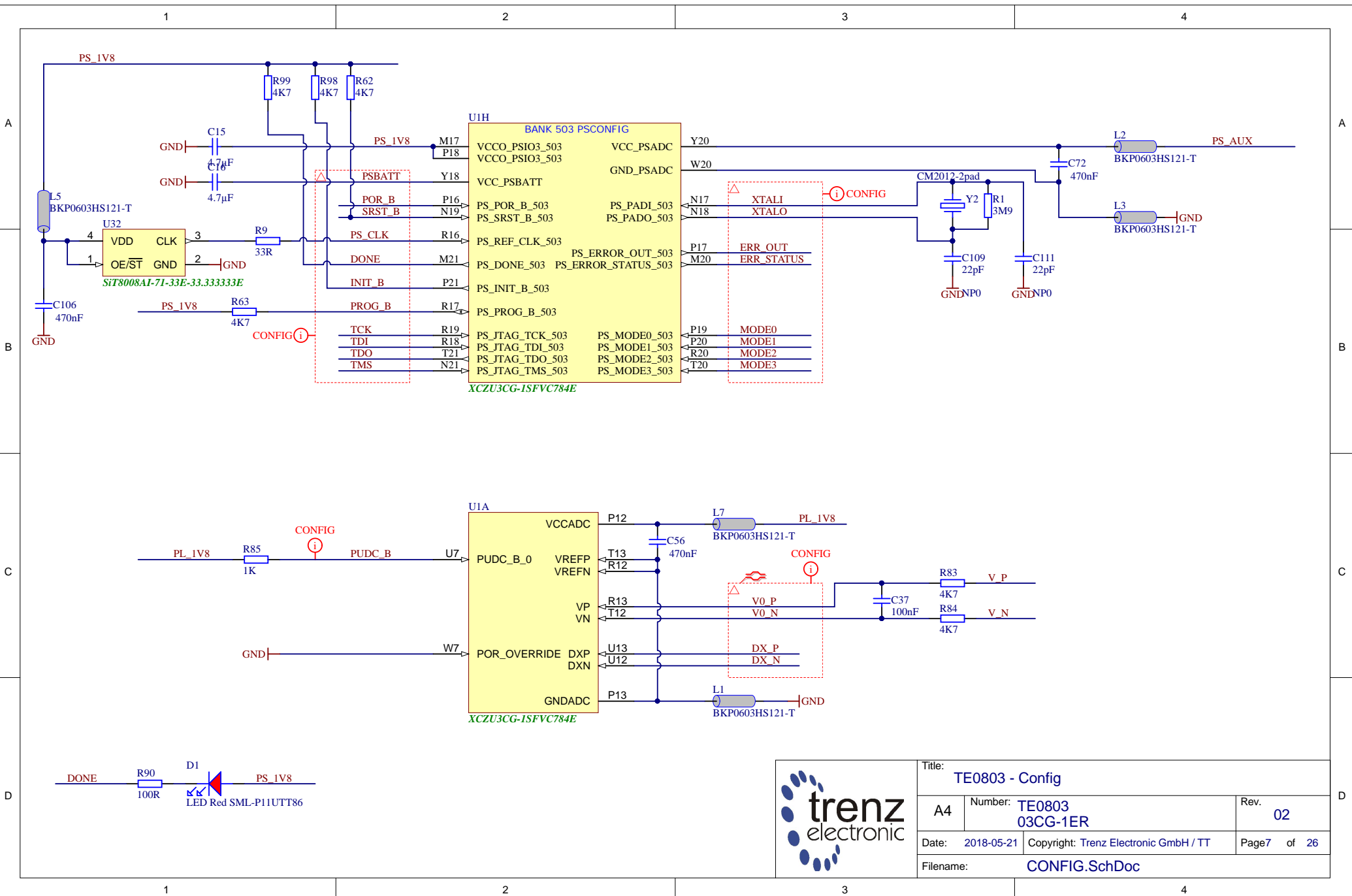
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Title: TE0803 - Connector J4		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page5 of 26
Filename: J4.SchDoc		



Title: TE0803 - HD Banks		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page6 of 26
Filename: B_HD.SchDoc		



Title: TE0803 - Config		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page 7 of 26
Filename: CONFIG.SchDoc		

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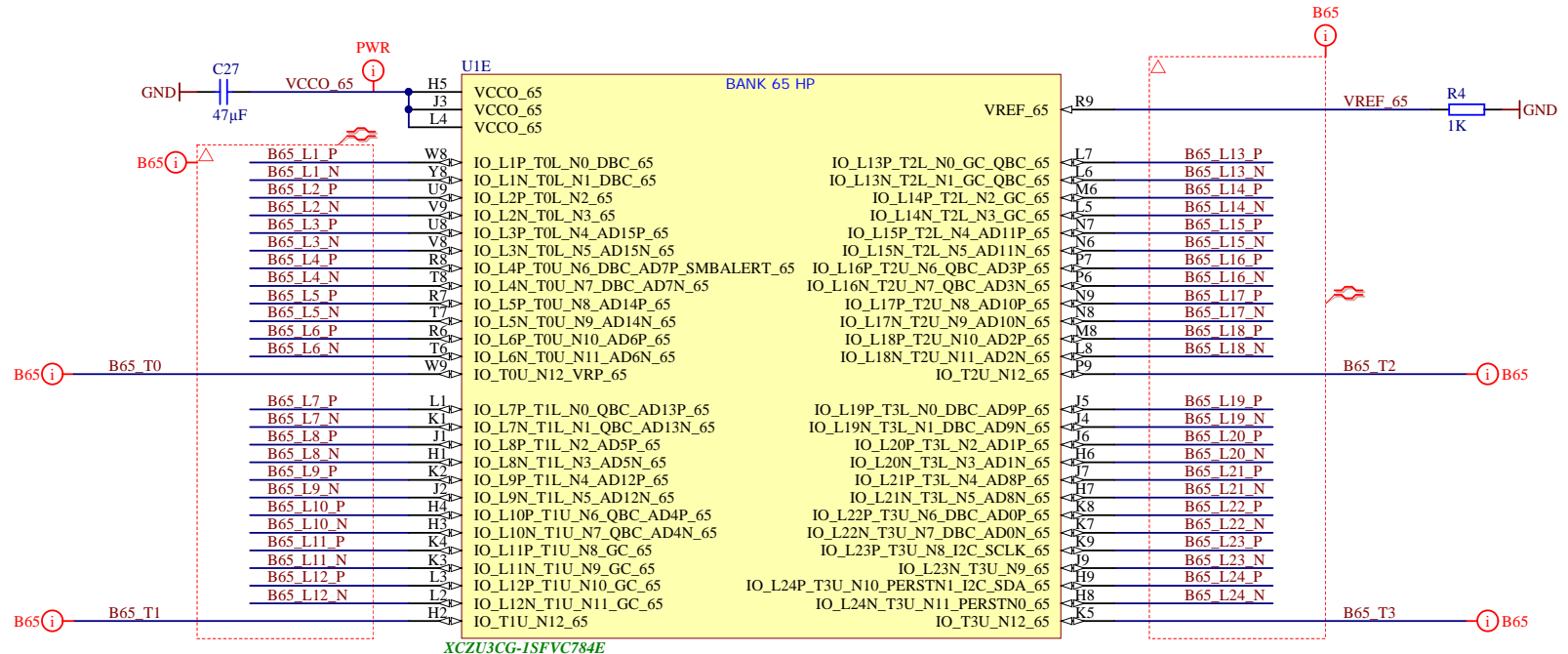
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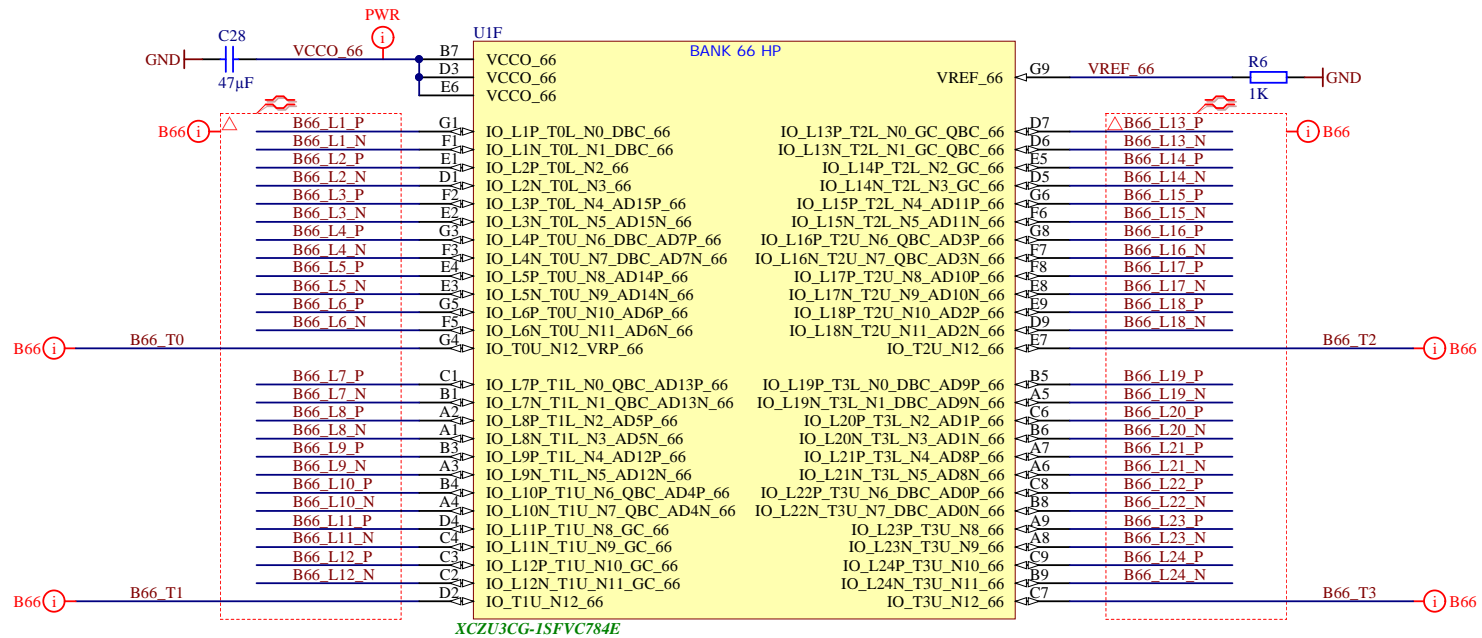
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	A4	Number: TE0803 03CG-1ER	Rev. 02
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page9 of 26
	Filename: B65.SchDoc		

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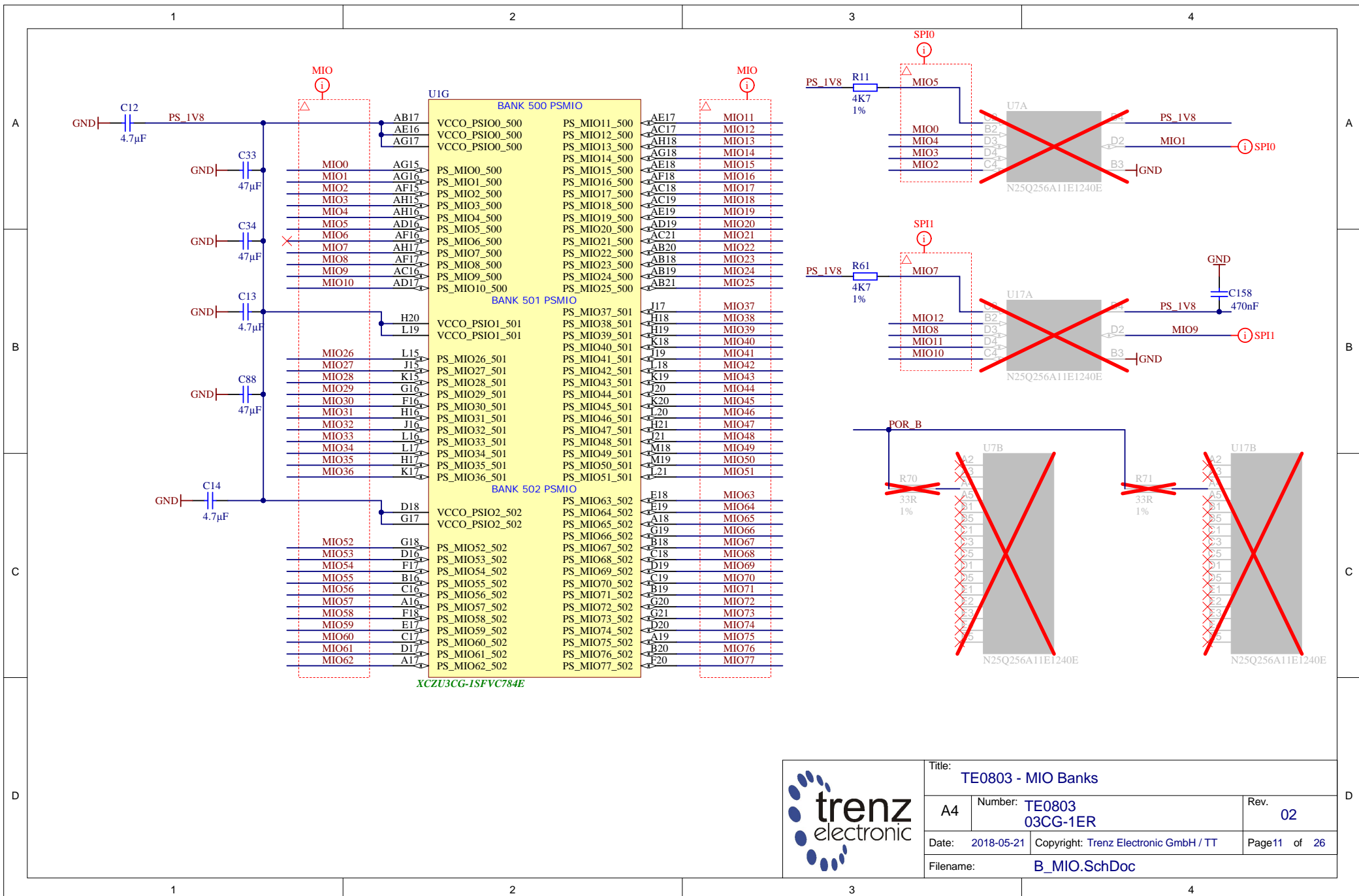
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	A4	Number: TE0803 03CG-1ER
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT
	Rev. 02	
Filename: B66.SchDoc		Page 10 of 26



	Title: TE0803 - MIO Banks	
	A4	Number: TE0803 03CG-1ER
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT
	Filename: B_MIO.SchDoc	Page 11 of 26
	Rev. 02	

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U11

BANK 504 PSDDR

AB22	VCCO_PSDDR_504	PS_DDR_CK0_504
AD23	VCCO_PSDDR_504	PS_DDR_CK_N0_504
AF24	VCCO_PSDDR_504	PS_DDR_CKE0_504
P23	VCCO_PSDDR_504	
T24	VCCO_PSDDR_504	
V25	VCCO_PSDDR_504	PS_DDR_CK1_504
Y26	VCCO_PSDDR_504	PS_DDR_CK_N1_504
	VCCO_PSDDR_504	PS_DDR_CKE1_504
U16	VCC_PSDDR_PLL	PS_DDR_A0_504
U18	VCC_PSDDR_PLL	PS_DDR_A1_504
	VCC_PSDDR_PLL	PS_DDR_A2_504
	VCC_PSDDR_PLL	PS_DDR_A3_504
	VCC_PSDDR_PLL	PS_DDR_A4_504
	VCC_PSDDR_PLL	PS_DDR_A5_504
AA20	VCC_PSINTFP_DDR	PS_DDR_A6_504
AA21	VCC_PSINTFP_DDR	PS_DDR_A7_504
Y19	VCC_PSINTFP_DDR	PS_DDR_A8_504
		PS_DDR_A9_504
		PS_DDR_A10_504
		PS_DDR_A11_504
		PS_DDR_A12_504
		PS_DDR_A13_504
		PS_DDR_A14_504
		PS_DDR_A15_504
		PS_DDR_A16_504
		PS_DDR_A17_504
	PS_DDR_CS_N0_504	
	PS_DDR_CS_N1_504	
	PS_DDR_BA0_504	
	PS_DDR_BA1_504	
	PS_DDR_BG0_504	
	PS_DDR_BG1_504	
	PS_DDR_PARITY_504	
	PS_DDR_RAM_RST_N_504	
	PS_DDR_ACT_N_504	
	PS_DDR_ALERT_N_504	
	PS_DDR_ZQ_504	
	PS_DDR_ODT0_504	
	PS_DDR_ODT1_504	

XCZU3CG-1SFVC784E

W25	DDR4-CLK0_P	
W26	DDR4-CLK0_N	
V28	DDR4-CKE0	
Y24		✗
Y25		✗
V27		✗
W28	DDR4-A0	
Y28	DDR4-A1	
AB28	DDR4-A2	
AA28	DDR4-A3	
Y27	DDR4-A4	
AA27	DDR4-A5	
Y22	DDR4-A6	
AA23	DDR4-A7	
AA22	DDR4-A8	
AB23	DDR4-A9	
AA25	DDR4-A10	
AA26	DDR4-A11	
AB25	DDR4-A12	
AB26	DDR4-A13	
AB24	DDR4-A14	
AC24	DDR4-A15	
AC23	DDR4-A16	
AC22	DDR4-A17	
W27	DDR4-CS	
V26		✗
V23	DDR4-BA0	
W22	DDR4-BA1	
W24	DDR4-BG0	
V22		✗
V24	DDR4-PAR	
U23	DDR4-RESET	
Y23	DDR4-ACT	
U25	DDR4-ALERT	
U24		
U28	DDR4-ODT0	
U26		✗

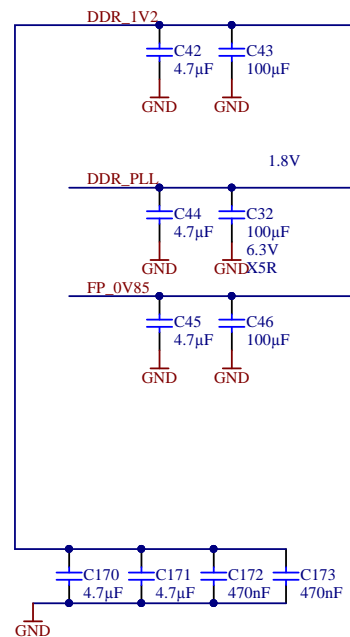
U1J

BANK 504 PSDDR

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DQ1	AE20	PS_DDR_DQ1_504
DQ2	AD20	PS_DDR_DQ2_504
DQ3	AF20	PS_DDR_DQ3_504
DQ4	AH21	PS_DDR_DQ4_504
DQ5	AH20	PS_DDR_DQ5_504
DQ6	AH19	PS_DDR_DQ6_504
DQ7	AG19	PS_DDR_DQ7_504
DQ8	AF22	PS_DDR_DQ8_504
DQ9	AH22	PS_DDR_DQ9_504
DQ10	AE22	PS_DDR_DQ10_504
DQ11	AD22	PS_DDR_DQ11_504
DQ12	AH23	PS_DDR_DQ12_504
DQ13	AH24	PS_DDR_DQ13_504
DQ14	AE24	PS_DDR_DQ14_504
DQ15	AG24	PS_DDR_DQ15_504
DQ16	AC26	PS_DDR_DQ16_504
DQ17	AH26	PS_DDR_DQ17_504
DQ18	AD25	PS_DDR_DQ18_504
DQ19	AD24	PS_DDR_DQ19_504
DQ20	AG26	PS_DDR_DQ20_504
DQ21	AH25	PS_DDR_DQ21_504
DQ22	AH26	PS_DDR_DQ22_504
DQ23	AG25	PS_DDR_DQ23_504
DQ24	AH27	PS_DDR_DQ24_504
DQ25	AH28	PS_DDR_DQ25_504
DQ26	AF28	PS_DDR_DQ26_504
DQ27	AG28	PS_DDR_DQ27_504
DQ28	AC27	PS_DDR_DQ28_504
DQ29	AD27	PS_DDR_DQ29_504
DQ30	AD28	PS_DDR_DQ30_504
DQ31	AC28	PS_DDR_DQ31_504
DDR4-DQS0_P	AF21	PS_DDR_DQS_P0_504
DDR4-DQS0_N	AG21	PS_DDR_DQS_N0_504
DDR4-DQS1_P	AF23	PS_DDR_DQS_P1_504
DDR4-DQS1_N	AG23	PS_DDR_DQS_N1_504
DDR4-DQS2_P	AF25	PS_DDR_DQS_P2_504
DDR4-DQS2_N	AF26	PS_DDR_DQS_N2_504
DDR4-DQS3_P	AE27	PS_DDR_DQS_P3_504
DDR4-DQS3_N	AF27	PS_DDR_DQS_N3_504
DDR4-DQS4_P	N23	PS_DDR_DQS_P4_504
DDR4-DQS4_N	M23	PS_DDR_DQS_N4_504
DDR4-DQS5_P	L23	PS_DDR_DQS_P5_504
DDR4-DQS5_N	K23	PS_DDR_DQS_N5_504
DDR4-DQS6_P	N26	PS_DDR_DQS_P6_504
DDR4-DQS6_N	N27	PS_DDR_DQS_N6_504
DDR4-DQS7_P	J26	PS_DDR_DQS_P7_504
DDR4-DQS7_N	J27	PS_DDR_DQS_N7_504
	R27	PS_DDR_DQS_P8_504
	T27	PS_DDR_DQS_N8_504

XCZU3CG-1SFVC784E

PS_DDR_DQ32_504	T22	DQ32
PS_DDR_DQ33_504	R22	DQ33
PS_DDR_DQ34_504	P22	DQ34
PS_DDR_DQ35_504	N22	DQ35
PS_DDR_DQ36_504	T23	DQ36
PS_DDR_DQ37_504	P24	DQ37
PS_DDR_DQ38_504	R24	DQ38
PS_DDR_DQ39_504	N24	DQ39
PS_DDR_DQ40_504	H24	DQ40
PS_DDR_DQ41_504	T24	DQ41
PS_DDR_DQ42_504	M24	DQ42
PS_DDR_DQ43_504	K24	DQ43
PS_DDR_DQ44_504	J22	DQ44
PS_DDR_DQ45_504	H22	DQ45
PS_DDR_DQ46_504	K22	DQ46
PS_DDR_DQ47_504	L22	DQ47
PS_DDR_DQ48_504	M25	DQ48
PS_DDR_DQ49_504	M26	DQ49
PS_DDR_DQ50_504	L25	DQ50
PS_DDR_DQ51_504	L26	DQ51
PS_DDR_DQ52_504	K28	DQ52
PS_DDR_DQ53_504	L28	DQ53
PS_DDR_DQ54_504	M28	DQ54
PS_DDR_DQ55_504	N28	DQ55
PS_DDR_DQ56_504	T28	DQ56
PS_DDR_DQ57_504	K27	DQ57
PS_DDR_DQ58_504	H28	DQ58
PS_DDR_DQ59_504	H27	DQ59
PS_DDR_DQ60_504	G26	DQ60
PS_DDR_DQ61_504	G25	DQ61
PS_DDR_DQ62_504	K25	DQ62
PS_DDR_DQ63_504	L25	DQ63
PS_DDR_DQ64_504	T28	✗
PS_DDR_DQ65_504	R28	✗
PS_DDR_DQ66_504	P28	✗
PS_DDR_DQ67_504	P27	✗
PS_DDR_DQ68_504	P26	✗
PS_DDR_DQ69_504	R25	✗
PS_DDR_DQ70_504	T25	✗
PS_DDR_DQ71_504	T25	✗
PS_DDR_DM0_504	AG20	DDR4-DM0
PS_DDR_DM1_504	AE23	DDR4-DM1
PS_DDR_DM2_504	AE25	DDR4-DM2
PS_DDR_DM3_504	AE28	DDR4-DM3
PS_DDR_DM4_504	R23	DDR4-DM4
PS_DDR_DM5_504	H23	DDR4-DM5
PS_DDR_DM6_504	L27	DDR4-DM6
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PS_DDR_DM8_504	T26	✗



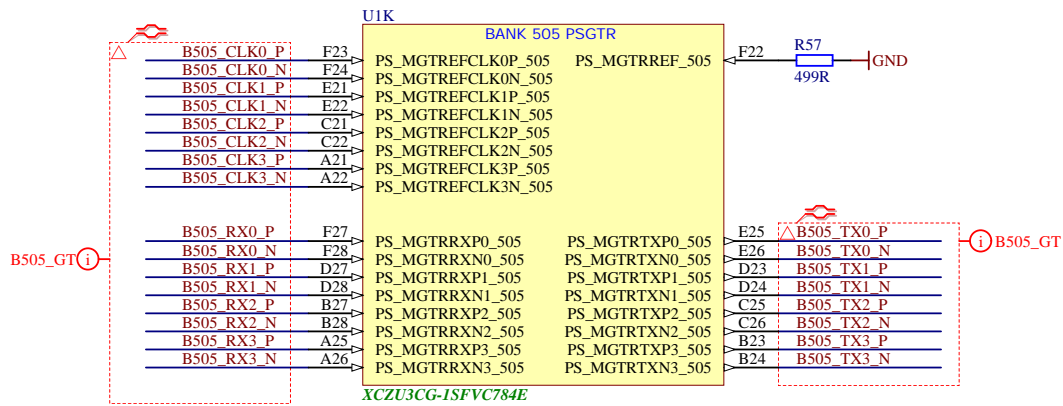
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A4	Number: TE0803 03CG-1ER	Rev. 02	
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page12 of 26	
Filename: PS_DDR.SchDoc			

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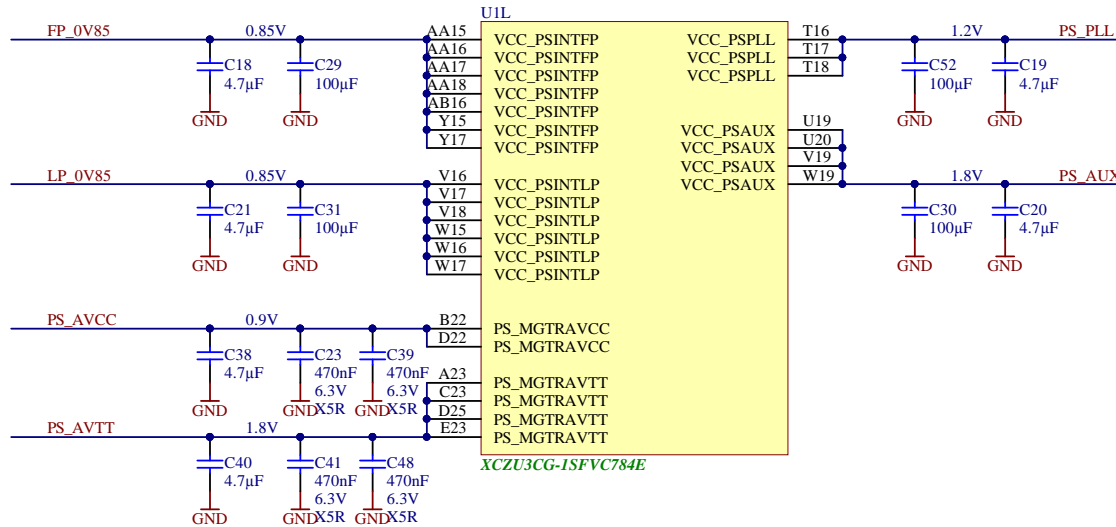
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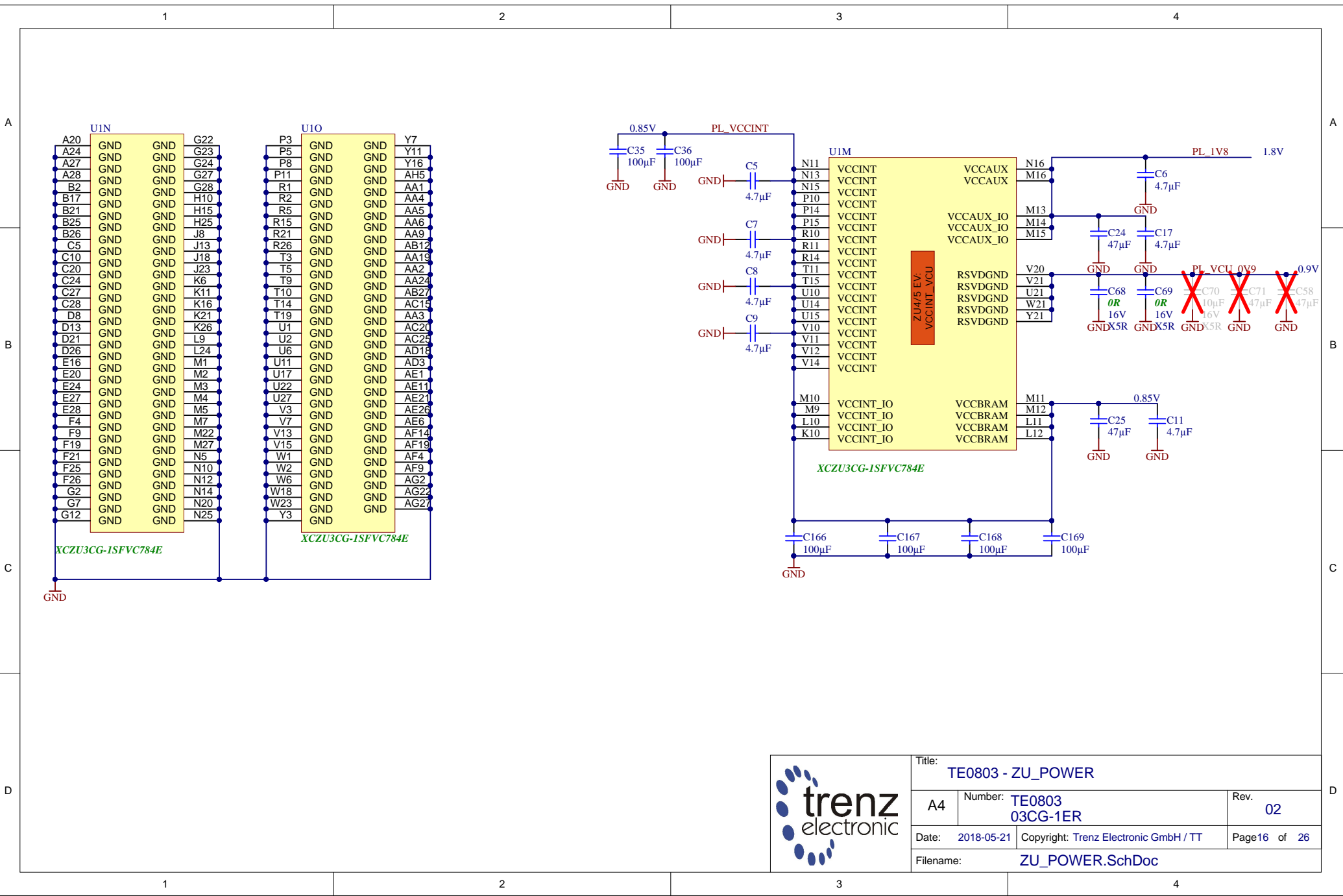
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	A4	Number: TE0803 03CG-1ER	Rev. 02
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page13 of 26
	Filename: B_PS_GT.SchDoc		



Title: TE0803 - ZU_PS_POWER		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page15 of 26
Filename: ZU_PS_POWER.SchDoc		



			Title: TE0803 - ZU_POWER	
			A4	Number: TE0803 03CG-1ER
Date: 2018-05-21		Copyright: Trenz Electronic GmbH / TT		Page 16 of 26
Filename: ZU_POWER.SchDoc				

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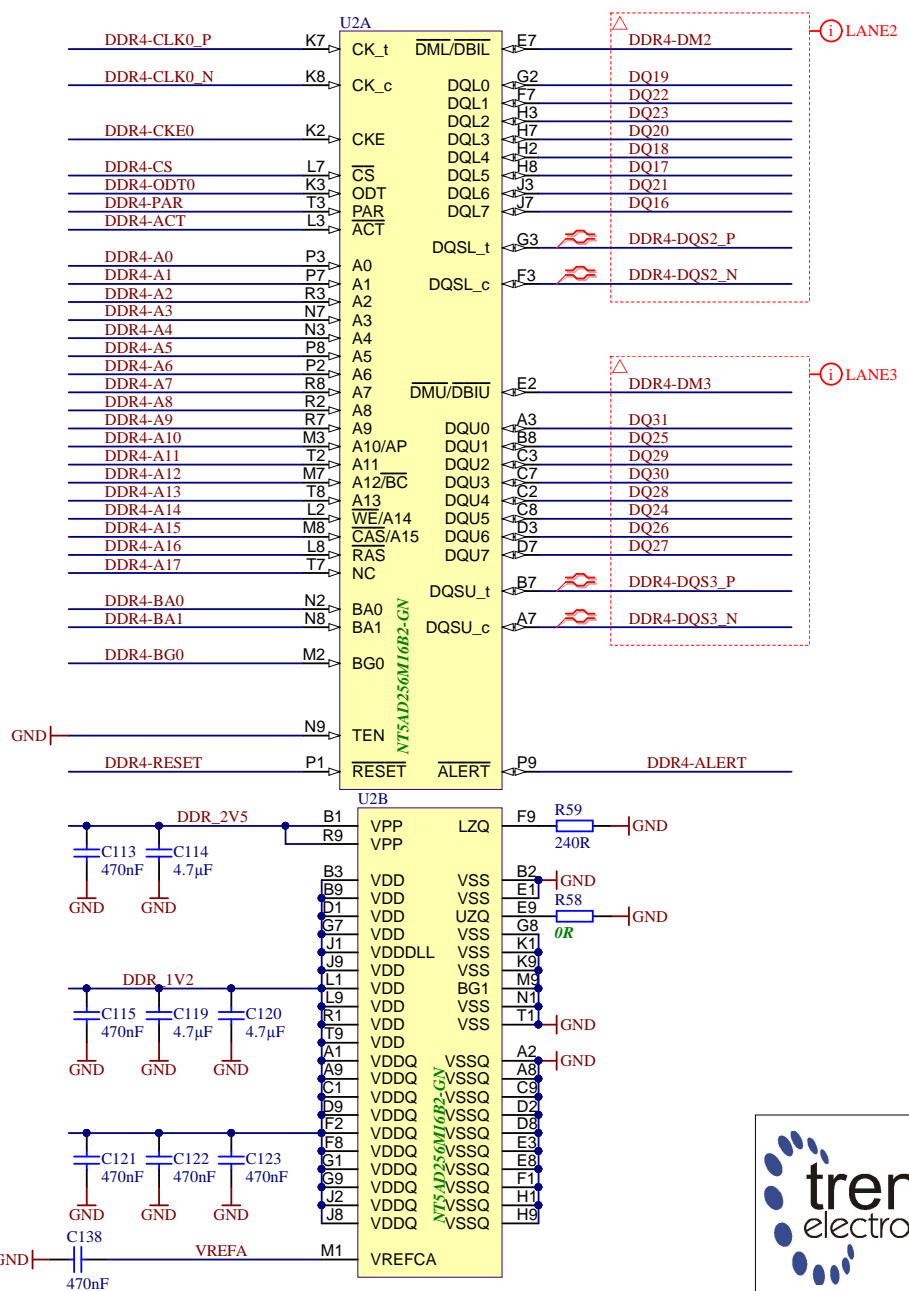
B

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Title: TE0803 - DDR4_1_RAM		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page 17 of 26
Filename: DDR4-RAM.SchDoc		

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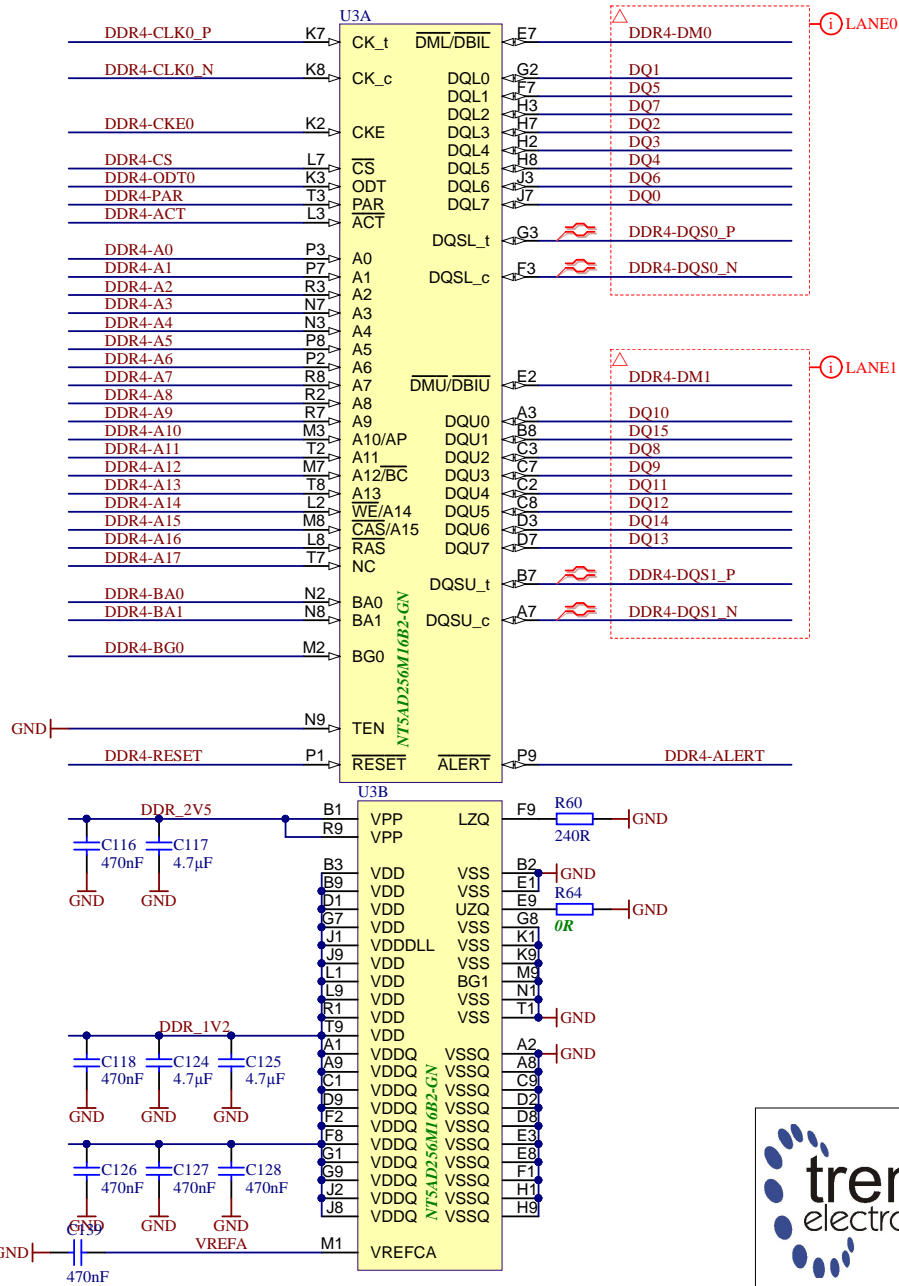

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Title: TE0803 - DDR4_2_RAM		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page 18 of 26
Filename: DDR4-RAM_2.SchDoc		

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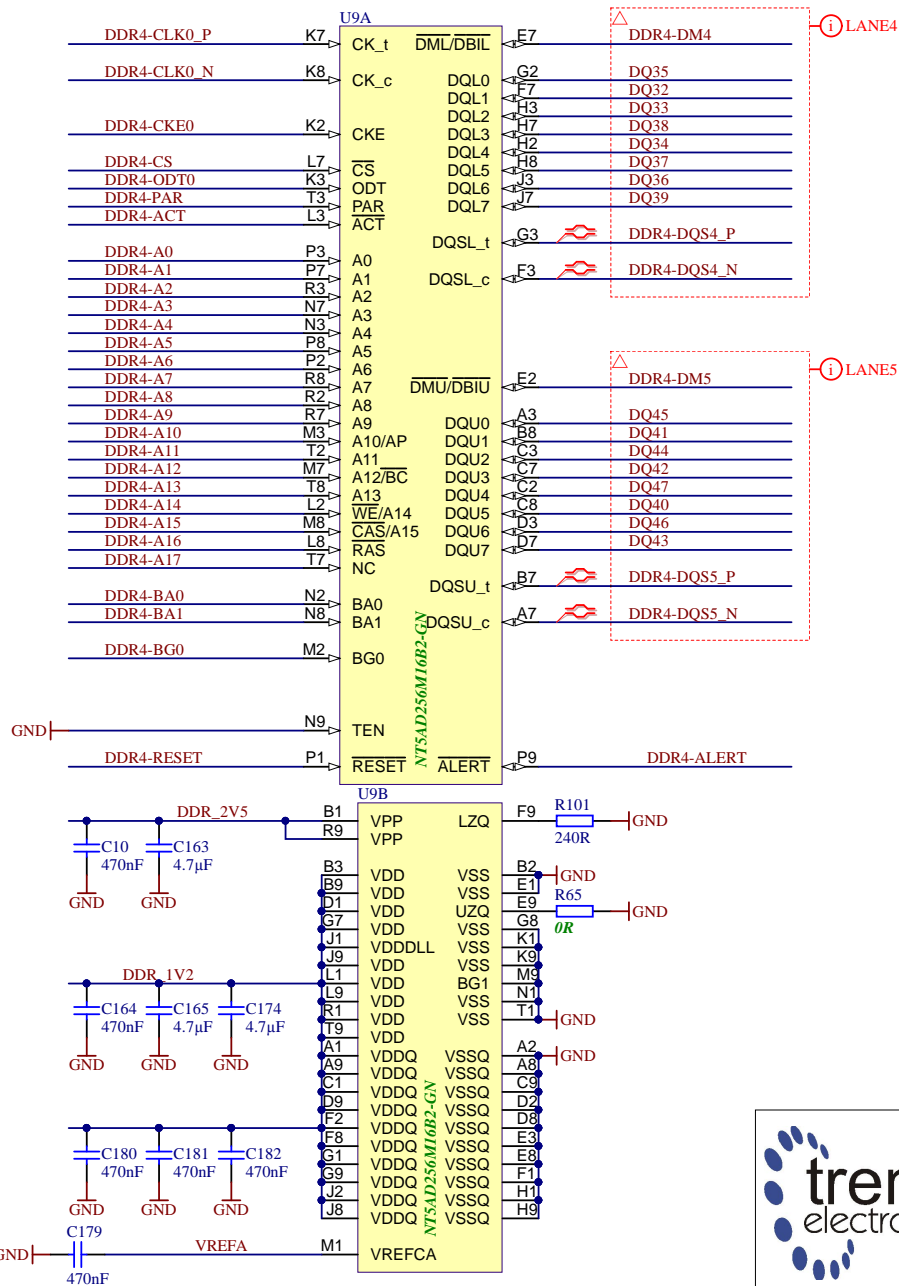
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C

C

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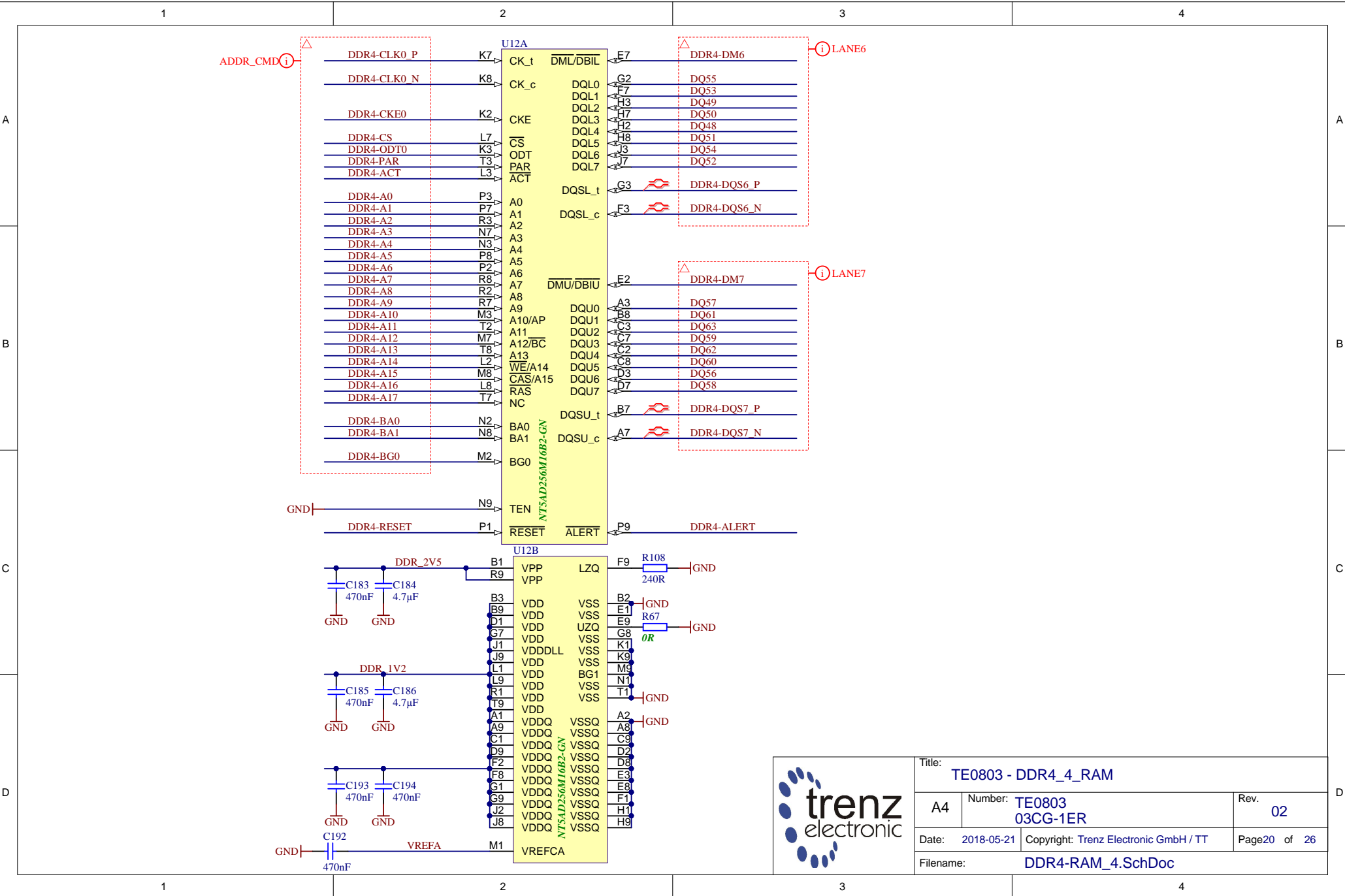
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A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page19 of 26
Filename: DDR4-RAM_3.SchDoc		

1

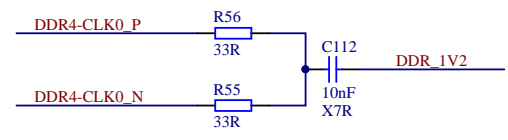
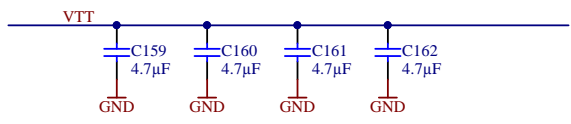
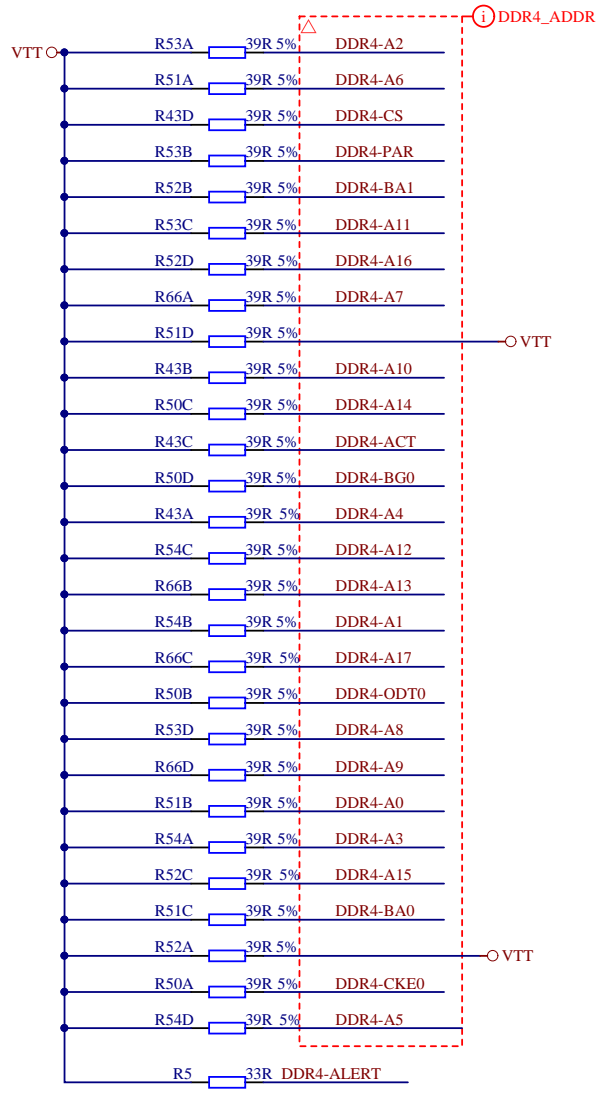
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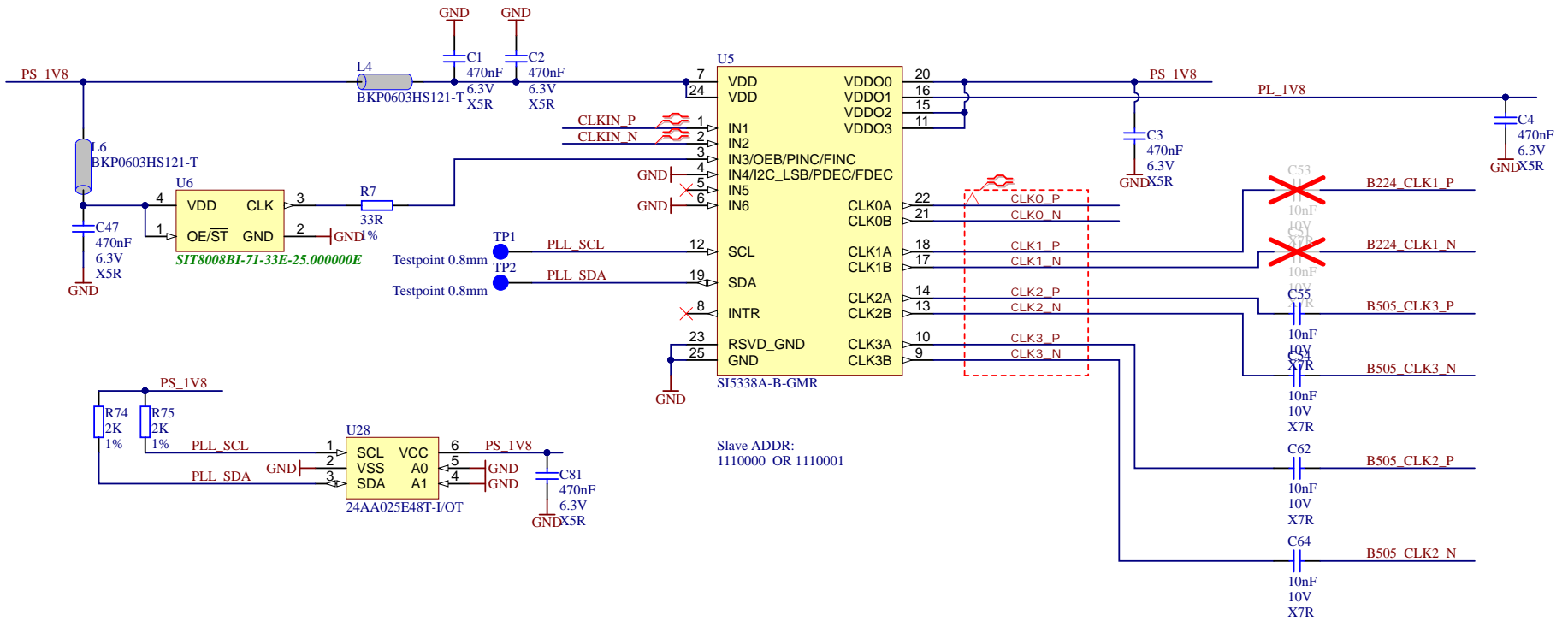
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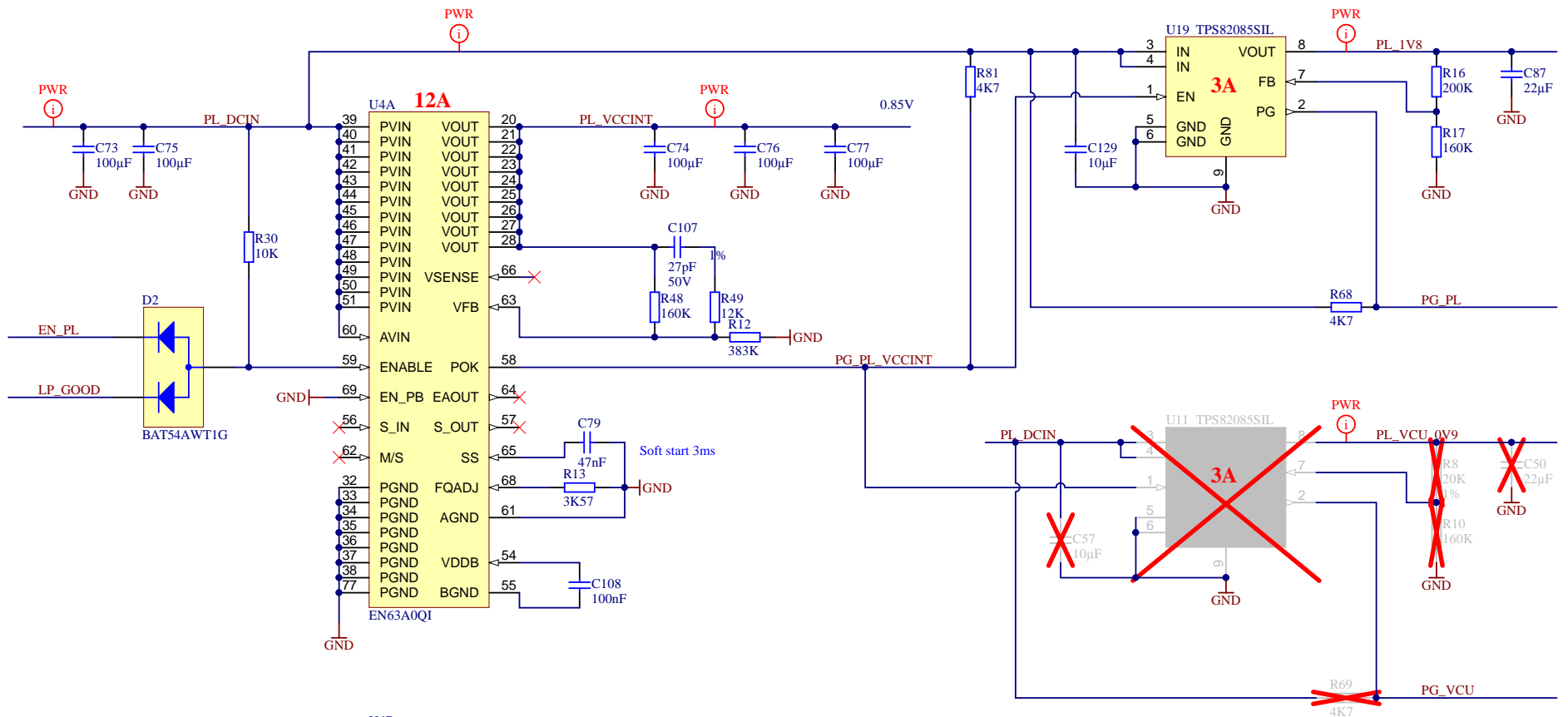
Title: TE0803 - DDR4_4_RAM		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page20 of 26
Filename: DDR4-RAM_4.SchDoc		



Title: TE0803 - DDR4_TERM		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page21 of 26
Filename: DDR4-TERM.SchDoc		



Title: TE0803 - CLOCK		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page22 of 26
Filename: Clock.SchDoc		



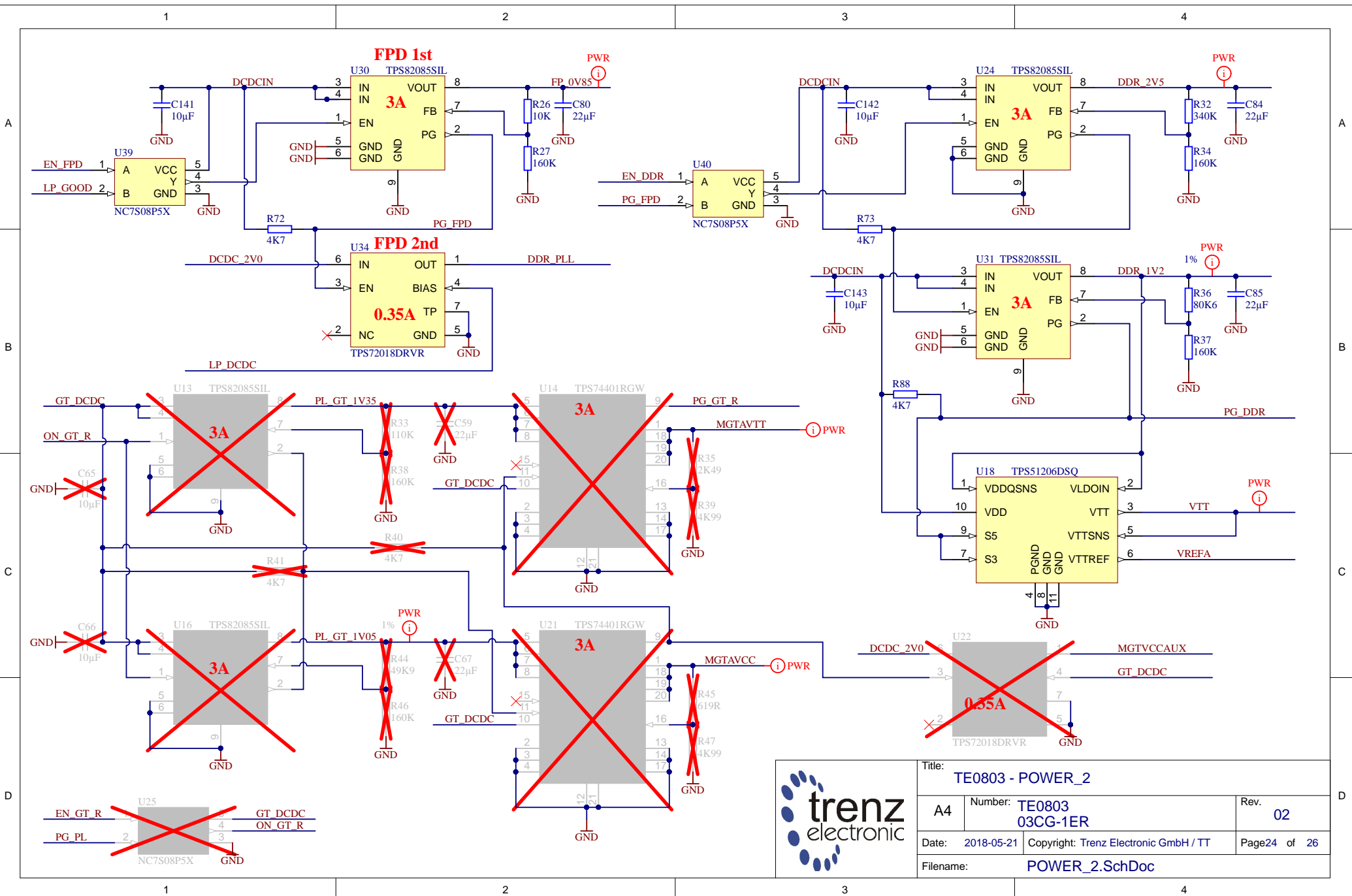
U4B

1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC(SW)	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76

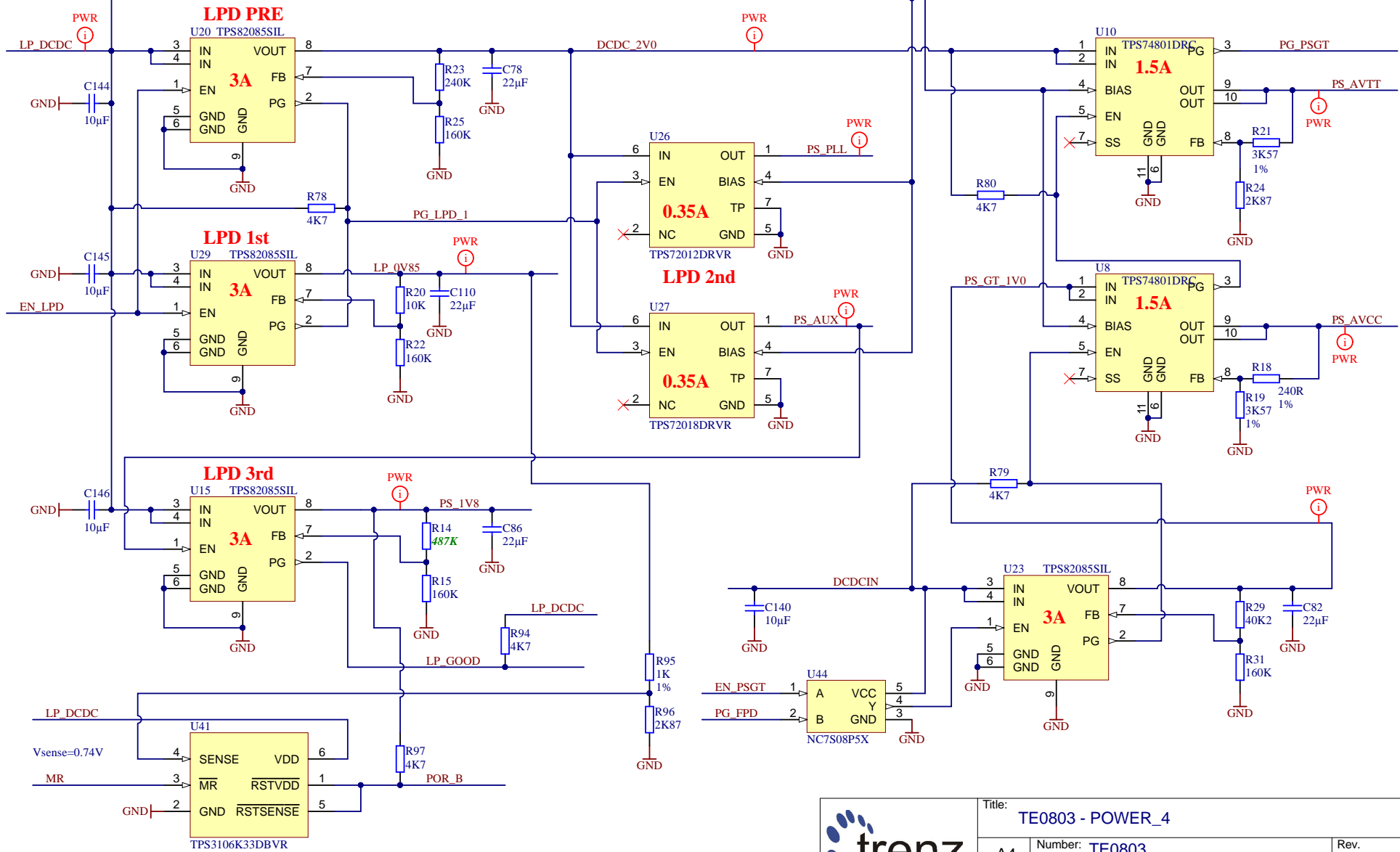
EN63A0QI




Title: TE0803 - POWER		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page23 of 26
Filename: POWER.SchDoc		



Title: TE0803 - POWER_2		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page24 of 26
Filename: POWER_2.SchDoc		



			Title: TE0803 - POWER_4	
			A4	Number: TE0803 03CG-1ER
Date: 2018-05-21		Copyright: Trenz Electronic GmbH / TT		Page25 of 26
Filename: POWER_4.SchDoc				

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CHANGES REV01a (20.11.2017):

1) VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9.

CHANGES REV02 (20.06.2018):

- 1) Added LDO to DDR_PLL
- 2) All differential pairs wath length matched with tollerance 0.1mm (excluding package delays)
- 3) Added MAC EEPROM U28
- 4) VPS_MGTRAVCC set to 0.85V
- 5) Added pull-up resistors R68,R69

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Title: TE0803 - Changes list		
A4	Number: TE0803 03CG-1ER	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH	Page26 of 26
Filename: Revision_Changes.SchDoc		

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