

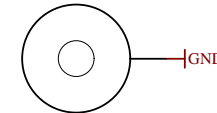
1

2

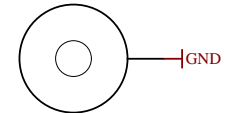
3

4

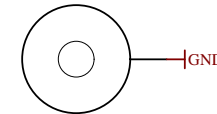
U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_DDR4-TERM DDR4-TERM.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_REV_CH Revision_Changes.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	
	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	



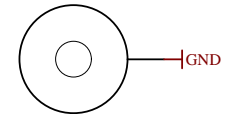
Mount.Hole 3.2mm für Unterlegscheibe



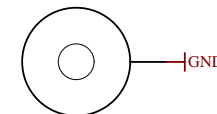
Mount.Hole 3.2mm für Unterlegscheibe



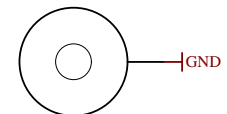
Mount.Hole 3.2mm für Unterlegscheibe



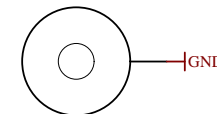
Mount.Hole 3.2mm für Unterlegscheibe



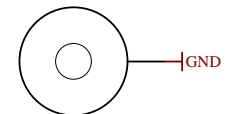
Mount.Hole 3.2mm für Unterlegscheibe



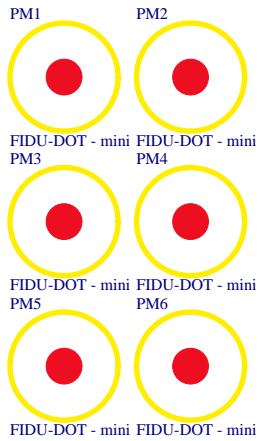
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe

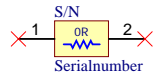


Mount.Hole 3.2mm für Unterlegscheibe



LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial
Serial
Serialnumber 6,3 x 6.3mm



Title: TE0803		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page1 of 26
Filename: TE0803.SchDoc		

1

2

3

4

A

A

B

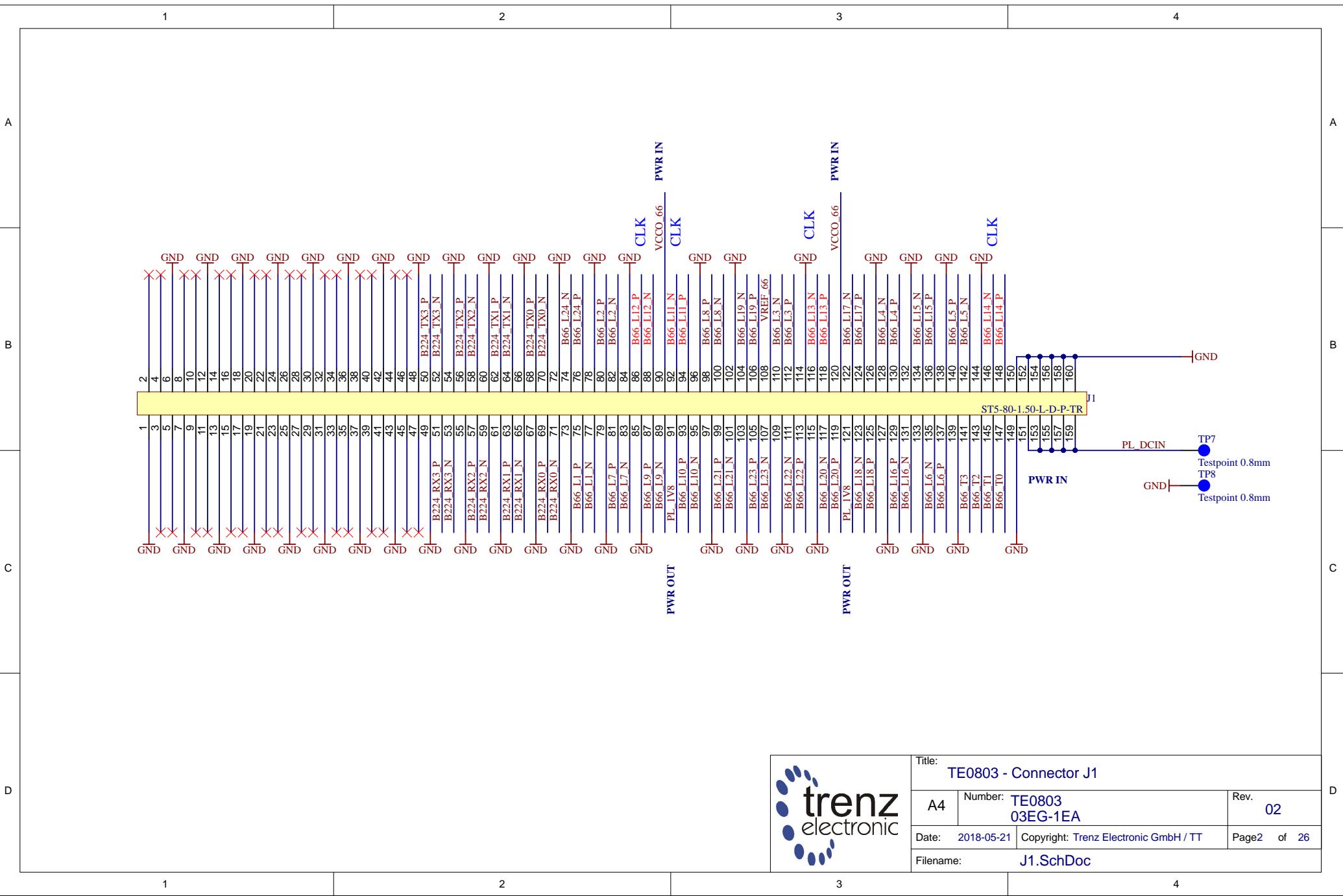
B


C

C

D

D



		Title: TE0803 - Connector J1	
		A4	Number: TE0803 03EG-1EA
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Rev. 02	Page2 of 26
Filename: J1.SchDoc			

1

2

3

4

A

A

B

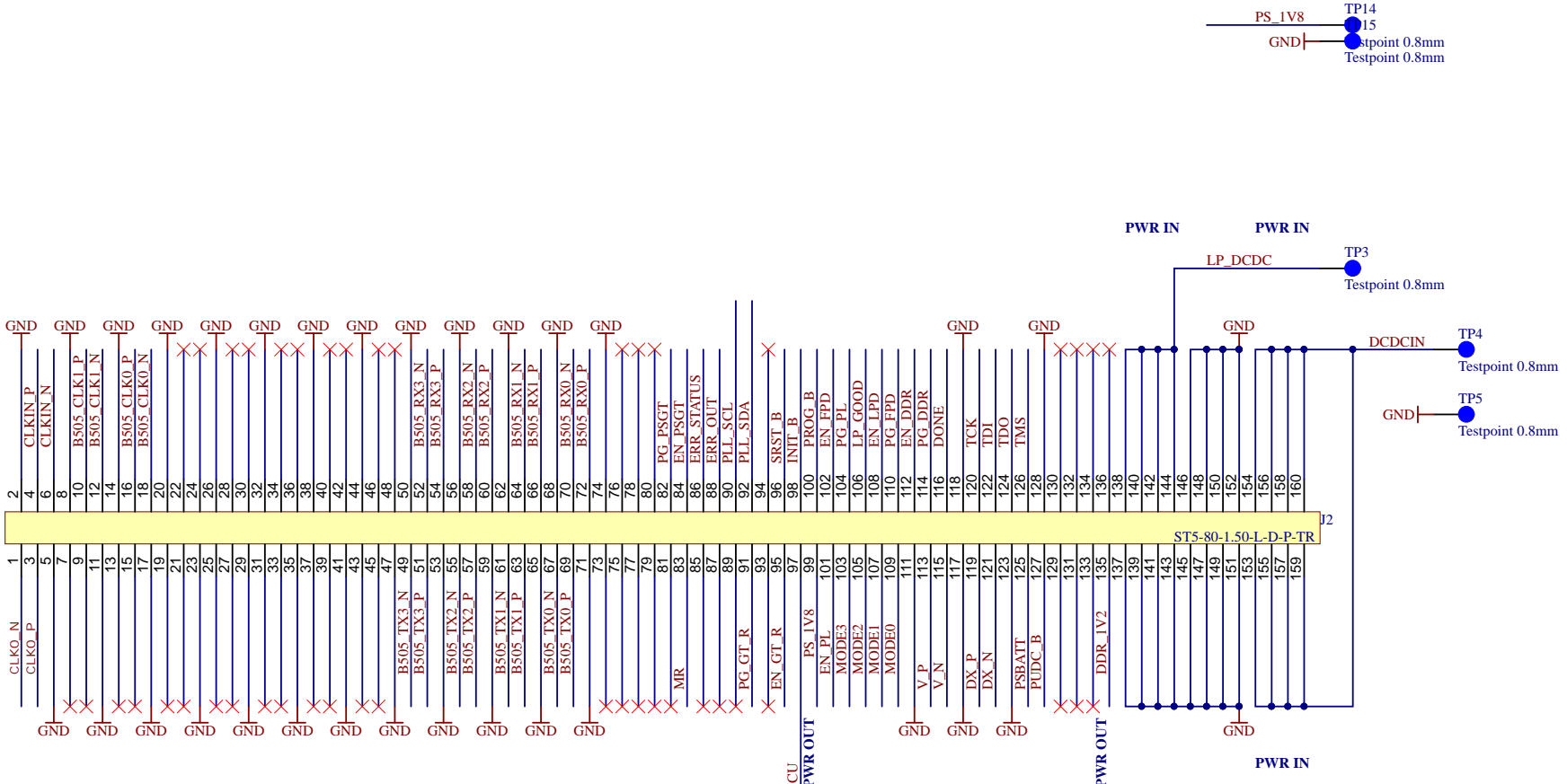

B

C

C

D

D

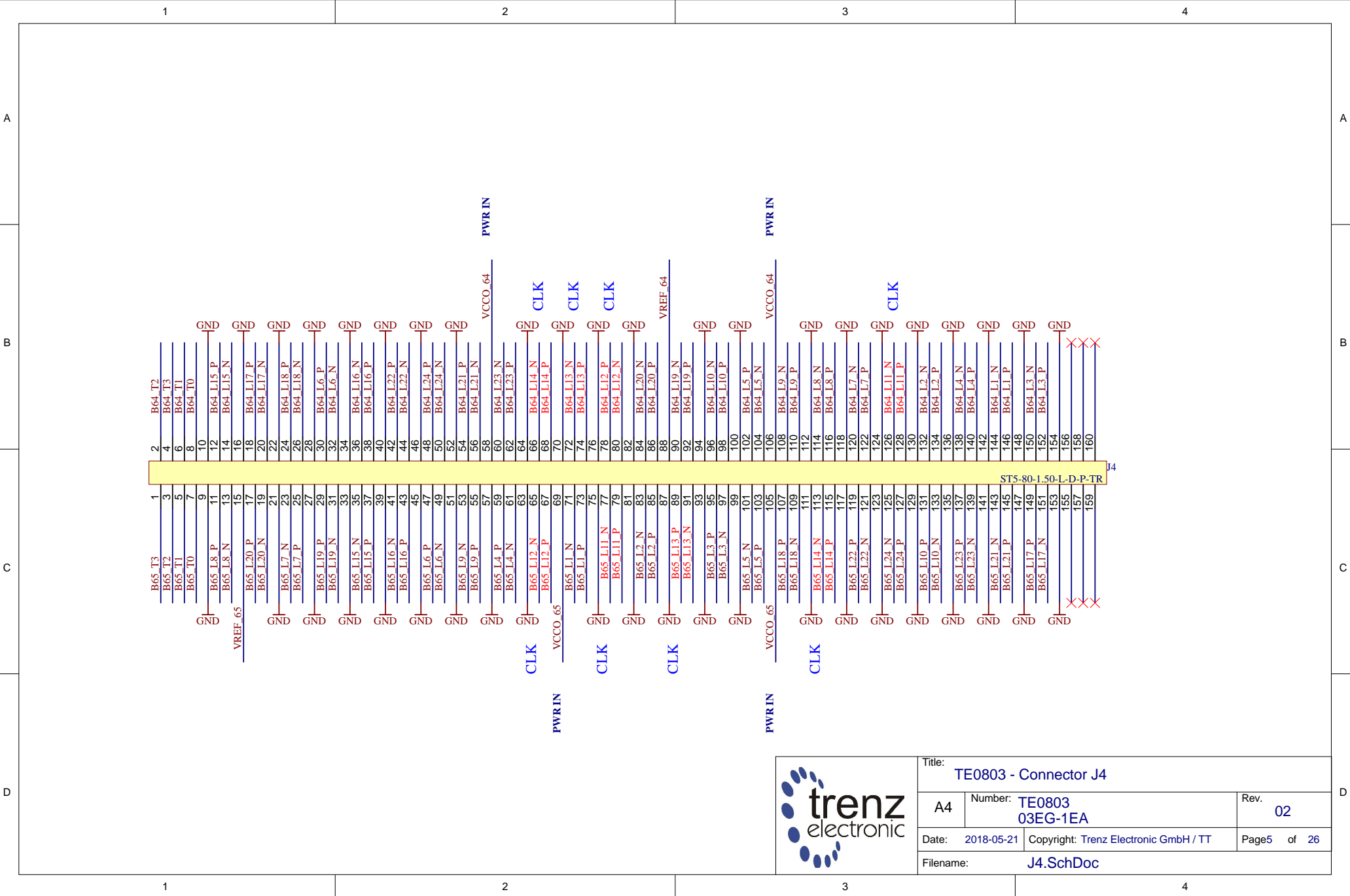
Title: TE0803 - Connector J2		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page3 of 26
Filename: J2.SchDoc		

1

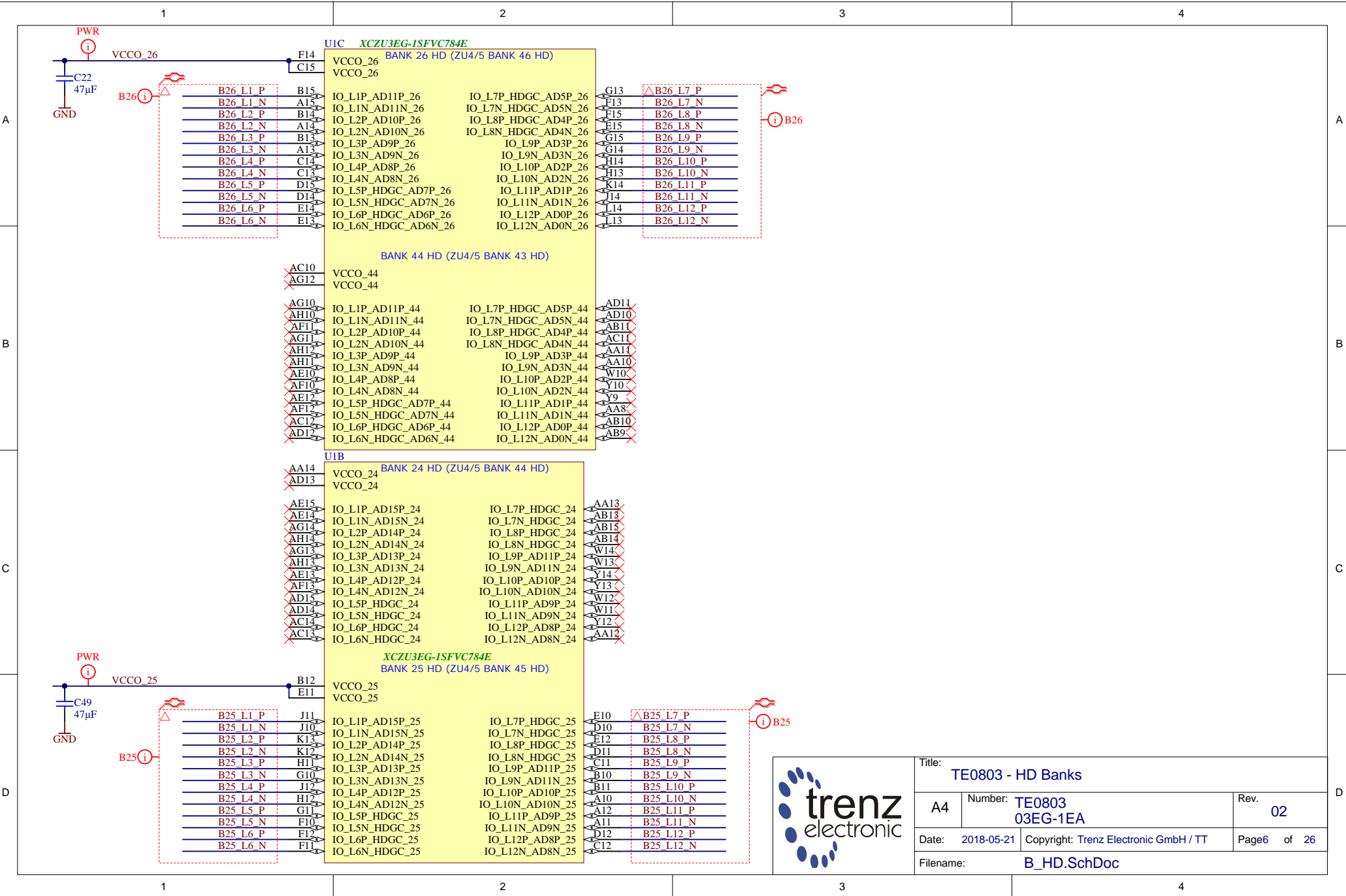
2

3

4



Title: TE0803 - Connector J4		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page5 of 26
Filename: J4.SchDoc		



UIC XCZU3EG-1SFVC784E
BANK 26 HD (ZU4/5 BANK 46 HD)

VCCO_26	F14	VCCO_26	G13	B26 L7 P
VCCO_26	C15	VCCO_26	F13	B26 L7 N
B26 L1 P	B15	IO_L1P_AD11P_26	F15	B26 L8 P
B26 L1 N	A15	IO_L1N_AD11N_26	F15	B26 L8 N
B26 L2 P	B14	IO_L2P_AD10P_26	G15	B26 L9 P
B26 L2 N	A14	IO_L2N_AD10N_26	G14	B26 L9 N
B26 L3 P	B13	IO_L3P_AD9P_26	H14	B26 L10 P
B26 L3 N	A13	IO_L3N_AD9N_26	H13	B26 L10 N
B26 L4 P	C14	IO_L4P_AD8P_26	K14	B26 L11 P
B26 L4 N	C13	IO_L4N_AD8N_26	J14	B26 L11 N
B26 L5 P	D15	IO_L5P_HDGC_AD7P_26	L14	B26 L12 P
B26 L5 N	D14	IO_L5N_HDGC_AD7N_26	L13	B26 L12 N
B26 L6 P	E14	IO_L6P_HDGC_AD6P_26		
B26 L6 N	E13	IO_L6N_HDGC_AD6N_26		
		IO_L7P_HDGC_AD5P_26		
		IO_L7N_HDGC_AD5N_26		
		IO_L8P_HDGC_AD4P_26		
		IO_L8N_HDGC_AD4N_26		
		IO_L9P_AD3P_26		
		IO_L9N_AD3N_26		
		IO_L10P_AD2P_26		
		IO_L10N_AD2N_26		
		IO_L11P_AD1P_26		
		IO_L11N_AD1N_26		
		IO_L12P_AD0P_26		
		IO_L12N_AD0N_26		

BANK 44 HD (ZU4/5 BANK 43 HD)

VCCO_44	AC10	VCCO_44	AD11	
VCCO_44	AG12	VCCO_44	AD10	
IO_L1P_AD11P_44	AG10	IO_L7P_HDGC_AD5P_44	AB11	
IO_L1N_AD11N_44	AH10	IO_L7N_HDGC_AD5N_44	AC11	
IO_L2P_AD10P_44	AF11	IO_L8P_HDGC_AD4P_44	AA11	
IO_L2N_AD10N_44	AG11	IO_L8N_HDGC_AD4N_44	AA10	
IO_L3P_AD9P_44	AH12	IO_L9P_AD3P_44	W10	
IO_L3N_AD9N_44	AH11	IO_L9N_AD3N_44	Y10	
IO_L4P_AD8P_44	AE10	IO_L10P_AD2P_44	Y9	
IO_L4N_AD8N_44	AF10	IO_L10N_AD2N_44	AA8	
IO_L5P_HDGC_AD7P_44	AE12	IO_L11P_AD1P_44	AB10	
IO_L5N_HDGC_AD7N_44	AF12	IO_L11N_AD1N_44	AB9	
IO_L6P_HDGC_AD6P_44	AC12	IO_L12P_AD0P_44		
IO_L6N_HDGC_AD6N_44	AD12	IO_L12N_AD0N_44		

UIB
BANK 24 HD (ZU4/5 BANK 44 HD)

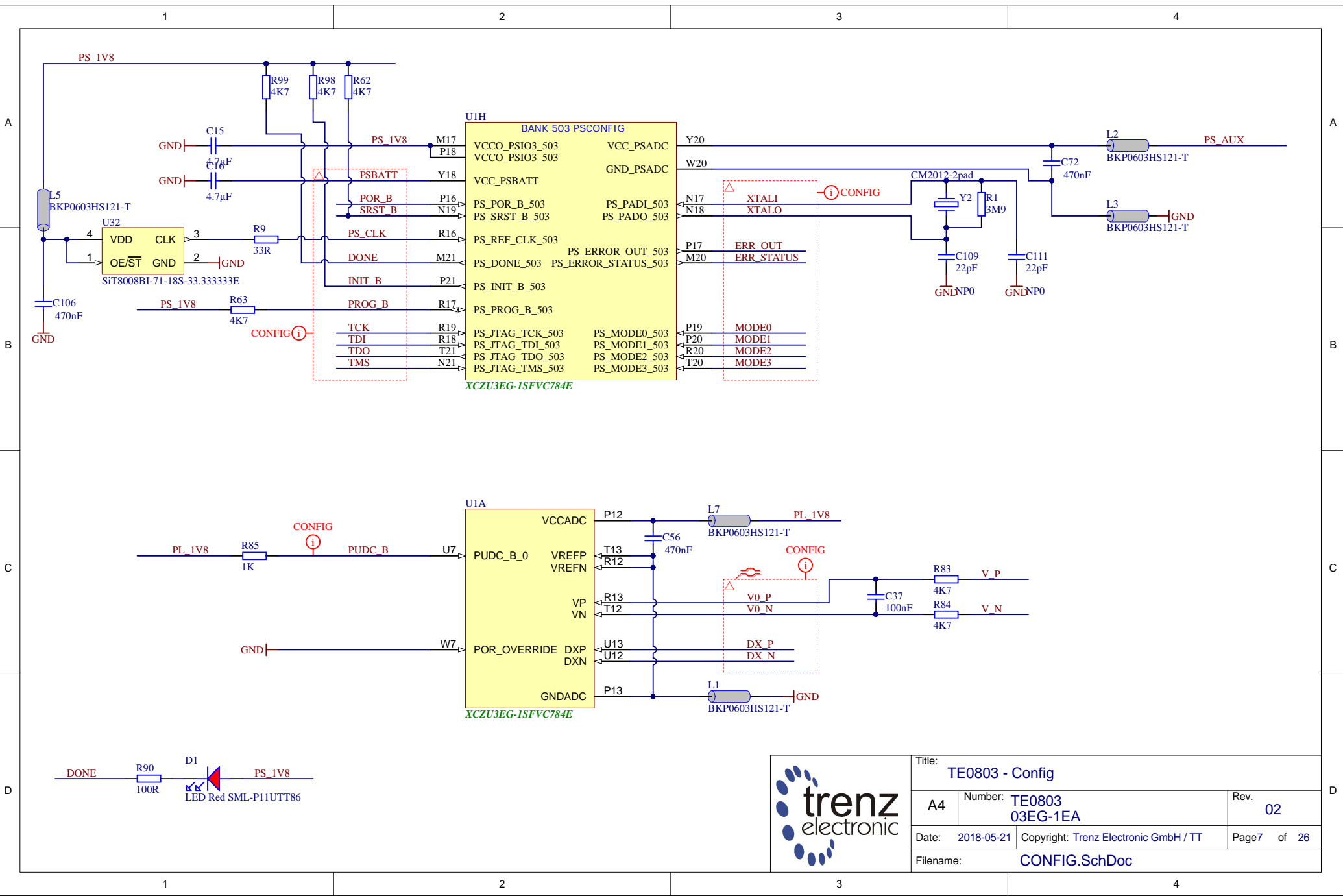
VCCO_24	AA14	VCCO_24	AA13	
VCCO_24	AD13	VCCO_24	AB13	
IO_L1P_AD15P_24	AE15	IO_L7P_HDGC_24	AB15	
IO_L1N_AD15N_24	AE14	IO_L7N_HDGC_24	AB14	
IO_L2P_AD14P_24	AG14	IO_L8P_HDGC_24	W14	
IO_L2N_AD14N_24	AH14	IO_L8N_HDGC_24	W13	
IO_L3P_AD13P_24	AG13	IO_L9P_AD11P_24	Y14	
IO_L3N_AD13N_24	AH13	IO_L9N_AD11N_24	Y13	
IO_L4P_AD12P_24	AE13	IO_L10P_AD10P_24	W12	
IO_L4N_AD12N_24	AF13	IO_L10N_AD10N_24	W11	
IO_L5P_HDGC_24	AD15	IO_L11P_AD9P_24	Y12	
IO_L5N_HDGC_24	AD14	IO_L11N_AD9N_24	AA12	
IO_L6P_HDGC_24	AC14	IO_L12P_AD8P_24		
IO_L6N_HDGC_24	AC13	IO_L12N_AD8N_24		

XCZU3EG-1SFVC784E
BANK 25 HD (ZU4/5 BANK 45 HD)

VCCO_25	B12	VCCO_25	E10	B25 L7 P
VCCO_25	E11	VCCO_25	D10	B25 L7 N
B25 L1 P	J11	IO_L1P_AD15P_25	E12	B25 L8 P
B25 L1 N	J10	IO_L1N_AD15N_25	D11	B25 L8 N
B25 L2 P	K13	IO_L2P_AD14P_25	C11	B25 L9 P
B25 L2 N	K12	IO_L2N_AD14N_25	B10	B25 L9 N
B25 L3 P	H11	IO_L3P_AD13P_25	B11	B25 L10 P
B25 L3 N	G10	IO_L3N_AD13N_25	A10	B25 L10 N
B25 L4 P	J12	IO_L4P_AD12P_25	A12	B25 L11 P
B25 L4 N	H12	IO_L4N_AD12N_25	A11	B25 L11 N
B25 L5 P	G11	IO_L5P_HDGC_25	D12	B25 L12 P
B25 L5 N	F10	IO_L5N_HDGC_25	C12	B25 L12 N
B25 L6 P	F12	IO_L6P_HDGC_25		
B25 L6 N	F11	IO_L6N_HDGC_25		
		IO_L7P_HDGC_25		
		IO_L7N_HDGC_25		
		IO_L8P_HDGC_25		
		IO_L8N_HDGC_25		
		IO_L9P_AD11P_25		
		IO_L9N_AD11N_25		
		IO_L10P_AD10P_25		
		IO_L10N_AD10N_25		
		IO_L11P_AD9P_25		
		IO_L11N_AD9N_25		
		IO_L12P_AD8P_25		
		IO_L12N_AD8N_25		



Title: TE0803 - HD Banks		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page6 of 26
Filename: B_HD.SchDoc		



Title: TE0803 - Config		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page7 of 26
Filename: CONFIG.SchDoc		

1

2

3

4

A

A

B

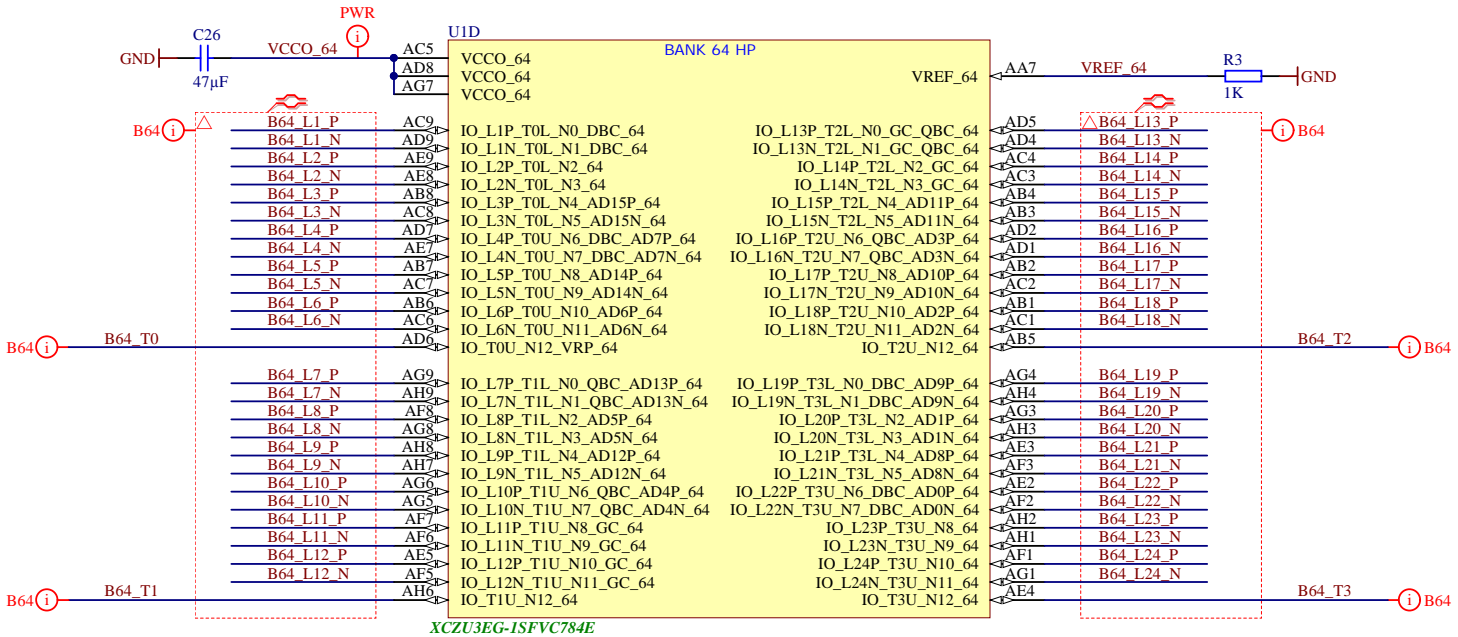

B

C

C

D

D

Title: TE0803 - B64		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page8 of 26
Filename: B64.SchDoc		

1

2

3

4

1

2

3

4

A

A

B

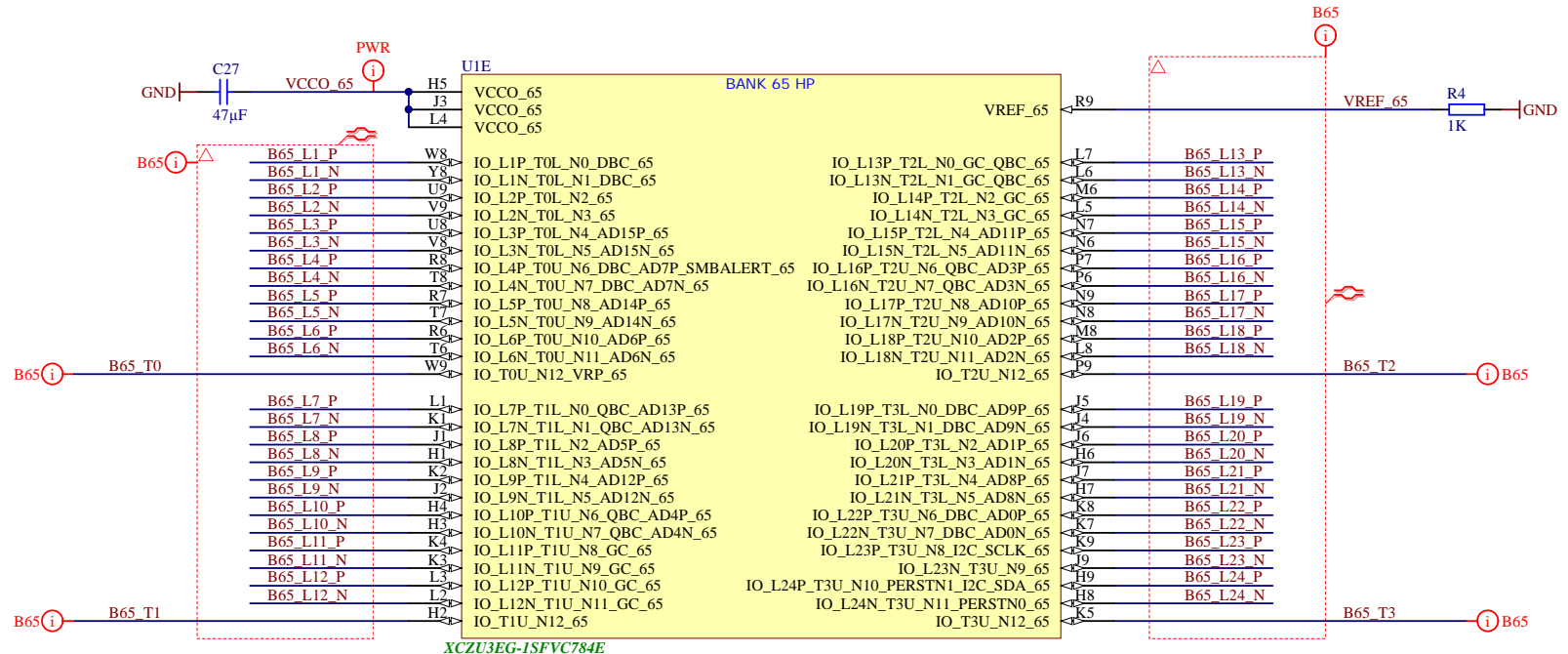
B

C

C

D

D



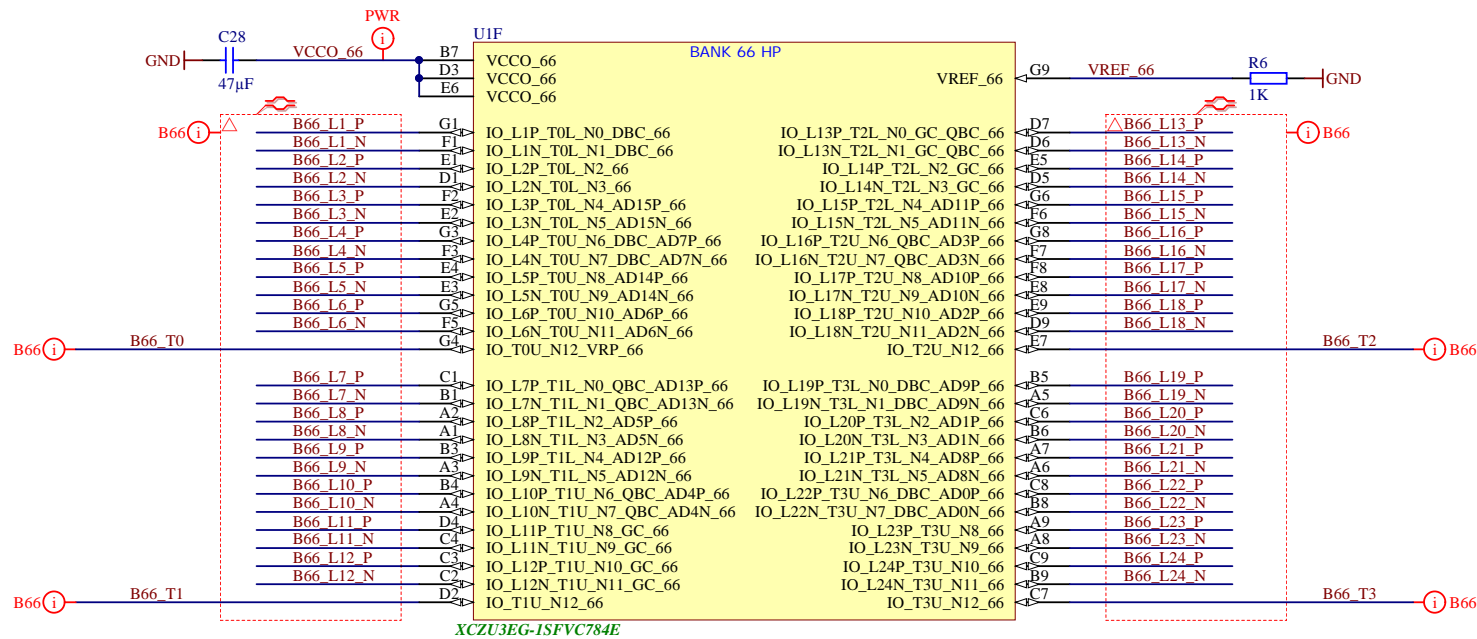
	Title: TE0803 - B65	
	A4	Number: TE0803 03EG-1EA
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT
	Rev. 02	Page9 of 26
Filename: B65.SchDoc		

1

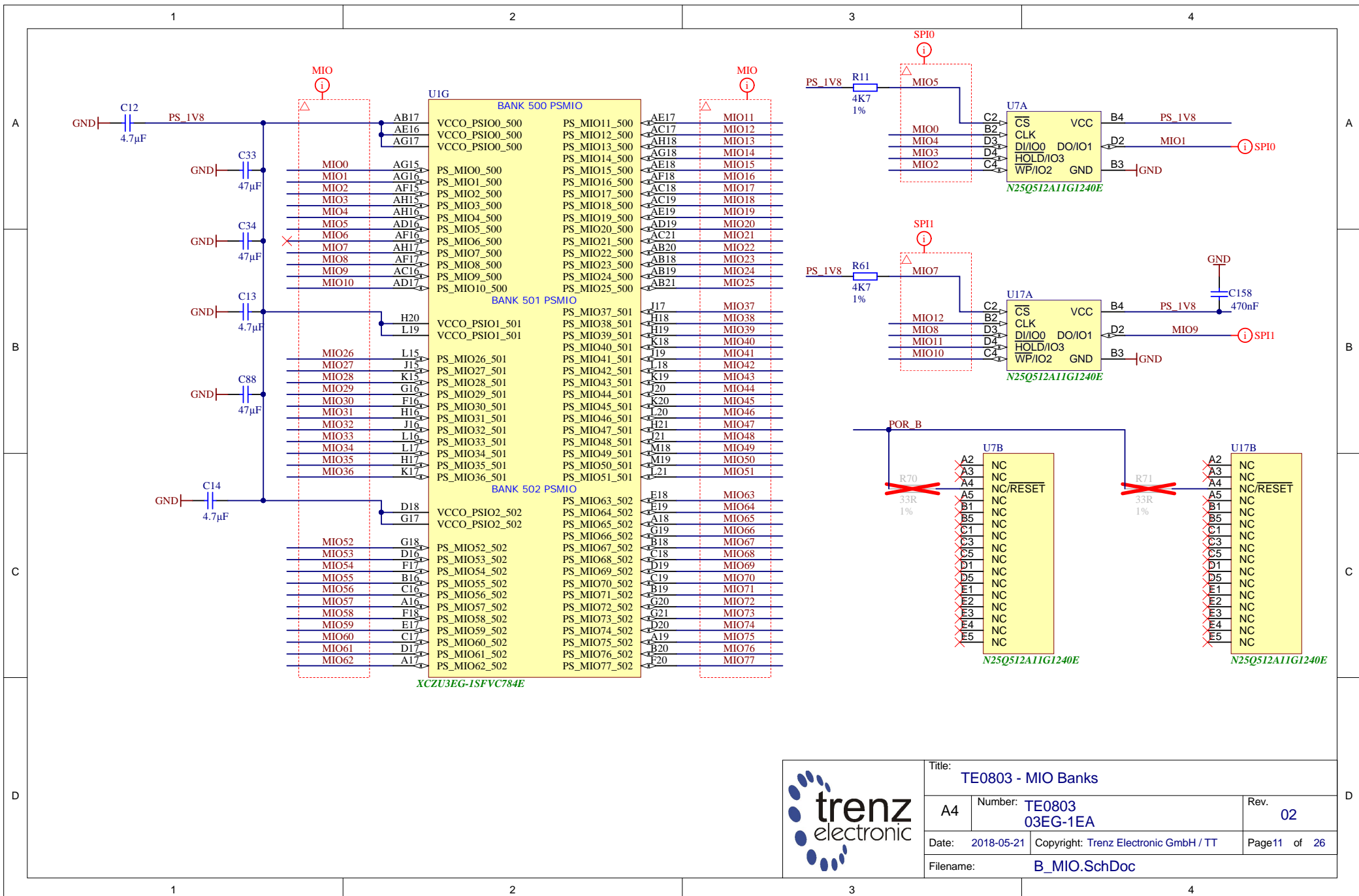
2

3

4



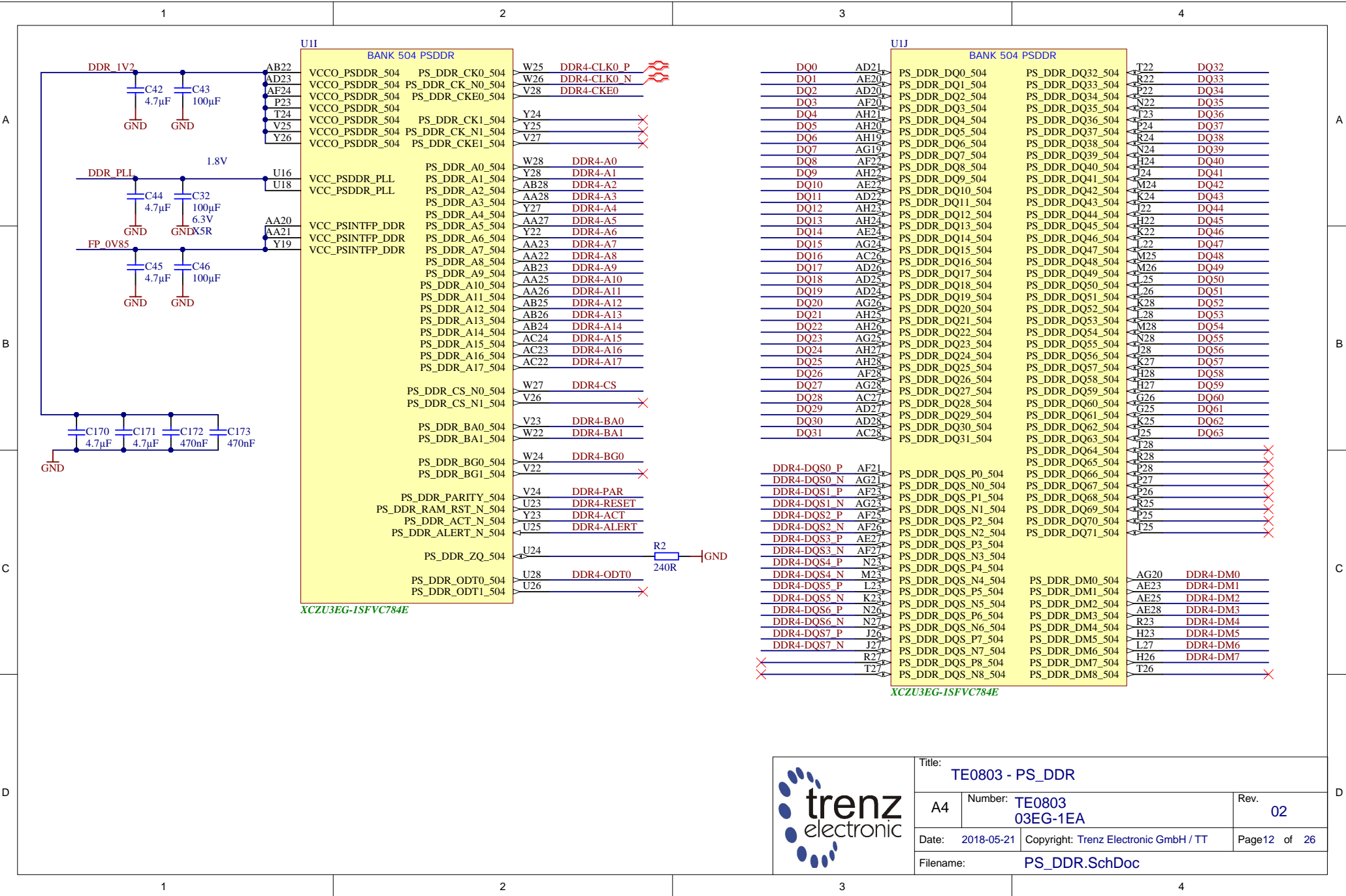
Title: TE0803 - B66		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page10 of 26
Filename: B66.SchDoc		



trenz electronic

Title: **TE0803 - MIO Banks**

A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page 11 of 26
Filename: B_MIO.SchDoc		



U11
BANK 504 PSDDR

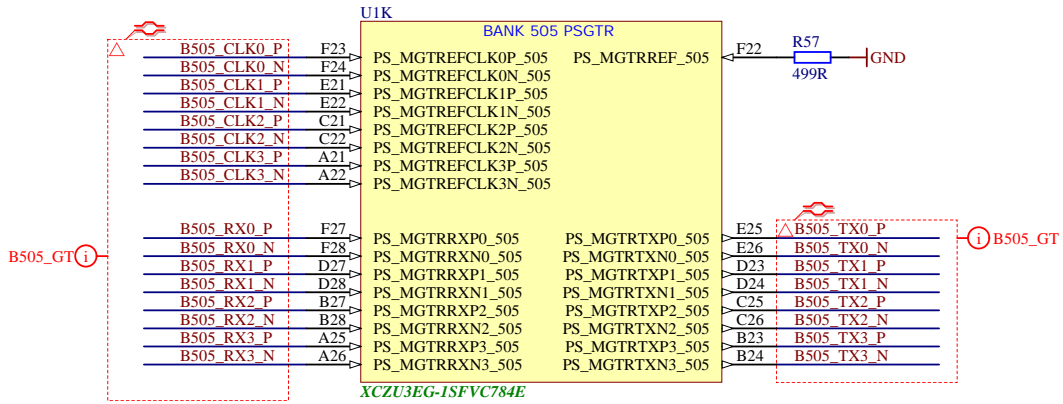
AB22	VCCO_PSDDR_504	PS_DDR_CK0_504
AD23	VCCO_PSDDR_504	PS_DDR_CK_N0_504
AF24	VCCO_PSDDR_504	PS_DDR_CKE0_504
P23	VCCO_PSDDR_504	
T24	VCCO_PSDDR_504	
V25	VCCO_PSDDR_504	PS_DDR_CK1_504
Y26	VCCO_PSDDR_504	PS_DDR_CK_N1_504
	VCCO_PSDDR_504	PS_DDR_CKE1_504
U16	VCC_PSDDR_PLL	PS_DDR_A0_504
U18	VCC_PSDDR_PLL	PS_DDR_A1_504
	VCC_PSDDR_PLL	PS_DDR_A2_504
	VCC_PSDDR_PLL	PS_DDR_A3_504
	VCC_PSDDR_PLL	PS_DDR_A4_504
	VCC_PSDDR_PLL	PS_DDR_A5_504
AA20	VCC_PSINTFP_DDR	PS_DDR_A6_504
AA21	VCC_PSINTFP_DDR	PS_DDR_A7_504
Y19	VCC_PSINTFP_DDR	PS_DDR_A8_504
		PS_DDR_A9_504
		PS_DDR_A10_504
		PS_DDR_A11_504
		PS_DDR_A12_504
		PS_DDR_A13_504
		PS_DDR_A14_504
		PS_DDR_A15_504
		PS_DDR_A16_504
		PS_DDR_A17_504
	PS_DDR_CS_N0_504	
	PS_DDR_CS_N1_504	
	PS_DDR_BA0_504	
	PS_DDR_BA1_504	
	PS_DDR_BG0_504	
	PS_DDR_BG1_504	
	PS_DDR_PARITY_504	
	PS_DDR_RAM_RST_N_504	
	PS_DDR_ACT_N_504	
	PS_DDR_ALERT_N_504	
	PS_DDR_ZQ_504	
	PS_DDR_ODT0_504	
	PS_DDR_ODT1_504	


XCZU3EG-1SFVC784E

W25	DDR4-CLK0_P	
W26	DDR4-CLK0_N	
V28	DDR4-CKE0	
Y24		X
Y25		X
V27		X
W28	DDR4-A0	
Y28	DDR4-A1	
AB28	DDR4-A2	
AA28	DDR4-A3	
Y27	DDR4-A4	
AA27	DDR4-A5	
Y22	DDR4-A6	
AA23	DDR4-A7	
AA22	DDR4-A8	
AB23	DDR4-A9	
AA25	DDR4-A10	
AA26	DDR4-A11	
AB25	DDR4-A12	
AB26	DDR4-A13	
AB24	DDR4-A14	
AC24	DDR4-A15	
AC23	DDR4-A16	
AC22	DDR4-A17	
W27	DDR4-CS	
V26		X
V23	DDR4-BA0	
W22	DDR4-BA1	
W24	DDR4-BG0	
V22		X
V24	DDR4-PAR	
U23	DDR4-RESET	
Y23	DDR4-ACT	
U25	DDR4-ALERT	
U24		
U28	DDR4-ODT0	
U26		X

U1J
BANK 504 PSDDR

DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504
DQ2	AF20	PS_DDR_DQ2_504	PS_DDR_DQ34_504
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504
DQ11	AD22	PS_DDR_DQ11_504	PS_DDR_DQ43_504
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504
DQ17	AH26	PS_DDR_DQ17_504	PS_DDR_DQ49_504
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504
		PS_DDR_DQ64_504	
		PS_DDR_DQ65_504	
		PS_DDR_DQ66_504	
		PS_DDR_DQ67_504	
		PS_DDR_DQ68_504	
		PS_DDR_DQ69_504	
		PS_DDR_DQ70_504	
		PS_DDR_DQ71_504	
		PS_DDR_DQ72_504	
		PS_DDR_DQ73_504	
		PS_DDR_DQ74_504	
		PS_DDR_DQ75_504	
		PS_DDR_DQ76_504	
		PS_DDR_DQ77_504	
		PS_DDR_DQ78_504	
		PS_DDR_DQ79_504	
		PS_DDR_DQ80_504	
		PS_DDR_DQ81_504	
		PS_DDR_DQ82_504	
		PS_DDR_DQ83_504	
		PS_DDR_DQ84_504	
		PS_DDR_DQ85_504	
		PS_DDR_DQ86_504	
		PS_DDR_DQ87_504	
		PS_DDR_DQ88_504	
		PS_DDR_DQ89_504	
		PS_DDR_DQ90_504	
		PS_DDR_DQ91_504	
		PS_DDR_DQ92_504	
		PS_DDR_DQ93_504	
		PS_DDR_DQ94_504	
		PS_DDR_DQ95_504	
		PS_DDR_DQ96_504	
		PS_DDR_DQ97_504	
		PS_DDR_DQ98_504	
		PS_DDR_DQ99_504	
		PS_DDR_DQ100_504	
		PS_DDR_DQ101_504	
		PS_DDR_DQ102_504	
		PS_DDR_DQ103_504	
		PS_DDR_DQ104_504	
		PS_DDR_DQ105_504	
		PS_DDR_DQ106_504	
		PS_DDR_DQ107_504	
		PS_DDR_DQ108_504	
		PS_DDR_DQ109_504	
		PS_DDR_DQ110_504	
		PS_DDR_DQ111_504	
		PS_DDR_DQ112_504	
		PS_DDR_DQ113_504	
		PS_DDR_DQ114_504	
		PS_DDR_DQ115_504	
		PS_DDR_DQ116_504	
		PS_DDR_DQ117_504	
		PS_DDR_DQ118_504	
		PS_DDR_DQ119_504	
		PS_DDR_DQ120_504	
		PS_DDR_DQ121_504	
		PS_DDR_DQ122_504	
		PS_DDR_DQ123_504	
		PS_DDR_DQ124_504	
		PS_DDR_DQ125_504	
		PS_DDR_DQ126_504	
		PS_DDR_DQ127_504	
		PS_DDR_DQ128_504	
		PS_DDR_DQ129_504	
		PS_DDR_DQ130_504	
		PS_DDR_DQ131_504	
		PS_DDR_DQ132_504	
		PS_DDR_DQ133_504	
		PS_DDR_DQ134_504	
		PS_DDR_DQ135_504	
		PS_DDR_DQ136_504	
		PS_DDR_DQ137_504	
		PS_DDR_DQ138_504	
		PS_DDR_DQ139_504	
		PS_DDR_DQ140_504	
		PS_DDR_DQ141_504	
		PS_DDR_DQ142_504	
		PS_DDR_DQ143_504	
		PS_DDR_DQ144_504	
		PS_DDR_DQ145_504	
		PS_DDR_DQ146_504	
		PS_DDR_DQ147_504	
		PS_DDR_DQ148_504	
		PS_DDR_DQ149_504	
		PS_DDR_DQ150_504	
		PS_DDR_DQ151_504	
		PS_DDR_DQ152_504	
		PS_DDR_DQ153_504	
		PS_DDR_DQ154_504	
		PS_DDR_DQ155_504	
		PS_DDR_DQ156_504	
		PS_DDR_DQ157_504	
		PS_DDR_DQ158_504	
		PS_DDR_DQ159_504	
		PS_DDR_DQ160_504	
		PS_DDR_DQ161_504	
		PS_DDR_DQ162_504	
		PS_DDR_DQ163_504	
		PS_DDR_DQ164_504	
		PS_DDR_DQ165_504	
		PS_DDR_DQ166_504	
		PS_DDR_DQ167_504	
		PS_DDR_DQ168_504	
		PS_DDR_DQ169_504	
		PS_DDR_DQ170_504	
		PS_DDR_DQ171_504	
		PS_DDR_DQ172_504	
		PS_DDR_DQ173_504	
		PS_DDR_DQ174_504	
		PS_DDR_DQ175_504	
		PS_DDR_DQ176_504	
		PS_DDR_DQ177_504	
		PS_DDR_DQ178_504	
		PS_DDR_DQ179_504	
		PS_DDR_DQ180_504	
		PS_DDR_DQ181_504	
		PS_DDR_DQ182_504	
		PS_DDR_DQ183_504	
		PS_DDR_DQ184_504	
		PS_DDR_DQ185_504	
		PS_DDR_DQ186_504	
		PS_DDR_DQ187_504	
		PS_DDR_DQ188_504	
		PS_DDR_DQ189_504	
		PS_DDR_DQ190_504	
		PS_DDR_DQ191_504	
		PS_DDR_DQ192_504	
		PS_DDR_DQ193_504	
		PS_DDR_DQ194_504	
		PS_DDR_DQ195_504	
		PS_DDR_DQ196_504	
		PS_DDR_DQ197_504	
		PS_DDR_DQ198_504	
		PS_DDR_DQ199_504	
		PS_DDR_DQ200_504	
		PS_DDR_DQ201_504	
		PS_DDR_DQ202_504	
		PS_DDR_DQ203_504	
		PS_DDR_DQ204_504	
		PS_DDR_DQ205_504	
		PS_DDR_DQ206_504	
		PS_DDR_DQ207_504	
		PS_DDR_DQ208_504	
		PS_DDR_DQ209_504	
		PS_DDR_DQ210_504	
		PS_DDR_DQ211_504	
		PS_DDR_DQ212_504	
		PS_DDR_DQ213_504	
		PS_DDR_DQ214_504	
		PS_DDR_DQ215_504	
		PS_DDR_DQ216_504	
		PS_DDR_DQ217_504	
		PS_DDR_DQ218_504	
		PS_DDR_DQ219_504	
		PS_DDR_DQ220_504	
		PS_DDR_DQ221_504	
		PS_DDR_DQ222_504	
		PS_DDR_DQ223_504	
		PS_DDR_DQ224_504	
		PS_DDR_DQ225_504	
		PS_DDR_DQ226_504	
		PS_DDR_DQ227_504	
		PS_DDR_DQ228_504	
		PS_DDR_DQ229_504	
		PS_DDR_DQ230_504	
		PS_DDR_DQ231_504	
		PS_DDR_DQ232_504	
		PS_DDR_DQ233_504	
		PS_DDR_DQ234_504	
		PS_DDR_DQ235_504	
		PS_DDR_DQ236_504	
		PS_DDR_DQ237_504	
		PS_DDR_DQ238_504	
		PS_DDR_DQ239_504	
		PS_DDR_DQ240_504	
		PS_DDR_DQ241_504	
		PS_DDR_DQ242_504	
		PS_DDR_DQ243_504	
		PS_DDR_DQ244_504	
		PS_DDR_DQ245_504	
		PS_DDR_DQ246_504	
		PS_DDR_DQ247_504	
		PS_DDR_DQ248_504	
		PS_DDR_DQ249_504	
		PS_DDR_DQ250_504	
		PS_DDR_DQ251_504	
		PS_DDR_DQ252_504	
		PS_DDR_DQ253_504	
		PS_DDR_DQ254_504	
		PS_DDR_DQ255_504	
		PS_DDR_DQ256_504	
		PS_DDR_DQ257_504	
		PS_DDR_DQ258_504	
		PS_DDR_DQ259_504	
		PS_DDR_DQ260_504	
		PS_DDR_DQ261_504	
		PS_DDR_DQ262_504	
		PS_DDR_DQ263_504	
		PS_DDR_DQ264_504	
		PS_DDR_DQ265_504	
		PS_DDR_DQ266_504	
		PS_DDR_DQ267_504	
		PS_DDR_DQ268_504	
		PS_DDR_DQ269_504	
		PS_DDR_DQ270_504	
		PS_DDR_DQ271_504	
		PS_DDR_DQ272_504	
		PS_DDR_DQ273_504	
		PS_DDR_DQ274_504	
		PS_DDR_DQ275_504	
		PS_DDR_DQ276_504	
		PS_DDR_DQ277_504	
		PS_DDR_DQ278_504	
		PS_DDR_DQ279_504	
		PS_DDR_DQ280_504	
		PS_DDR_DQ281_504	
		PS_DDR_DQ282_504	
		PS_DDR_DQ283_504	
		PS_DDR_DQ284_504	
		PS_DDR_DQ285_504	
		PS_DDR_DQ286_504	
		PS_DDR_DQ287_504	
		PS_DDR_DQ288_504	
		PS_DDR_DQ289_504	
		PS_DDR_DQ290_504	
		PS_DDR_DQ291_504	
		PS_DDR_DQ292_504	
		PS_DDR_DQ293_504	
		PS_DDR_DQ294_504	
		PS_DDR_DQ295_504	
		PS_DDR_DQ296_504	
		PS_DDR_DQ297_504	
		PS_DDR_DQ298_504	
		PS_DDR_DQ299_504	
		PS_DDR_DQ300_504	
		PS_DDR_DQ301_504	
		PS_DDR_DQ302_504	
		PS_DDR_DQ303_504	
		PS_DDR_DQ304_504	
		PS_DDR_DQ305_504	
		PS_DDR_DQ306_504	
		PS_DDR_DQ307_504	
		PS_DDR_DQ308_504	
		PS_DDR_DQ309_504	
		PS_DDR_DQ310_504	
		PS_DDR_DQ311_504	
		PS_DDR_DQ312_504	
		PS_DDR_DQ313_504	



	Title: TE0803 - PS_GT		
	A4	Number: TE0803 03EG-1EA	Rev. 02
	Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page13 of 26
	Filename: B_PS_GT.SchDoc		

1

2

3

4

A

A

B

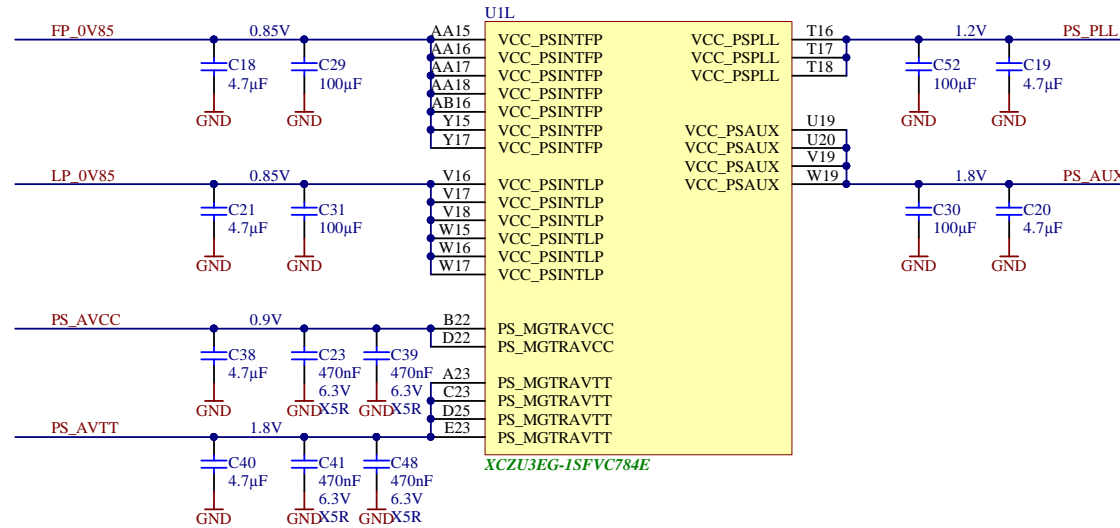
B

C

C

D

D



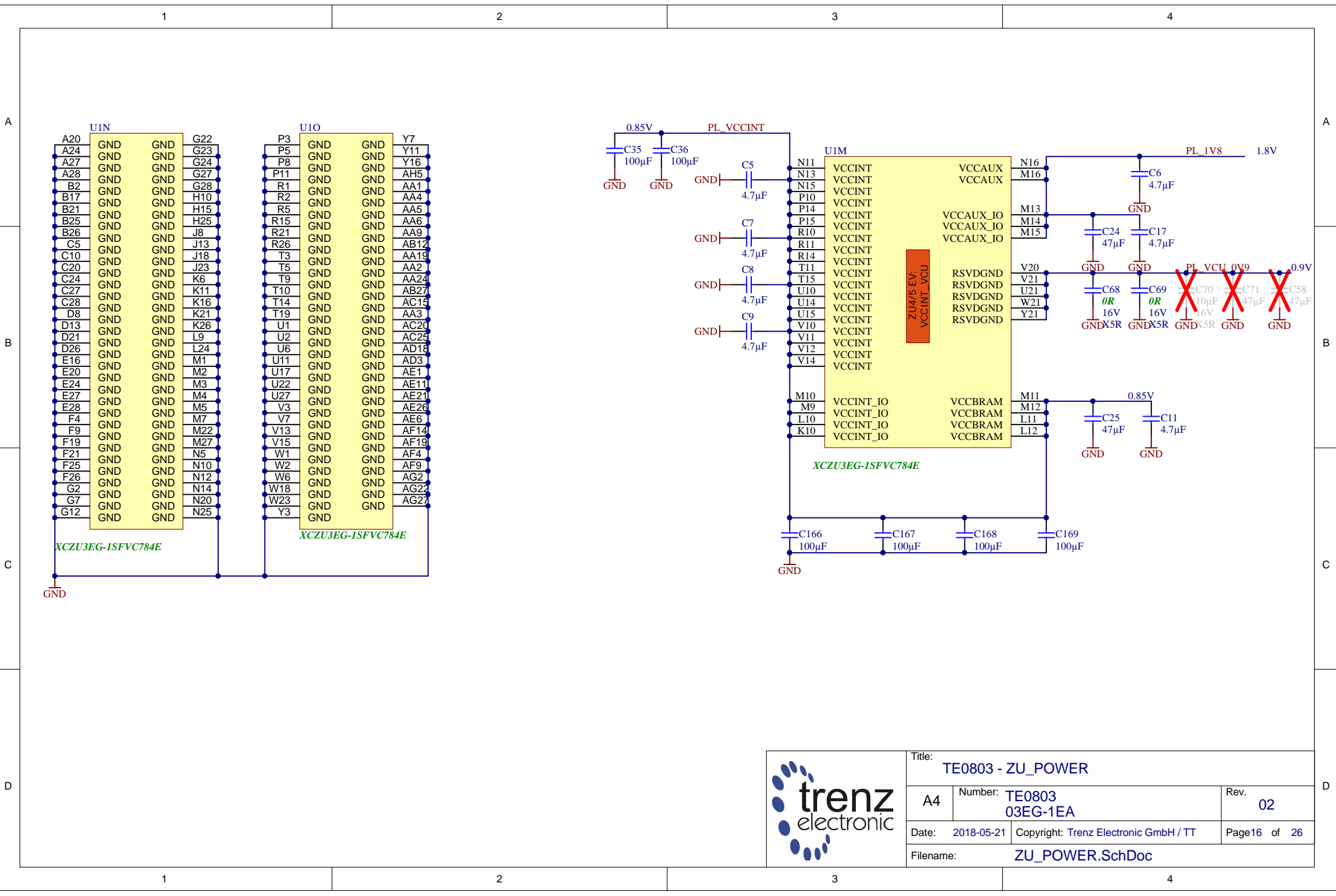
Title: TE0803 - ZU_PS_POWER		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page15 of 26
Filename: ZU_PS_POWER.SchDoc		


1

2

3

4



			Title: TE0803 - ZU_POWER	
			A4	Number: TE0803 03EG-1EA
Date: 2018-05-21		Copyright: Trenz Electronic GmbH / TT		Page 16 of 26
Filename: ZU_POWER.SchDoc				

1

2

3

4

A

A

B

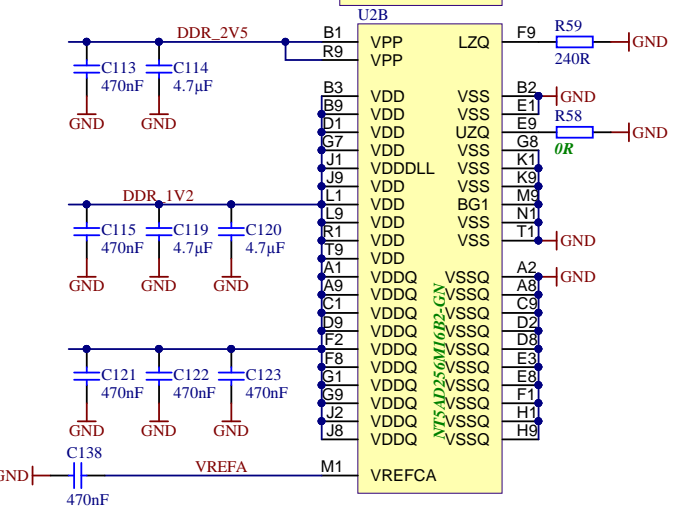
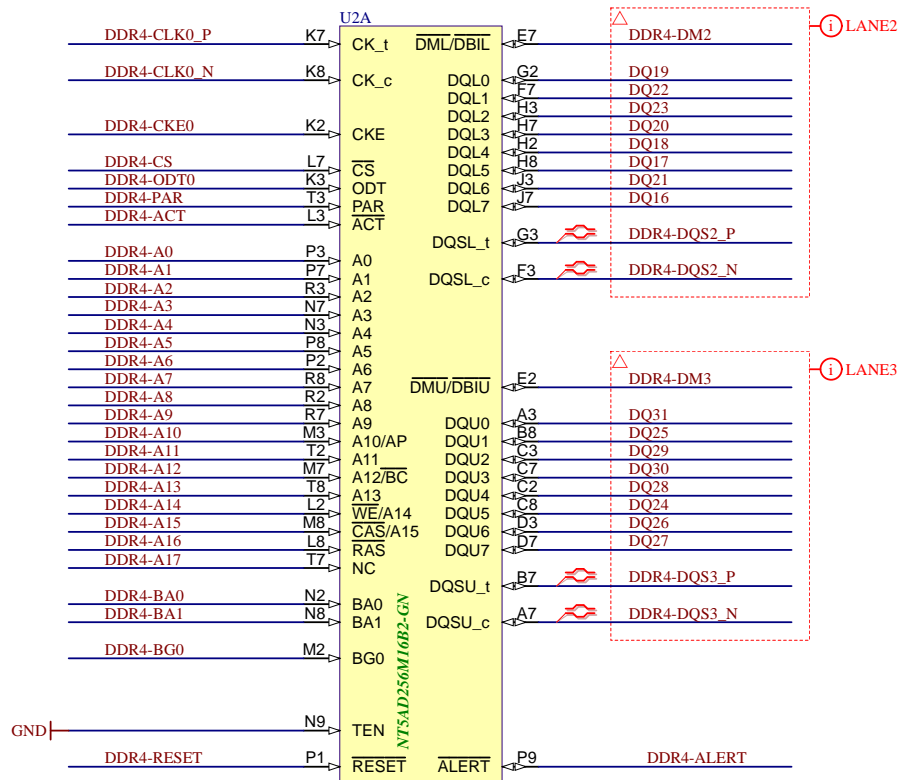
B

C

C

D

D



Title: TE0803 - DDR4_1_RAM		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page 17 of 26
Filename: DDR4-RAM.SchDoc		

1

2

3

4

1

2

3

4

A

A

B

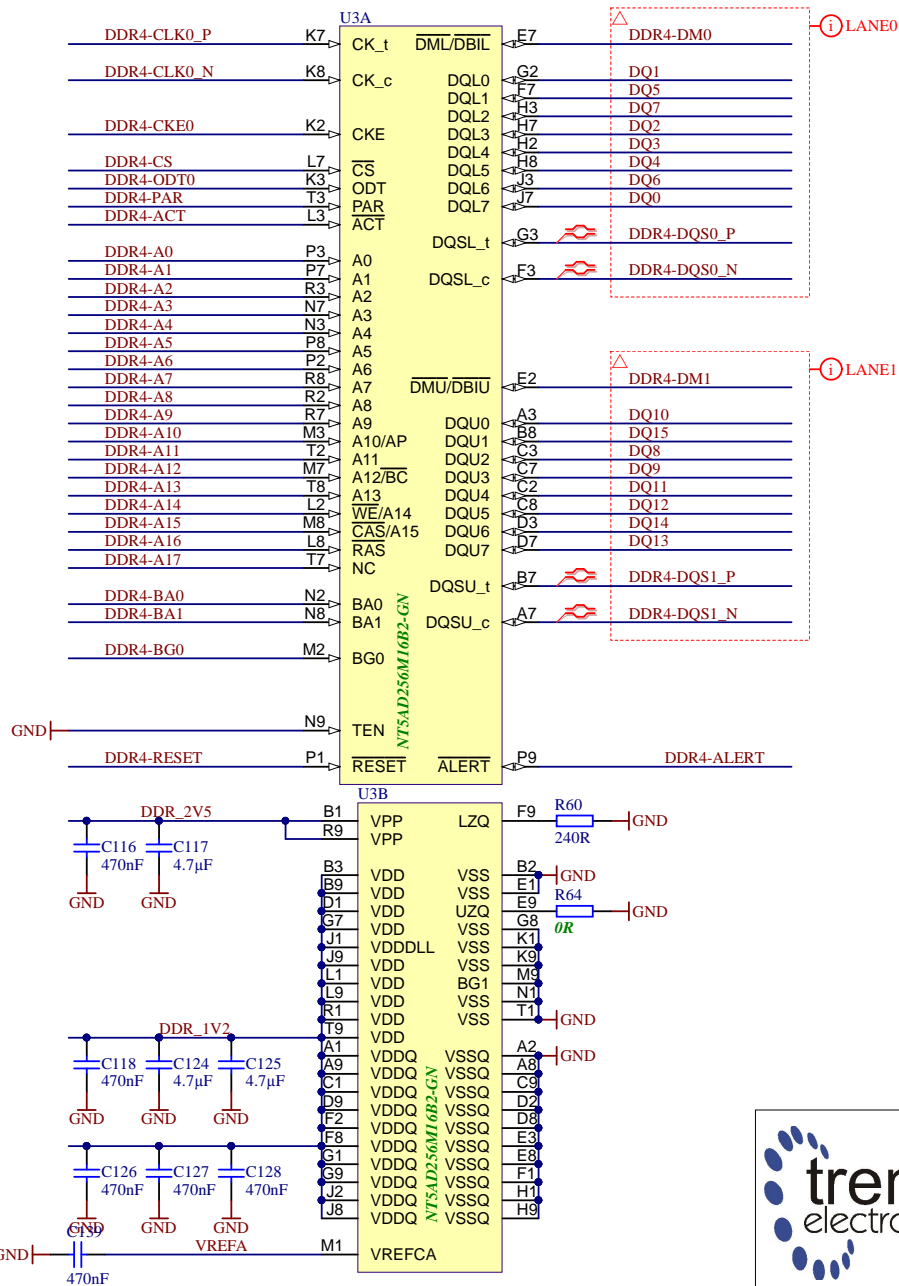

B

C

C

D

D

Title: TE0803 - DDR4_2_RAM		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page18 of 26
Filename: DDR4-RAM_2.SchDoc		

1

2

3

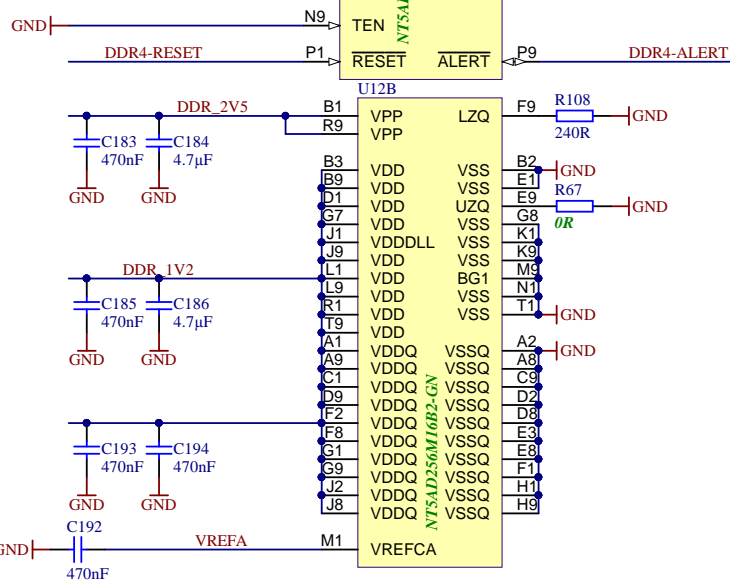
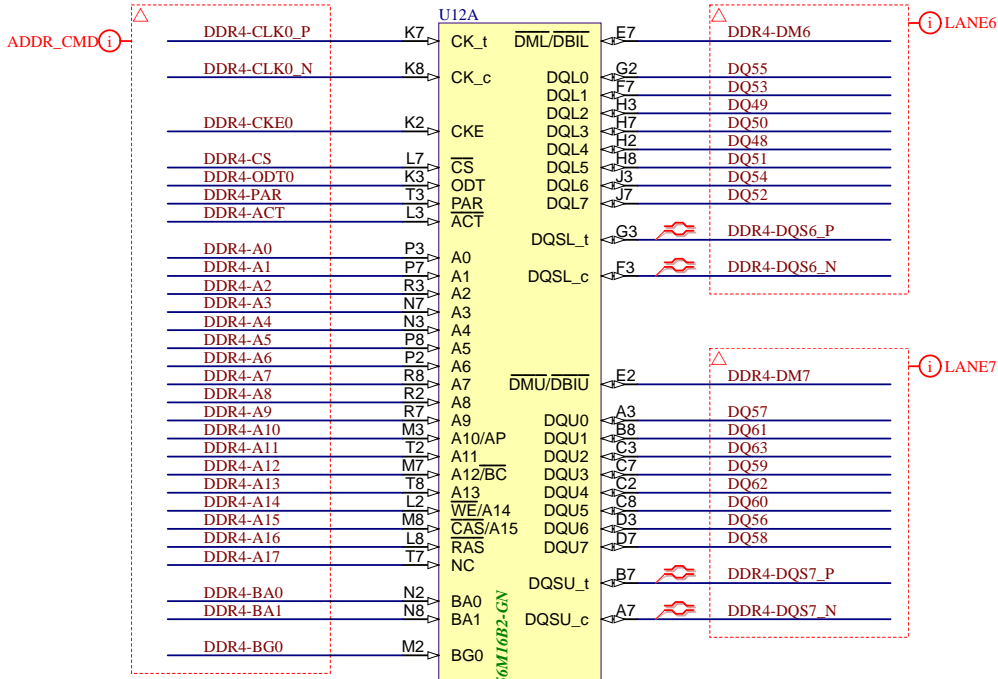
4

1

2

3

4



Title: TE0803 - DDR4_4_RAM		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page20 of 26
Filename: DDR4-RAM_4.SchDoc		

1

2

3

4

A

A

B

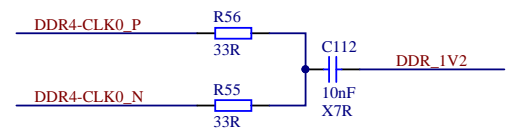
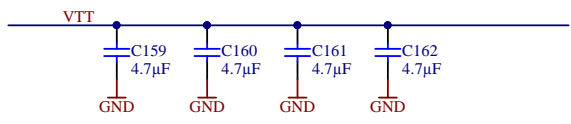
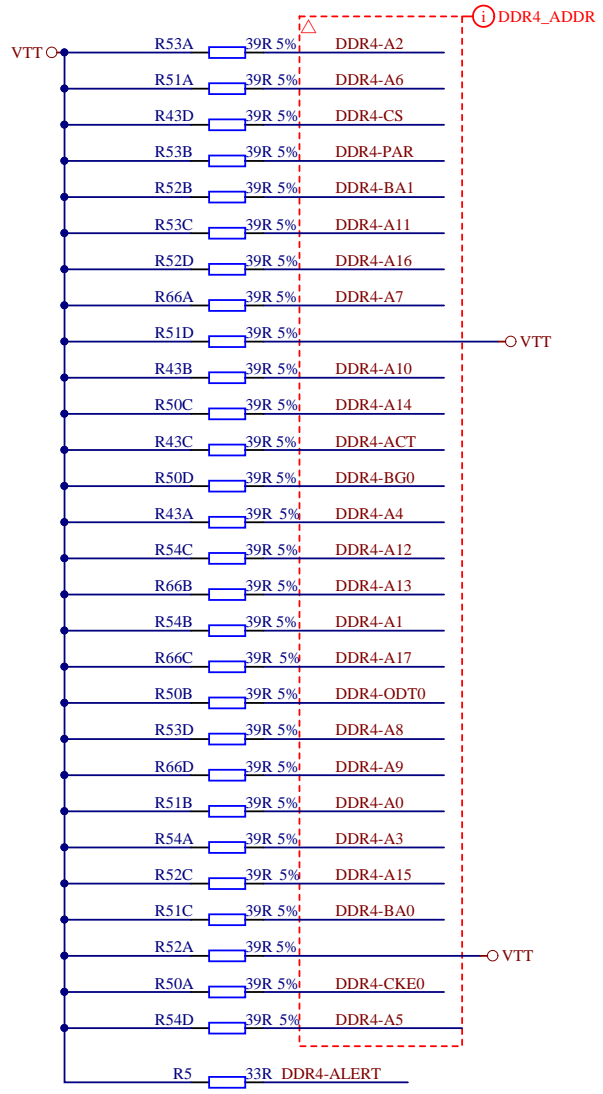
B

C

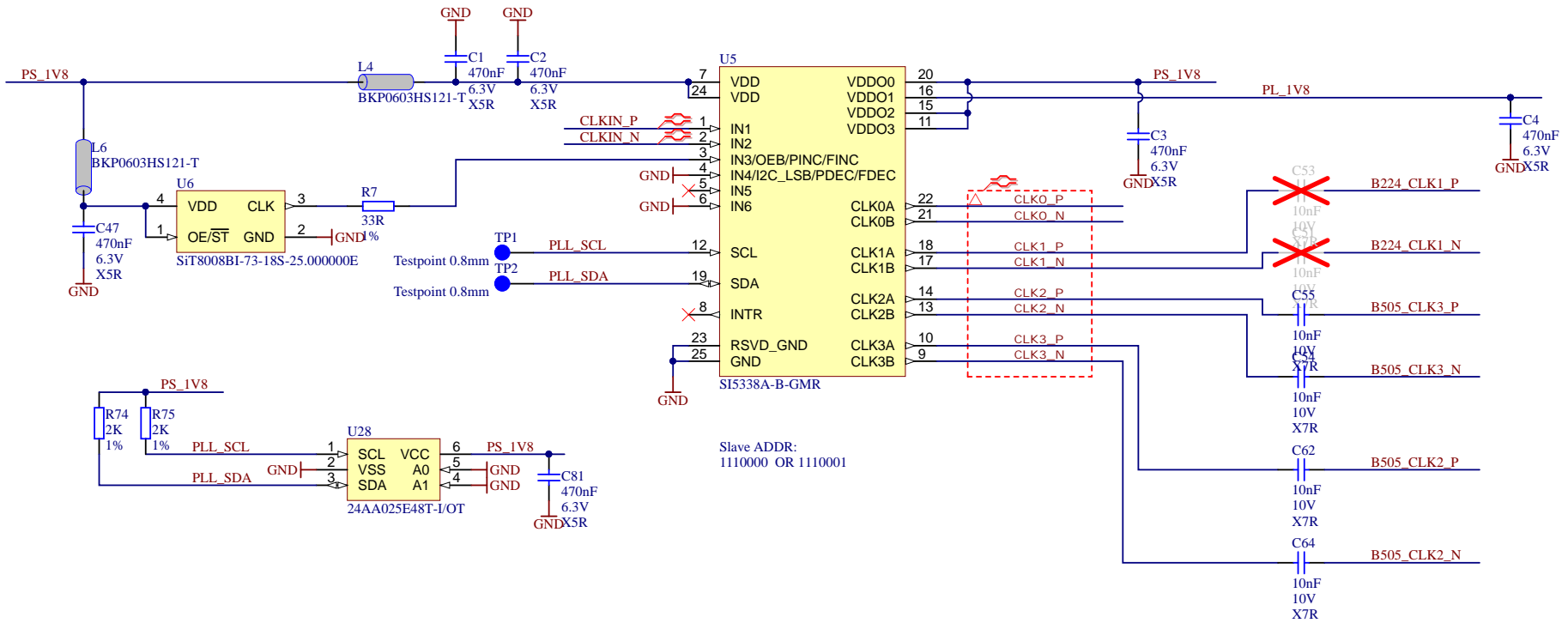
C

D

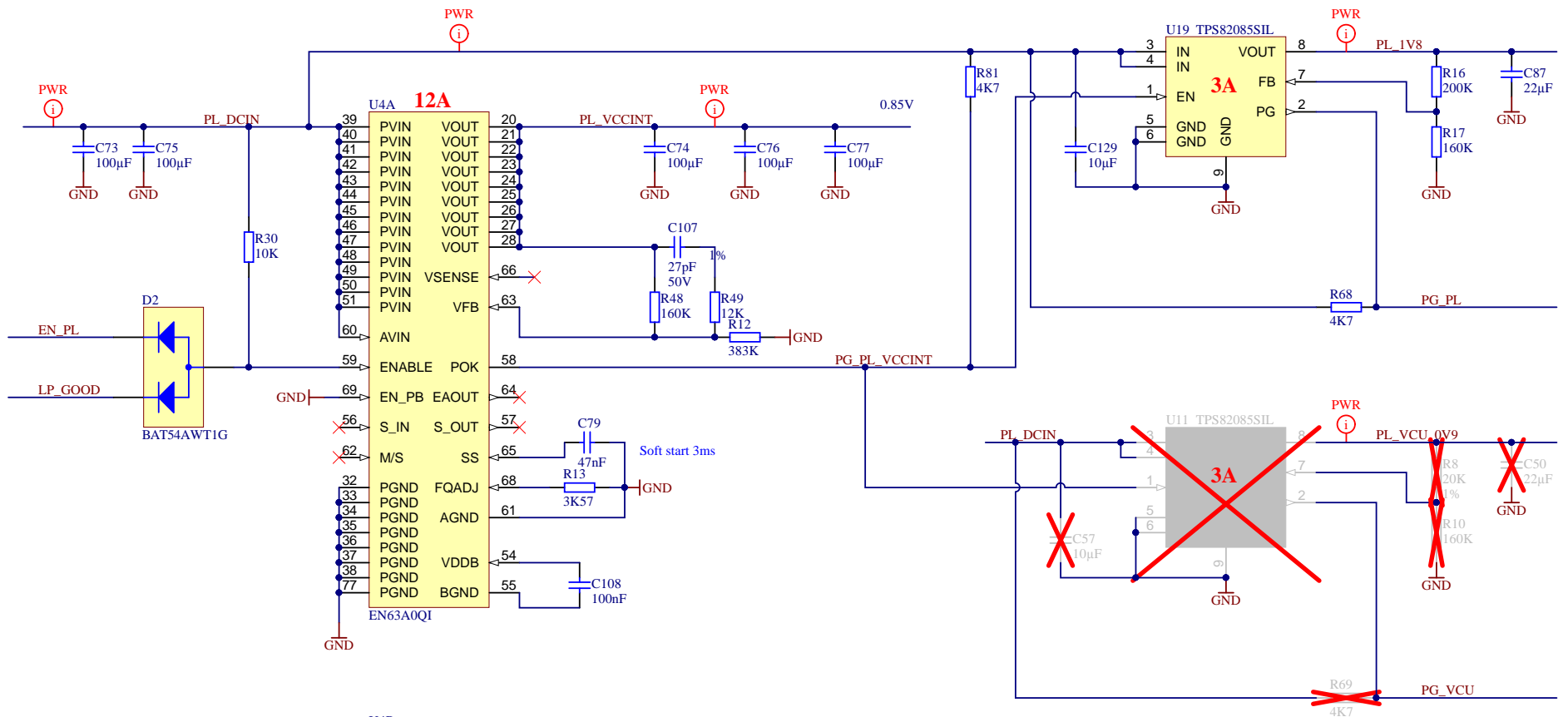
D



Title: TE0803 - DDR4_TERM		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page21 of 26
Filename: DDR4-TERM.SchDoc		



Title: TE0803 - CLOCK		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page22 of 26
Filename: Clock.SchDoc		

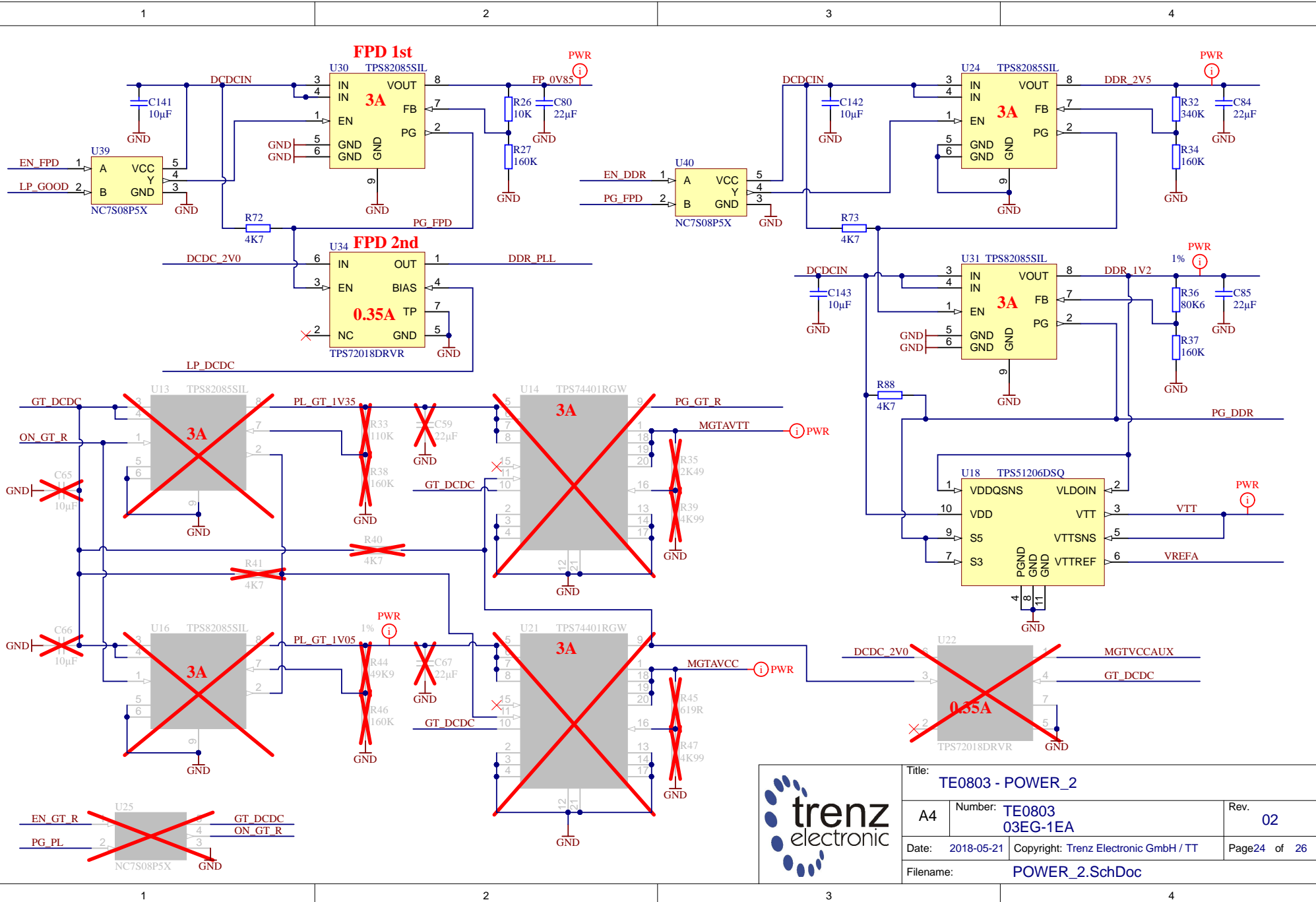


U4B
EN63A0QI

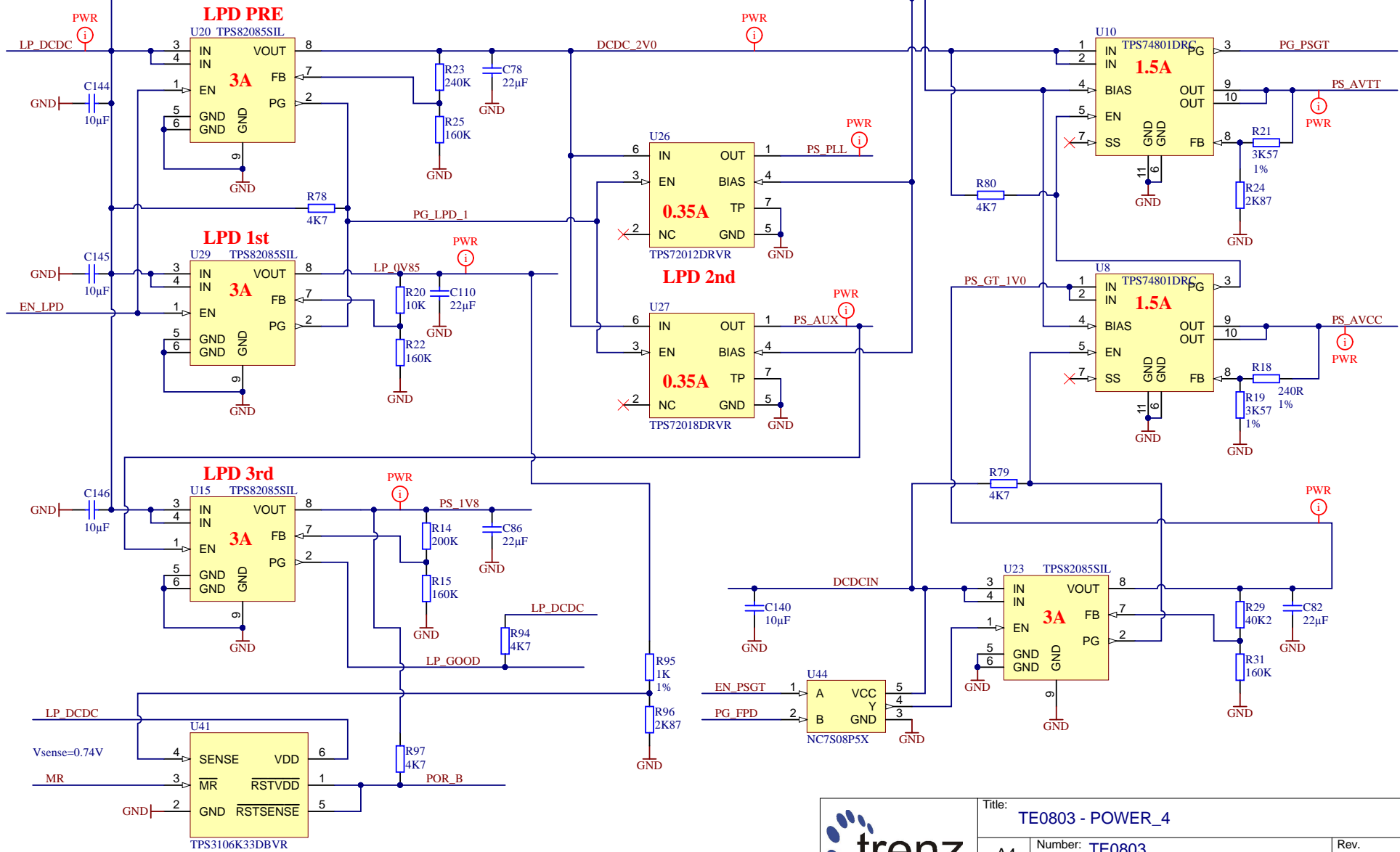
1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC(SW)	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76




Title: TE0803 - POWER		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page23 of 26
Filename: POWER.SchDoc		



Title: TE0803 - POWER_2		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH / TT	Page24 of 26
Filename: POWER_2.SchDoc		



			Title: TE0803 - POWER_4	
			A4	Number: TE0803 03EG-1EA
Date: 2018-05-21		Copyright: Trenz Electronic GmbH / TT		Page25 of 26
Filename: POWER_4.SchDoc				

1

2

3

4

CHANGES REV01a (20.11.2017):

1) VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9.

CHANGES REV02 (20.06.2018):

- 1) Added LDO to DDR_PLL
- 2) All differential pairs wath length matched with tollerance 0.1mm (excluding package delays)
- 3) Added MAC EEPROM U28
- 4) VPS_MGTRAVCC set to 0.85V
- 5) Added pull-up resistors R68,R69

A

A

B

B

C

C

D

D



Title: TE0803 - Changes list		
A4	Number: TE0803 03EG-1EA	Rev. 02
Date: 2018-05-21	Copyright: Trenz Electronic GmbH	Page26 of 26
Filename: Revision_Changes.SchDoc		

1

2

3

4