

1

2

3

4

U_J1
J1.SchDoc

U_J2
J2.SchDoc

U_J3
J3.SchDoc

U_J4
J4.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

U_B64
B64.SchDoc

U_B65
B65.SchDoc

U_B66
B66.SchDoc

U_B_GT
B_GT.SchDoc

U_B_PS_GT
B_PS_GT.SchDoc

U_PS_DDR
PS_DDR.SchDoc

U_B_MIO
B_MIO.SchDoc

U_B_HD
B_HD.SchDoc

U_Clock
Clock.SchDoc

U_CONFIG
CONFIG.SchDoc

U_DDR4-RAM
DDR4-RAM.SchDoc

U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

U_DDR4-RAM_3
DDR4-RAM_3.SchDoc

U_DDR4-RAM_4
DDR4-RAM_4.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

U_ZU_POWER
ZU_POWER.SchDoc

U_ZU_PS_POWER
ZU_PS_POWER.SchDoc

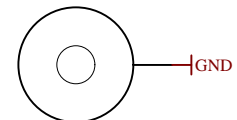
U_POWER
POWER.SchDoc

U_POWER_2
POWER_2.SchDoc

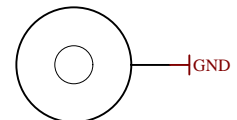
U_POWER_4
POWER_4.SchDoc

U_REV_CH
Revision_Changes.SchDoc

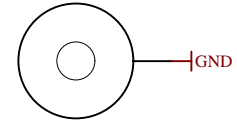
Special notes:



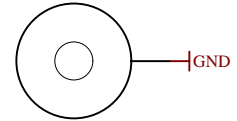
Mount.Hole 3.2mm für Unterlegscheibe



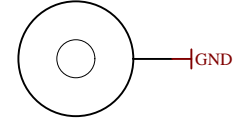
Mount.Hole 3.2mm für Unterlegscheibe



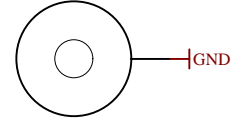
Mount.Hole 3.2mm für Unterlegscheibe



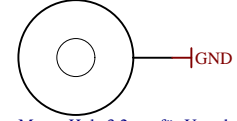
Mount.Hole 3.2mm für Unterlegscheibe



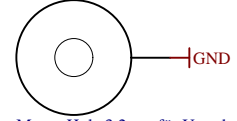
Mount.Hole 3.2mm für Unterlegscheibe



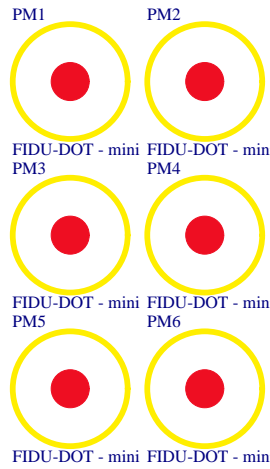
Mount.Hole 3.2mm für Unterlegscheibe



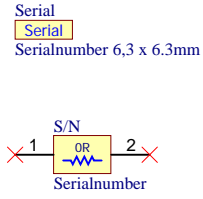
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



LOGO1
TE Logo PRINT Layer
LOGO PRINT



Assembly variant	2BE13-A
Created by	VY
Modified by	VY
Modified at	2021-06-24
SVN Revision	9226



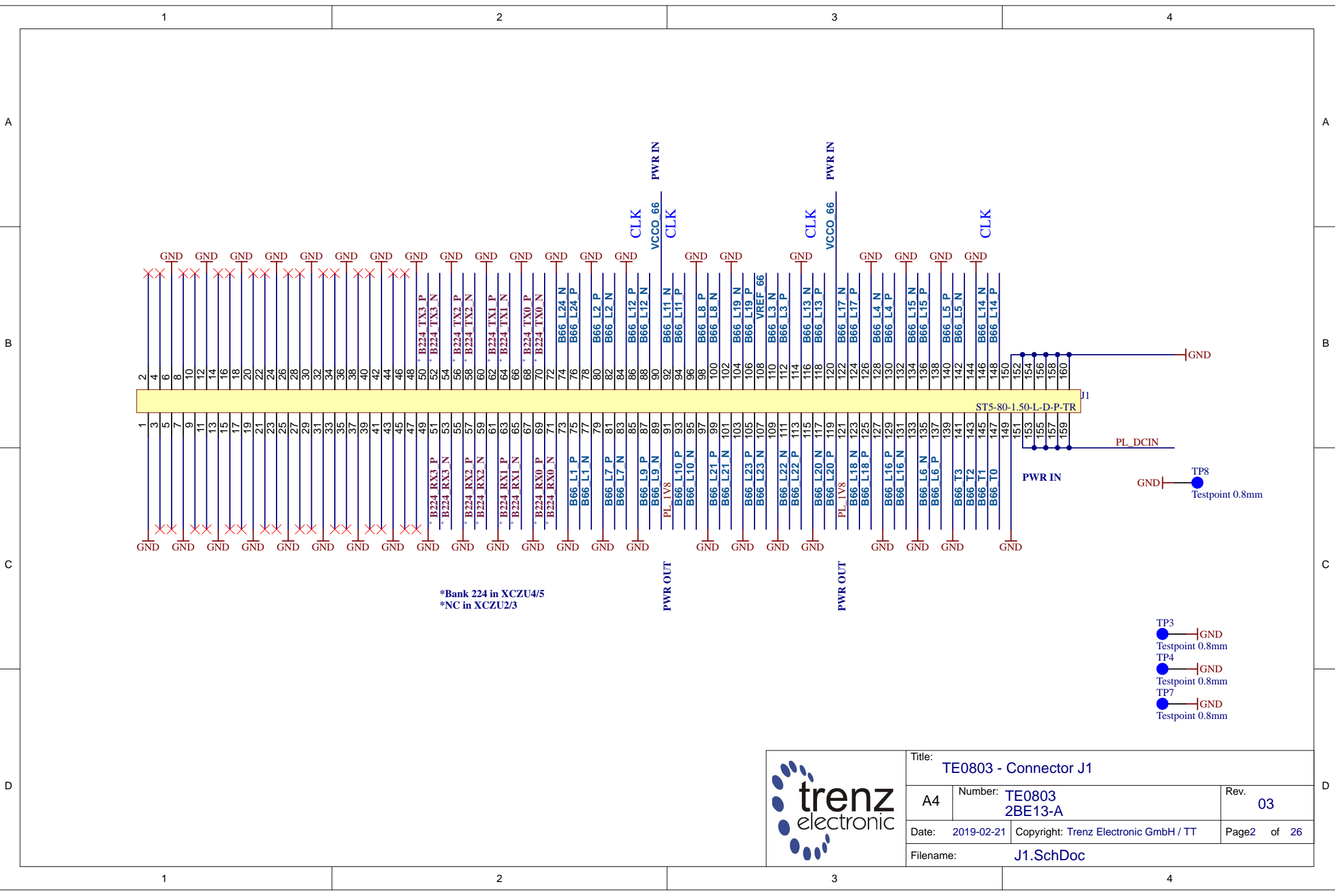
Title: TE0803		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page1 of 26
Filename: TE0803.SchDoc		

1

2

3

4



*Bank 224 in XCZU4/5
 *NC in XCZU2/3

TP3 — GND
 Testpoint 0.8mm
 TP4 — GND
 Testpoint 0.8mm
 TP7 — GND
 Testpoint 0.8mm
 TP8 — GND
 Testpoint 0.8mm



Title: TE0803 - Connector J1		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page2 of 26
Filename: J1.SchDoc		

1

2

3

4

A

A

B

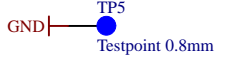
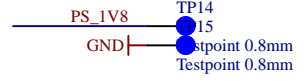
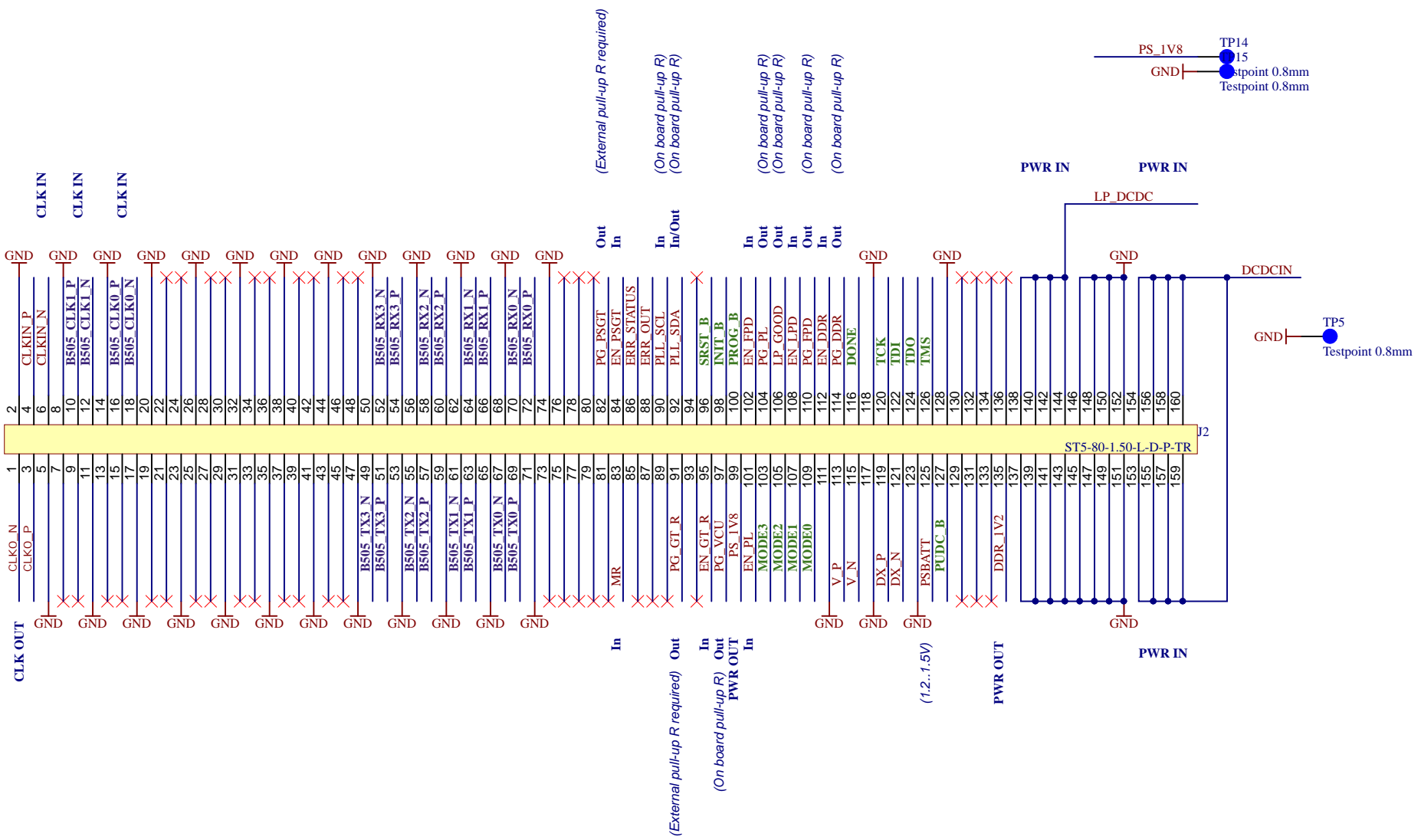
B


C

C

D

D



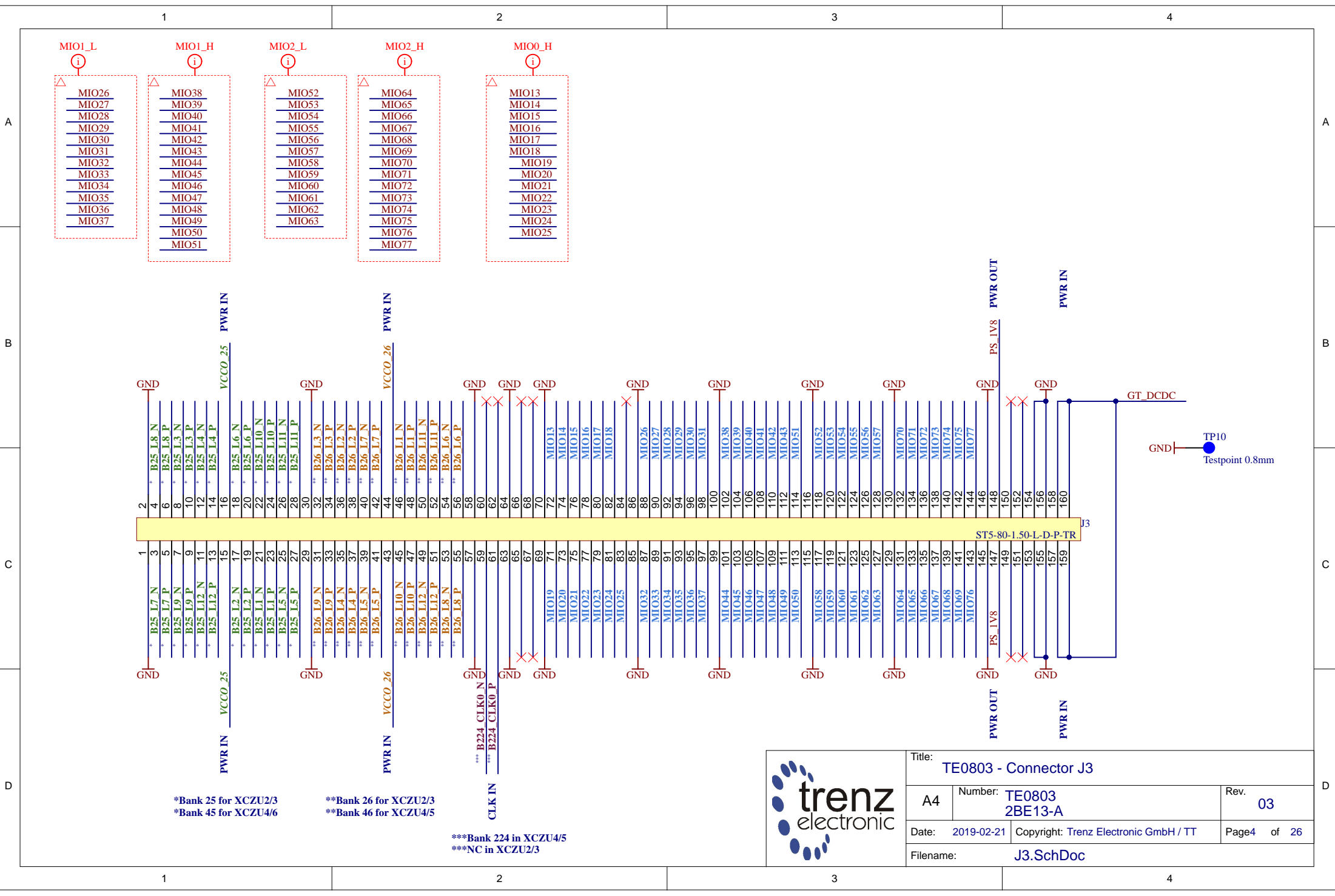
			Title: TE0803 - Connector J2	
			A4	Number: TE0803 2BE13-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT		Page3 of 26
Filename: J2.SchDoc				

1

2

3

4



*Bank 25 for XCZU2/3
*Bank 45 for XCZU4/6

**Bank 26 for XCZU2/3
**Bank 46 for XCZU4/5

***Bank 224 in XCZU4/5
***NC in XCZU2/3



Title: TE0803 - Connector J3		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page4 of 26
Filename: J3.SchDoc		

1

2

3

4

A

A

B

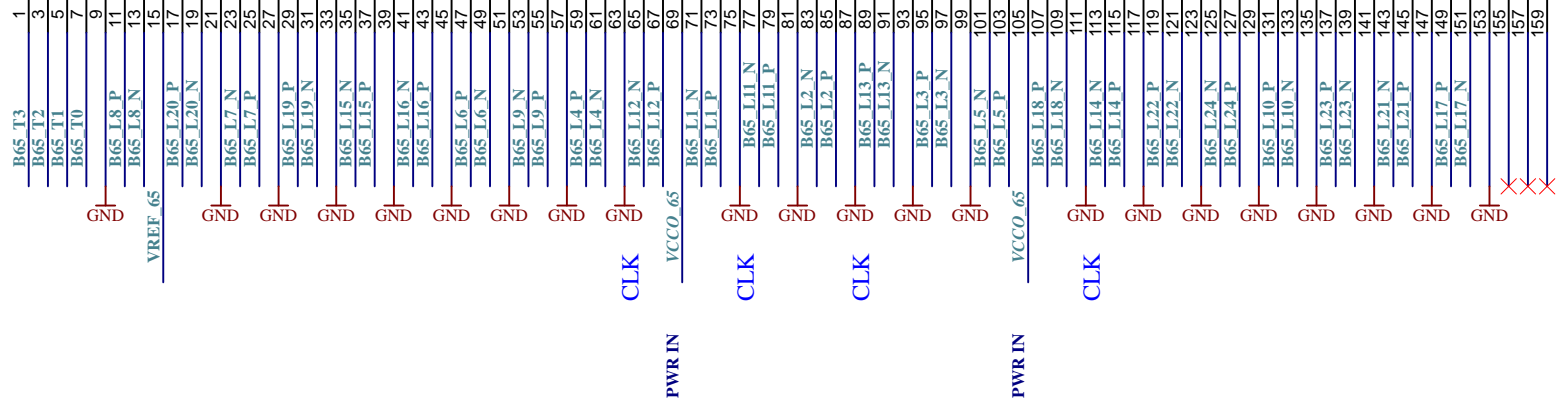
B

C

C

D

D




1

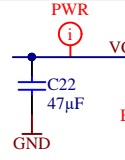
2

3

4

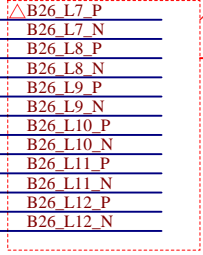


Title: TE0803 - Connector J4		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page5 of 26
Filename: J4.SchDoc		



U1C XCZU2EG-1SFVC784E
BANK 26 HD (ZU4/5 BANK 46 HD)

F14	VCCO_26	B15	IO_L1P_AD11P_26	IO_L7P_HDGC_AD5P_26	G13	B26 L7 P
C15	VCCO_26	A15	IO_L1N_AD11N_26	IO_L7N_HDGC_AD5N_26	F13	B26 L7 N
		B14	IO_L2P_AD10P_26	IO_L8P_HDGC_AD4P_26	F15	B26 L8 P
		A14	IO_L2N_AD10N_26	IO_L8N_HDGC_AD4N_26	E15	B26 L8 N
		B13	IO_L3P_AD9P_26	IO_L9P_AD3P_26	G15	B26 L9 P
		A13	IO_L3N_AD9N_26	IO_L9N_AD3N_26	G14	B26 L9 N
		C14	IO_L4P_AD8P_26	IO_L10P_AD2P_26	H14	B26 L10 P
		C13	IO_L4N_AD8N_26	IO_L10N_AD2N_26	H13	B26 L10 N
		D15	IO_L5P_HDGC_AD7P_26	IO_L11P_AD1P_26	K14	B26 L11 P
		D14	IO_L5N_HDGC_AD7N_26	IO_L11N_AD1N_26	J14	B26 L11 N
		E14	IO_L6P_HDGC_AD6P_26	IO_L12P_AD0P_26	L14	B26 L12 P
		E13	IO_L6N_HDGC_AD6N_26	IO_L12N_AD0N_26	L13	B26 L12 N

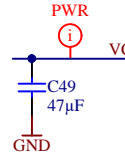


BANK 44 HD (ZU4/5 BANK 43 HD)

AC10	VCCO_44	AG12	VCCO_44	AD11	AD10
AG10	IO_L1P_AD11P_44	AH10	IO_L1N_AD11N_44	AB11	AC11
AF11	IO_L2P_AD10P_44	AH12	IO_L2N_AD10N_44	AA11	AA10
AG11	IO_L2N_AD10N_44	AH11	IO_L3P_AD9P_44	W10	Y10
AH12	IO_L3N_AD9N_44	AE10	IO_L4P_AD8P_44	Y10	Y9
AH11	IO_L3N_AD9N_44	AF10	IO_L4N_AD8N_44	Y9	AA8
AE10	IO_L4P_AD8P_44	AE12	IO_L5P_HDGC_AD7P_44	AB10	AB9
AF10	IO_L4N_AD8N_44	AF12	IO_L5N_HDGC_AD7N_44	AB10	AB9
AE12	IO_L5P_HDGC_AD7P_44	AC13	IO_L6P_HDGC_AD6P_44	AB9	AB9
AF12	IO_L5N_HDGC_AD7N_44	AD12	IO_L6N_HDGC_AD6N_44	AB9	AB9
AC13	IO_L6P_HDGC_AD6P_44				
AD12	IO_L6N_HDGC_AD6N_44				

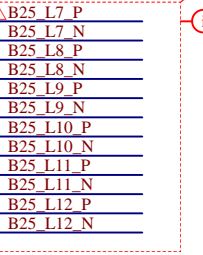
U1B XCZU2EG-1SFVC784E
BANK 24 HD (ZU4/5 BANK 44 HD)

AA14	VCCO_24	AD13	VCCO_24	AA13	AB13
AE15	IO_L1P_AD15P_24	AG14	IO_L1N_AD15N_24	AB15	AB15
AE14	IO_L1N_AD15N_24	AH11	IO_L2P_AD14P_24	AB14	AB14
AG14	IO_L2P_AD14P_24	AG13	IO_L2N_AD14N_24	W14	W13
AH11	IO_L2N_AD14N_24	AH13	IO_L3P_AD13P_24	W13	W13
AG13	IO_L3P_AD13P_24	AE13	IO_L3N_AD13N_24	Y14	Y14
AH13	IO_L3N_AD13N_24	AF13	IO_L4P_AD12P_24	Y13	Y13
AE13	IO_L4P_AD12P_24	AD13	IO_L4N_AD12N_24	W12	W12
AF13	IO_L4N_AD12N_24	AD14	IO_L5P_HDGC_24	W11	W11
AD13	IO_L5P_HDGC_24	AC14	IO_L5N_HDGC_24	Y12	Y12
AD14	IO_L5N_HDGC_24	AC13	IO_L6P_HDGC_24	AA12	AA12
AC14	IO_L6P_HDGC_24				
AC13	IO_L6N_HDGC_24				

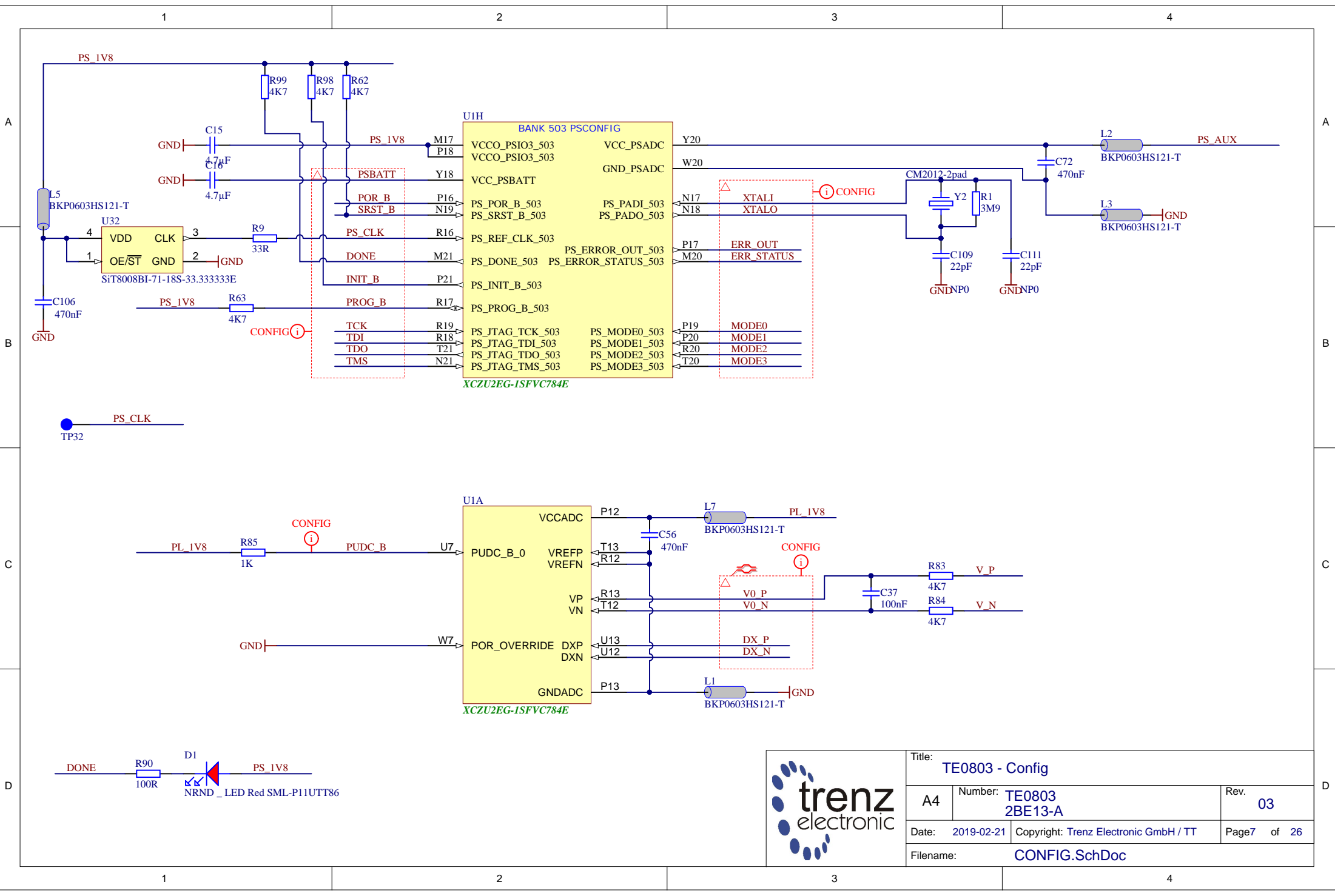


BANK 25 HD (ZU4/5 BANK 45 HD)

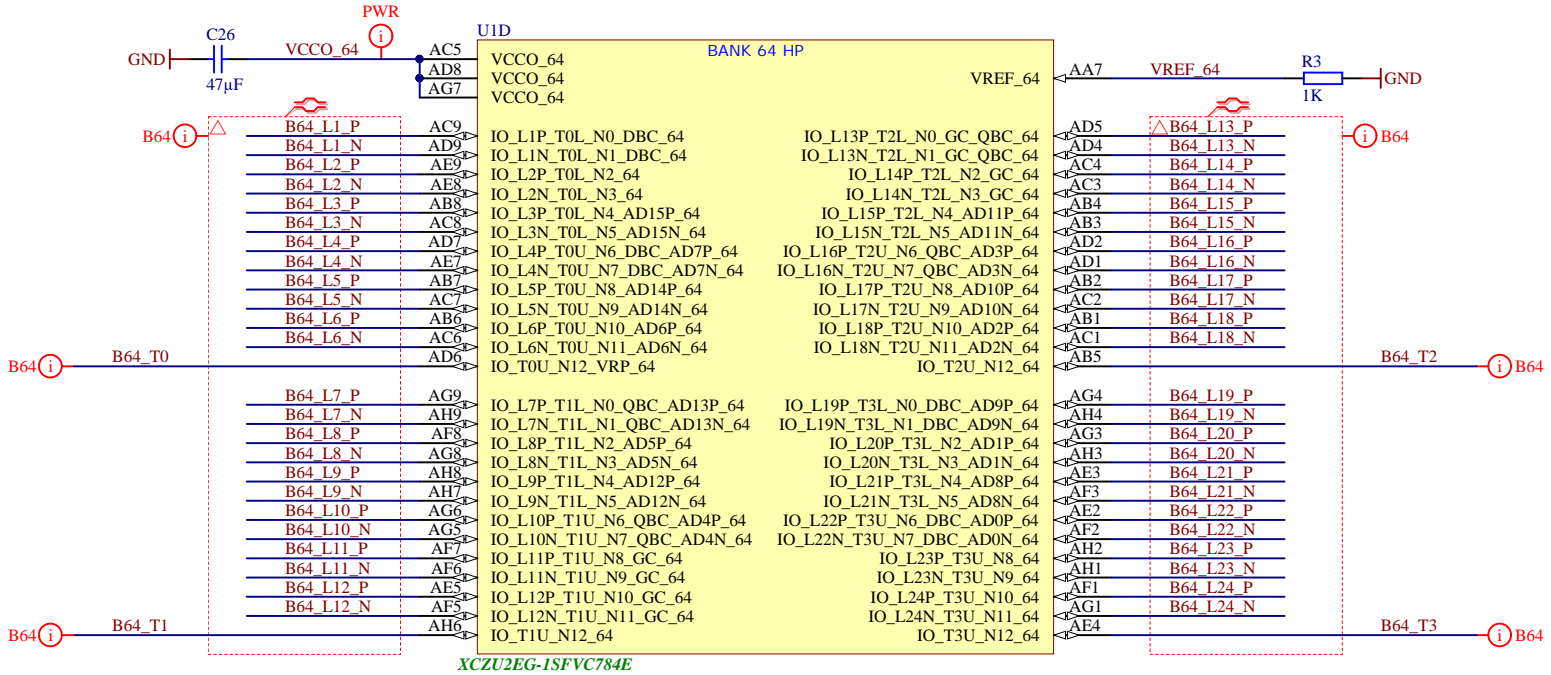
B12	VCCO_25	J11	IO_L1P_AD15P_25	IO_L7P_HDGC_25	E10	B25 L7 P
E11	VCCO_25	J10	IO_L1N_AD15N_25	IO_L7N_HDGC_25	D10	B25 L7 N
		K13	IO_L2P_AD14P_25	IO_L8P_HDGC_25	E12	B25 L8 P
		K12	IO_L2N_AD14N_25	IO_L8N_HDGC_25	D11	B25 L8 N
		H11	IO_L3P_AD13P_25	IO_L9P_AD11P_25	C11	B25 L9 P
		G10	IO_L3N_AD13N_25	IO_L9N_AD11N_25	B10	B25 L9 N
		J12	IO_L4P_AD12P_25	IO_L10P_AD10P_25	B11	B25 L10 P
		H12	IO_L4N_AD12N_25	IO_L10N_AD10N_25	A10	B25 L10 N
		G11	IO_L5P_HDGC_25	IO_L11P_AD9P_25	A12	B25 L11 P
		F11	IO_L5N_HDGC_25	IO_L11N_AD9N_25	A11	B25 L11 N
		F12	IO_L6P_HDGC_25	IO_L12P_AD8P_25	D12	B25 L12 P
		F11	IO_L6N_HDGC_25	IO_L12N_AD8N_25	C12	B25 L12 N



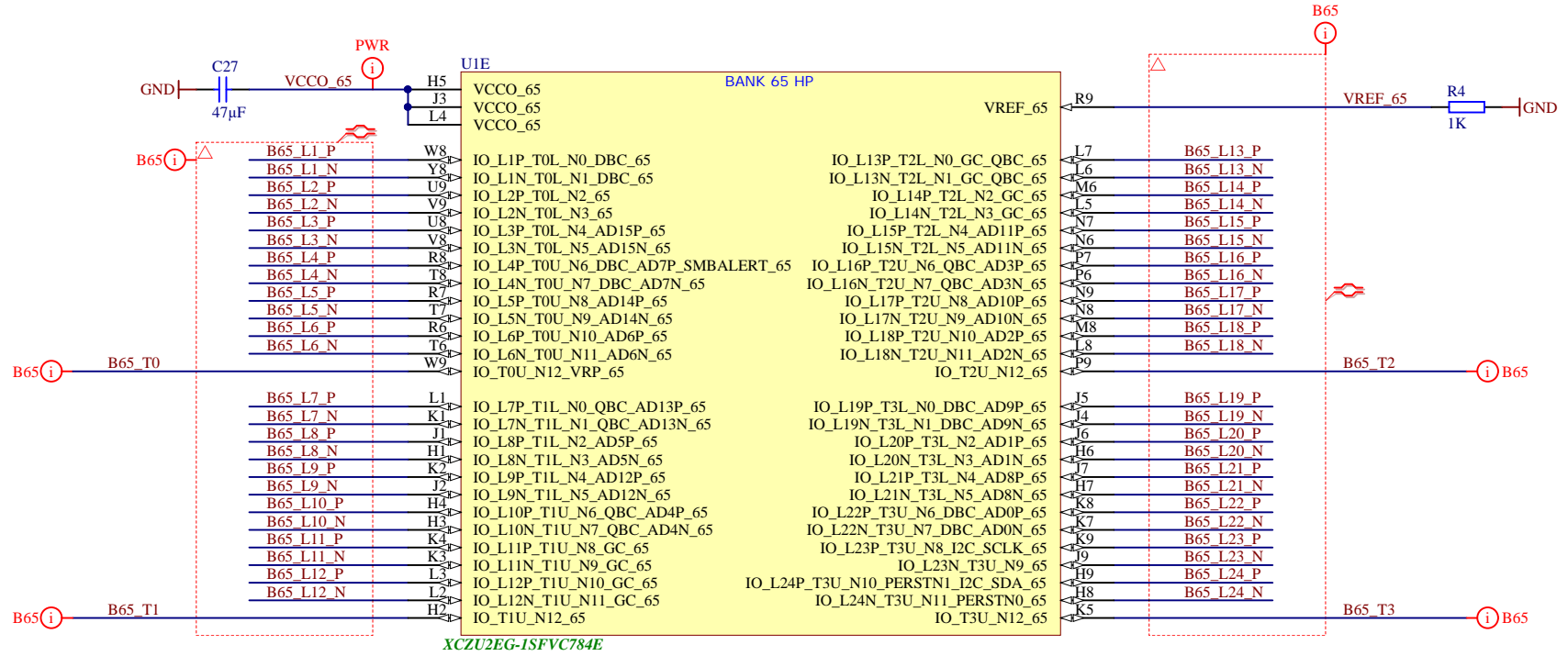
Title: TE0803 - HD Banks			
A4	Number: TE0803 2BE13-A	Rev. 03	
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page6 of 26	
Filename: B_HD.SchDoc			



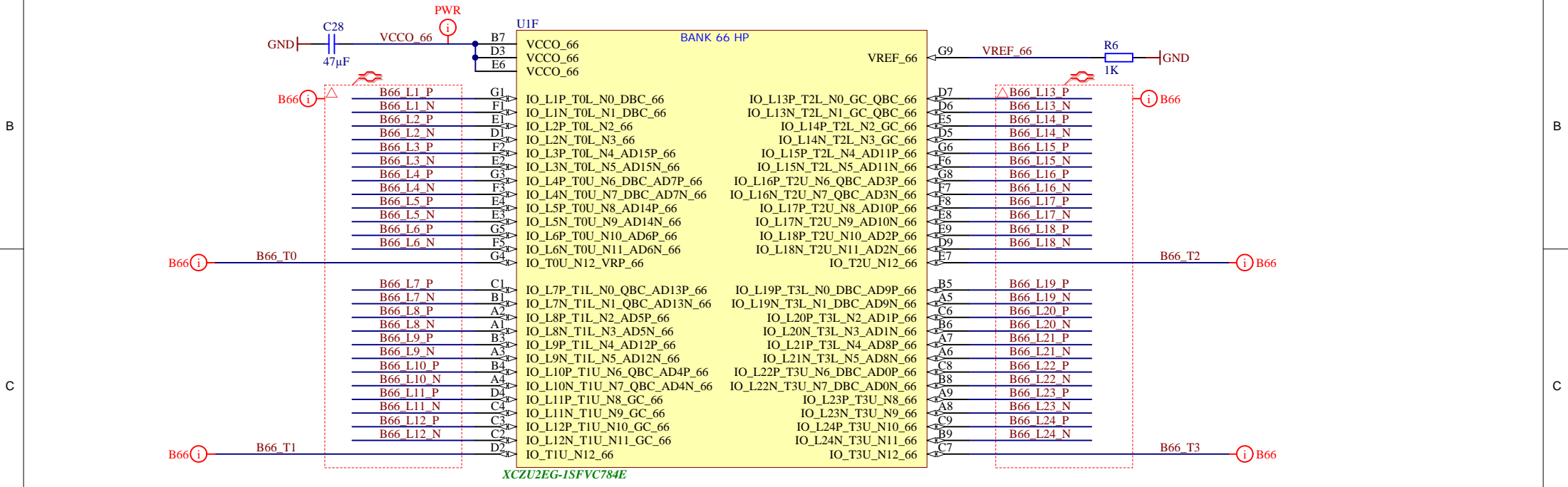
Title: TE0803 - Config		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 7 of 26
Filename: CONFIG.SchDoc		



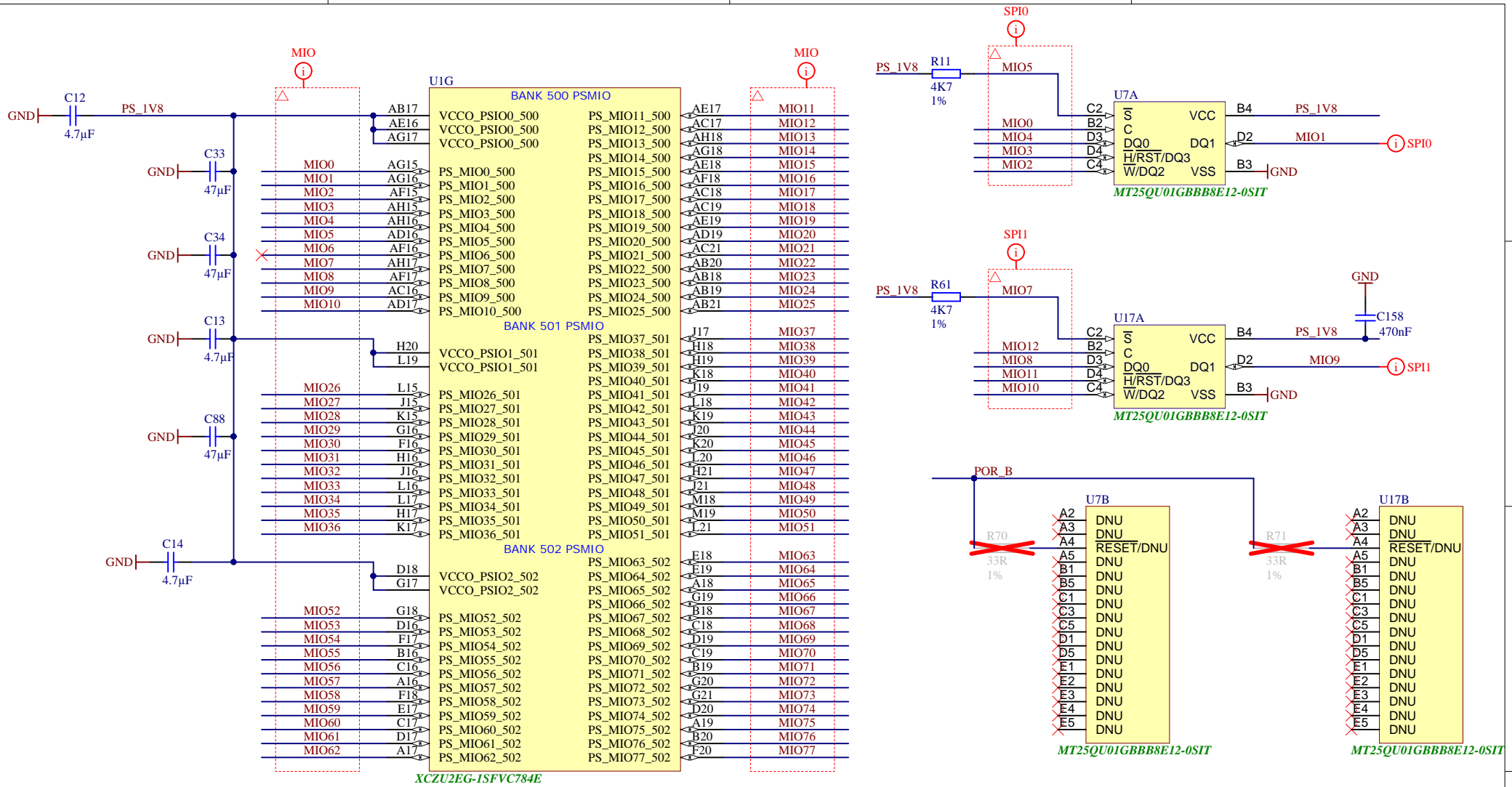
Title: TE0803 - B64		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 8 of 26
Filename: B64.SchDoc		




Title: TE0803 - B65		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 9 of 26
Filename: B65.SchDoc		



	Title: TE0803 - B66		
	A4	Number: TE0803 2BE13-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 10 of 26
	Filename: B66.SchDoc		



			Title: TE0803 - MIO Banks	
			A4	Number: TE0803 2BE13-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT		Page 11 of 26
Filename: B_MIO.SchDoc				

A

B

C

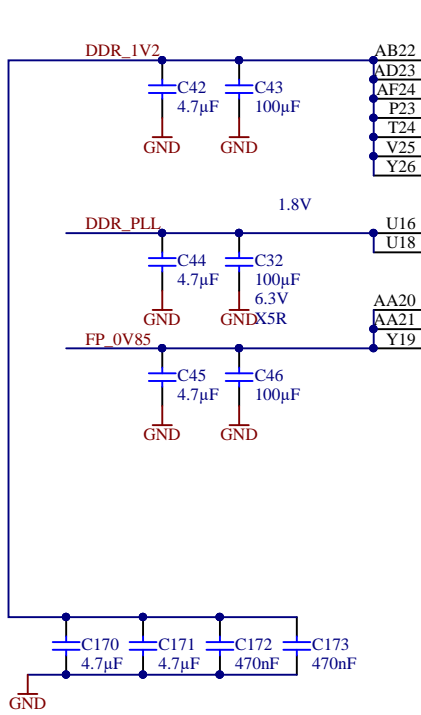
D

A

B

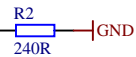
C

D



U1I		BANK 504 PSDDR	
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0 P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0 N
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25	
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27	
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2
VCC_PSDDR_PLL	PS_DDR_A3_504	AA28	DDR4-A3
VCC_PSDDR_PLL	PS_DDR_A4_504	Y27	DDR4-A4
VCC_PSINTFP_DDR	PS_DDR_A5_504	AA27	DDR4-A5
VCC_PSINTFP_DDR	PS_DDR_A6_504	Y22	DDR4-A6
VCC_PSINTFP_DDR	PS_DDR_A7_504	AA23	DDR4-A7
VCC_PSINTFP_DDR	PS_DDR_A8_504	AA22	DDR4-A8
VCC_PSINTFP_DDR	PS_DDR_A9_504	AB23	DDR4-A9
VCC_PSINTFP_DDR	PS_DDR_A10_504	AA25	DDR4-A10
VCC_PSINTFP_DDR	PS_DDR_A11_504	AA26	DDR4-A11
VCC_PSINTFP_DDR	PS_DDR_A12_504	AB25	DDR4-A12
VCC_PSINTFP_DDR	PS_DDR_A13_504	AB26	DDR4-A13
VCC_PSINTFP_DDR	PS_DDR_A14_504	AB24	DDR4-A14
VCC_PSINTFP_DDR	PS_DDR_A15_504	AC24	DDR4-A15
VCC_PSINTFP_DDR	PS_DDR_A16_504	AC23	DDR4-A16
VCC_PSINTFP_DDR	PS_DDR_A17_504	AC22	DDR4-A17
PS_DDR_CS_N0_504	PS_DDR_CS_N1_504	W27	DDR4-CS
PS_DDR_CS_N0_504	PS_DDR_CS_N1_504	V26	
PS_DDR_BA0_504	PS_DDR_BA1_504	V23	DDR4-BA0
PS_DDR_BA0_504	PS_DDR_BA1_504	W22	DDR4-BA1
PS_DDR_BG0_504	PS_DDR_BG1_504	W24	DDR4-BG0
PS_DDR_BG0_504	PS_DDR_BG1_504	V22	DDR4-BG1
PS_DDR_PARITY_504	PS_DDR_RAM_RST_N_504	V24	DDR4-PAR
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504	U23	DDR4-RESET
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504	Y23	DDR4-ACT
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504	U25	DDR4-ALERT
PS_DDR_ZQ_504	PS_DDR_ODT0_504	U24	DDR4-ZQ
PS_DDR_ZQ_504	PS_DDR_ODT1_504	U28	DDR4-ODT0
PS_DDR_ZQ_504	PS_DDR_ODT1_504	U26	

XCZU2EG-1SFVC784E

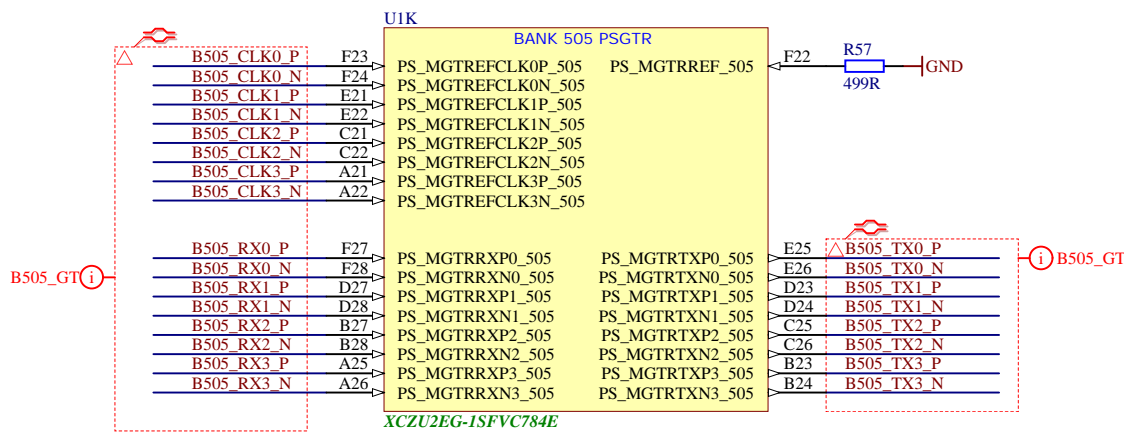



U1J		BANK 504 PSDDR	
DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504
DQ11	AD22	PS_DDR_DQ11_504	PS_DDR_DQ43_504
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504
DDR4-DQS0 P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ64_504
DDR4-DQS0 N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ65_504
DDR4-DQS1 P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ66_504
DDR4-DQS1 N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ67_504
DDR4-DQS2 P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504
DDR4-DQS2 N	AF26	PS_DDR_DQS_N2_504	PS_DDR_DQ69_504
DDR4-DQS3 P	AE27	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504
DDR4-DQS3 N	AF27	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504
DDR4-DQS4 P	N23	PS_DDR_DQS_P4_504	PS_DDR_DM0_504
DDR4-DQS4 N	M23	PS_DDR_DQS_N4_504	PS_DDR_DM1_504
DDR4-DQS5 P	L23	PS_DDR_DQS_P5_504	PS_DDR_DM2_504
DDR4-DQS5 N	K23	PS_DDR_DQS_N5_504	PS_DDR_DM3_504
DDR4-DQS6 P	N26	PS_DDR_DQS_P6_504	PS_DDR_DM4_504
DDR4-DQS6 N	N27	PS_DDR_DQS_N6_504	PS_DDR_DM5_504
DDR4-DQS7 P	J26	PS_DDR_DQS_P7_504	PS_DDR_DM6_504
DDR4-DQS7 N	J27	PS_DDR_DQS_N7_504	PS_DDR_DM7_504
	R27	PS_DDR_DQS_P8_504	PS_DDR_DM8_504
	T27	PS_DDR_DQS_N8_504	

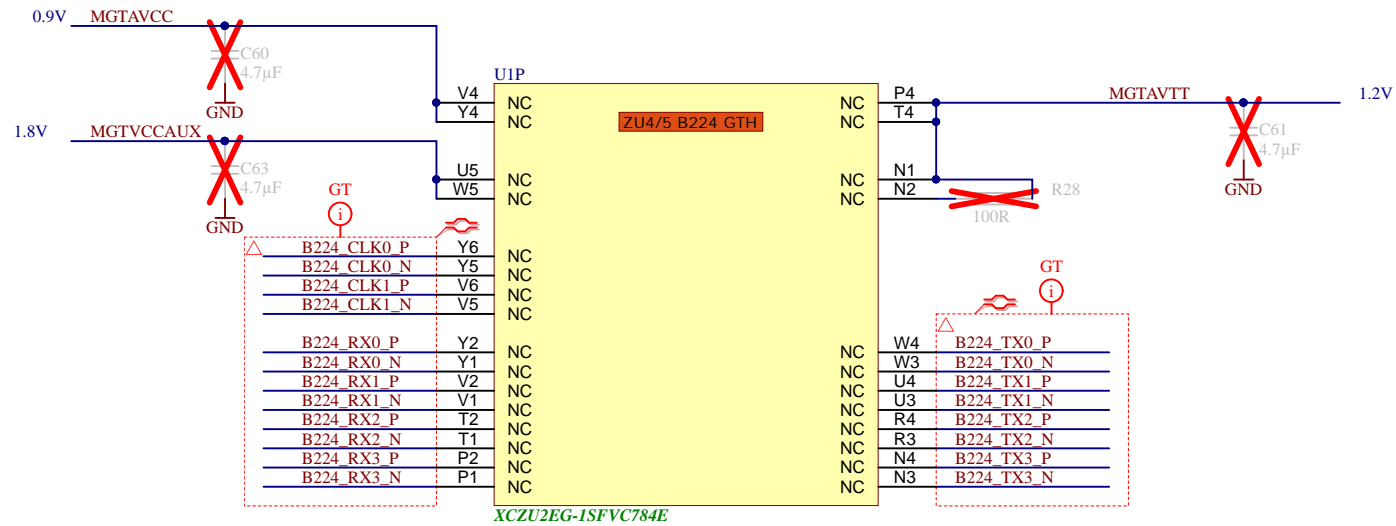
XCZU2EG-1SFVC784E




Title: TE0803 - PS_DDR		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 12 of 26
Filename: PS_DDR.SchDoc		



	Title: TE0803 - PS_GT		
	A4	Number: TE0803 2BE13-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 13 of 26
	Filename: B_PS_GT.SchDoc		



	Title: TE0803 - B224GTH		
	A4	Number: TE0803 2BE13-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 14 of 26
	Filename: B_GT.SchDoc		

1

2

3

4

A

A

B

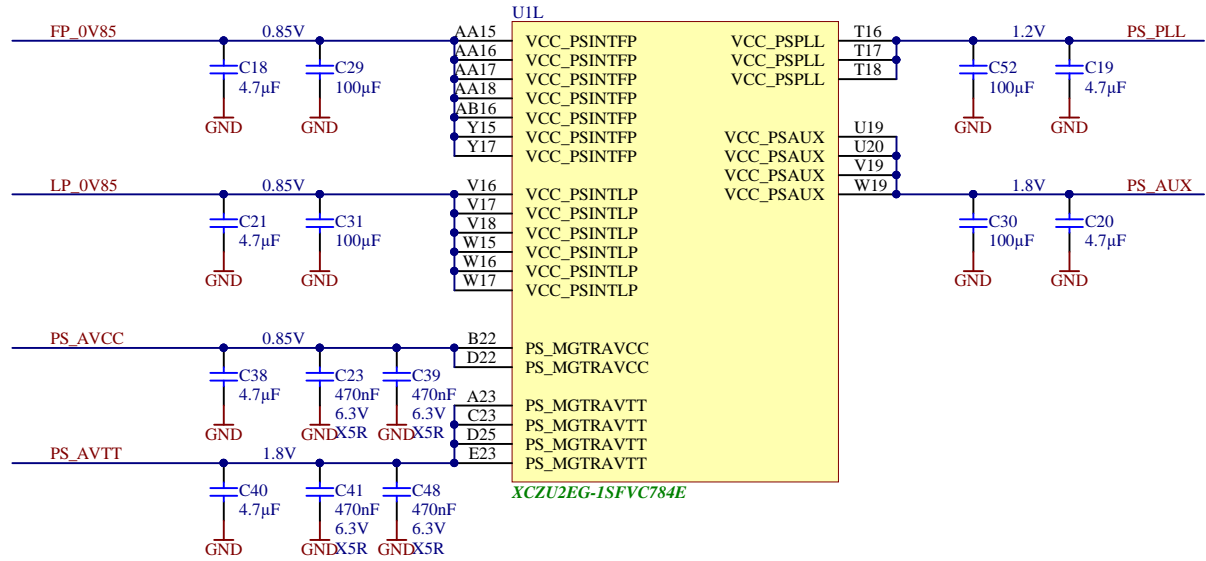
B


C

C

D

D



	Title: TE0803 - ZU_PS_POWER		
	A4	Number: TE0803 2BE13-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 15 of 26
	Filename: ZU_PS_POWER.SchDoc		

1

2

3

4

1

2

3

4

A

A

B

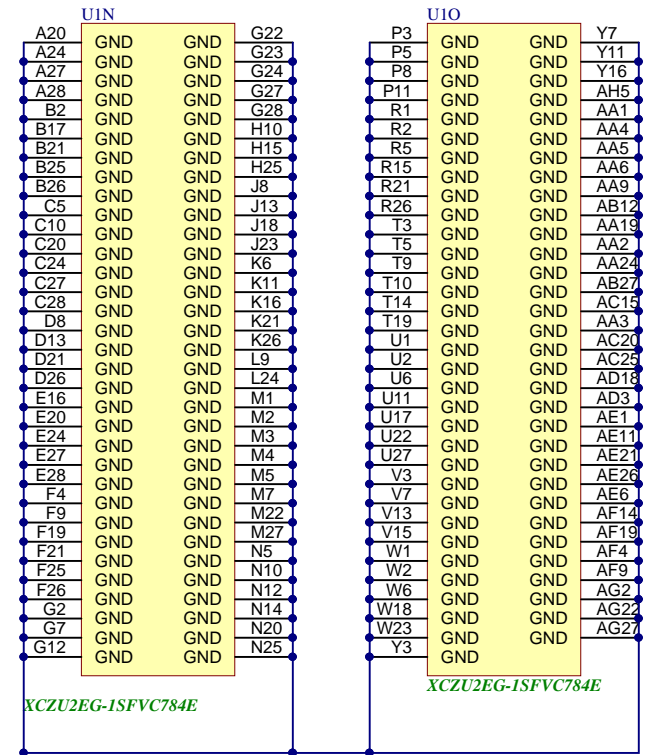
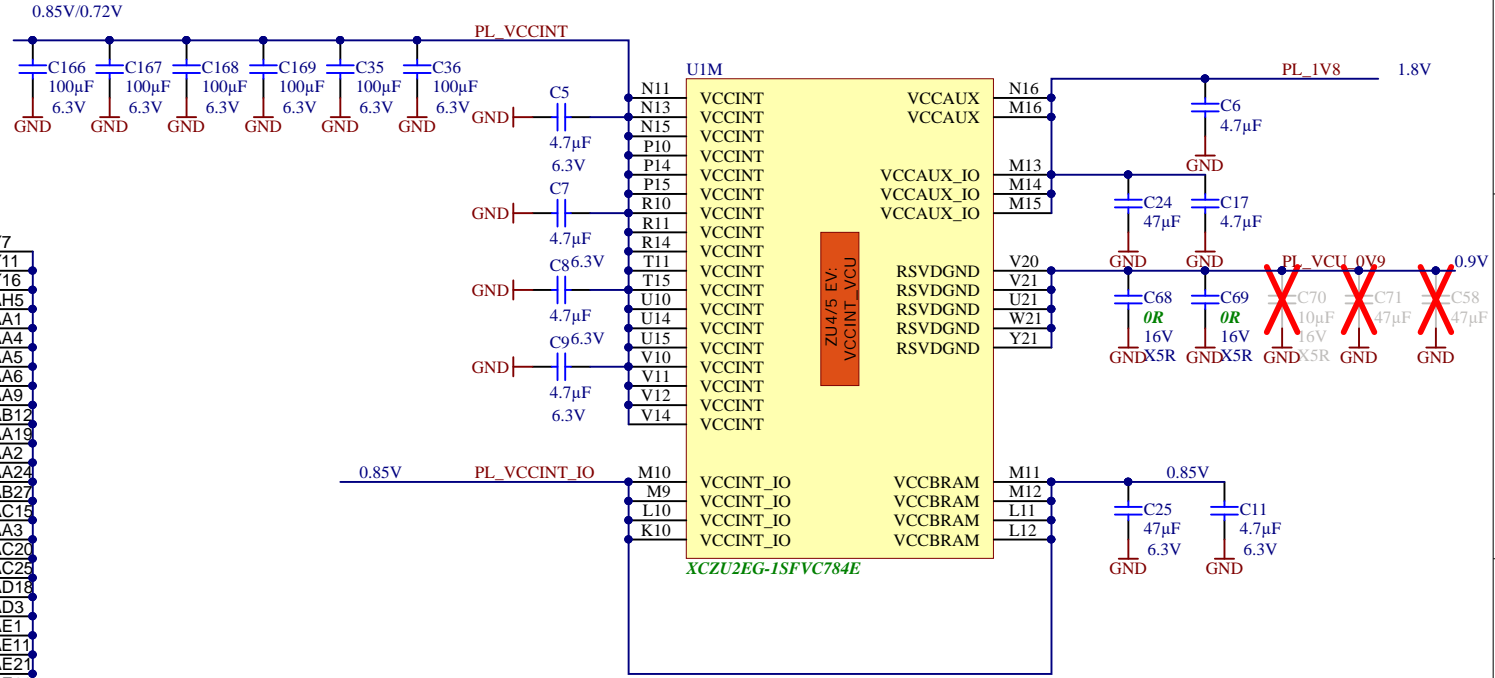
B

C

C

D

D



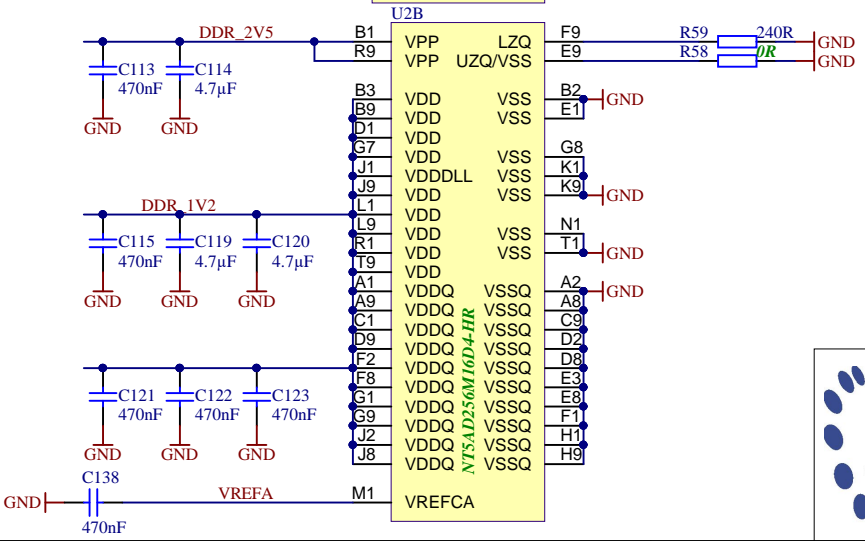
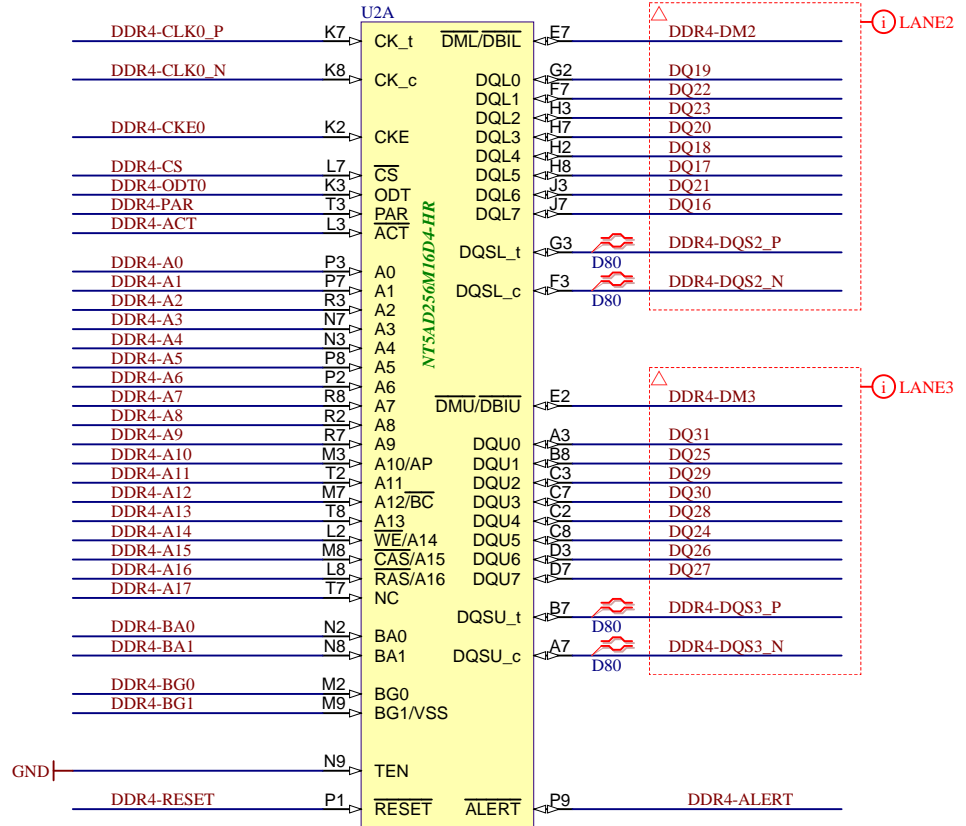
	Title: TE0803 - ZU_POWER		
	A4	Number: TE0803 2BE13-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 16 of 26
	Filename: ZU_POWER.SchDoc		

1

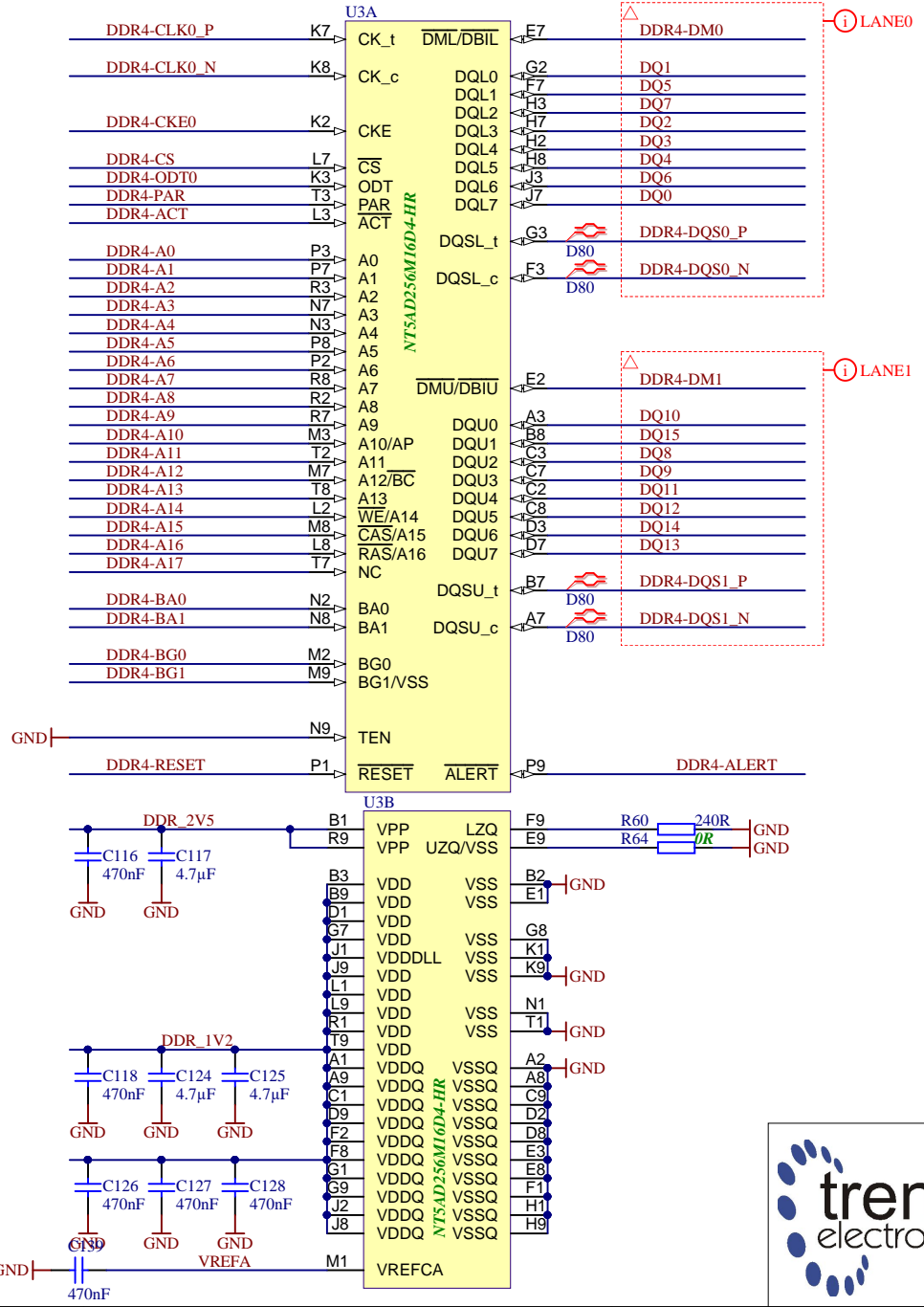

2

3

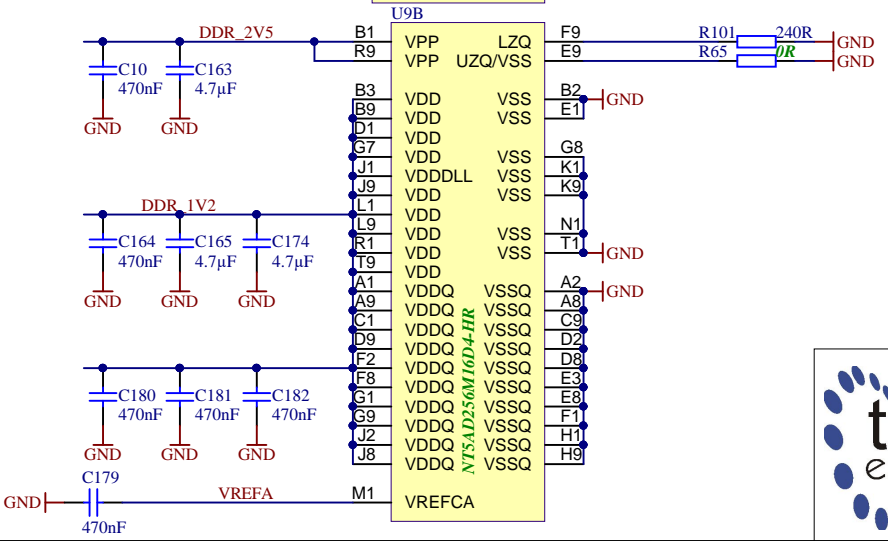
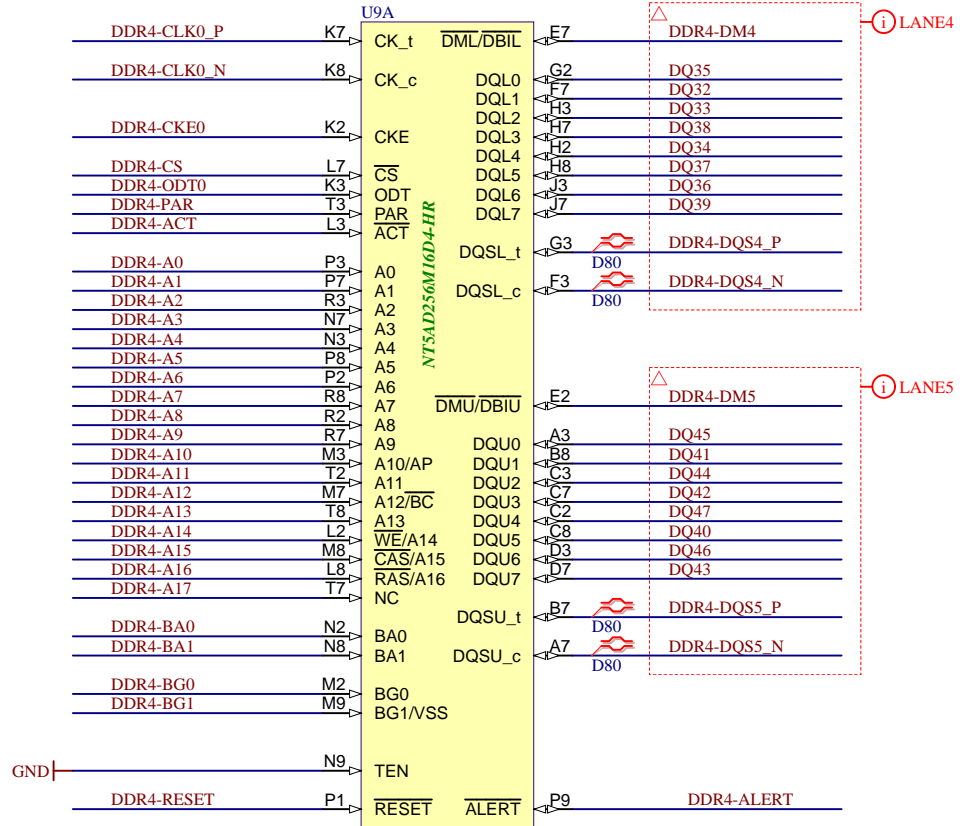
4



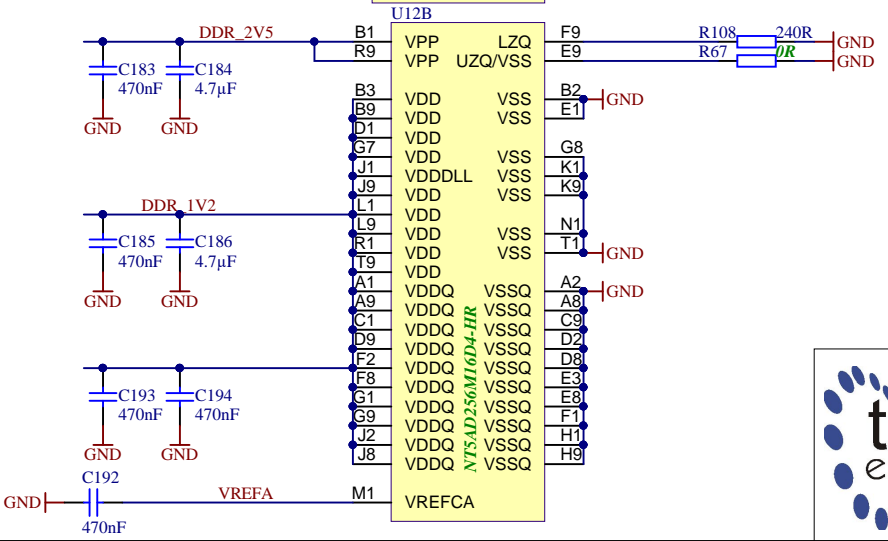
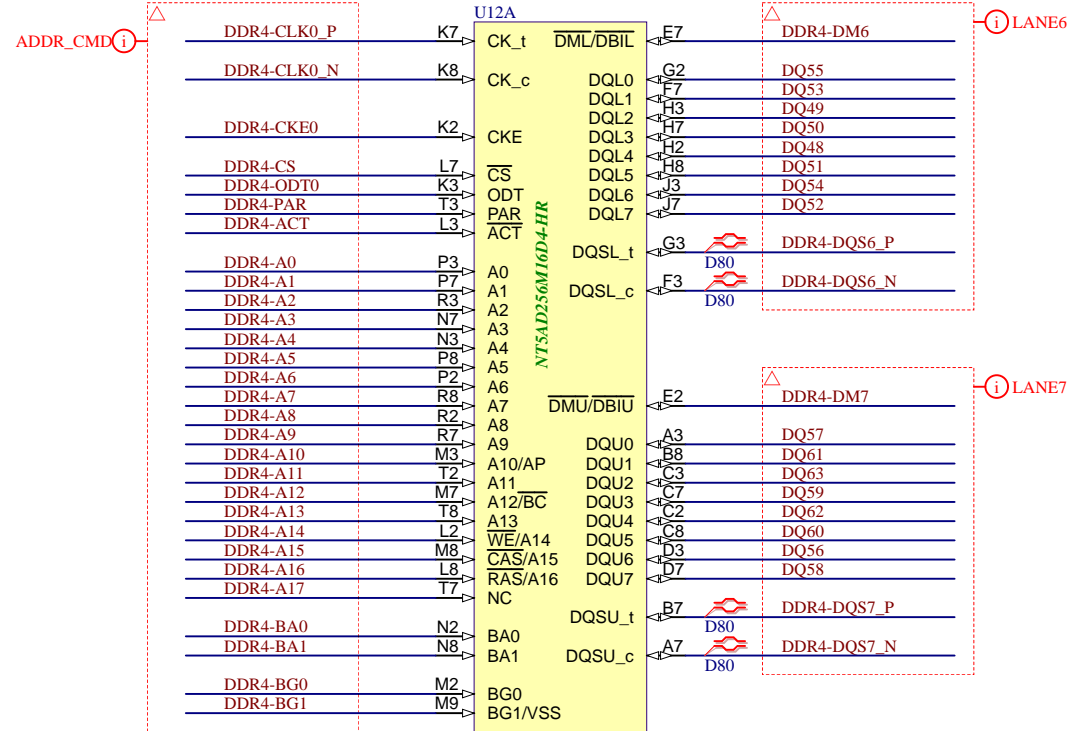
Title: TE0803 - DDR4_1_RAM		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 17 of 26
Filename: DDR4-RAM.SchDoc		





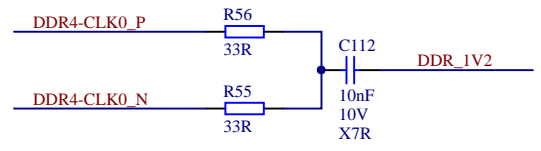
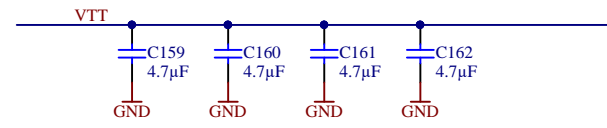
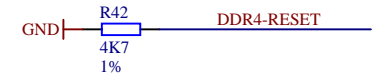
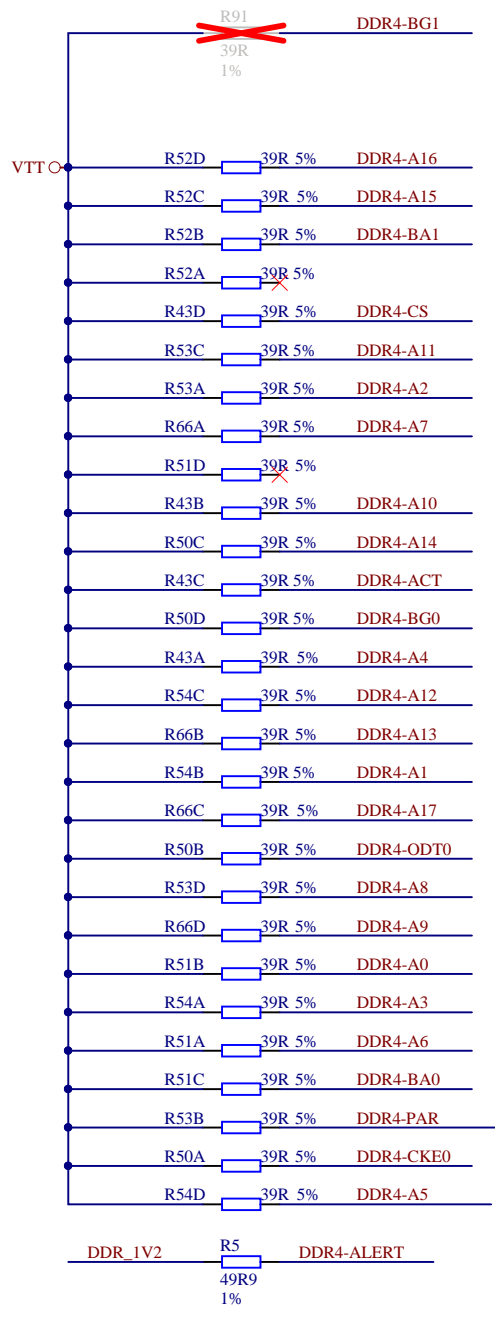
Title: TE0803 - DDR4_2_RAM		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page18 of 26
Filename: DDR4-RAM_2.SchDoc		



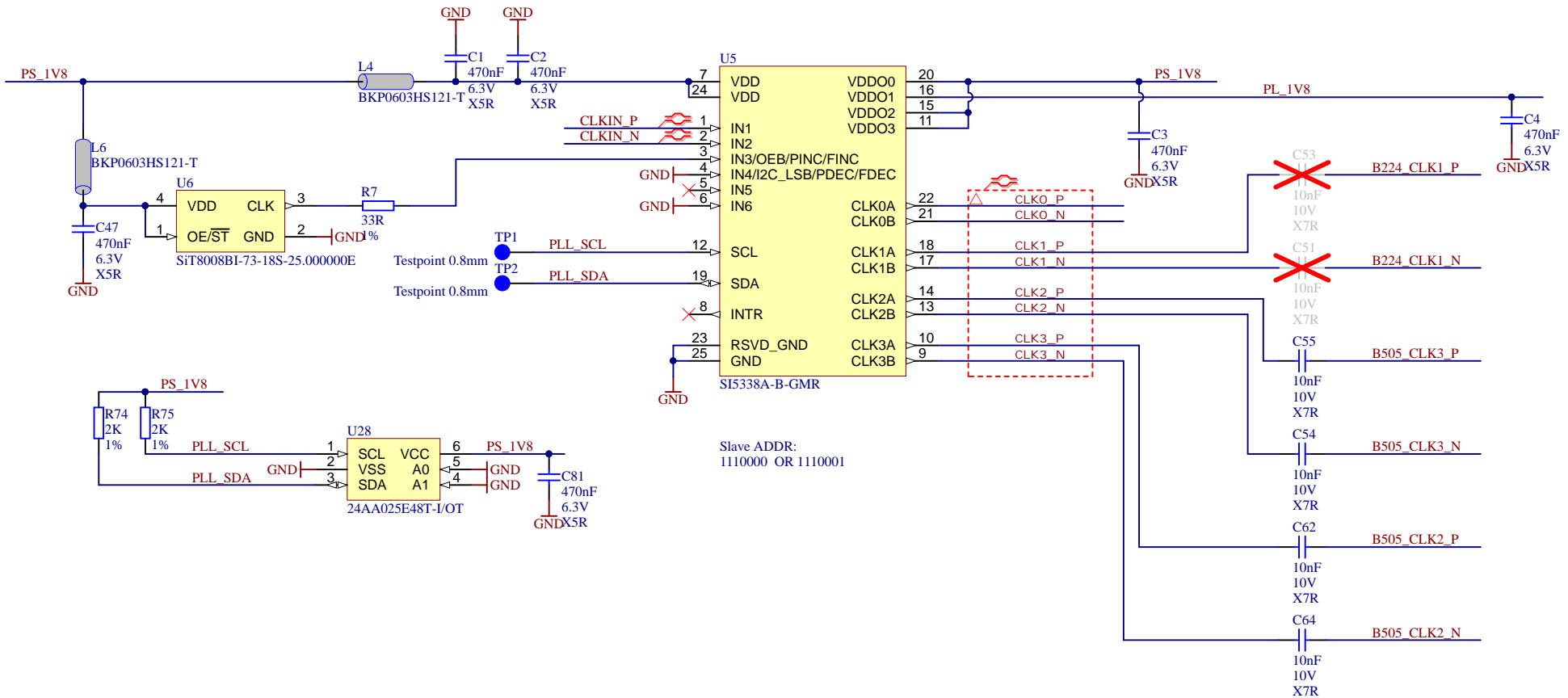
Title: TE0803 - DDR4_3_RAM		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 19 of 26
Filename: DDR4-RAM_3.SchDoc		




			Title: TE0803 - DDR4_4_RAM	
			A4	Number: TE0803 2BE13-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT		Page20 of 26
Filename: DDR4-RAM_4.SchDoc				

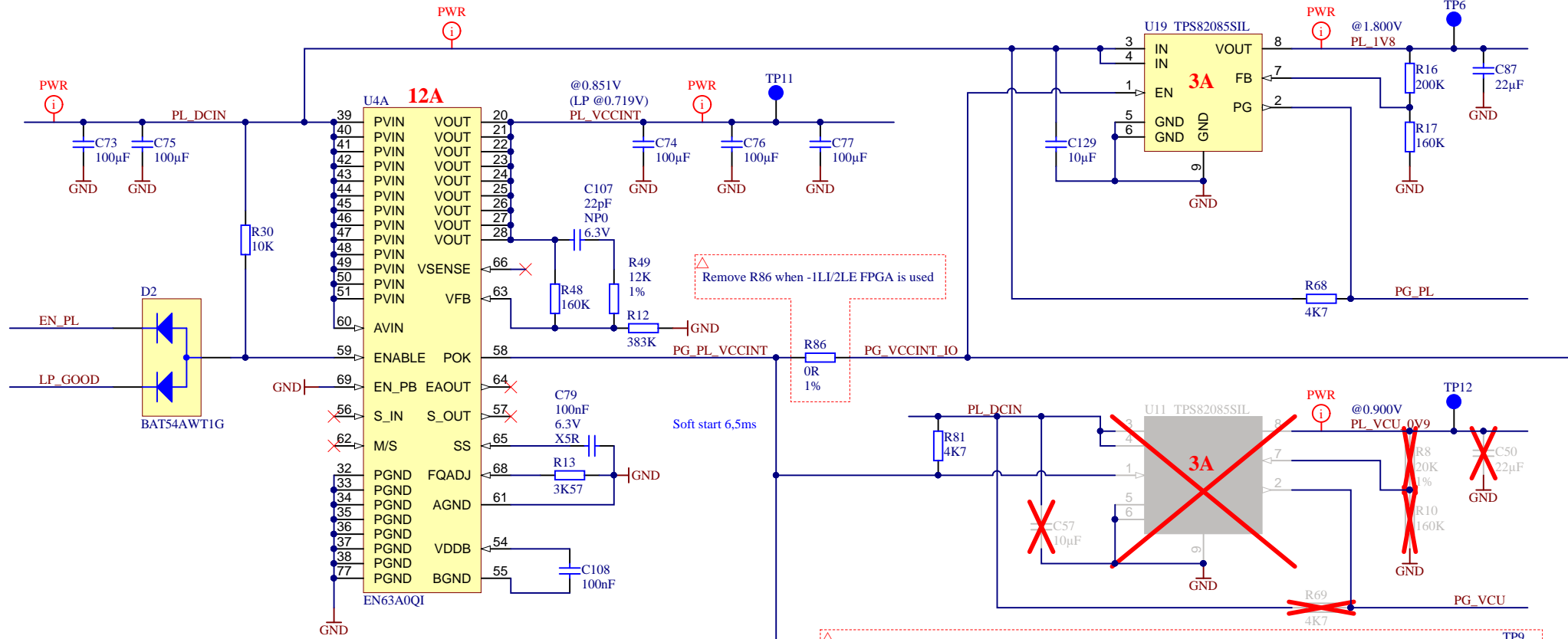


Title: TE0803 - DDR4_TERM		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 21 of 26
Filename: DDR4-TERM.SchDoc		



Slave ADDR:
1110000 OR 1110001

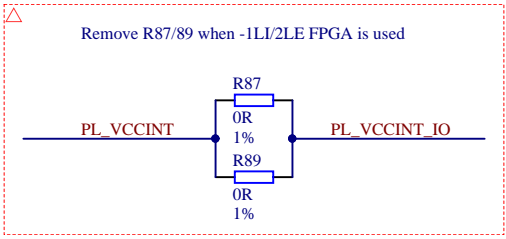
			Title: TE0803 - CLOCK	
			A4	Number: TE0803 2BE13-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT		Page 22 of 26
Filename: Clock.SchDoc				



U4B

1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76

EN63A0QI

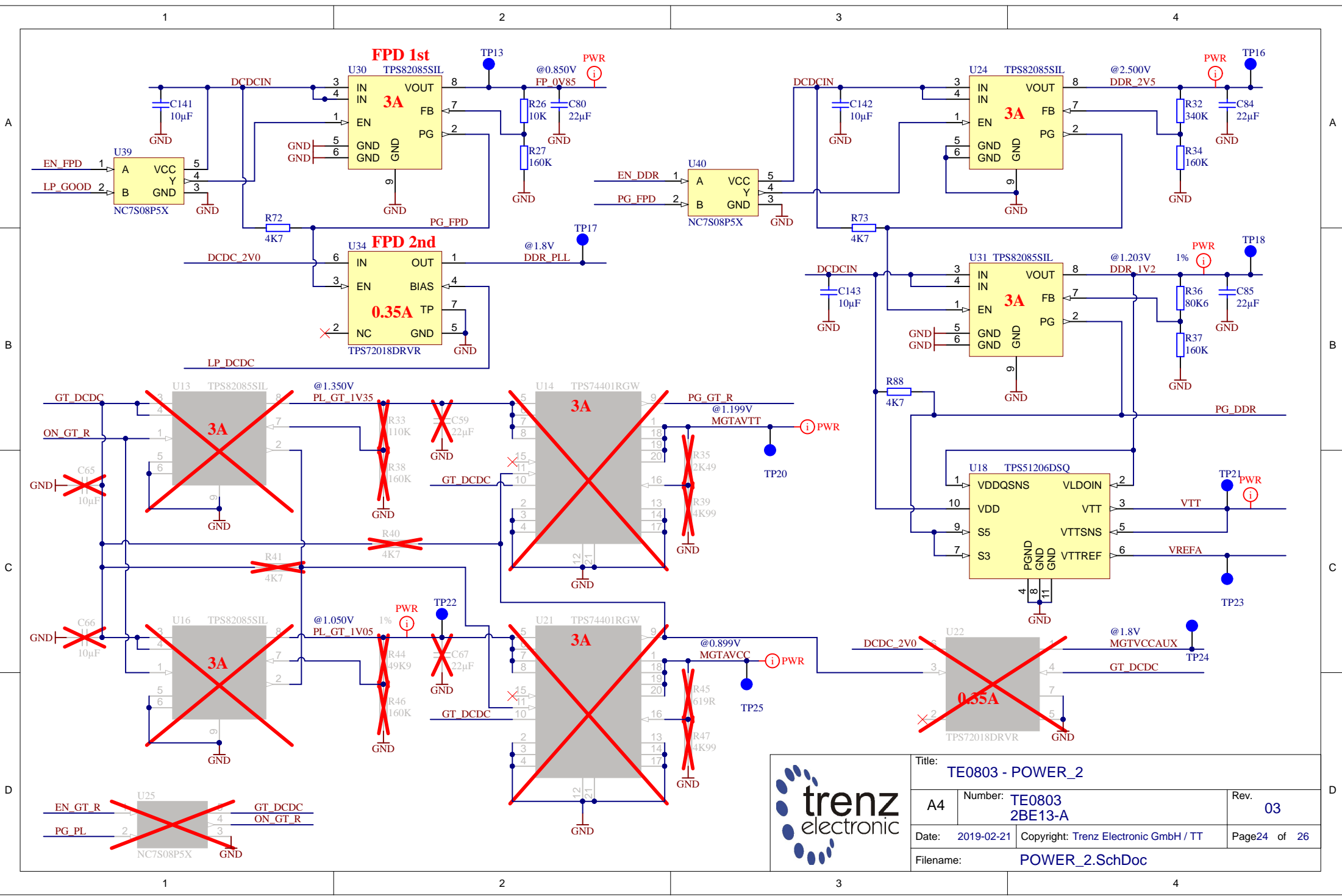


Remove R86 when -1L1/2LE FPGA is used

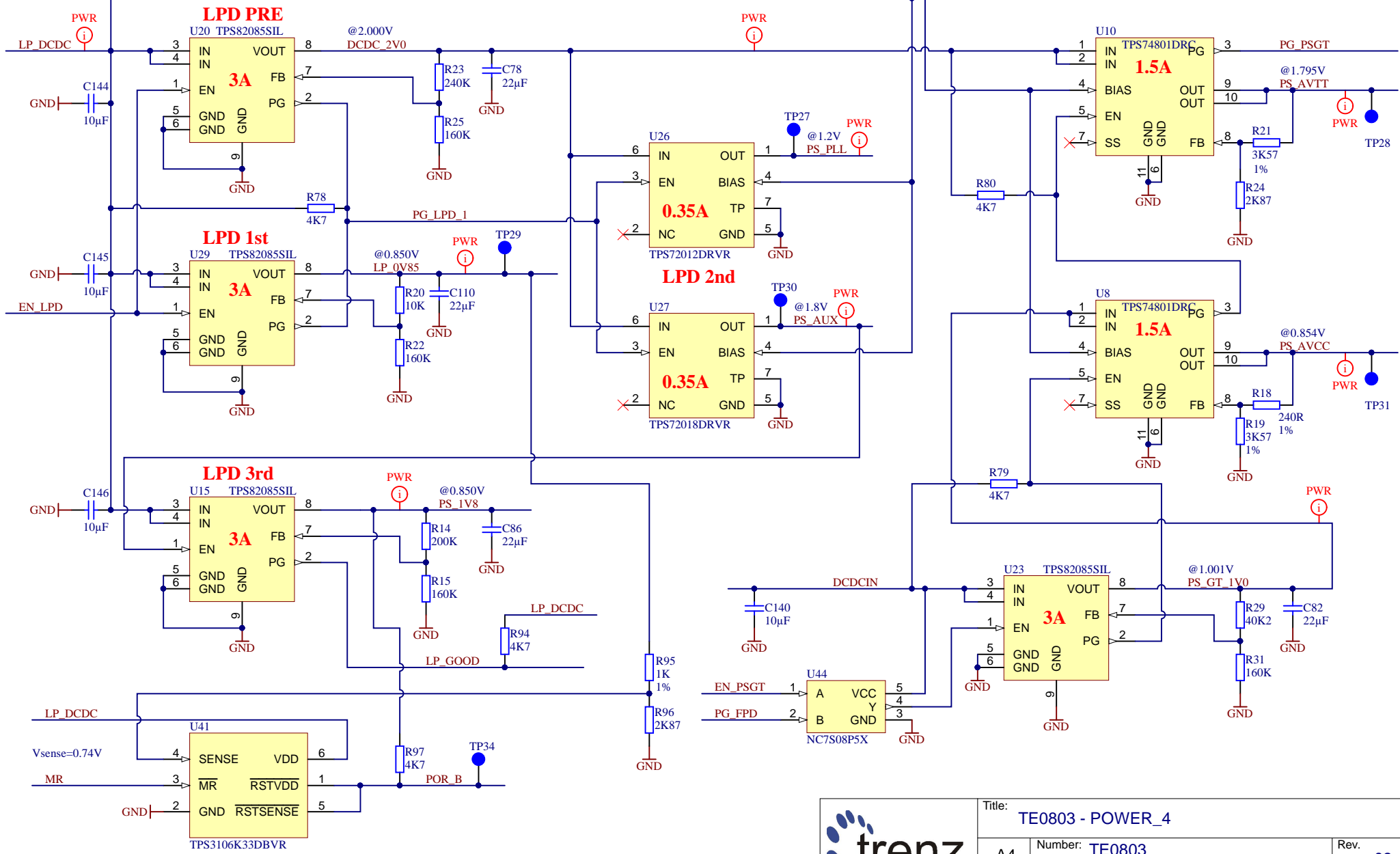
Add U33 when -1L1/2LE FPGA is used



Title: TE0803 - POWER		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 23 of 26
Filename: POWER.SchDoc		



Title: TE0803 - POWER_2		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 24 of 26
Filename: POWER_2.SchDoc		



Title: TE0803 - POWER_4		
A4	Number: TE0803 2BE13-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 25 of 26
Filename: POWER_4.SchDoc		

1

2

3

4

CHANGES REV01a (20.11.2017):

- 1) VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9.

CHANGES REV02 (20.06.2018):

- 1) Added LDO to DDR_PLL
- 2) All differential pairs wath length matched with tollerance 0.1mm (excluding package delays)
- 3) Added MAC EEPROM U28
- 4) VPS_MGTRAVCC set to 0.85V
- 5) Added pull-up resistors R68,R69

CHANGES REV03 (21.02.2019):

- 1) Added support of DDP DDR4
- 2) Added support of Low power FPGA (-L1/L2).
- 3) Revised testpoints
- 4) Revised J1-J4 connectors net label style

A

A

B


B

C

C

D

D

	Title: TE0803 - Changes list		
	A4	Number: TE0803 2BE13-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH	Page26 of 26
	Filename: Revision_Changes.SchDoc		

1

2

3

4