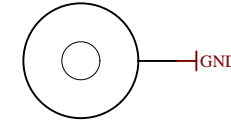
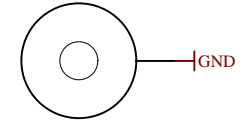


U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_DDR4-TERM DDR4-TERM.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_REV_CH Revision_Changes.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	
	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

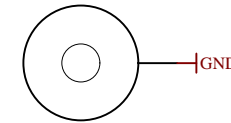
Special notes:



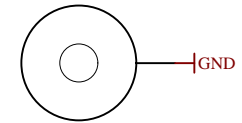
Mount.Hole 3.2mm für Unterlegscheibe



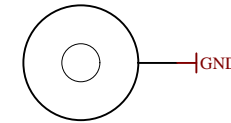
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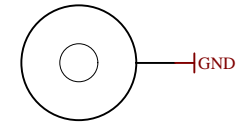
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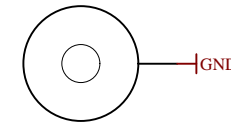
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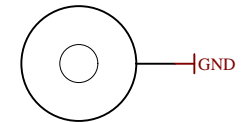
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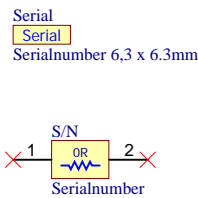
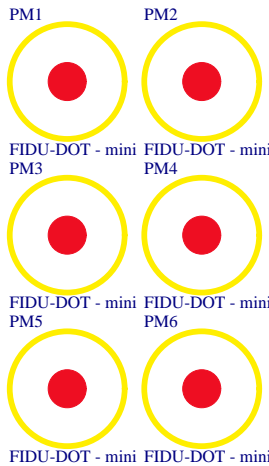
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Mount.Hole 3.2mm für Unterlegscheibe



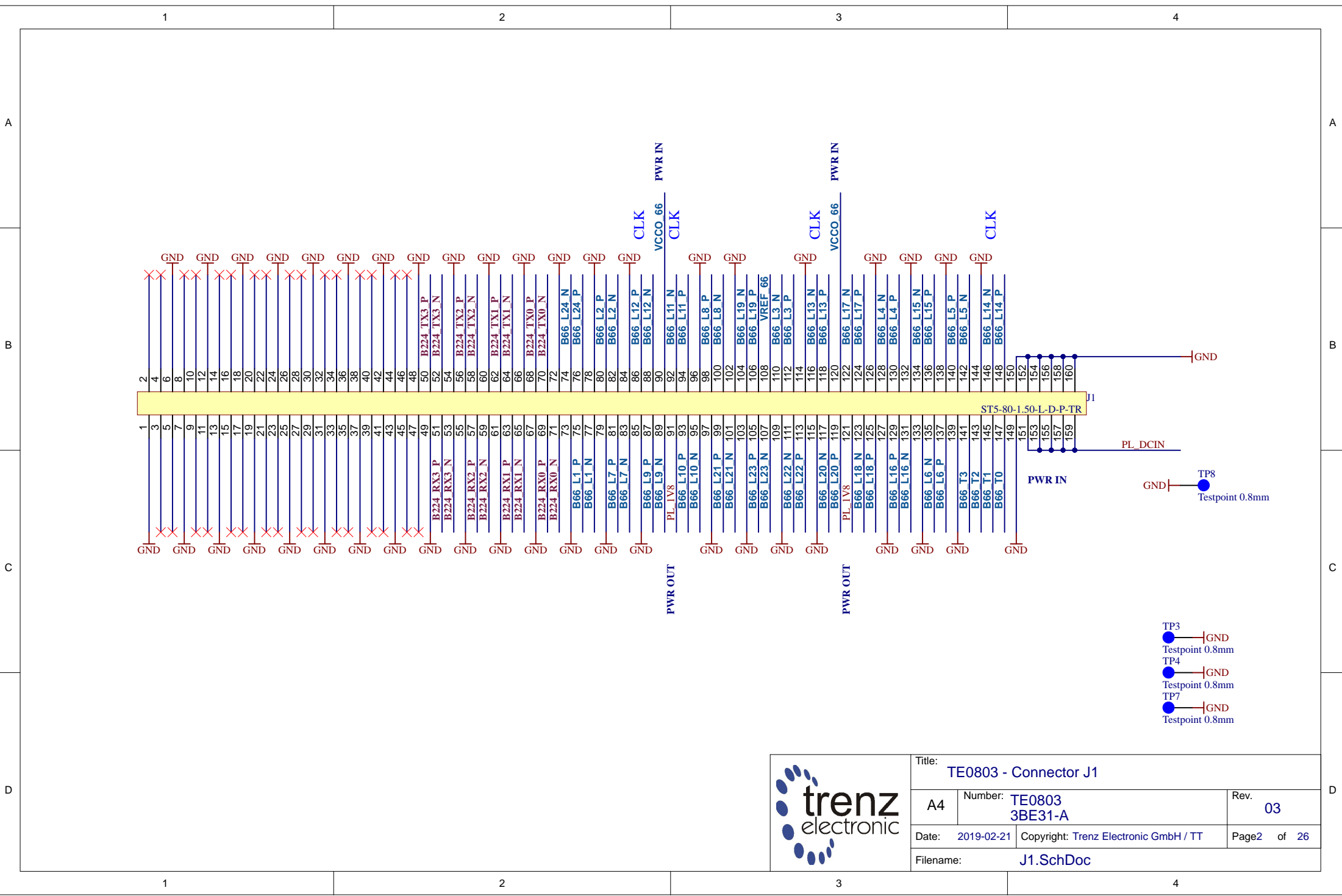
Mount.Hole 3.2mm für Unterlegscheibe



Assembly variant	3BE31-A
Created by	VY
Modified by	VY
Modified at	2020-04-15
SVN Revision	9226



Title: TE0803		
A4	Number: TE0803 3BE31-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page1 of 26
Filename: TE0803.SchDoc		



Title: TE0803 - Connector J1		
A4	Number: TE0803 3BE31-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page2 of 26
Filename: J1.SchDoc		

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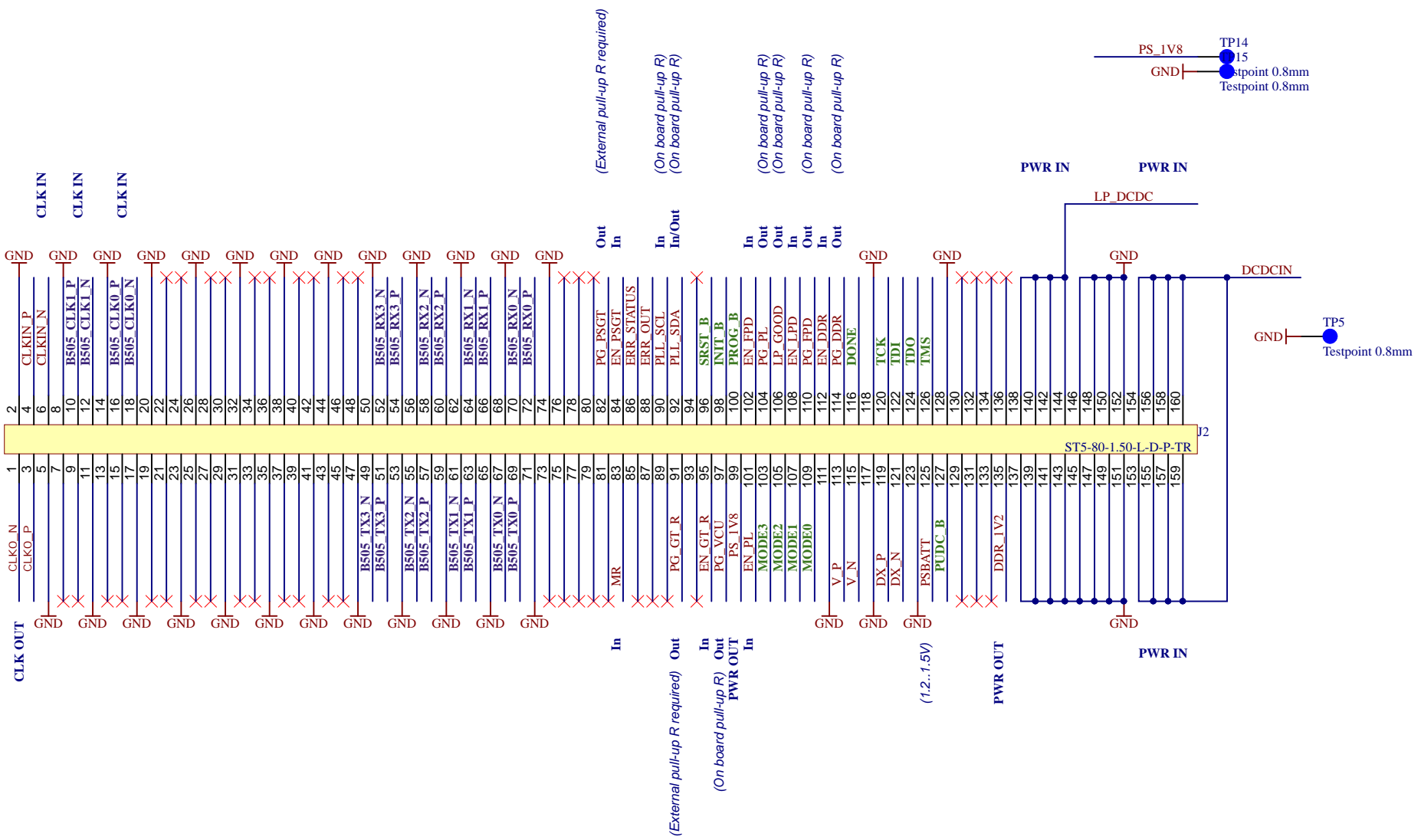
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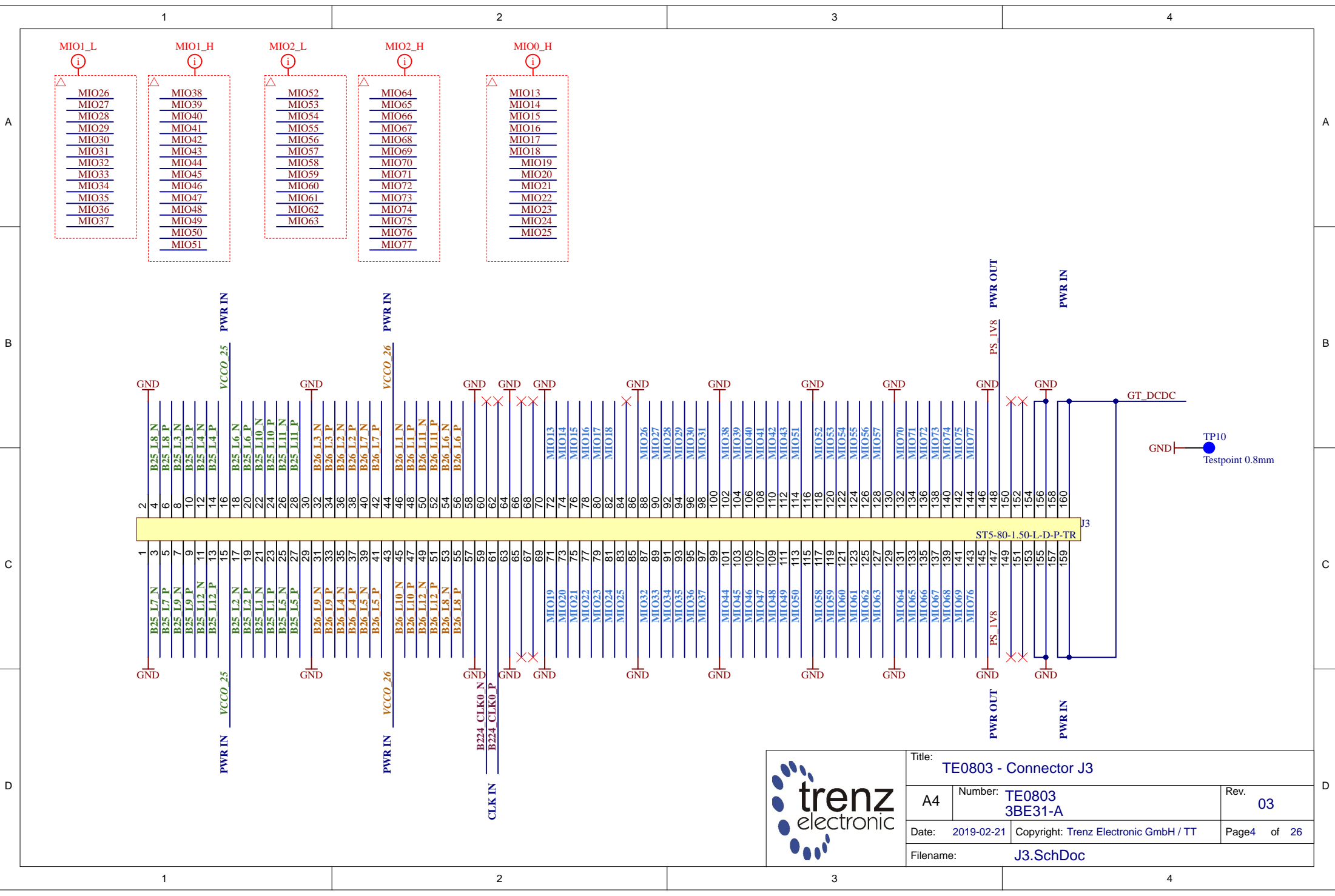

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			A4	Number: TE0803 3BE31-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT		Page3 of 26
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Title: TE0803 - Connector J3		
A4	Number: TE0803 3BE31-A	Rev. 03
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Filename: J3.SchDoc		

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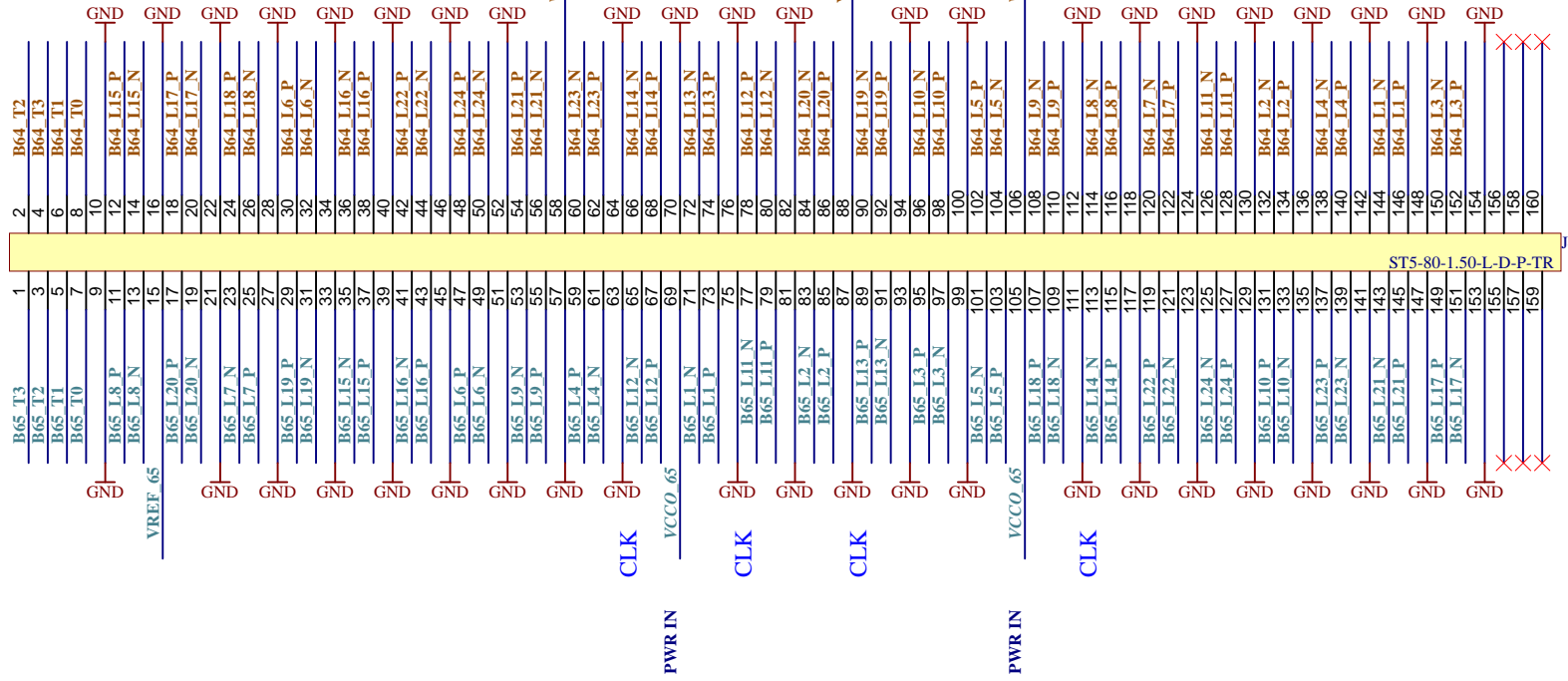

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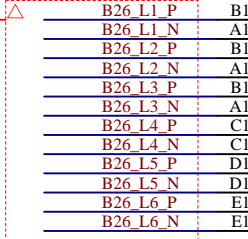
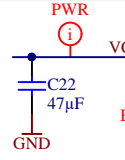
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A4	Number: TE0803 3BE31-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page5 of 26
Filename: J4.SchDoc		

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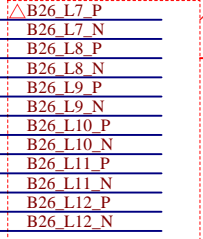
3

4



U1C XCZU3EG-1SFVC784E
BANK 26 HD (ZU4/5 BANK 46 HD)

F14	VCCO_26	B15	IO_L1P_AD11P_26	IO_L7P_HDGC_AD5P_26	G13	B26 L7 P
C15	VCCO_26	A15	IO_L1N_AD11N_26	IO_L7N_HDGC_AD5N_26	F13	B26 L7 N
		B14	IO_L2P_AD10P_26	IO_L8P_HDGC_AD4P_26	F15	B26 L8 P
		A14	IO_L2N_AD10N_26	IO_L8N_HDGC_AD4N_26	E15	B26 L8 N
		B13	IO_L3P_AD9P_26	IO_L9P_AD3P_26	G15	B26 L9 P
		A13	IO_L3N_AD9N_26	IO_L9N_AD3N_26	G14	B26 L9 N
		C14	IO_L4P_AD8P_26	IO_L10P_AD2P_26	H14	B26 L10 P
		C13	IO_L4N_AD8N_26	IO_L10N_AD2N_26	H13	B26 L10 N
		D15	IO_L5P_HDGC_AD7P_26	IO_L11P_AD1P_26	K14	B26 L11 P
		D14	IO_L5N_HDGC_AD7N_26	IO_L11N_AD1N_26	J14	B26 L11 N
		E14	IO_L6P_HDGC_AD6P_26	IO_L12P_AD0P_26	L14	B26 L12 P
		E13	IO_L6N_HDGC_AD6N_26	IO_L12N_AD0N_26	L13	B26 L12 N

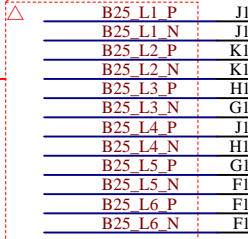
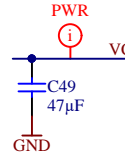


BANK 44 HD (ZU4/5 BANK 43 HD)

AC10	VCCO_44	AG12	VCCO_44	AD11	AD10
AG10	IO_L1P_AD11P_44	AH10	IO_L1N_AD11N_44	AB11	AC11
AH10	IO_L2P_AD10P_44	AF11	IO_L2N_AD10N_44	AA11	AA10
AF11	IO_L3P_AD9P_44	AG11	IO_L3N_AD9N_44	AW10	Y10
AG11	IO_L4P_AD8P_44	AH12	IO_L4N_AD8N_44	Y10	Y9
AH12	IO_L5P_HDGC_AD7P_44	AH11	IO_L5N_HDGC_AD7N_44	Y9	AA8
AH11	IO_L6P_HDGC_AD6P_44	AE10	IO_L6N_HDGC_AD6N_44	AB10	AB9
AE10		AF10		AB9	
AF10		AE12			
AE12		AF12			
AF12		AC13			
AC13		AD12			
AD12					

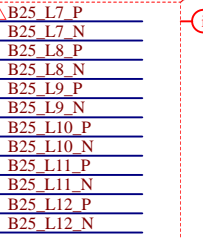
U1B
BANK 24 HD (ZU4/5 BANK 44 HD)

AA14	VCCO_24	AD13	VCCO_24	AA13	AB13
AE15	IO_L1P_AD15P_24	AG14	IO_L1N_AD15N_24	AB15	AB14
AE14	IO_L2P_AD14P_24	AH11	IO_L2N_AD14N_24	W14	W13
AG14	IO_L3P_AD13P_24	AH13	IO_L3N_AD13N_24	W13	Y14
AH11	IO_L4P_AD12P_24	AE13	IO_L4N_AD12N_24	Y14	Y13
AH13	IO_L5P_HDGC_24	AF13	IO_L5N_HDGC_24	Y13	W12
AE13	IO_L6P_HDGC_24	AD12	IO_L6N_HDGC_24	W12	W11
AF13		AD14		W11	Y12
AD12		AC14		Y12	AA12
AD14		AC13		AA12	
AC14					
AC13					

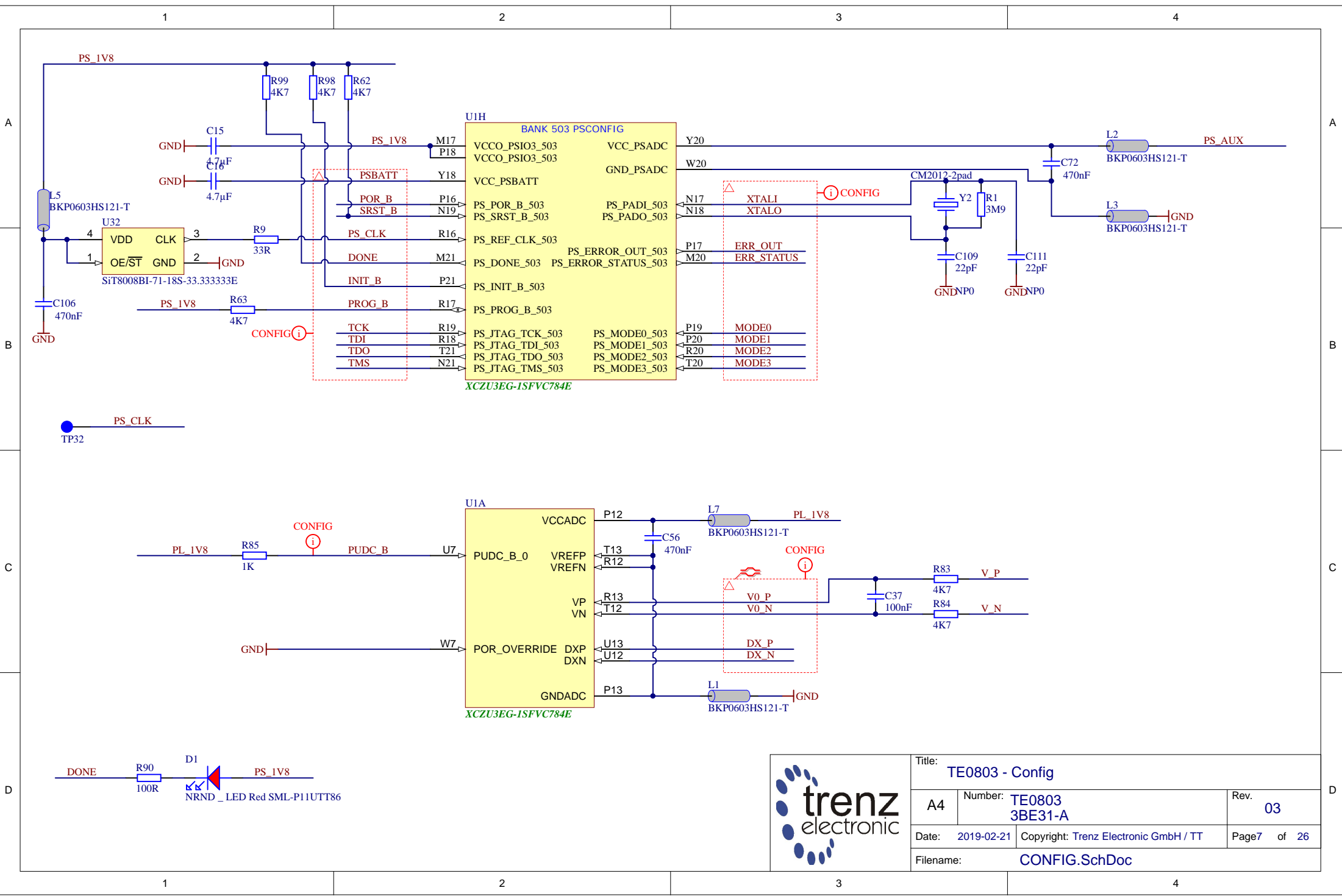


XCZU3EG-1SFVC784E
BANK 25 HD (ZU4/5 BANK 45 HD)

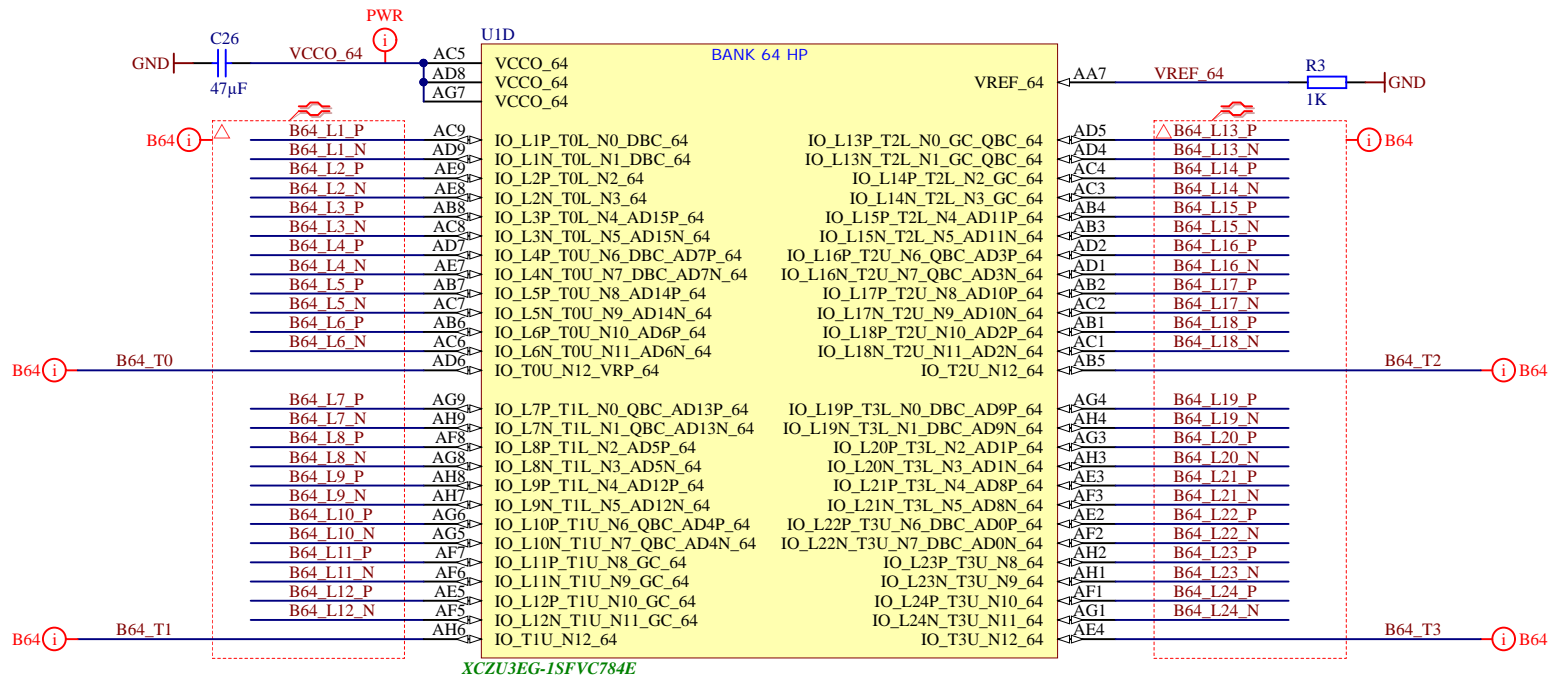
B12	VCCO_25	J11	IO_L1P_AD15P_25	IO_L7P_HDGC_25	E10	B25 L7 P
E11	VCCO_25	J10	IO_L1N_AD15N_25	IO_L7N_HDGC_25	D10	B25 L7 N
		K13	IO_L2P_AD14P_25	IO_L8P_HDGC_25	E12	B25 L8 P
		K12	IO_L2N_AD14N_25	IO_L8N_HDGC_25	D11	B25 L8 N
		H11	IO_L3P_AD13P_25	IO_L9P_AD11P_25	C11	B25 L9 P
		G10	IO_L3N_AD13N_25	IO_L9N_AD11N_25	B10	B25 L9 N
		J12	IO_L4P_AD12P_25	IO_L10P_AD10P_25	B11	B25 L10 P
		H12	IO_L4N_AD12N_25	IO_L10N_AD10N_25	A10	B25 L10 N
		G11	IO_L5P_HDGC_25	IO_L11P_AD9P_25	A12	B25 L11 P
		F11	IO_L5N_HDGC_25	IO_L11N_AD9N_25	A11	B25 L11 N
		F12	IO_L6P_HDGC_25	IO_L12P_AD8P_25	D12	B25 L12 P
		F11	IO_L6N_HDGC_25	IO_L12N_AD8N_25	C12	B25 L12 N




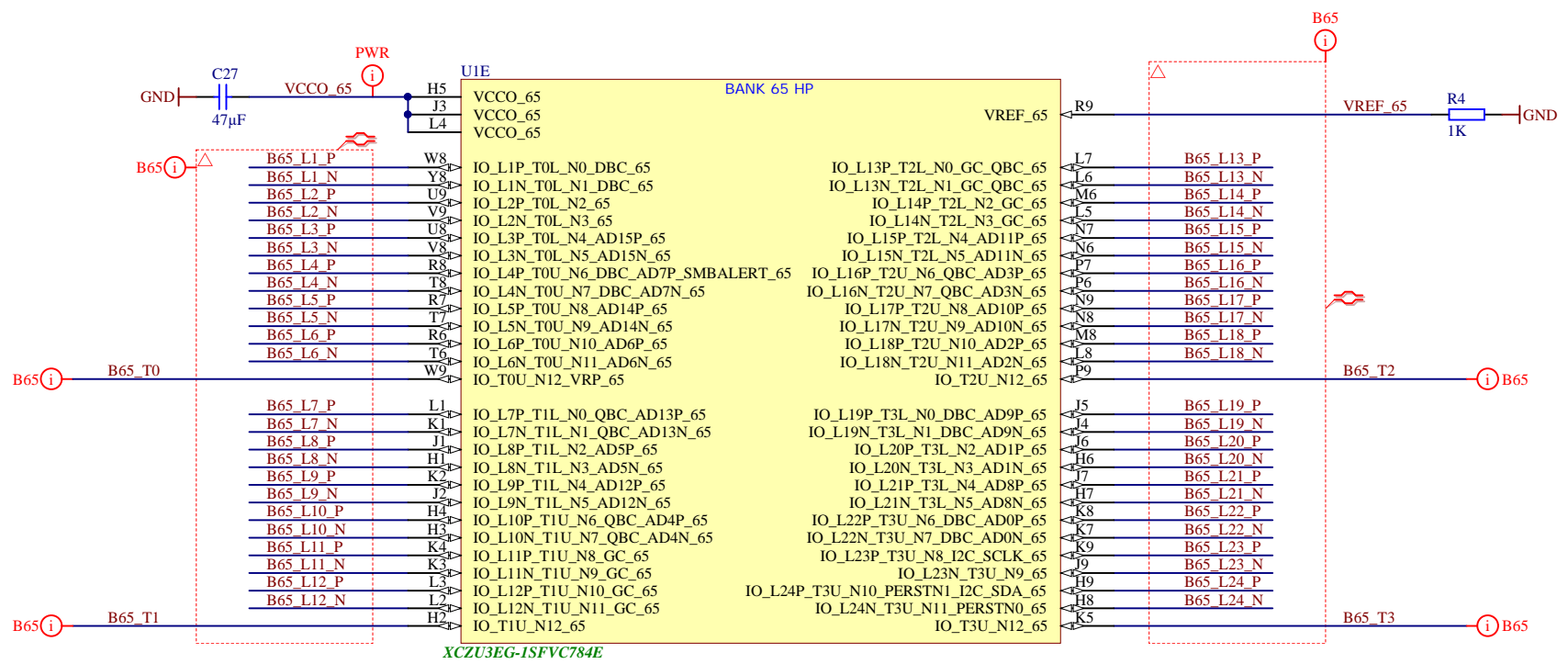
Title: TE0803 - HD Banks		
A4	Number: TE0803 3BE31-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page6 of 26
Filename: B_HD.SchDoc		



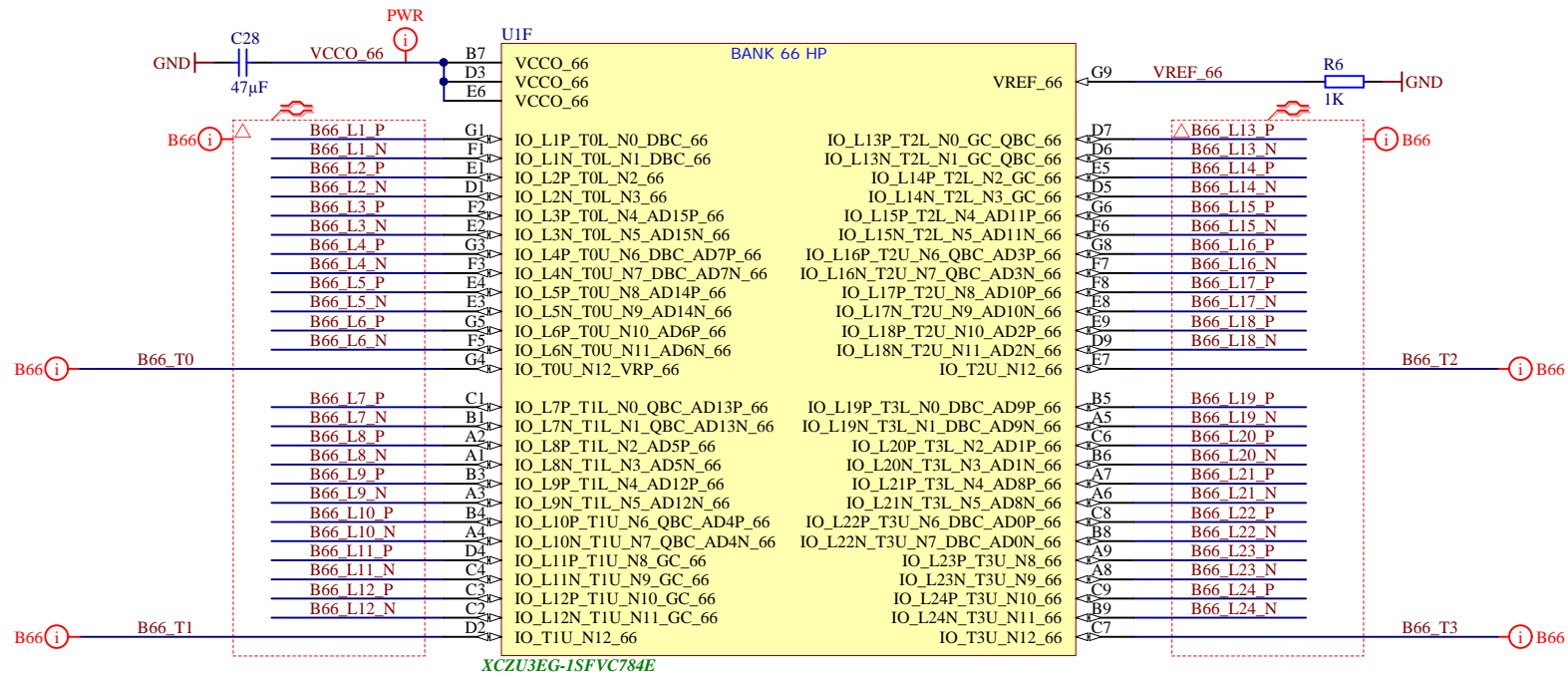
Title: TE0803 - Config		
A4	Number: TE0803 3BE31-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 7 of 26
Filename: CONFIG.SchDoc		



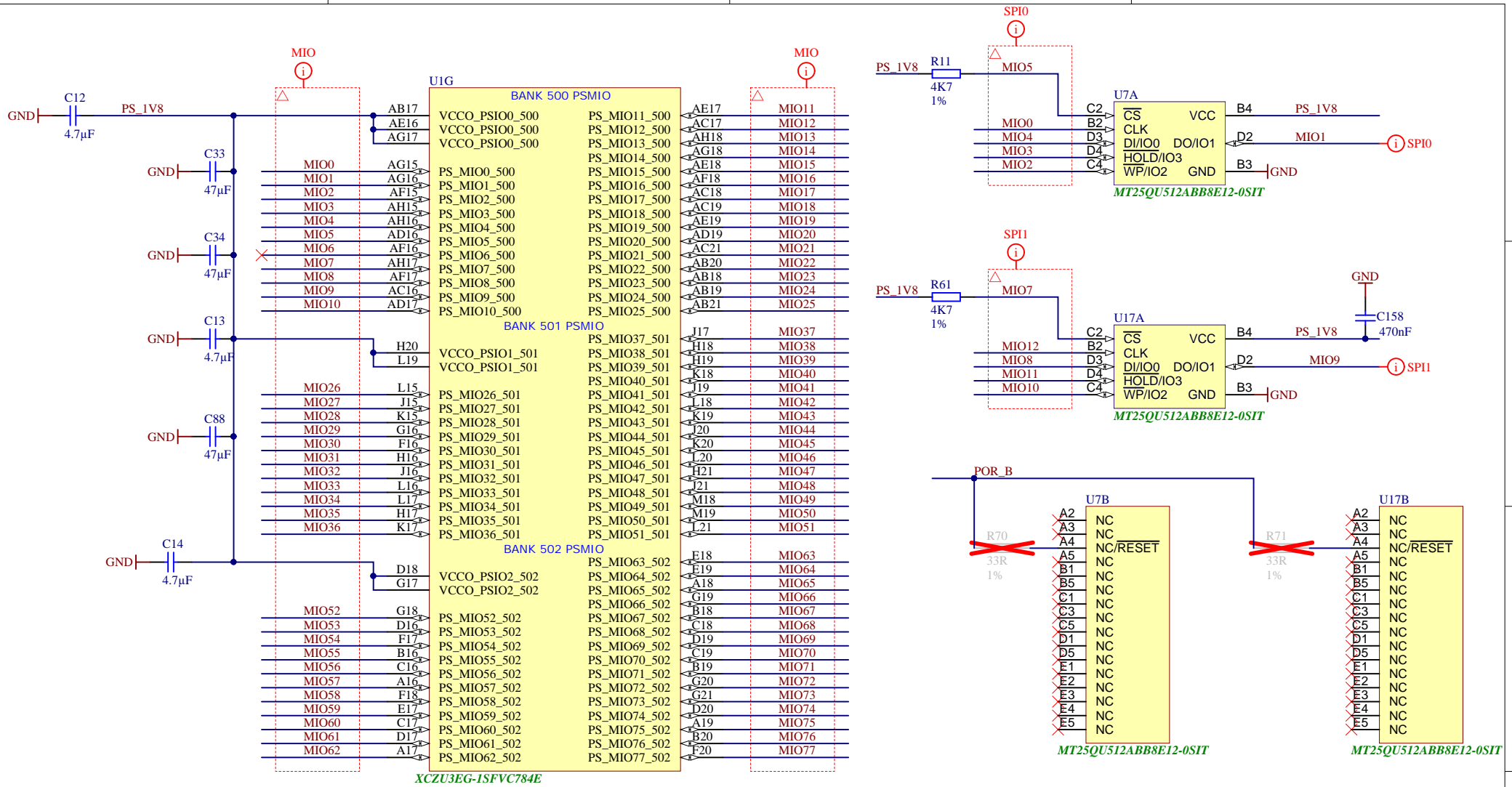
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	A4	Number: TE0803 3BE31-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 8 of 26
	Filename: B64.SchDoc		




Title: TE0803 - B65		
A4	Number: TE0803 3BE31-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page9 of 26
Filename: B65.SchDoc		



Title: TE0803 - B66		
A4	Number: TE0803 3BE31-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 10 of 26
Filename: B66.SchDoc		



		Title: TE0803 - MIO Banks	
		A4	Number: TE0803 3BE31-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: B_MIO.SchDoc		Page 11 of 26	

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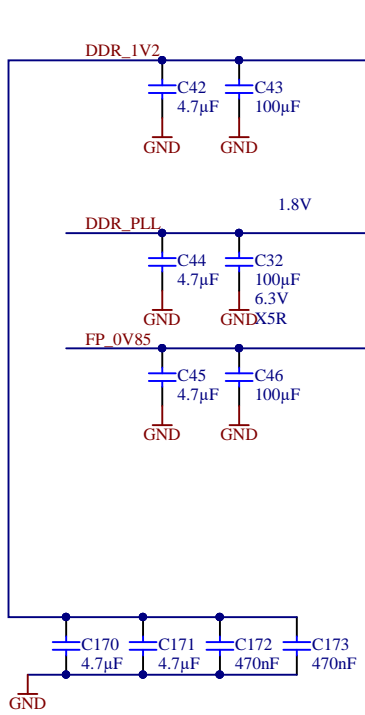
D

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U11		BANK 504 PSDDR			
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0_P	D80	
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0_N	D80	
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0		
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24			✗
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25			✗
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27			✗
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0		
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1		
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2		
VCC_PSDDR_PLL	PS_DDR_A3_504	AA28	DDR4-A3		
VCC_PSDDR_PLL	PS_DDR_A4_504	Y27	DDR4-A4		
VCC_PSINTFP_DDR	PS_DDR_A5_504	AA27	DDR4-A5		
VCC_PSINTFP_DDR	PS_DDR_A6_504	Y22	DDR4-A6		
VCC_PSINTFP_DDR	PS_DDR_A7_504	AA23	DDR4-A7		
VCC_PSINTFP_DDR	PS_DDR_A8_504	AA22	DDR4-A8		
VCC_PSINTFP_DDR	PS_DDR_A9_504	AB23	DDR4-A9		
VCC_PSINTFP_DDR	PS_DDR_A10_504	AA25	DDR4-A10		
VCC_PSINTFP_DDR	PS_DDR_A11_504	AA26	DDR4-A11		
VCC_PSINTFP_DDR	PS_DDR_A12_504	AB25	DDR4-A12		
VCC_PSINTFP_DDR	PS_DDR_A13_504	AB26	DDR4-A13		
VCC_PSINTFP_DDR	PS_DDR_A14_504	AB24	DDR4-A14		
VCC_PSINTFP_DDR	PS_DDR_A15_504	AC24	DDR4-A15		
VCC_PSINTFP_DDR	PS_DDR_A16_504	AC23	DDR4-A16		
VCC_PSINTFP_DDR	PS_DDR_A17_504	AC22	DDR4-A17		
PS_DDR_CS_N0_504		W27	DDR4-CS		
PS_DDR_CS_N1_504		V26			✗
PS_DDR_BA0_504		V23	DDR4-BA0		
PS_DDR_BA1_504		W22	DDR4-BA1		
PS_DDR_BG0_504		W24	DDR4-BG0		
PS_DDR_BG1_504		V22	DDR4-BG1		
PS_DDR_PARITY_504		V24	DDR4-PAR		
PS_DDR_RAM_RST_N_504		U23	DDR4-RESET		
PS_DDR_ACT_N_504		Y23	DDR4-ACT		
PS_DDR_ALERT_N_504		U25	DDR4-ALERT		
PS_DDR_ZQ_504		U24		R2 240R	GND
PS_DDR_ODT0_504		U28	DDR4-ODT0		
PS_DDR_ODT1_504		U26			✗

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U1J		BANK 504 PSDDR			
DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504	T22	DQ32
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504	R22	DQ33
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504	P22	DQ34
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504	N22	DQ35
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504	T23	DQ36
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504	P24	DQ37
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	R24	DQ38
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	N24	DQ39
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504	H24	DQ40
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504	J24	DQ41
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504	M24	DQ42
DQ11	AD22	PS_DDR_DQ11_504	PS_DDR_DQ43_504	K24	DQ43
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504	J22	DQ44
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504	H22	DQ45
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504	K22	DQ46
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504	J22	DQ47
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504	M25	DQ48
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504	M26	DQ49
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504	L25	DQ50
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504	L26	DQ51
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504	K28	DQ52
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504	L28	DQ53
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504	M28	DQ54
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504	N28	DQ55
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504	J28	DQ56
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504	K27	DQ57
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504	H28	DQ58
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504	H27	DQ59
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504	G26	DQ60
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504	G25	DQ61
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504	K25	DQ62
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504	J25	DQ63
DDR4-DQS0_P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ64_504	T28	
DDR4-DQS0_N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ65_504	R28	
DDR4-DQS1_P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ66_504	P28	
DDR4-DQS1_N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ67_504	P27	
DDR4-DQS2_P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504	R25	
DDR4-DQS2_N	AF26	PS_DDR_DQS_N2_504	PS_DDR_DQ69_504	P25	
DDR4-DQS3_P	AE27	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504	T25	
DDR4-DQS3_N	AF27	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504		
DDR4-DQS4_P	N23	PS_DDR_DQS_P4_504			
DDR4-DQS4_N	M23	PS_DDR_DQS_N4_504	PS_DDR_DM0_504	AG20	DDR4-DM0
DDR4-DQS5_P	L23	PS_DDR_DQS_P5_504	PS_DDR_DM1_504	AE23	DDR4-DM1
DDR4-DQS5_N	K23	PS_DDR_DQS_N5_504	PS_DDR_DM2_504	AE25	DDR4-DM2
DDR4-DQS6_P	N26	PS_DDR_DQS_P6_504	PS_DDR_DM3_504	AE28	DDR4-DM3
DDR4-DQS6_N	N27	PS_DDR_DQS_N6_504	PS_DDR_DM4_504	R23	DDR4-DM4
DDR4-DQS7_P	J26	PS_DDR_DQS_P7_504	PS_DDR_DM5_504	H23	DDR4-DM5
DDR4-DQS7_N	J27	PS_DDR_DQS_N7_504	PS_DDR_DM6_504	L27	DDR4-DM6
	R27	PS_DDR_DQS_P8_504	PS_DDR_DM7_504	H26	DDR4-DM7
	T27	PS_DDR_DQS_N8_504	PS_DDR_DM8_504	T26	

XCZU3EG-1SFVC784E



Title: TE0803 - PS_DDR		
A4	Number: TE0803 3BE31-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 12 of 26
Filename: PS_DDR.SchDoc		

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A

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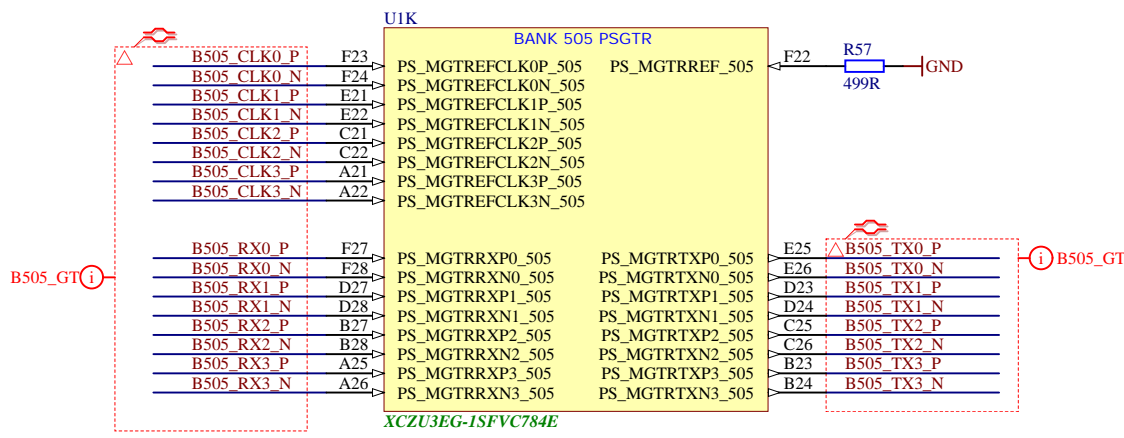
B

C

C

D

D



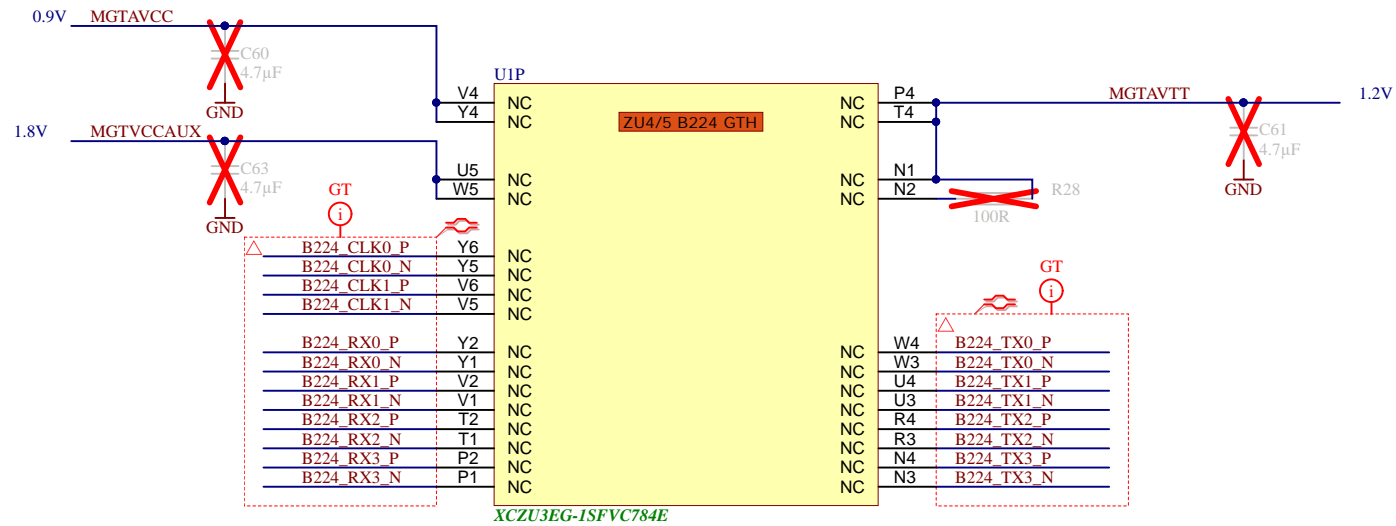
	Title: TE0803 - PS_GT		
	A4	Number: TE0803 3BE31-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	
	Page 13 of 26		
Filename: B_PS_GT.SchDoc			


1

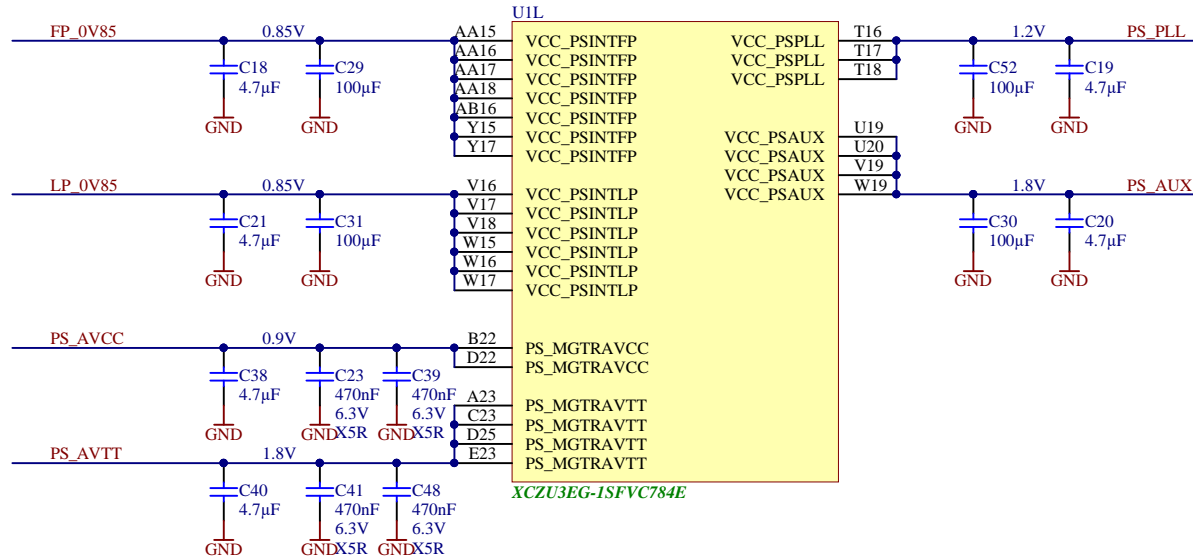
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		Title: TE0803 - B224GTH	
		A4	Number: TE0803 3BE31-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: B_GT.SchDoc		Page 14 of 26	



	Title: TE0803 - ZU_PS_POWER	
	A4	Number: TE0803 3BE31-A
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT
	Filename: ZU_PS_POWER.SchDoc	Rev. 03 Page 15 of 26

A

A

B

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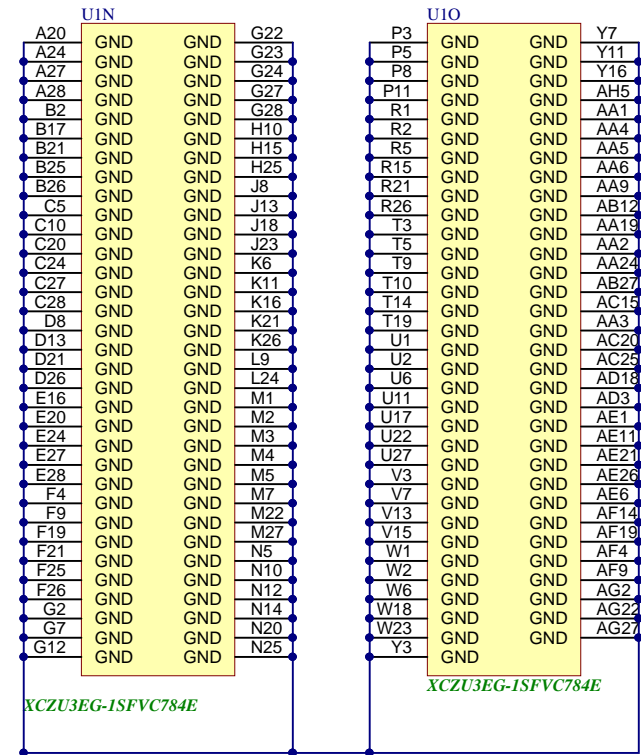
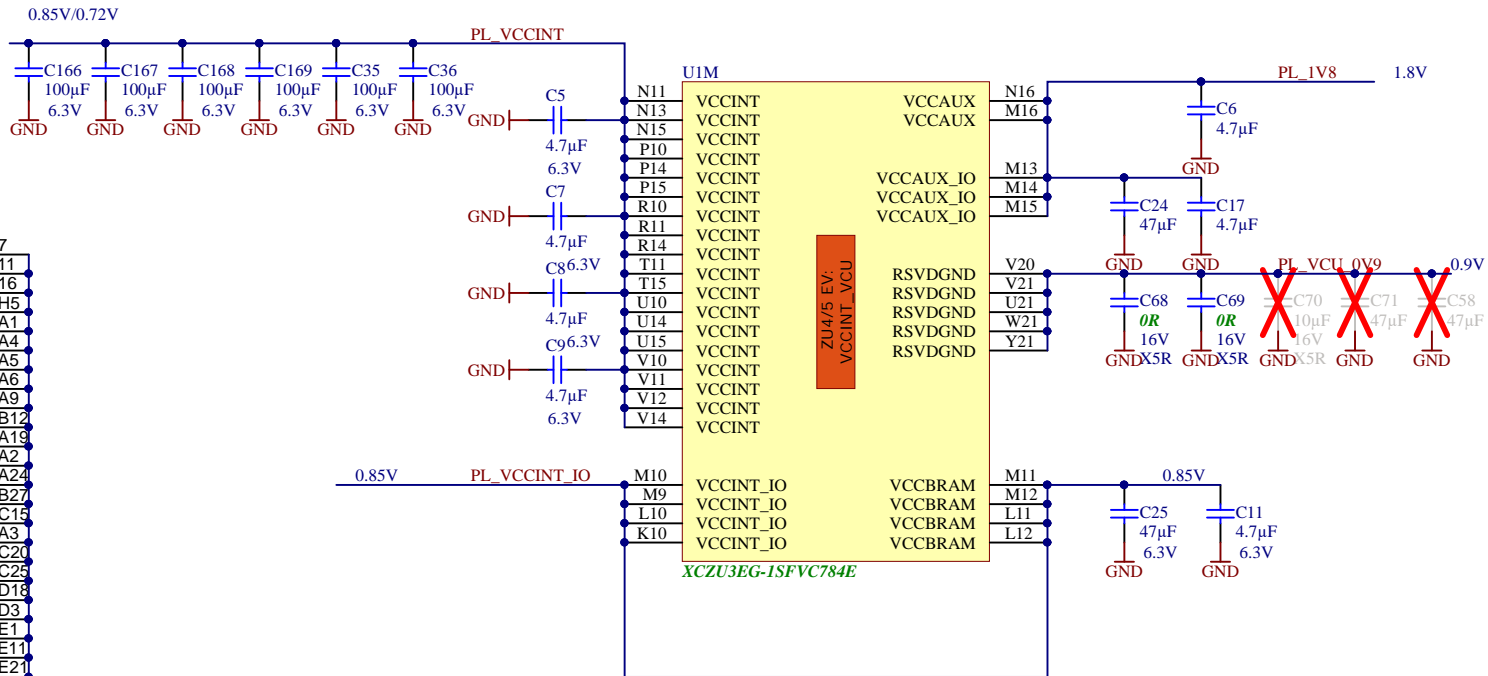
D

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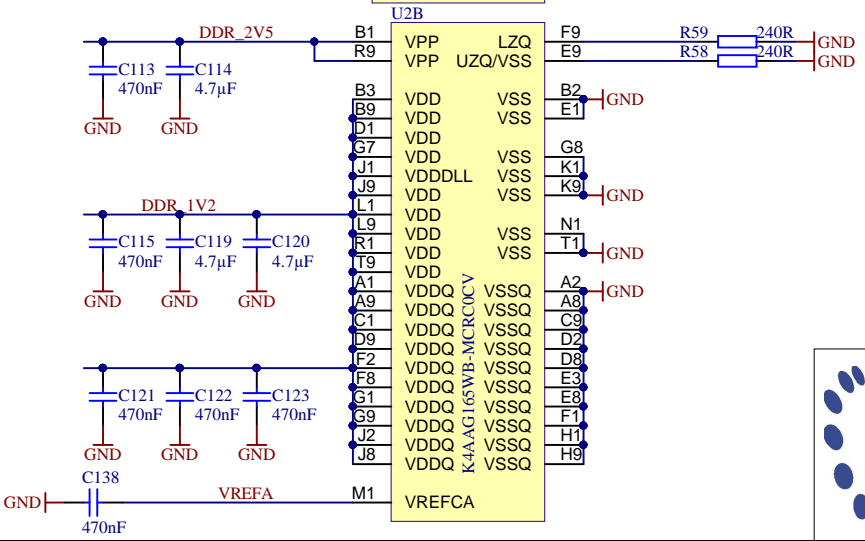
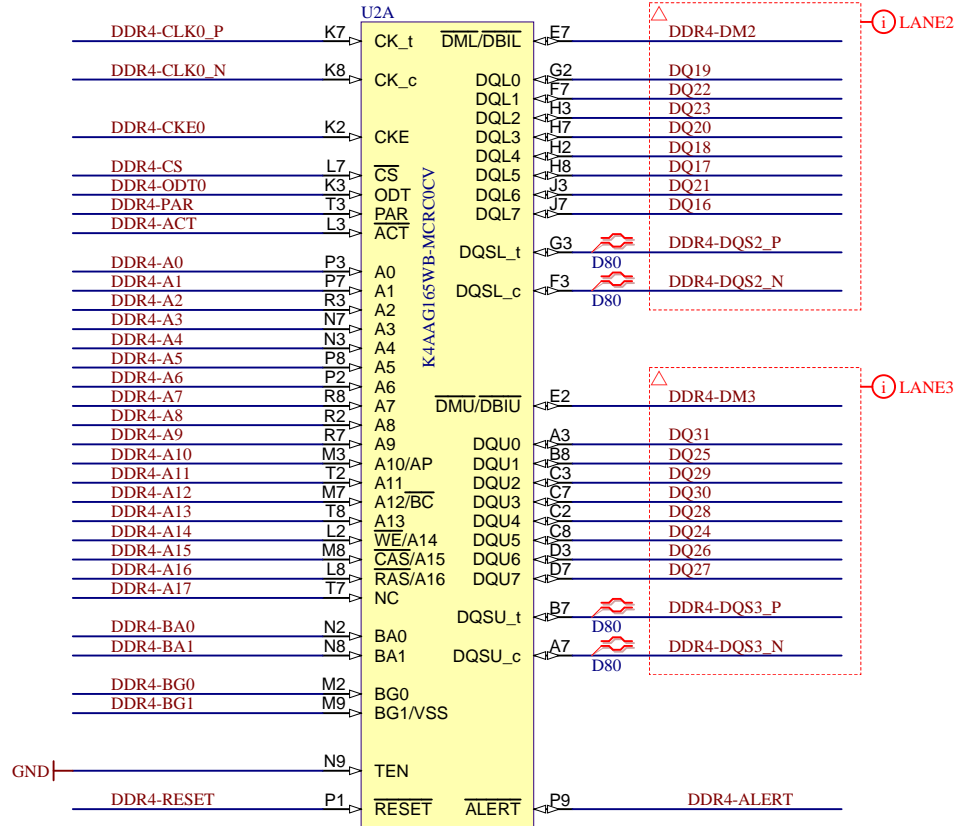
	Title: TE0803 - ZU_POWER		
	A4	Number: TE0803 3BE31-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 16 of 26
	Filename: ZU_POWER.SchDoc		

1

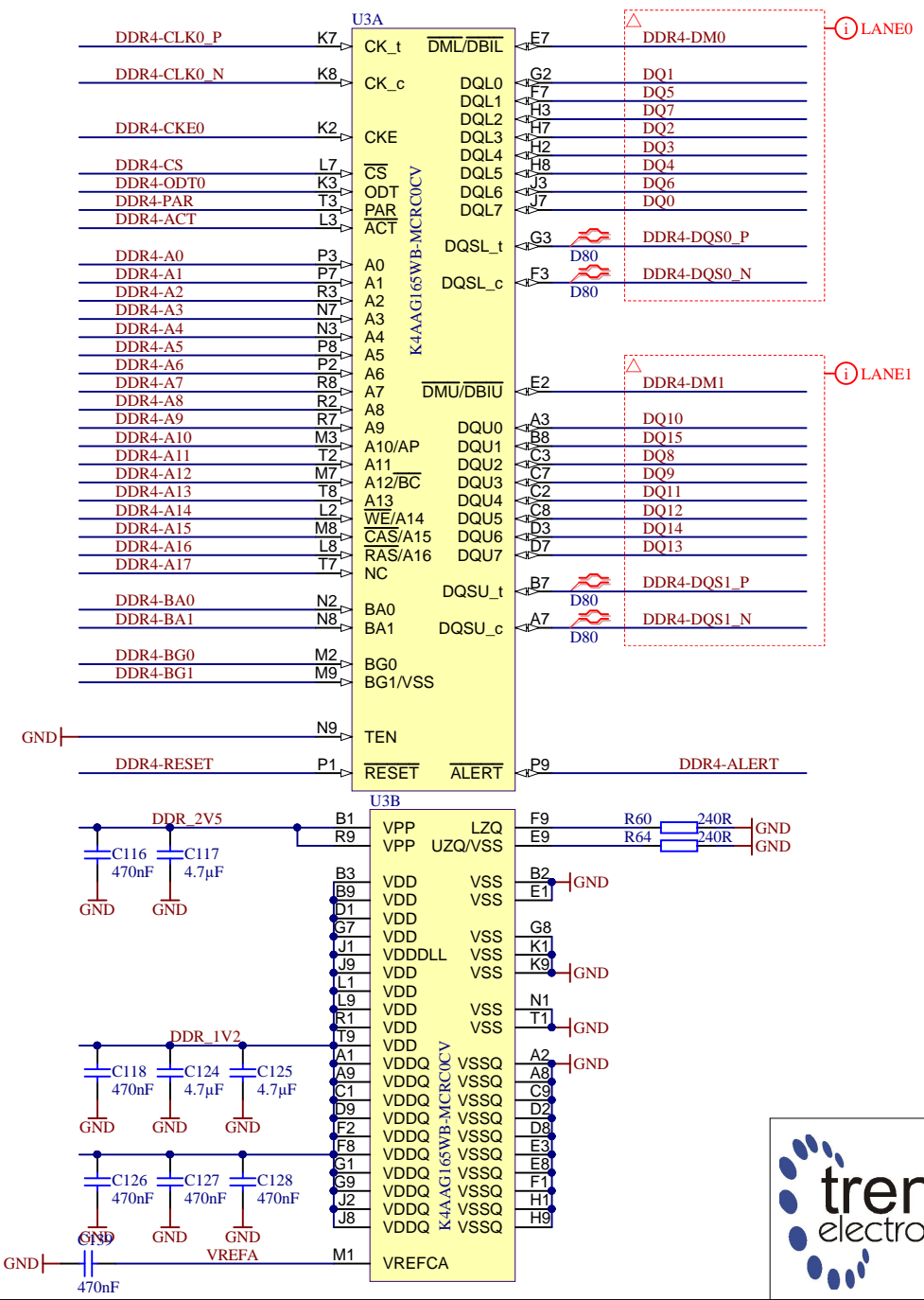
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3

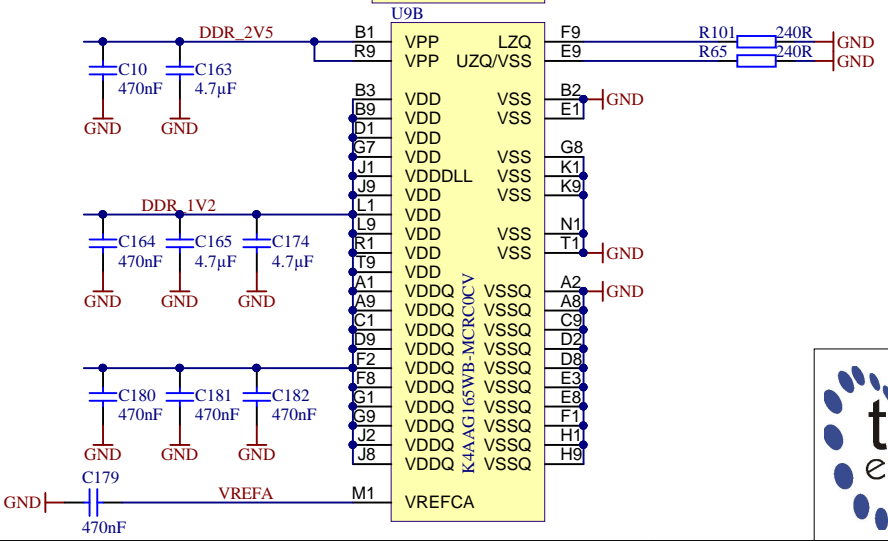
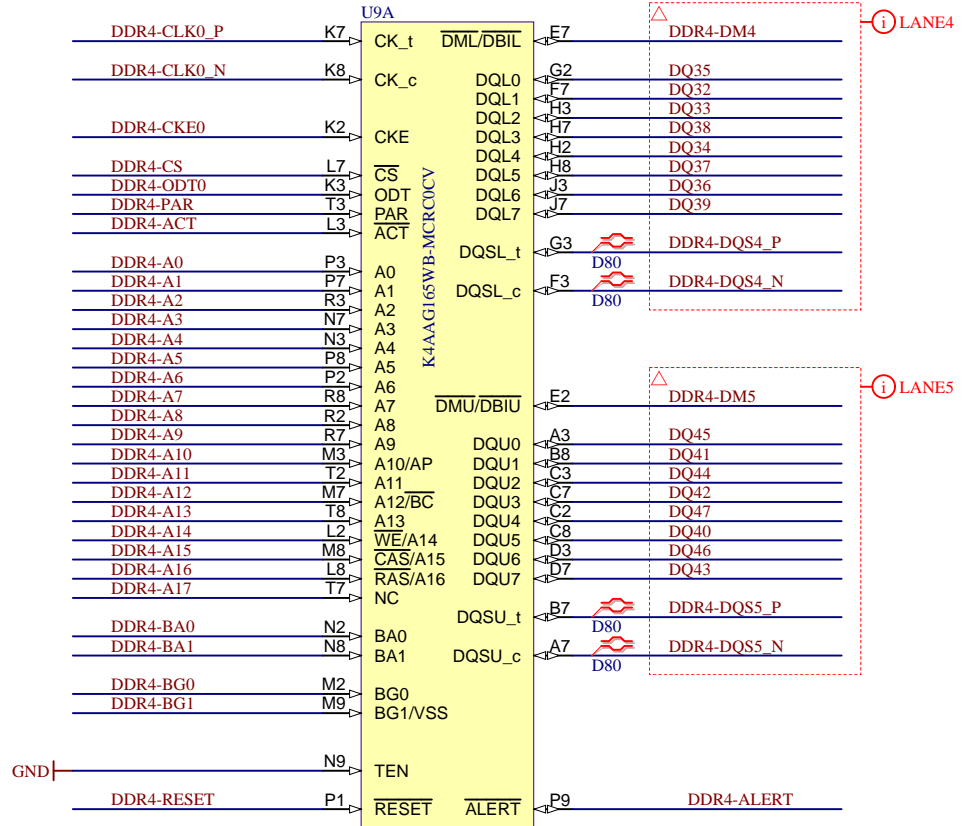
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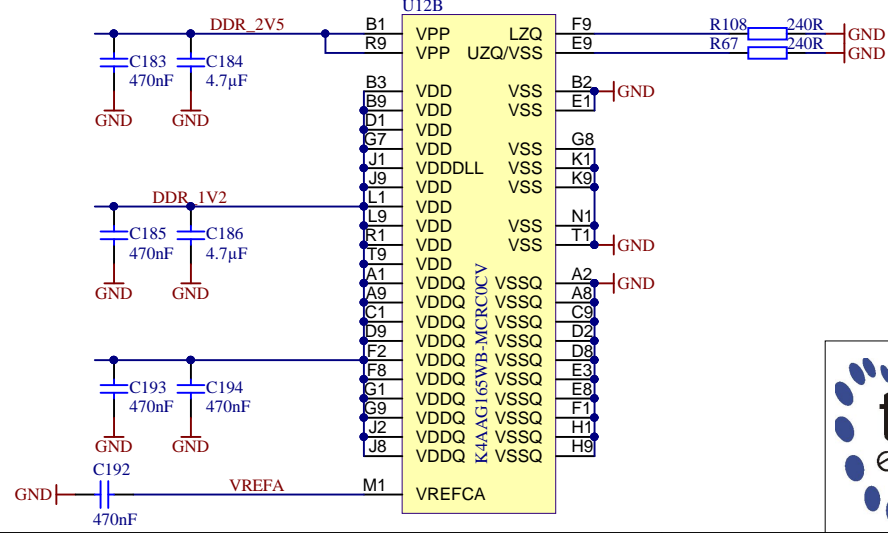
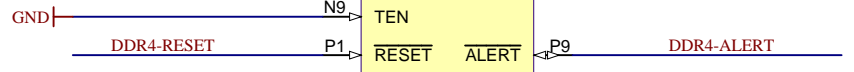
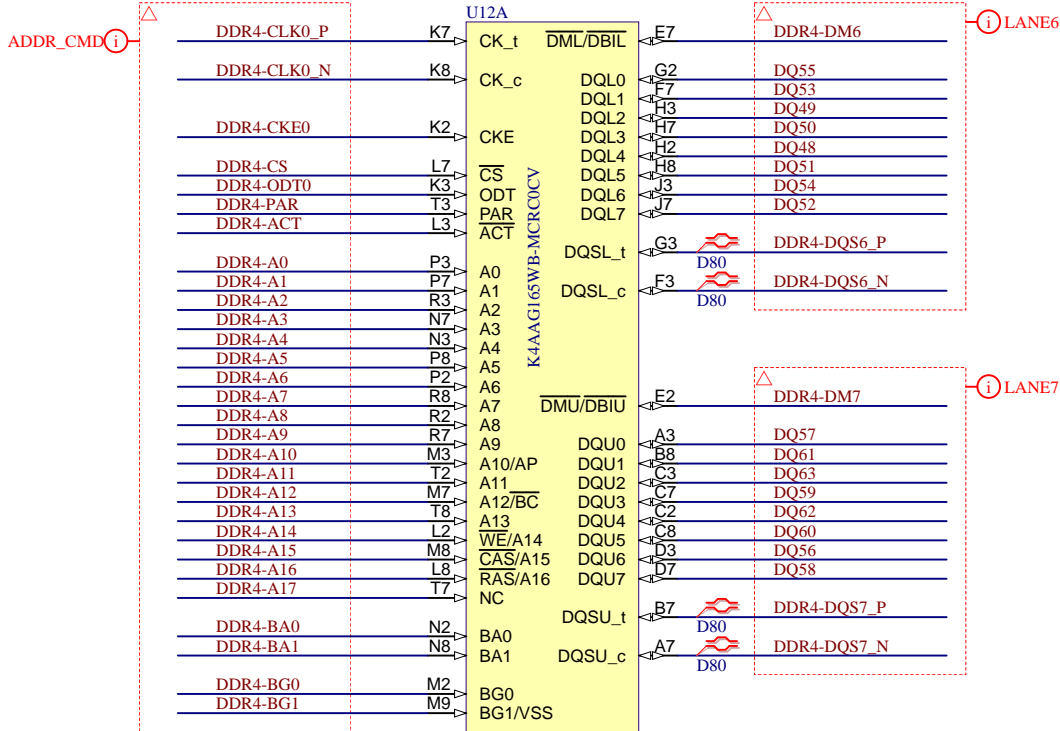

Title: TE0803 - DDR4_1_RAM		
A4	Number: TE0803 3BE31-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 17 of 26
Filename: DDR4-RAM.SchDoc		



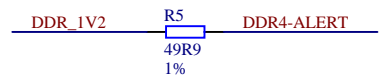
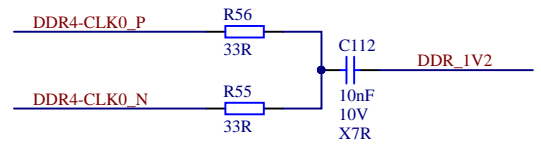
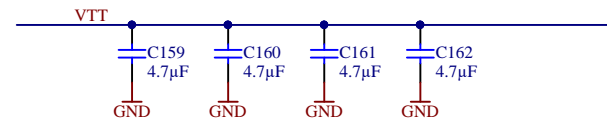
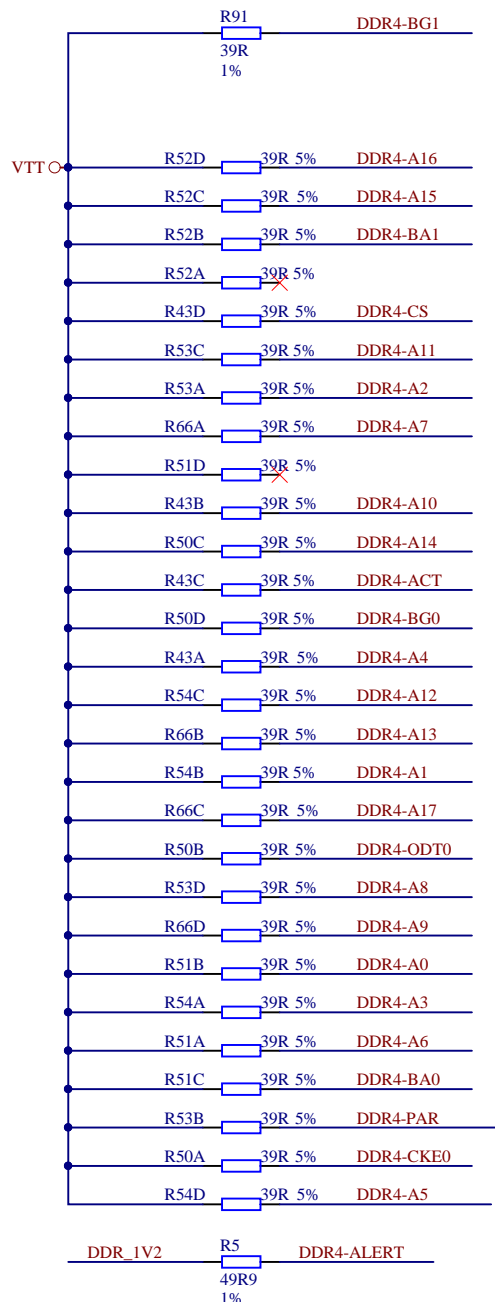
Title: TE0803 - DDR4_2_RAM		
A4	Number: TE0803 3BE31-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 18 of 26
Filename: DDR4-RAM_2.SchDoc		



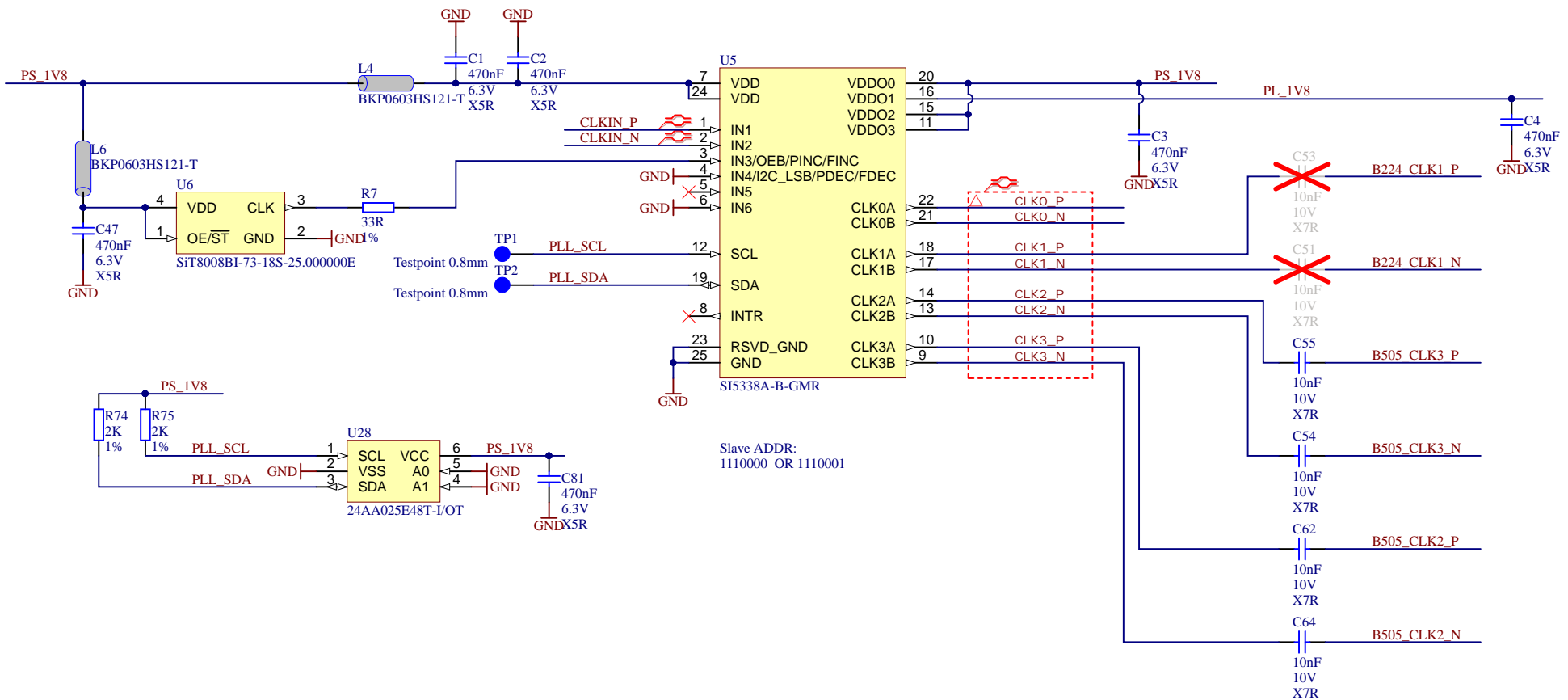
Title: TE0803 - DDR4_3_RAM		
A4	Number: TE0803 3BE31-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 19 of 26
Filename: DDR4-RAM_3.SchDoc		





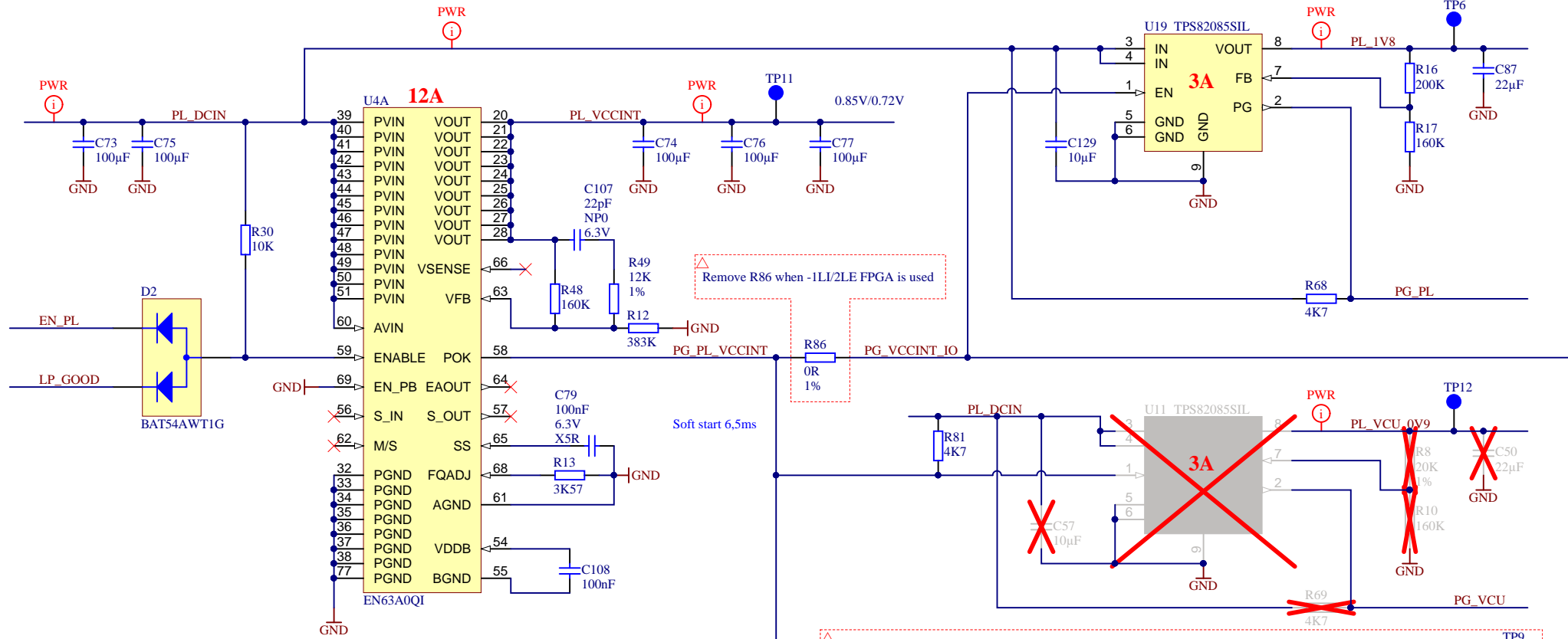
Title: TE0803 - DDR4_4_RAM		
A4	Number: TE0803 3BE31-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page20 of 26
Filename: DDR4-RAM_4.SchDoc		



Title: TE0803 - DDR4_TERM		
A4	Number: TE0803 3BE31-A	Rev. 03
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Filename: DDR4-TERM.SchDoc		



		Title: TE0803 - CLOCK	
		A4	Number: TE0803 3BE31-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
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Filename: Clock.SchDoc			



Remove R86 when -1L1/2LE FPGA is used

Add U33 when -1L1/2LE FPGA is used

Remove R87/89 when -1L1/2LE FPGA is used

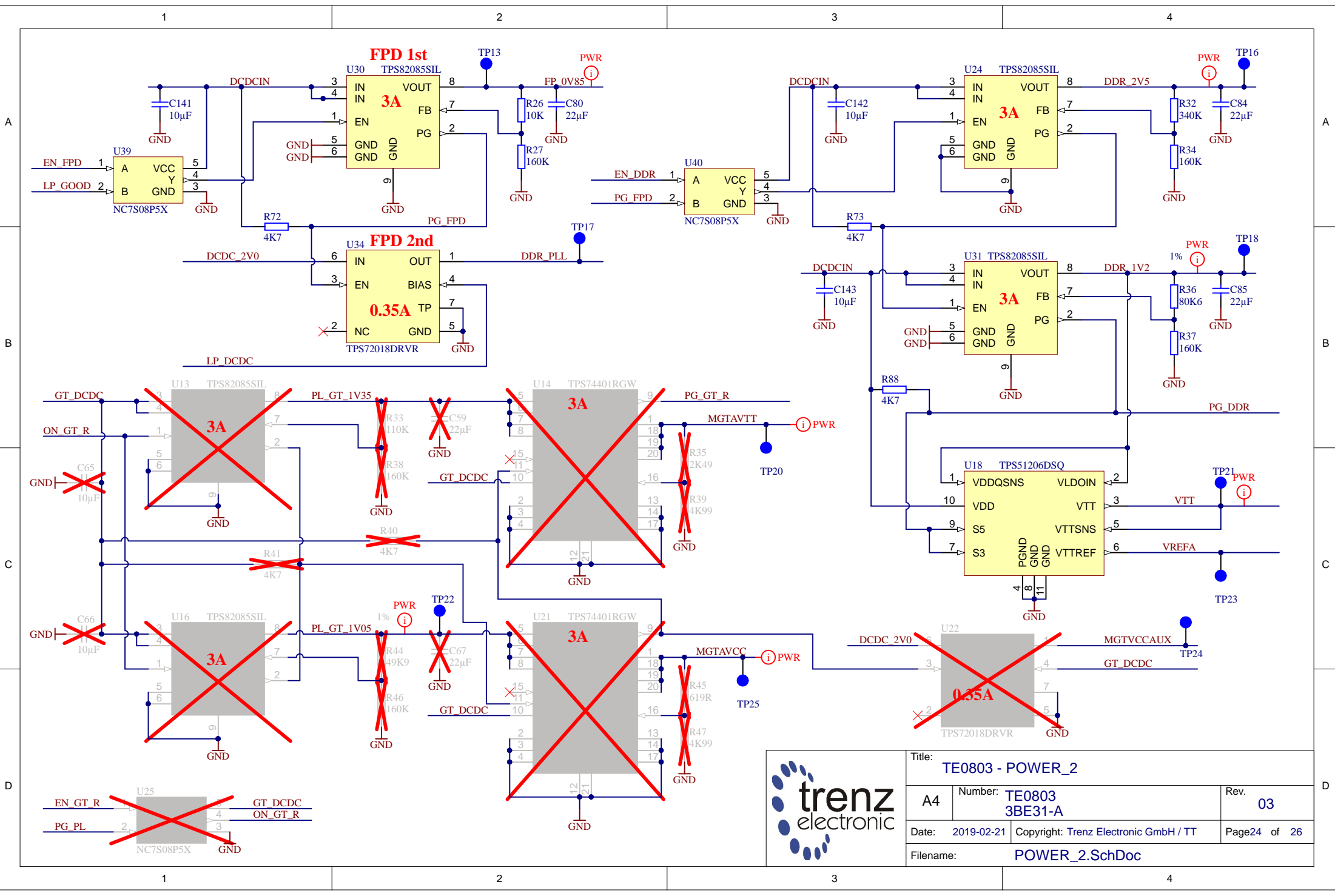
Soft start 6,5ms

U4B		
1	NC	NC
2	NC	NC
3	NC	NC
4	NC	NC
5	NC	NC
6	NC	NC(SW)
7	NC	NC(SW)
8	NC	NC
9	NC	NC
10	NC	NC
11	NC	NC(SW)
12	NC	NC(SW)
13	NC	NC
14	NC	NC
15	NC	NC
16	NC	NC

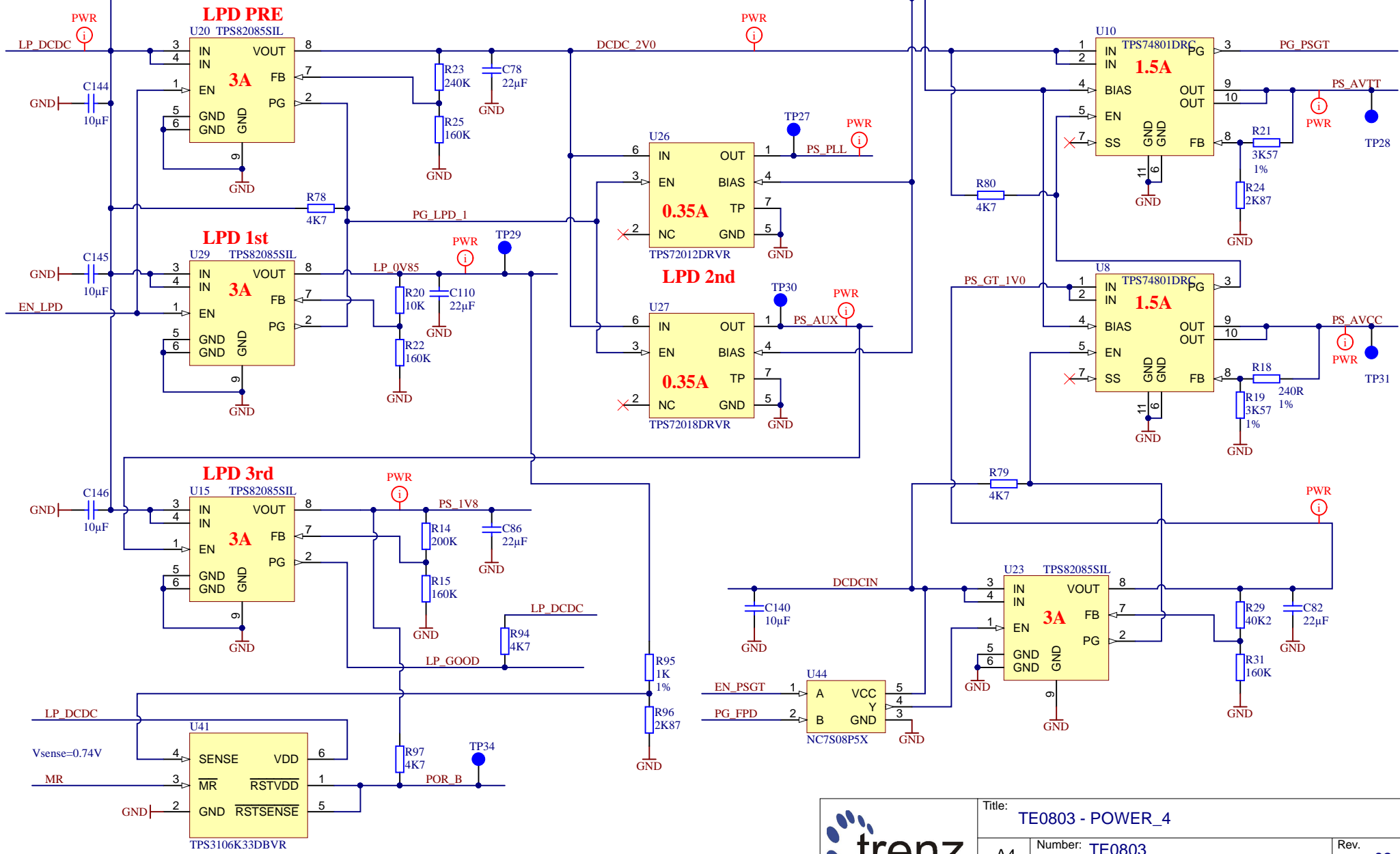
EN63A0QI		
17	NC	17
18	NC	18
19	NC	19
20	NC	20
21	NC	21
22	NC	22
23	NC	23
24	NC	24
25	NC	25
26	NC	26
27	NC	27
28	NC	28
29	NC	29
30	NC	30
31	NC	31
32	NC	32
33	NC	33
34	NC	34
35	NC	35
36	NC	36
37	NC	37
38	NC	38
39	NC	39
40	NC	40
41	NC	41
42	NC	42
43	NC	43
44	NC	44
45	NC	45
46	NC	46
47	NC	47
48	NC	48
49	NC	49
50	NC	50
51	NC	51
52	NC	52
53	NC	53
54	NC	54
55	NC	55
56	NC	56
57	NC	57
58	NC	58
59	NC	59
60	NC	60
61	NC	61
62	NC	62
63	NC	63
64	NC	64
65	NC	65
66	NC	66
67	NC	67
68	NC	68
69	NC	69
70	NC	70
71	NC	71
72	NC	72
73	NC	73
74	NC	74
75	NC	75
76	NC	76



Title: TE0803 - POWER		
A4	Number: TE0803 3BE31-A	Rev. 03
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Filename: POWER.SchDoc		



Title: TE0803 - POWER_2		
A4	Number: TE0803 3BE31-A	Rev. 03
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Filename: POWER_2.SchDoc		



Title: TE0803 - POWER_4		
A4	Number: TE0803 3BE31-A	Rev. 03
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Filename: POWER_4.SchDoc		

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CHANGES REV01a (20.11.2017):

- 1) VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9.

CHANGES REV02 (20.06.2018):

- 1) Added LDO to DDR_PLL
- 2) All differential pairs with length matched with tolerance 0.1mm (excluding package delays)
- 3) Added MAC EEPROM U28
- 4) VPS_MGTRAVCC set to 0.85V
- 5) Added pull-up resistors R68,R69

CHANGES REV03 (21.02.2019):

- 1) Added support of DDP DDR4
- 2) Added support of Low power FPGA (-L1/L2).
- 3) Revised testpoints
- 4) Revised J1-J4 connectors net label style

A

A

B


B

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D

D

		Title: TE0803 - Changes list		
		A4	Number: TE0803 3BE31-A	Rev. 03
		Date: 2019-02-21	Copyright: Trenz Electronic GmbH	Page 26 of 26
		Filename: Revision_Changes.SchDoc		

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