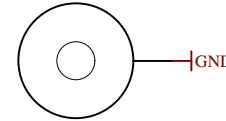
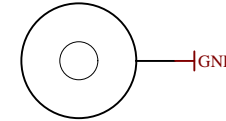


U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_DDR4-TERM DDR4-TERM.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_REV_CH Revision_Changes.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	
	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

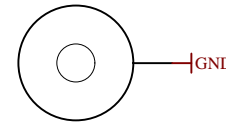
Special notes:



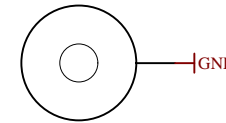
Mount.Hole 3.2mm für Unterlegscheibe



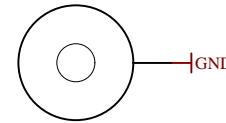
Mount.Hole 3.2mm für Unterlegscheibe



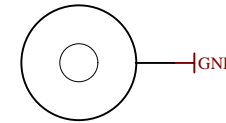
Mount.Hole 3.2mm für Unterlegscheibe



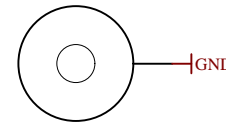
Mount.Hole 3.2mm für Unterlegscheibe



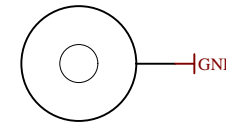
Mount.Hole 3.2mm für Unterlegscheibe



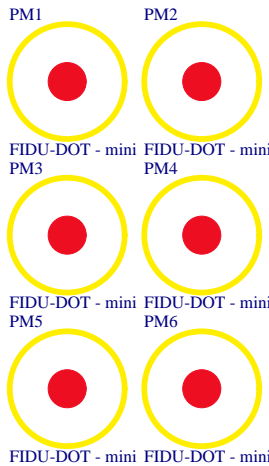
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe

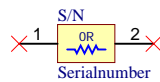


Mount.Hole 3.2mm für Unterlegscheibe



LOGO1  
TE Logo PRINT Layer  
LOGO PRINT

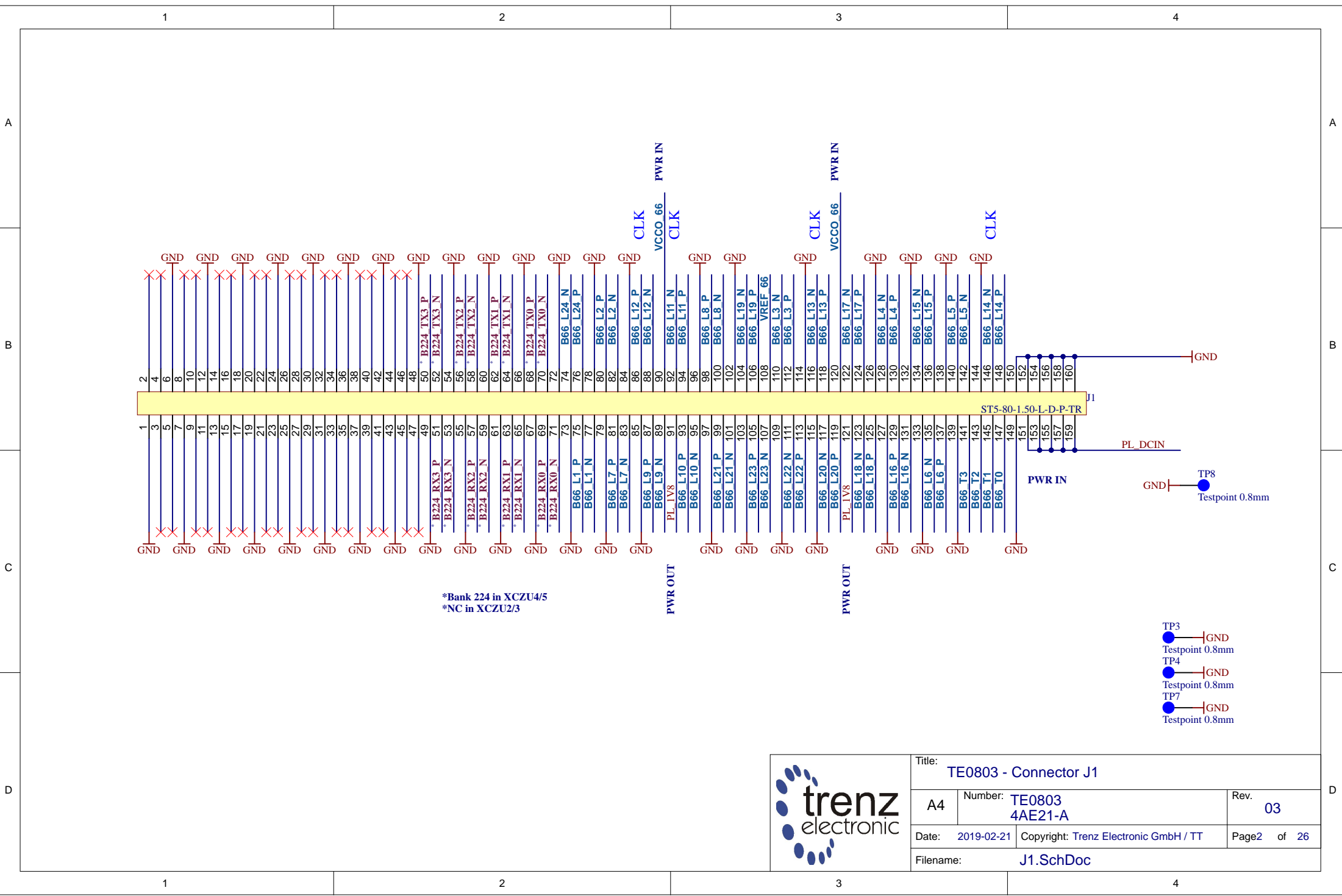
Serial  
Serialnummer 6,3 x 6.3mm



Assembly variant	4AE21-A
Created by	VY
Modified by	VY
Modified at	2020-07-23
SVN Revision	9226



Title: <b>TE0803</b>		
A4	Number: <b>TE0803 4AE21-A</b>	Rev. <b>03</b>
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page1 of 26
Filename: <b>TE0803.SchDoc</b>		



\*Bank 224 in XCZU4/5  
\*NC in XCZU2/3



Title: TE0803 - Connector J1		
A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page2 of 26
Filename: J1.SchDoc		

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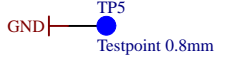
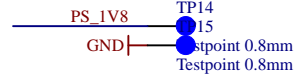
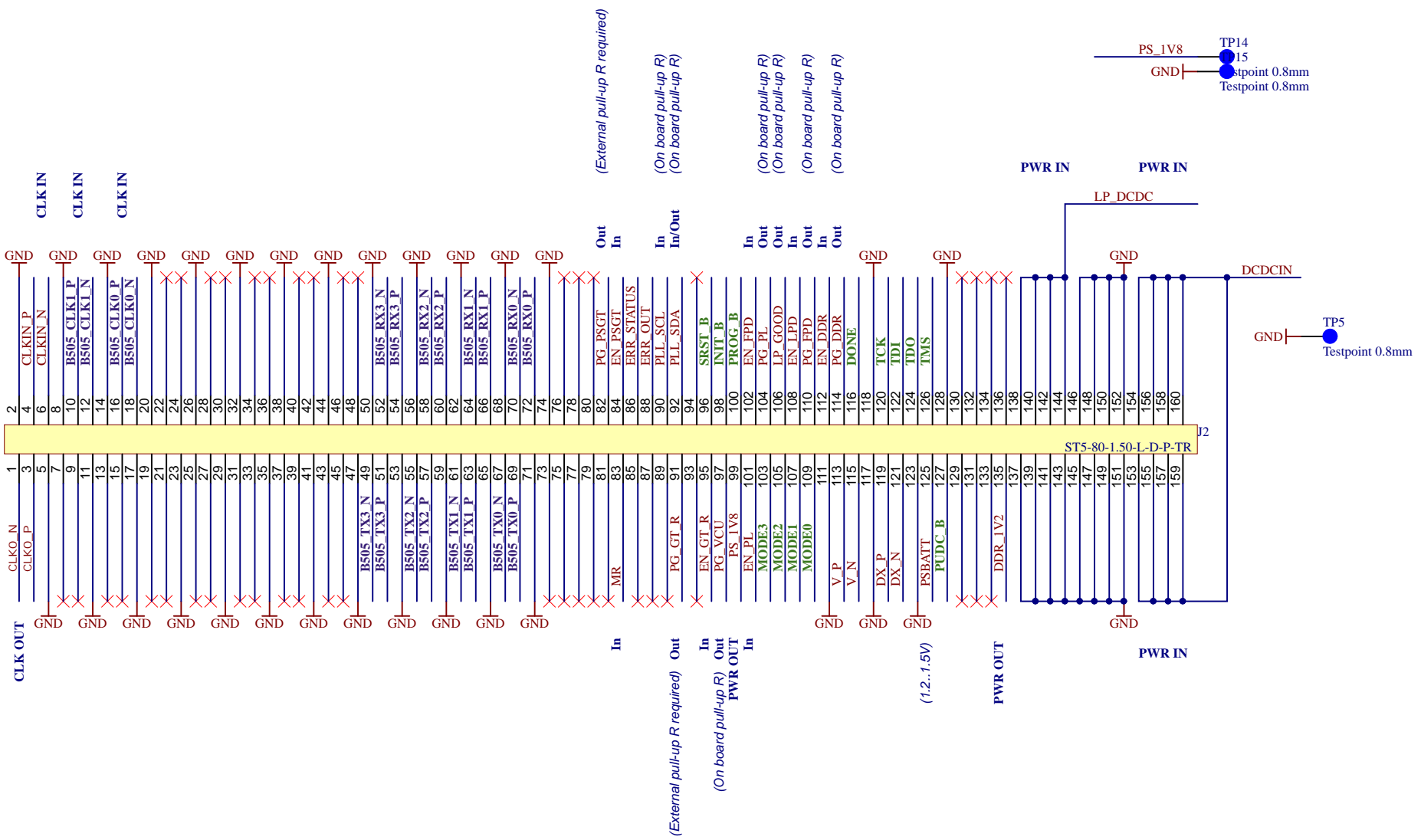
B


C

C

D

D



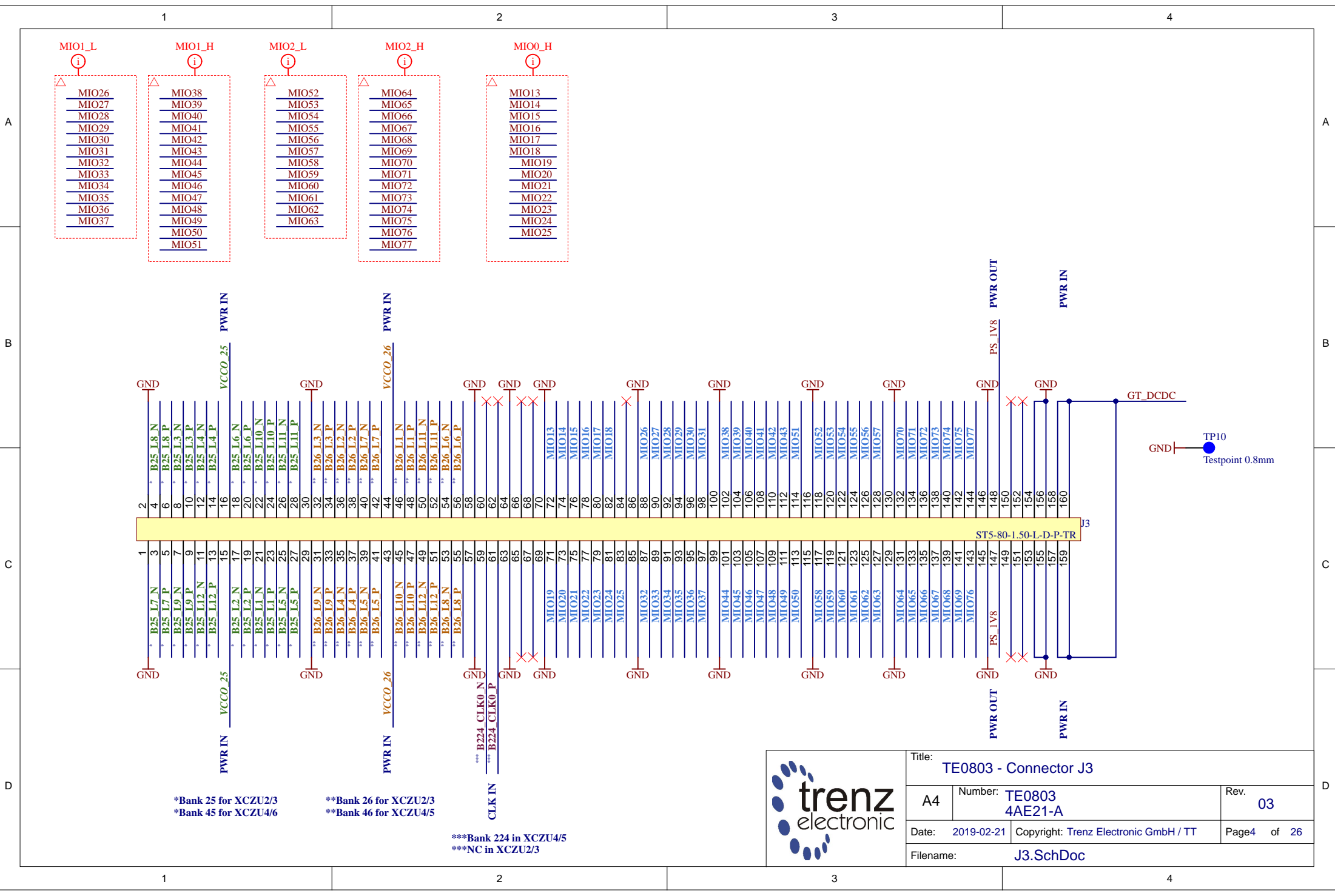
			Title: TE0803 - Connector J2	
			A4	Number: TE0803 4AE21-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT		Page3 of 26
Filename: J2.SchDoc				

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\*Bank 25 for XCZU2/3  
 \*Bank 45 for XCZU4/6

\*\*Bank 26 for XCZU2/3  
 \*\*Bank 46 for XCZU4/5

\*\*\*Bank 224 in XCZU4/5  
 \*\*\*NC in XCZU2/3



Title: TE0803 - Connector J3		
A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page4 of 26
Filename: J3.SchDoc		

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A

A

B

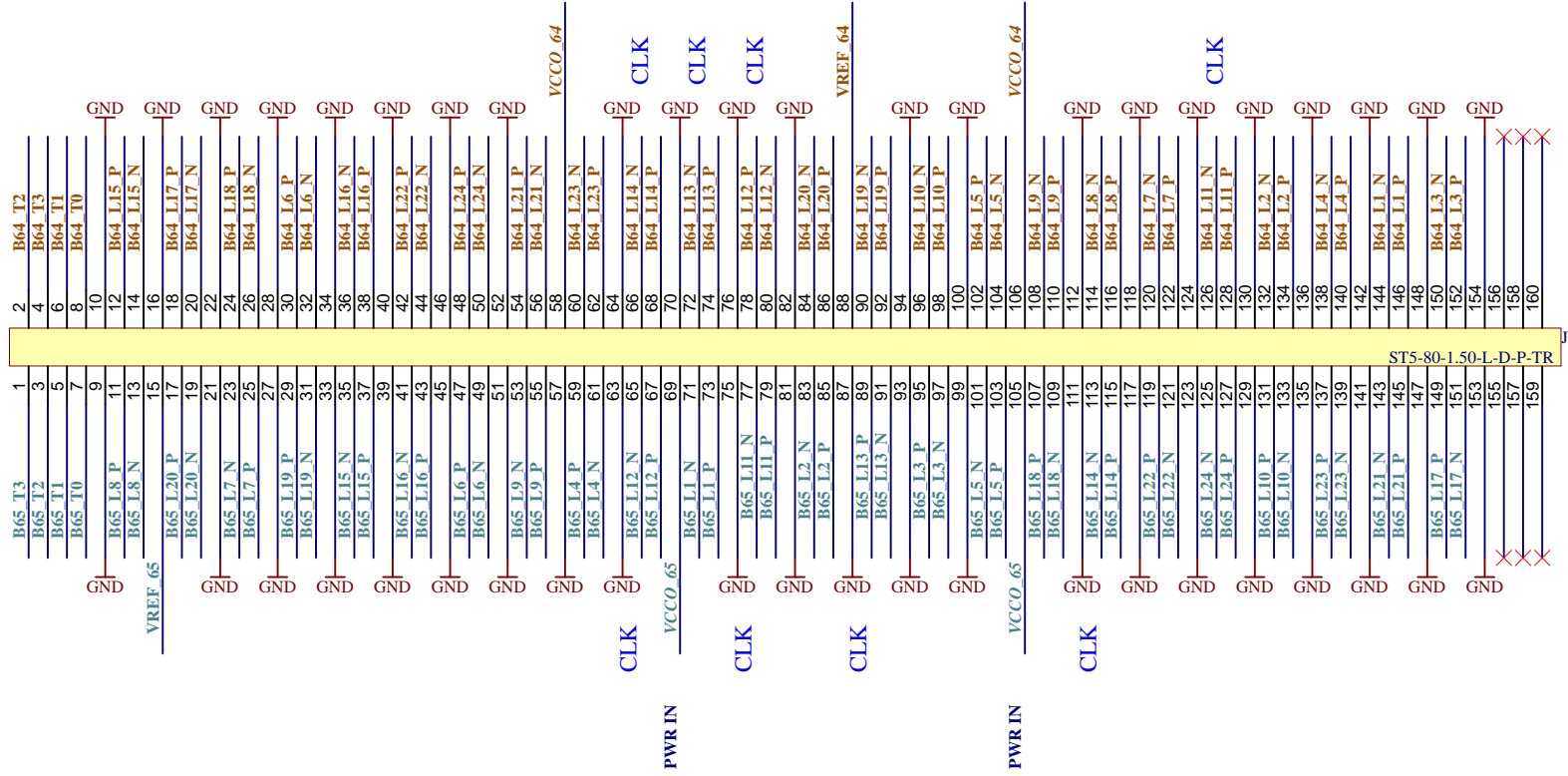
B

C

C

D

D



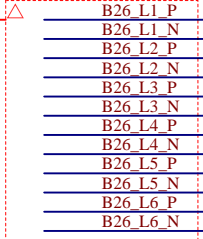
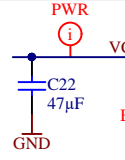
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A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page5 of 26
Filename: J4.SchDoc		

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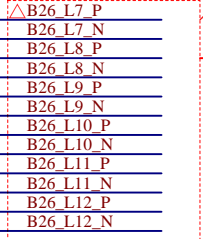
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**U1C XCZU4CG-1SFVC784E**  
BANK 46 HD (ZU2/3 BANK 26 HD)

F14	VCCO_46	B15	IO_L1P_AD11P_46	IO_L7P_HDGC_AD5P_46	G13	B26 L7 P
C15	VCCO_46	A15	IO_L1N_AD11N_46	IO_L7N_HDGC_AD5N_46	F13	B26 L7 N
		B14	IO_L2P_AD10P_46	IO_L8P_HDGC_AD4P_46	F15	B26 L8 P
		A14	IO_L2N_AD10N_46	IO_L8N_HDGC_AD4N_46	E15	B26 L8 N
		B13	IO_L3P_AD9P_46	IO_L9P_AD3P_46	G15	B26 L9 P
		A13	IO_L3N_AD9N_46	IO_L9N_AD3N_46	G14	B26 L9 N
		C14	IO_L4P_AD8P_46	IO_L10P_AD2P_46	H14	B26 L10 P
		C13	IO_L4N_AD8N_46	IO_L10N_AD2N_46	H13	B26 L10 N
		D15	IO_L5P_HDGC_AD7P_46	IO_L11P_AD1P_46	K14	B26 L11 P
		D14	IO_L5N_HDGC_AD7N_46	IO_L11N_AD1N_46	J14	B26 L11 N
		E14	IO_L6P_HDGC_AD6P_46	IO_L12P_AD0P_46	L14	B26 L12 P
		E13	IO_L6N_HDGC_AD6N_46	IO_L12N_AD0N_46	L13	B26 L12 N

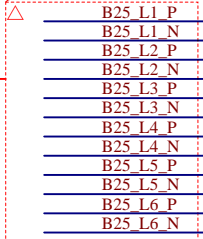
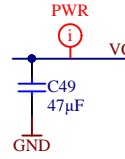


**BANK 43 HD (ZU2/3 BANK 44 HD)**

<del>AC10</del>	<del>VCCO_43</del>	<del>AG12</del>	<del>VCCO_43</del>	<del>AG10</del>	<del>IO_L1P_AD11P_43</del>	<del>IO_L7P_HDGC_AD5P_43</del>	<del>AD11</del>
<del>AG10</del>	<del>IO_L1N_AD11N_43</del>	<del>AH10</del>	<del>IO_L7N_HDGC_AD5N_43</del>	<del>AH10</del>	<del>IO_L2P_AD10P_43</del>	<del>IO_L8P_HDGC_AD4P_43</del>	<del>AD10</del>
<del>AF11</del>	<del>IO_L2N_AD10N_43</del>	<del>AG11</del>	<del>IO_L8N_HDGC_AD4N_43</del>	<del>AH11</del>	<del>IO_L3P_AD9P_43</del>	<del>IO_L9P_AD3P_43</del>	<del>AB11</del>
<del>AH12</del>	<del>IO_L3N_AD9N_43</del>	<del>AH12</del>	<del>IO_L9N_HDGC_AD3N_43</del>	<del>AA11</del>	<del>IO_L4P_AD8P_43</del>	<del>IO_L10P_AD2P_43</del>	<del>AC11</del>
<del>AH11</del>	<del>IO_L4N_AD8N_43</del>	<del>AE10</del>	<del>IO_L10N_AD2N_43</del>	<del>AA10</del>	<del>IO_L5P_HDGC_AD7P_43</del>	<del>IO_L11P_AD1P_43</del>	<del>AW10</del>
<del>AE10</del>	<del>IO_L5N_HDGC_AD7N_43</del>	<del>AF10</del>	<del>IO_L11N_AD1N_43</del>	<del>Y10</del>	<del>IO_L6P_HDGC_AD6P_43</del>	<del>IO_L12P_AD0P_43</del>	<del>Y9</del>
<del>AF12</del>	<del>IO_L6N_HDGC_AD6N_43</del>	<del>AE12</del>	<del>IO_L12N_AD0N_43</del>	<del>Y9</del>	<del>AD12</del>	<del>IO_L6N_HDGC_AD6N_43</del>	<del>AA8</del>
<del>AC13</del>		<del>AF12</del>		<del>AA8</del>	<del>AD12</del>		<del>AB10</del>
<del>AD12</del>		<del>AC13</del>		<del>AB10</del>	<del>AD12</del>		<del>AB9</del>
		<del>AD12</del>		<del>AB9</del>			

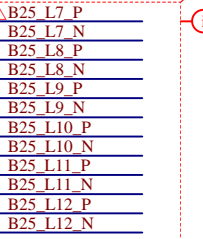
**U1B XCZU4CG-1SFVC784E**  
BANK 44 HD (ZU2/3 BANK 24 HD)

<del>AA14</del>	<del>VCCO_44</del>	<del>AD13</del>	<del>VCCO_44</del>	<del>AE15</del>	<del>IO_L1P_AD15P_44</del>	<del>IO_L7P_HDGC_44</del>	<del>AA13</del>
<del>AE15</del>	<del>IO_L1N_AD15N_44</del>	<del>AG14</del>	<del>IO_L7N_HDGC_44</del>	<del>AE14</del>	<del>IO_L2P_AD14P_44</del>	<del>IO_L8P_HDGC_44</del>	<del>AB13</del>
<del>AG14</del>	<del>IO_L2N_AD14N_44</del>	<del>AH14</del>	<del>IO_L8N_HDGC_44</del>	<del>AG14</del>	<del>IO_L3P_AD13P_44</del>	<del>IO_L9P_AD11P_44</del>	<del>AB15</del>
<del>AH14</del>	<del>IO_L3N_AD13N_44</del>	<del>AG13</del>	<del>IO_L9N_HDGC_44</del>	<del>AH13</del>	<del>IO_L4P_AD12P_44</del>	<del>IO_L10P_AD10P_44</del>	<del>AB14</del>
<del>AG13</del>	<del>IO_L4N_AD12N_44</del>	<del>AH13</del>	<del>IO_L10N_AD10N_44</del>	<del>AE13</del>	<del>IO_L5P_HDGC_44</del>	<del>IO_L11P_AD9P_44</del>	<del>W14</del>
<del>AH13</del>	<del>IO_L5N_HDGC_44</del>	<del>AE13</del>	<del>IO_L11N_AD9N_44</del>	<del>AF13</del>	<del>IO_L6P_HDGC_44</del>	<del>IO_L12P_AD8P_44</del>	<del>W13</del>
<del>AE13</del>	<del>IO_L6N_HDGC_44</del>	<del>AD13</del>	<del>IO_L12N_AD8N_44</del>	<del>AD13</del>	<del>IO_L6N_HDGC_44</del>	<del>IO_L12N_AD8N_44</del>	<del>Y14</del>
<del>AD13</del>		<del>AC14</del>		<del>AD13</del>			<del>Y13</del>
<del>AC14</del>		<del>AC13</del>		<del>AD13</del>			<del>W12</del>
<del>AC13</del>		<del>AC13</del>		<del>AD13</del>			<del>W11</del>
		<del>AC13</del>		<del>AD13</del>			<del>Y12</del>
		<del>AC13</del>		<del>AD13</del>			<del>AA12</del>

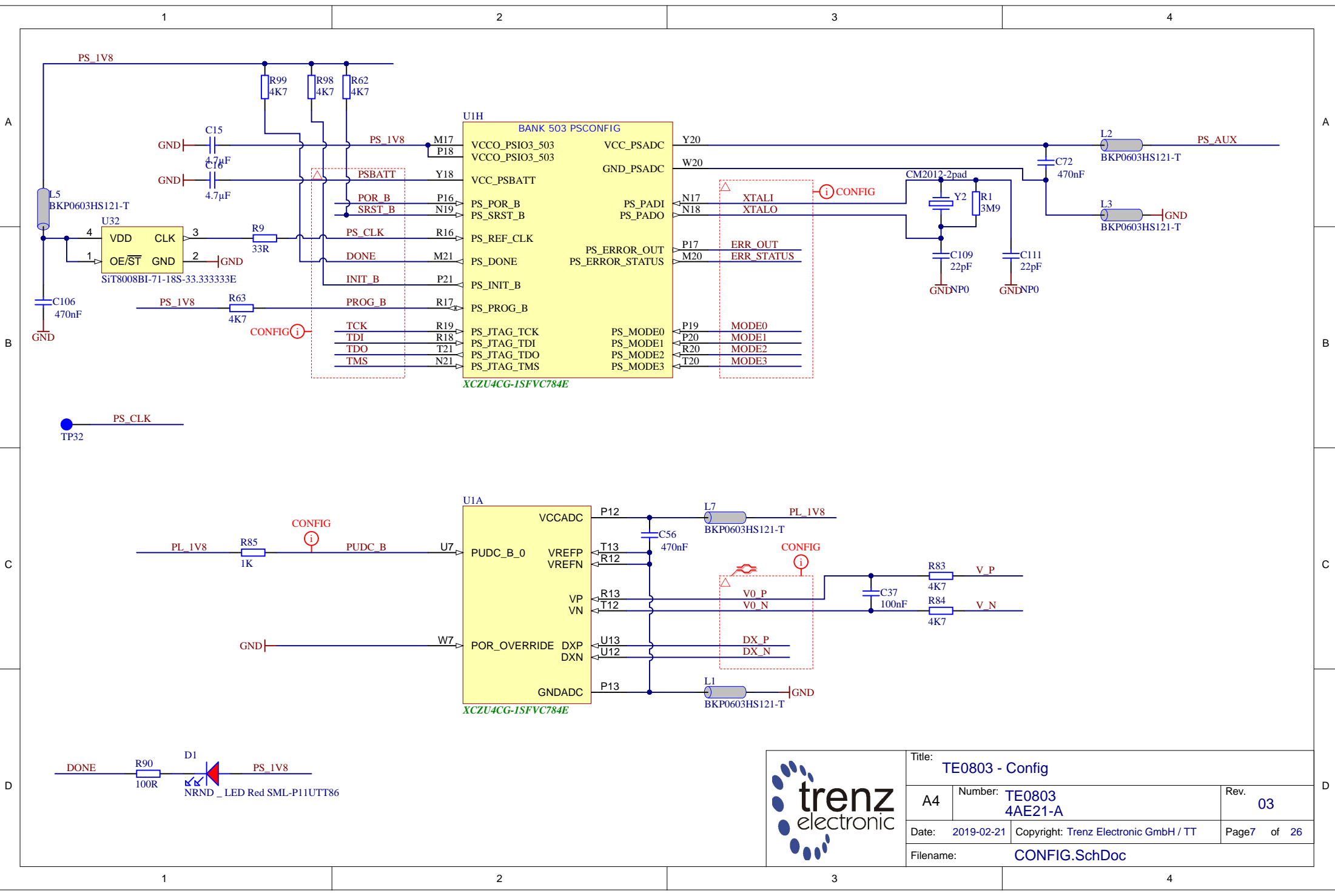


**BANK 45 HD (ZU2/3 BANK 25 HD)**

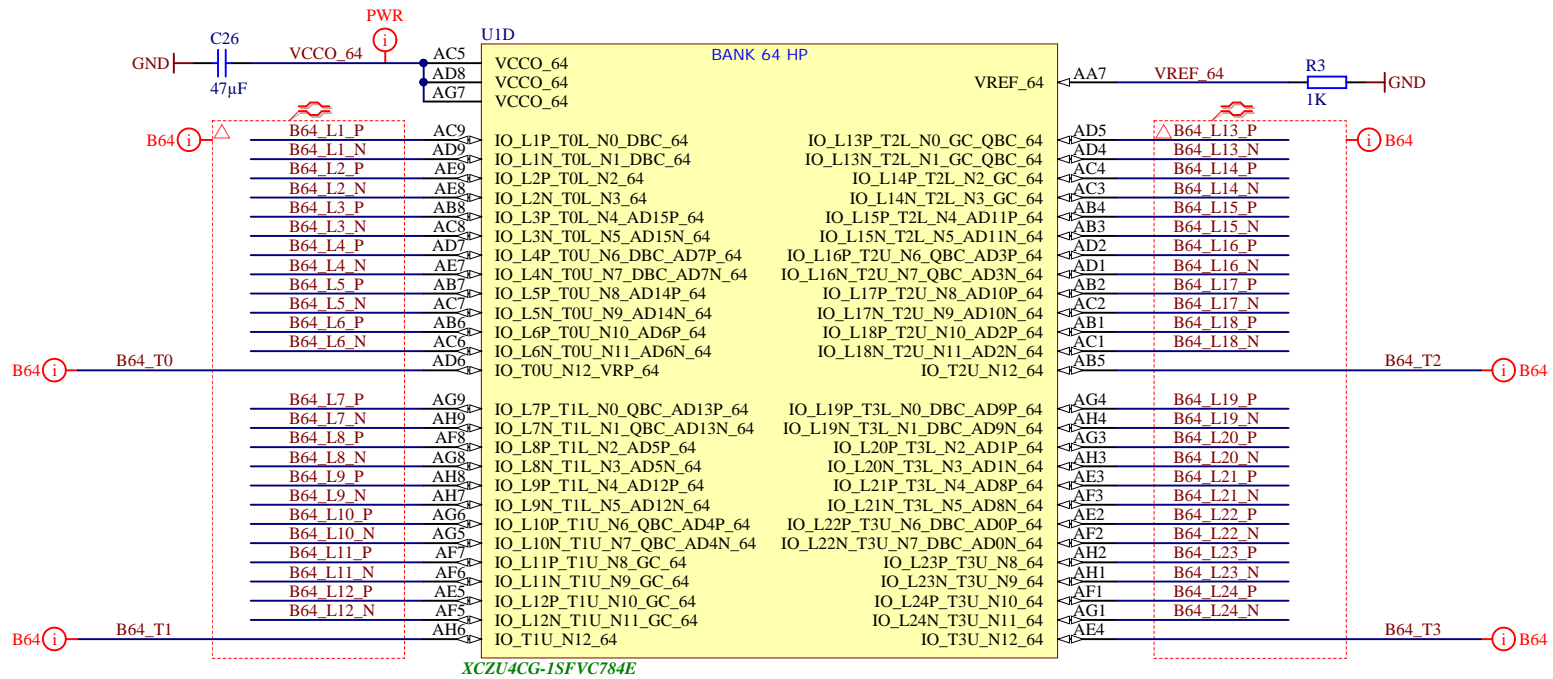
B12	VCCO_45	J11	IO_L1P_AD15P_45	IO_L7P_HDGC_45	E10	B25 L7 P
E11	VCCO_45	J10	IO_L1N_AD15N_45	IO_L7N_HDGC_45	D10	B25 L7 N
		K13	IO_L2P_AD14P_45	IO_L8P_HDGC_45	E12	B25 L8 P
		K12	IO_L2N_AD14N_45	IO_L8N_HDGC_45	D11	B25 L8 N
		H11	IO_L3P_AD13P_45	IO_L9P_AD11P_45	C11	B25 L9 P
		G10	IO_L3N_AD13N_45	IO_L9N_AD11N_45	B10	B25 L9 N
		J12	IO_L4P_AD12P_45	IO_L10P_AD10P_45	B11	B25 L10 P
		H12	IO_L4N_AD12N_45	IO_L10N_AD10N_45	A10	B25 L10 N
		G11	IO_L5P_HDGC_45	IO_L11P_AD9P_45	A12	B25 L11 P
		F11	IO_L5N_HDGC_45	IO_L11N_AD9N_45	A11	B25 L11 N
		F12	IO_L6P_HDGC_45	IO_L12P_AD8P_45	D12	B25 L12 P
		F11	IO_L6N_HDGC_45	IO_L12N_AD8N_45	C12	B25 L12 N



Title: <b>TE0803 - HD Banks</b>		
A4	Number: <b>TE0803 4AE21-A</b>	Rev. <b>03</b>
Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>6</b> of <b>26</b>
Filename: <b>B_HD.SchDoc</b>		

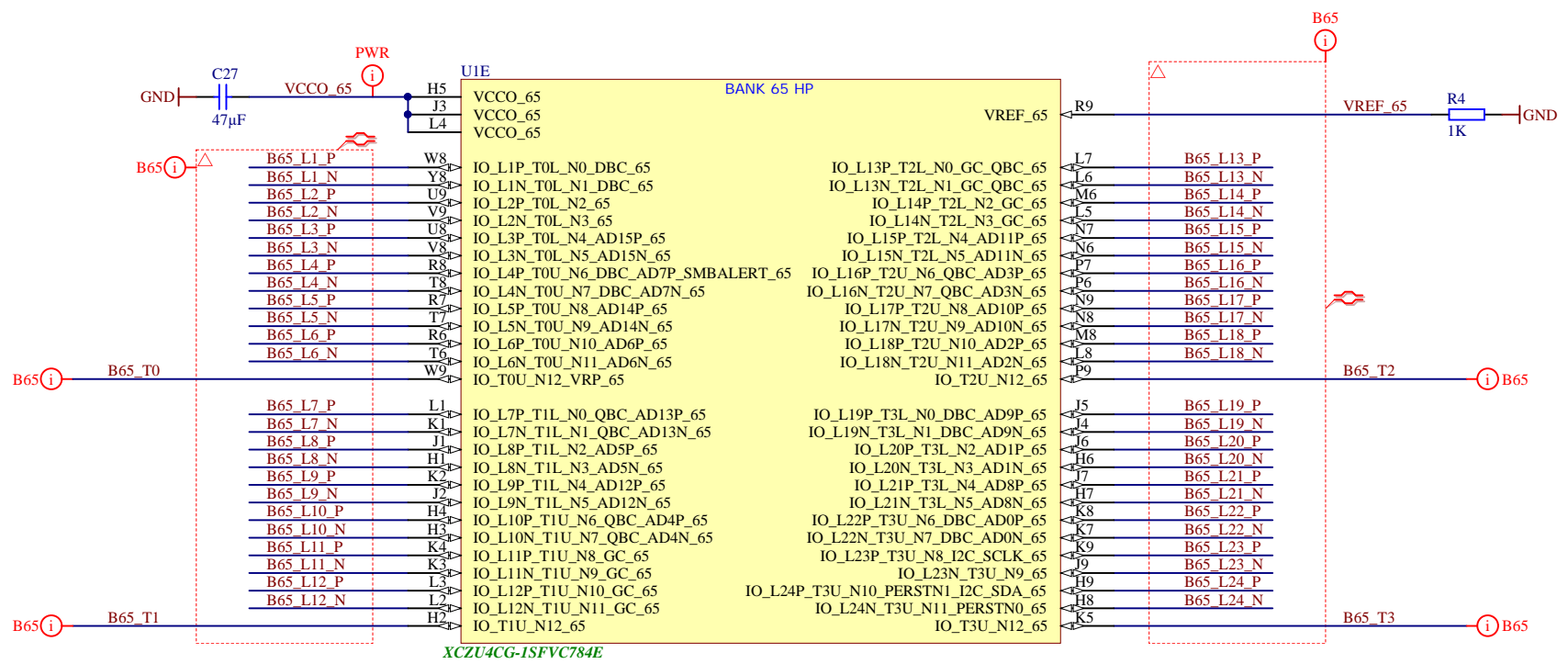


Title: TE0803 - Config		
A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 7 of 26
Filename: CONFIG.SchDoc		

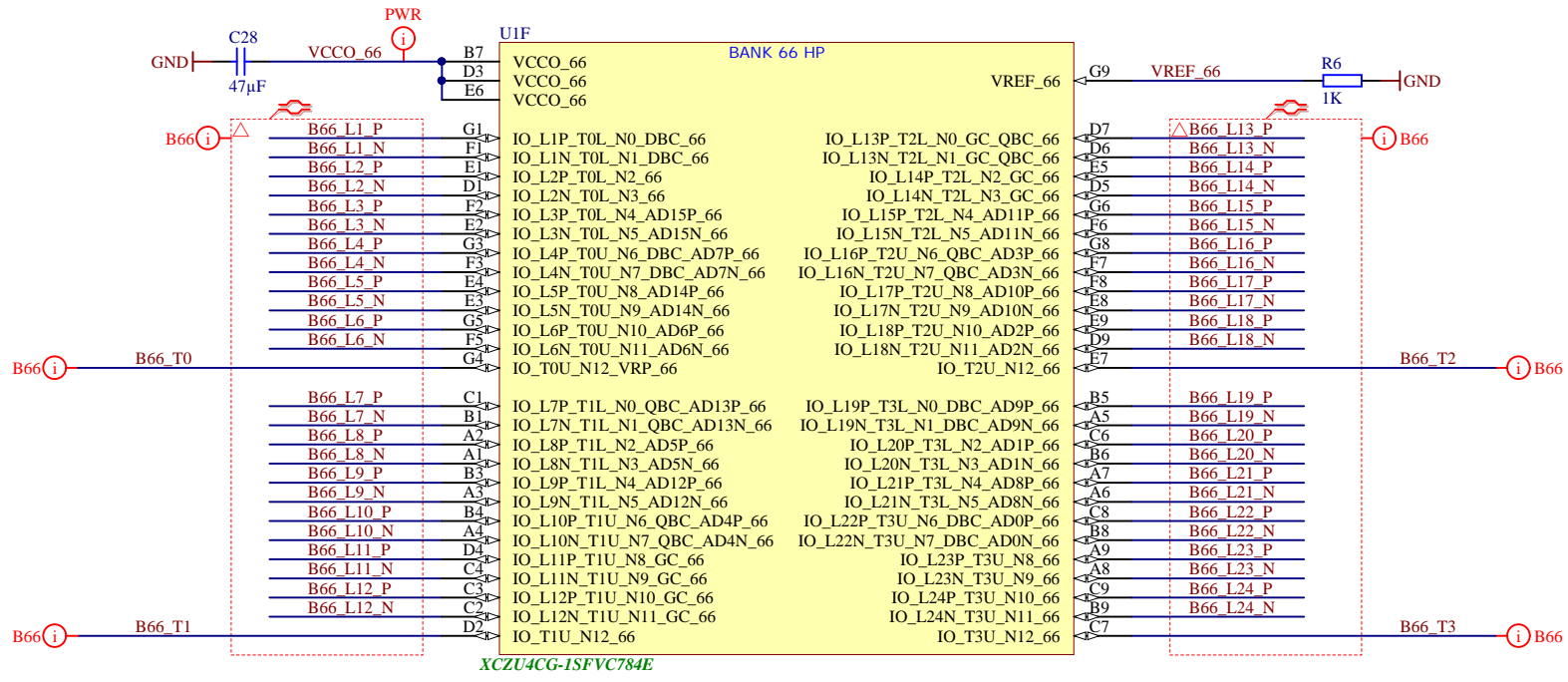


Title: <b>TE0803 - B64</b>		
A4	Number: <b>TE0803 4AE21-A</b>	Rev. <b>03</b>
Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>8</b> of <b>26</b>
Filename: <b>B64.SchDoc</b>		

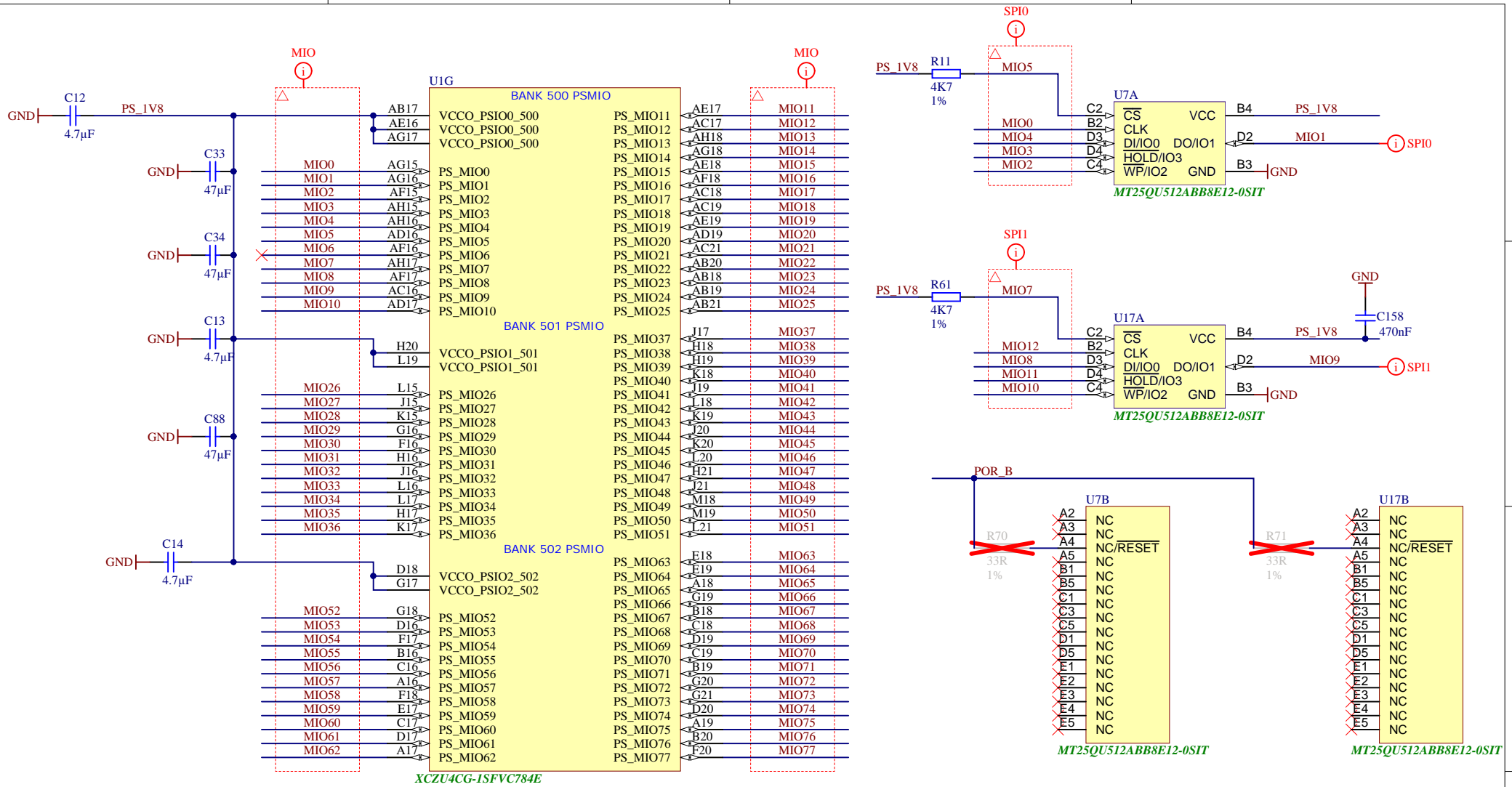




Title: TE0803 - B65		
A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page9 of 26
Filename: B65.SchDoc		



Title: TE0803 - B66		
A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 10 of 26
Filename: B66.SchDoc		



		Title: <b>TE0803 - MIO Banks</b>	
		A4	Number: <b>TE0803 4AE21-A</b> Date: 2019-02-21 Filename: <b>B_MIO.SchDoc</b>
		Copyright: Trenz Electronic GmbH / TT	Rev. <b>03</b>
		Page 11 of 26	

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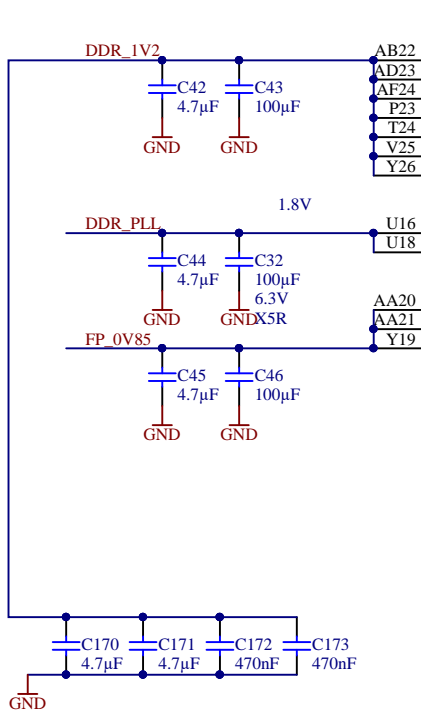
D

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U11		BANK 504 PSDDR			
VCCO_PSDDR_504	PS_DDR_CK0	W25	DDR4-CLK0 P	D80	
VCCO_PSDDR_504	PS_DDR_CK_N0	W26	DDR4-CLK0 N	D80	
VCCO_PSDDR_504	PS_DDR_CKE0	V28	DDR4-CKE0		
VCCO_PSDDR_504	PS_DDR_CK1	Y24			✗
VCCO_PSDDR_504	PS_DDR_CK_N1	Y25			✗
VCCO_PSDDR_504	PS_DDR_CKE1	V27			✗
VCC_PSDDR_PLL	PS_DDR_A0	W28	DDR4-A0		
VCC_PSDDR_PLL	PS_DDR_A1	Y28	DDR4-A1		
VCC_PSDDR_PLL	PS_DDR_A2	AB28	DDR4-A2		
VCC_PSDDR_PLL	PS_DDR_A3	AA28	DDR4-A3		
VCC_PSDDR_PLL	PS_DDR_A4	Y27	DDR4-A4		
VCC_PSINTRFP_DDR	PS_DDR_A5	AA27	DDR4-A5		
VCC_PSINTRFP_DDR	PS_DDR_A6	Y22	DDR4-A6		
VCC_PSINTRFP_DDR	PS_DDR_A7	AA23	DDR4-A7		
VCC_PSINTRFP_DDR	PS_DDR_A8	AA22	DDR4-A8		
VCC_PSINTRFP_DDR	PS_DDR_A9	AB23	DDR4-A9		
VCC_PSINTRFP_DDR	PS_DDR_A10	AA25	DDR4-A10		
VCC_PSINTRFP_DDR	PS_DDR_A11	AA26	DDR4-A11		
VCC_PSINTRFP_DDR	PS_DDR_A12	AB25	DDR4-A12		
VCC_PSINTRFP_DDR	PS_DDR_A13	AB26	DDR4-A13		
VCC_PSINTRFP_DDR	PS_DDR_A14	AB24	DDR4-A14		
VCC_PSINTRFP_DDR	PS_DDR_A15	AC24	DDR4-A15		
VCC_PSINTRFP_DDR	PS_DDR_A16	AC23	DDR4-A16		
VCC_PSINTRFP_DDR	PS_DDR_A17	AC22	DDR4-A17		
PS_DDR_CS_N0	PS_DDR_CS_N1	W27	DDR4-CS		
PS_DDR_CS_N0	PS_DDR_CS_N1	V26			✗
PS_DDR_BA0	PS_DDR_BA1	V23	DDR4-BA0		
PS_DDR_BA0	PS_DDR_BA1	W22	DDR4-BA1		
PS_DDR_BG0	PS_DDR_BG1	W24	DDR4-BG0		
PS_DDR_BG0	PS_DDR_BG1	V22	DDR4-BG1		
PS_DDR_PARITY	PS_DDR_RAM_RST_N	Y24	DDR4-PAR		
PS_DDR_RAM_RST_N	PS_DDR_ACT_N	U23	DDR4-RESET		
PS_DDR_ACT_N	PS_DDR_ALERT_N	Y23	DDR4-ACT		
PS_DDR_ALERT_N	PS_DDR_ALERT_N	U25	DDR4-ALERT		
PS_DDR_ZQ	PS_DDR_ZQ	U24		R2 240R	GND
PS_DDR_ODT0	PS_DDR_ODT1	U28	DDR4-ODT0		
PS_DDR_ODT0	PS_DDR_ODT1	U26			✗

XCZU4CG-1SFVC784E

U1J		BANK 504 PSDDR			
DQ0	AD21	PS_DDR_DQ0	PS_DDR_DQ32	T22	DQ32
DQ1	AE20	PS_DDR_DQ1	PS_DDR_DQ33	R22	DQ33
DQ2	AD20	PS_DDR_DQ2	PS_DDR_DQ34	P22	DQ34
DQ3	AF20	PS_DDR_DQ3	PS_DDR_DQ35	N22	DQ35
DQ4	AH21	PS_DDR_DQ4	PS_DDR_DQ36	T23	DQ36
DQ5	AH20	PS_DDR_DQ5	PS_DDR_DQ37	P24	DQ37
DQ6	AH19	PS_DDR_DQ6	PS_DDR_DQ38	R24	DQ38
DQ7	AG19	PS_DDR_DQ7	PS_DDR_DQ39	N24	DQ39
DQ8	AF22	PS_DDR_DQ8	PS_DDR_DQ40	H24	DQ40
DQ9	AH22	PS_DDR_DQ9	PS_DDR_DQ41	J24	DQ41
DQ10	AE22	PS_DDR_DQ10	PS_DDR_DQ42	M24	DQ42
DQ11	AD22	PS_DDR_DQ11	PS_DDR_DQ43	K24	DQ43
DQ12	AH23	PS_DDR_DQ12	PS_DDR_DQ44	J22	DQ44
DQ13	AH24	PS_DDR_DQ13	PS_DDR_DQ45	H22	DQ45
DQ14	AE24	PS_DDR_DQ14	PS_DDR_DQ46	K22	DQ46
DQ15	AG24	PS_DDR_DQ15	PS_DDR_DQ47	J22	DQ47
DQ16	AC26	PS_DDR_DQ16	PS_DDR_DQ48	M25	DQ48
DQ17	AD26	PS_DDR_DQ17	PS_DDR_DQ49	M26	DQ49
DQ18	AD25	PS_DDR_DQ18	PS_DDR_DQ50	L25	DQ50
DQ19	AD24	PS_DDR_DQ19	PS_DDR_DQ51	L26	DQ51
DQ20	AG26	PS_DDR_DQ20	PS_DDR_DQ52	K28	DQ52
DQ21	AH25	PS_DDR_DQ21	PS_DDR_DQ53	L28	DQ53
DQ22	AH26	PS_DDR_DQ22	PS_DDR_DQ54	M28	DQ54
DQ23	AG25	PS_DDR_DQ23	PS_DDR_DQ55	N28	DQ55
DQ24	AH27	PS_DDR_DQ24	PS_DDR_DQ56	J28	DQ56
DQ25	AH28	PS_DDR_DQ25	PS_DDR_DQ57	K27	DQ57
DQ26	AF28	PS_DDR_DQ26	PS_DDR_DQ58	H28	DQ58
DQ27	AG28	PS_DDR_DQ27	PS_DDR_DQ59	H27	DQ59
DQ28	AC27	PS_DDR_DQ28	PS_DDR_DQ60	G26	DQ60
DQ29	AD27	PS_DDR_DQ29	PS_DDR_DQ61	G25	DQ61
DQ30	AD28	PS_DDR_DQ30	PS_DDR_DQ62	K25	DQ62
DQ31	AC28	PS_DDR_DQ31	PS_DDR_DQ63	J25	DQ63
DDR4-DQS0 P	AF21	PS_DDR_DQS_P0	PS_DDR_DQ64	T28	
DDR4-DQS0 N	AG21	PS_DDR_DQS_N0	PS_DDR_DQ65	R28	
DDR4-DQS1 P	AF23	PS_DDR_DQS_P1	PS_DDR_DQ66	P28	
DDR4-DQS1 N	AG23	PS_DDR_DQS_N1	PS_DDR_DQ67	P27	
DDR4-DQS2 P	AF25	PS_DDR_DQS_P2	PS_DDR_DQ68	P26	
DDR4-DQS2 N	AF26	PS_DDR_DQS_N2	PS_DDR_DQ69	R25	
DDR4-DQS3 P	AE27	PS_DDR_DQS_P3	PS_DDR_DQ70	P25	
DDR4-DQS3 N	AF27	PS_DDR_DQS_N3	PS_DDR_DQ71	T25	
DDR4-DQS4 P	N23	PS_DDR_DQS_P4	PS_DDR_DQ72		
DDR4-DQS4 N	M23	PS_DDR_DQS_N4	PS_DDR_DM0	AG20	DDR4-DM0
DDR4-DQS5 P	L23	PS_DDR_DQS_P5	PS_DDR_DM1	AE23	DDR4-DM1
DDR4-DQS5 N	K23	PS_DDR_DQS_N5	PS_DDR_DM2	AE25	DDR4-DM2
DDR4-DQS6 P	N26	PS_DDR_DQS_P6	PS_DDR_DM3	AE28	DDR4-DM3
DDR4-DQS6 N	N27	PS_DDR_DQS_N6	PS_DDR_DM4	R23	DDR4-DM4
DDR4-DQS7 P	J26	PS_DDR_DQS_P7	PS_DDR_DM5	H23	DDR4-DM5
DDR4-DQS7 N	J27	PS_DDR_DQS_N7	PS_DDR_DM6	L27	DDR4-DM6
	R27	PS_DDR_DQS_P8	PS_DDR_DM7	H26	DDR4-DM7
	T27	PS_DDR_DQS_N8	PS_DDR_DM8	T26	

XCZU4CG-1SFVC784E



Title: TE0803 - PS_DDR		
A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 12 of 26
Filename: PS_DDR.SchDoc		

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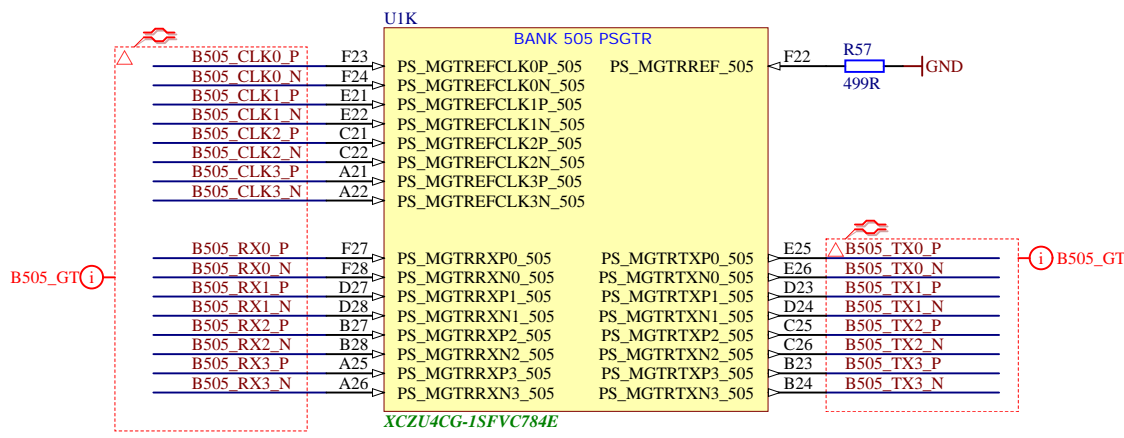
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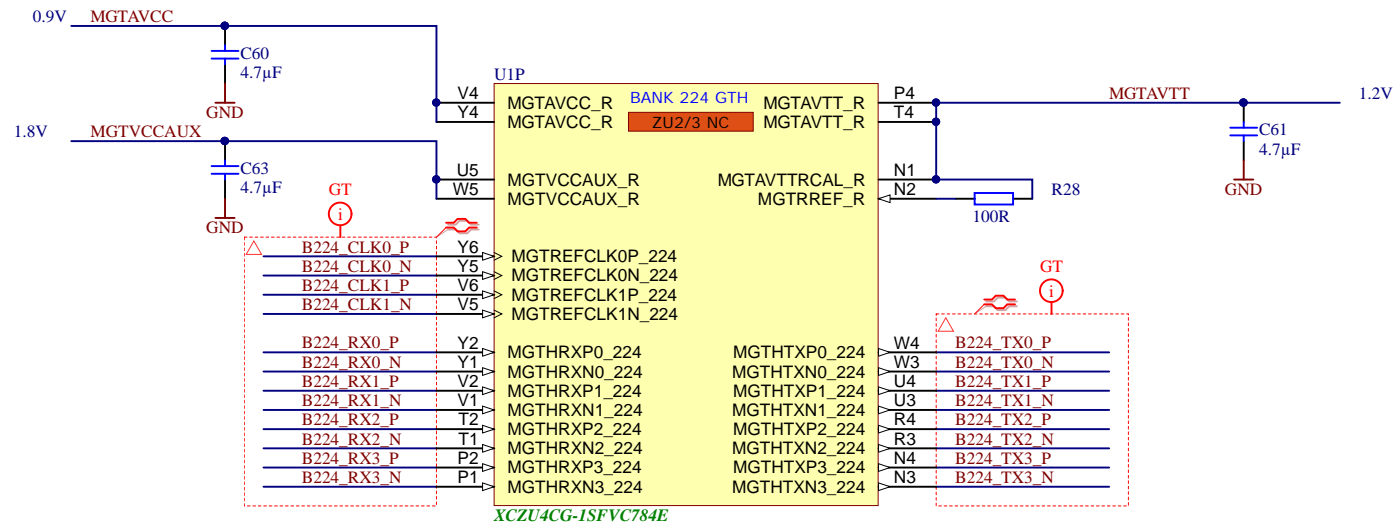
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	A4	Number: <b>TE0803 4AE21-A</b>	Rev. <b>03</b>
	Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>13</b> of <b>26</b>
	Filename: <b>B_PS_GT.SchDoc</b>		


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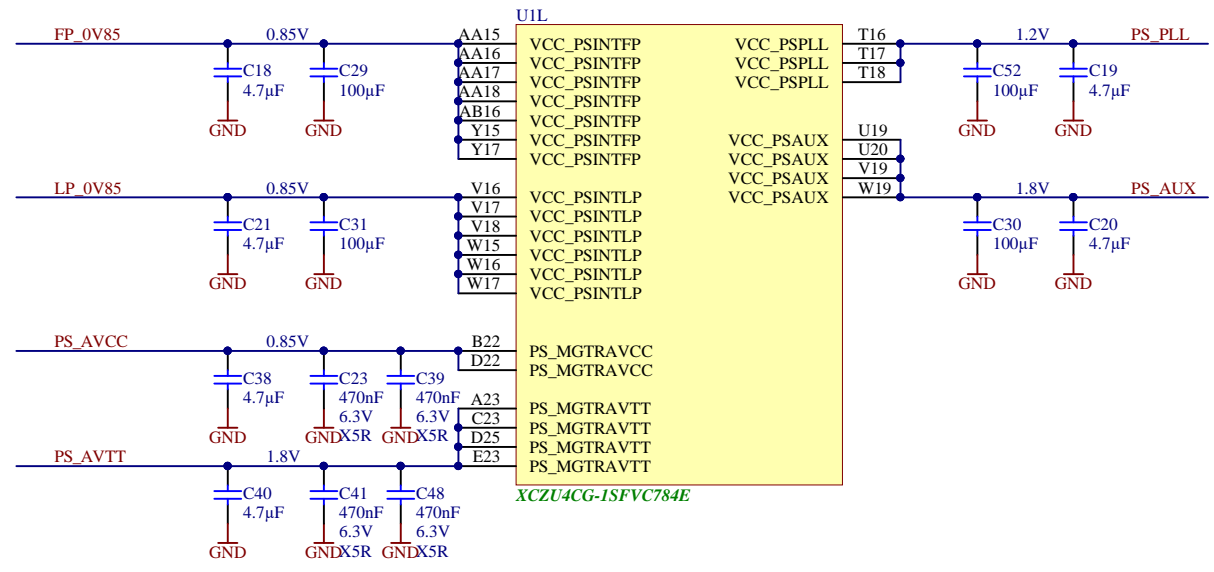
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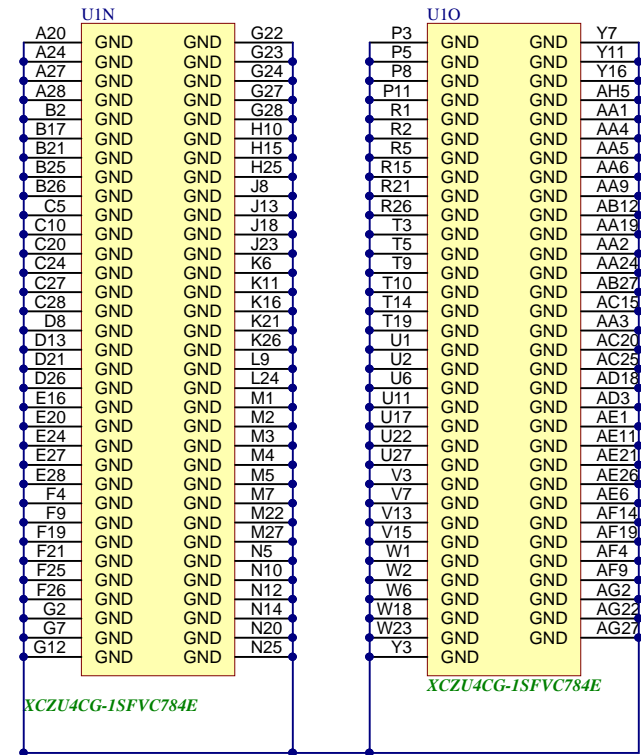
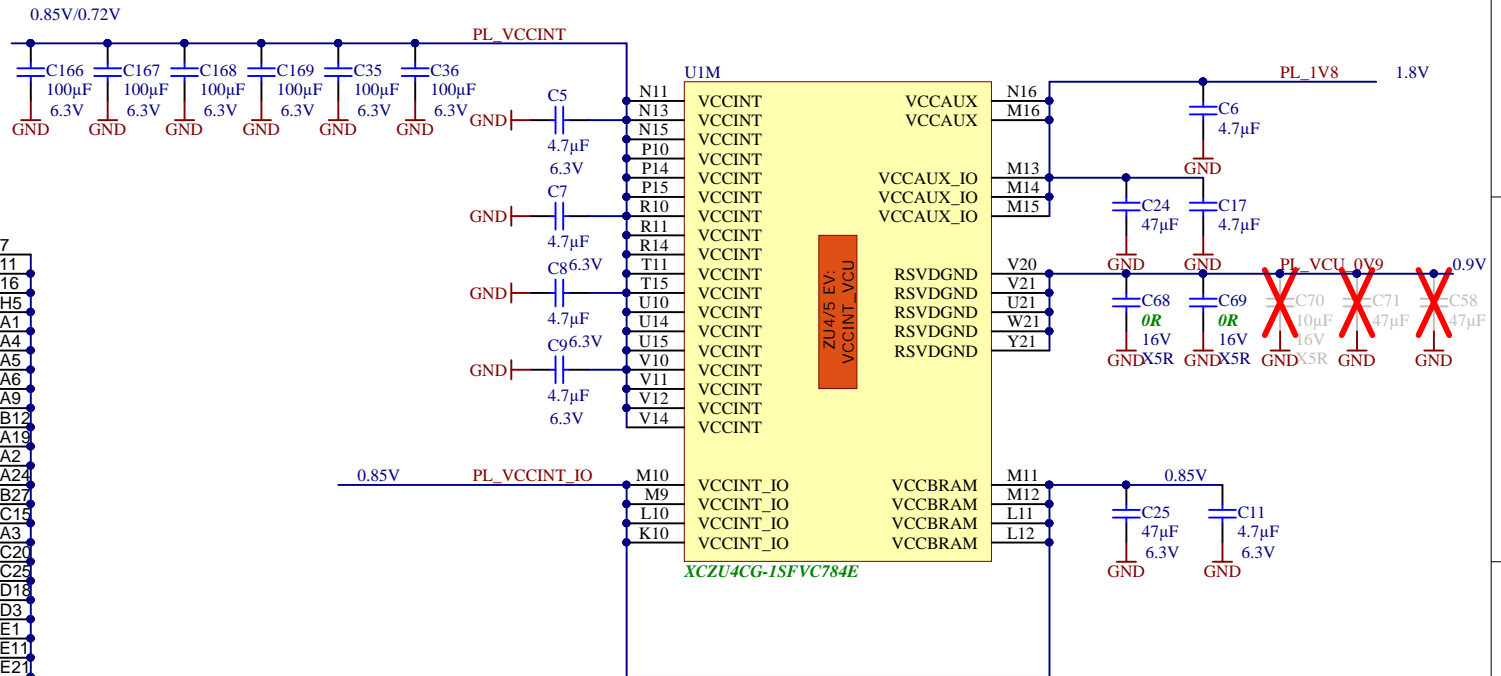
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	Title: TE0803 - B224GTH		
	A4	Number: TE0803 4AE21-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 14 of 26
	Filename: B_GT.SchDoc		

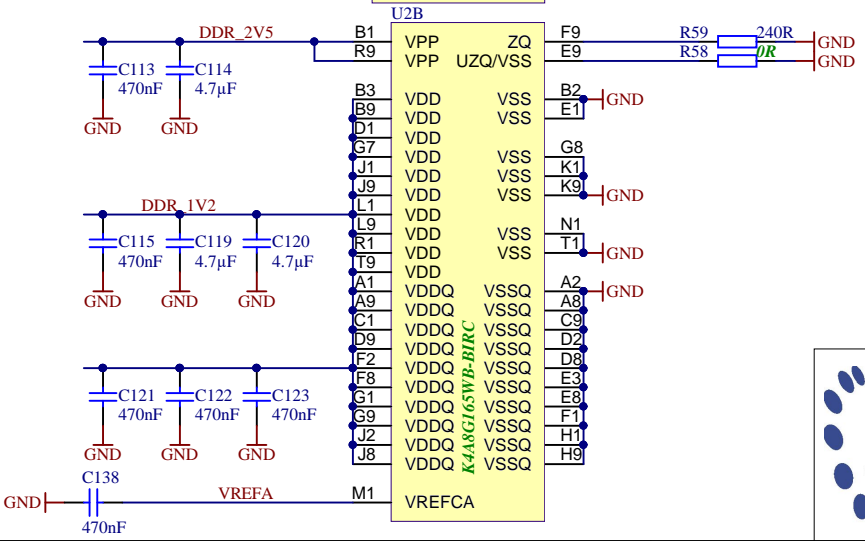
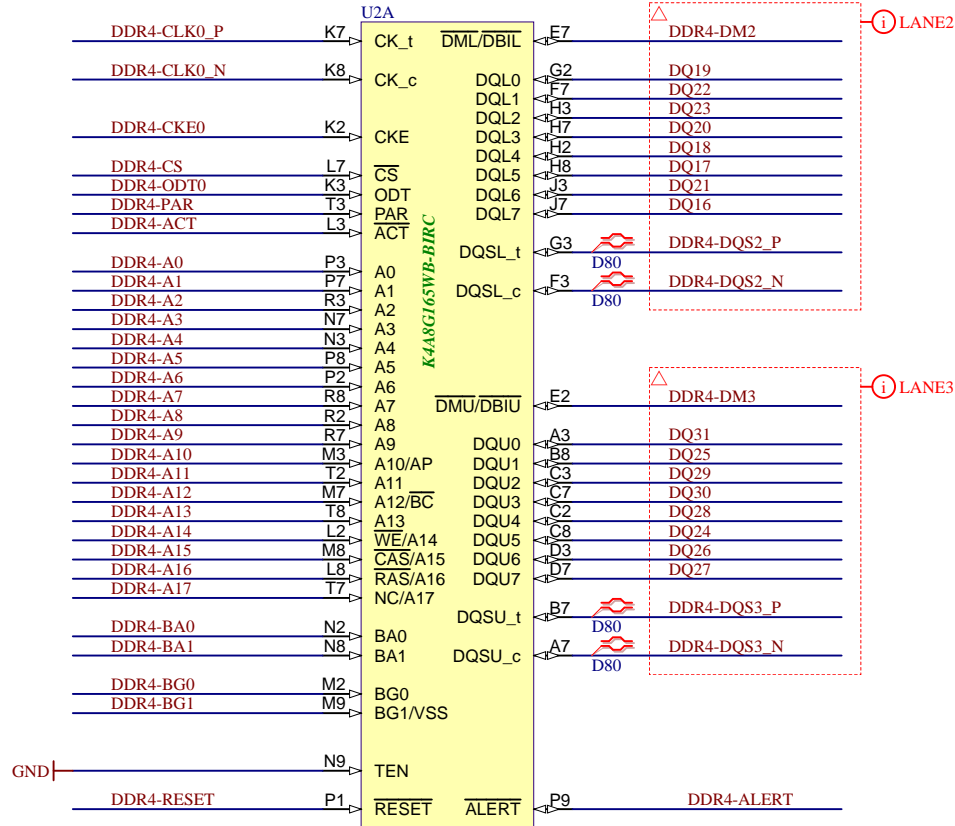


		Title: TE0803 - ZU_PS_POWER	
		A4	Number: TE0803 4AE21-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: ZU_PS_POWER.SchDoc		Page 15 of 26	

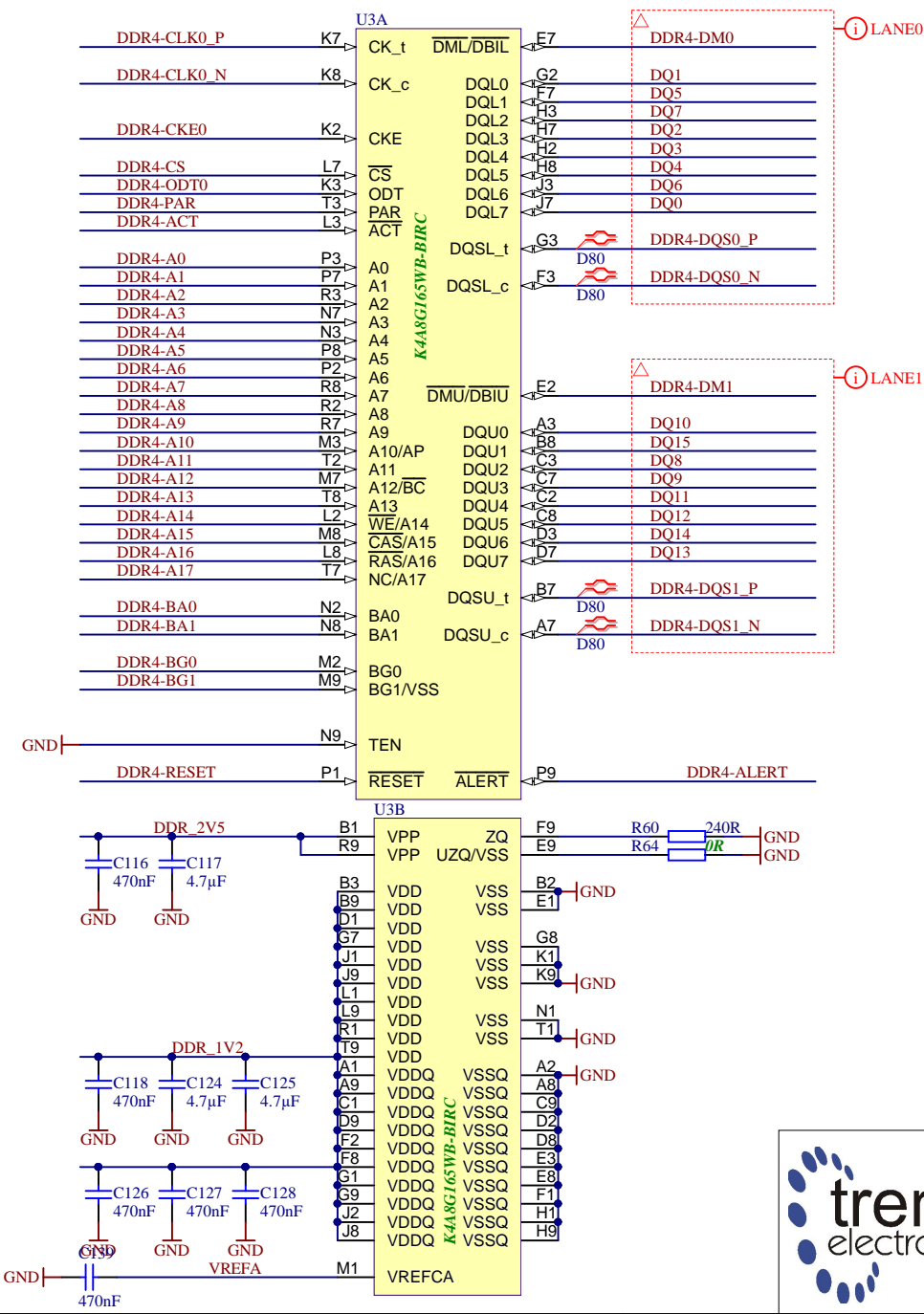



	Title: TE0803 - ZU_POWER		
	A4	Number: TE0803 4AE21-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 16 of 26
	Filename: ZU_POWER.SchDoc		

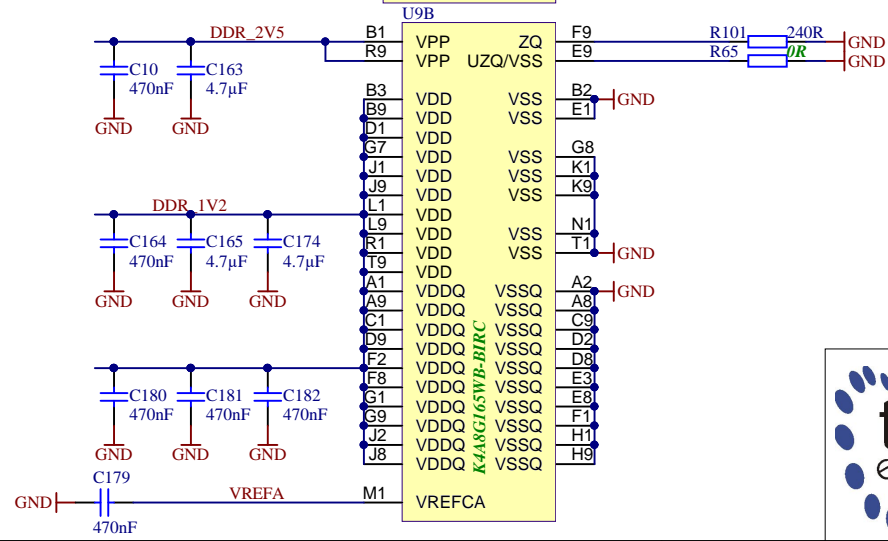
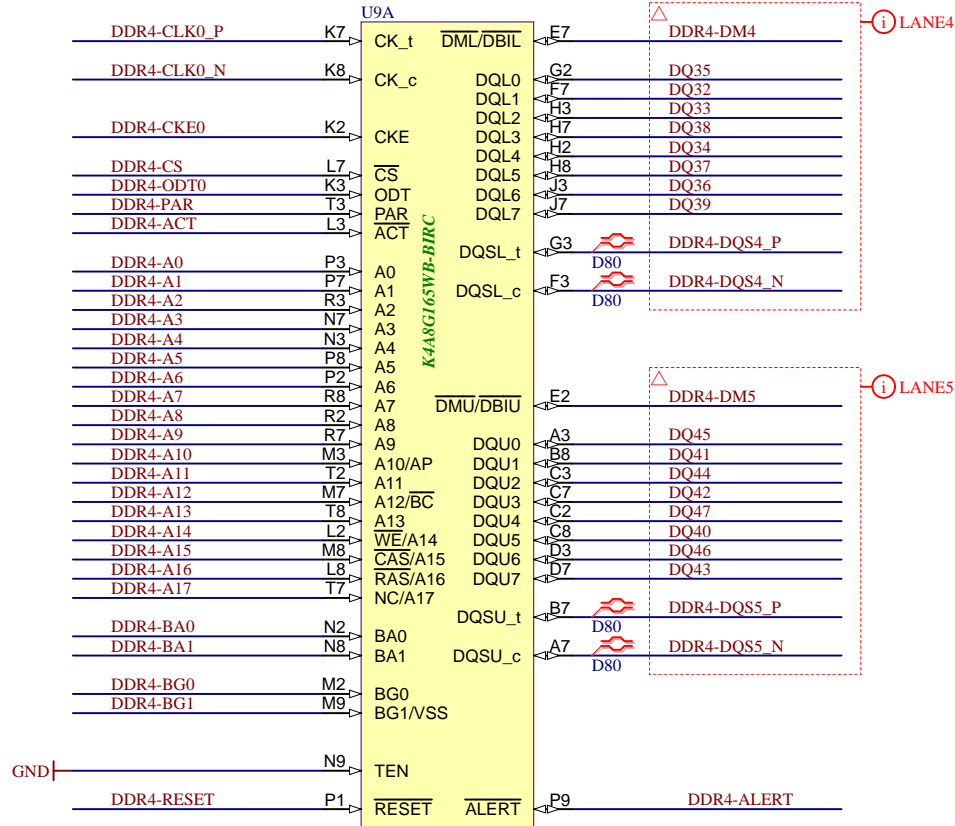




Title: TE0803 - DDR4_1_RAM		
A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 17 of 26
Filename: DDR4-RAM.SchDoc		

Title: TE0803 - DDR4_2_RAM		
A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 18 of 26
Filename: DDR4-RAM_2.SchDoc		



Title: TE0803 - DDR4_3_RAM		
A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 19 of 26
Filename: DDR4-RAM_3.SchDoc		

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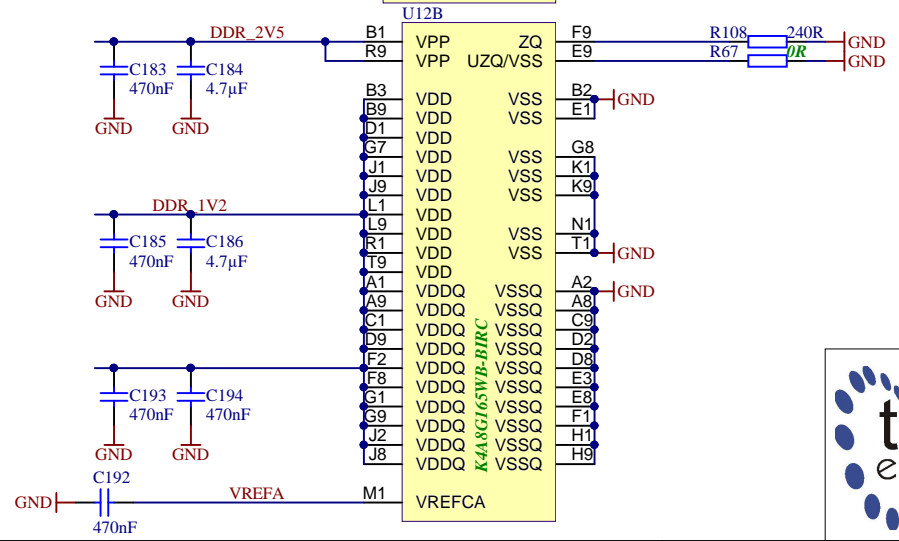
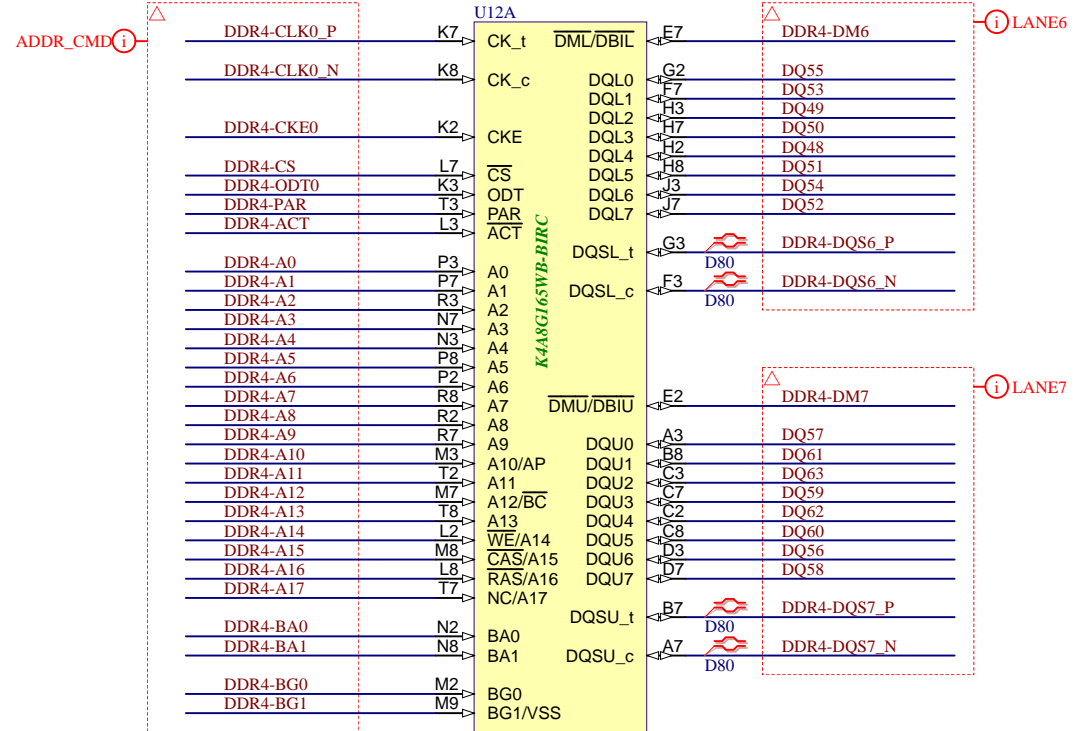

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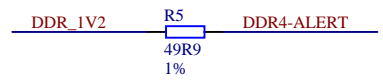
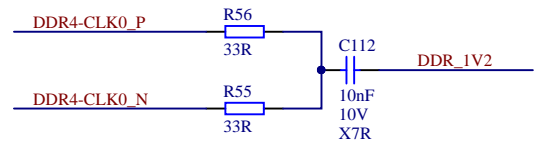
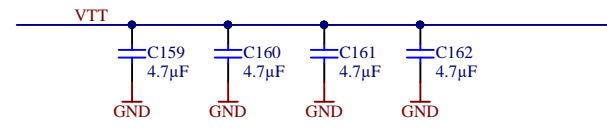
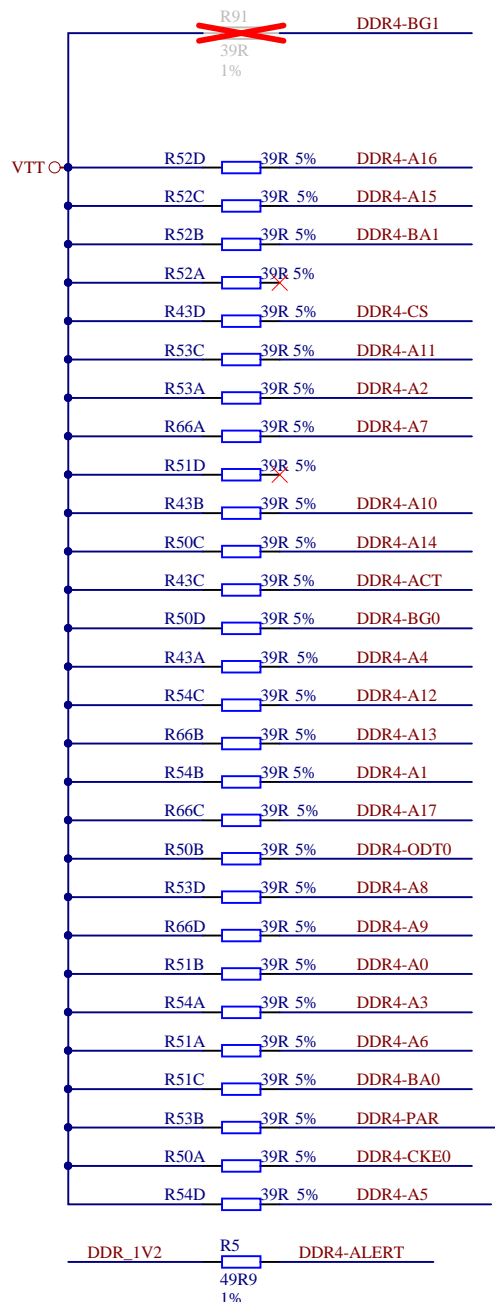
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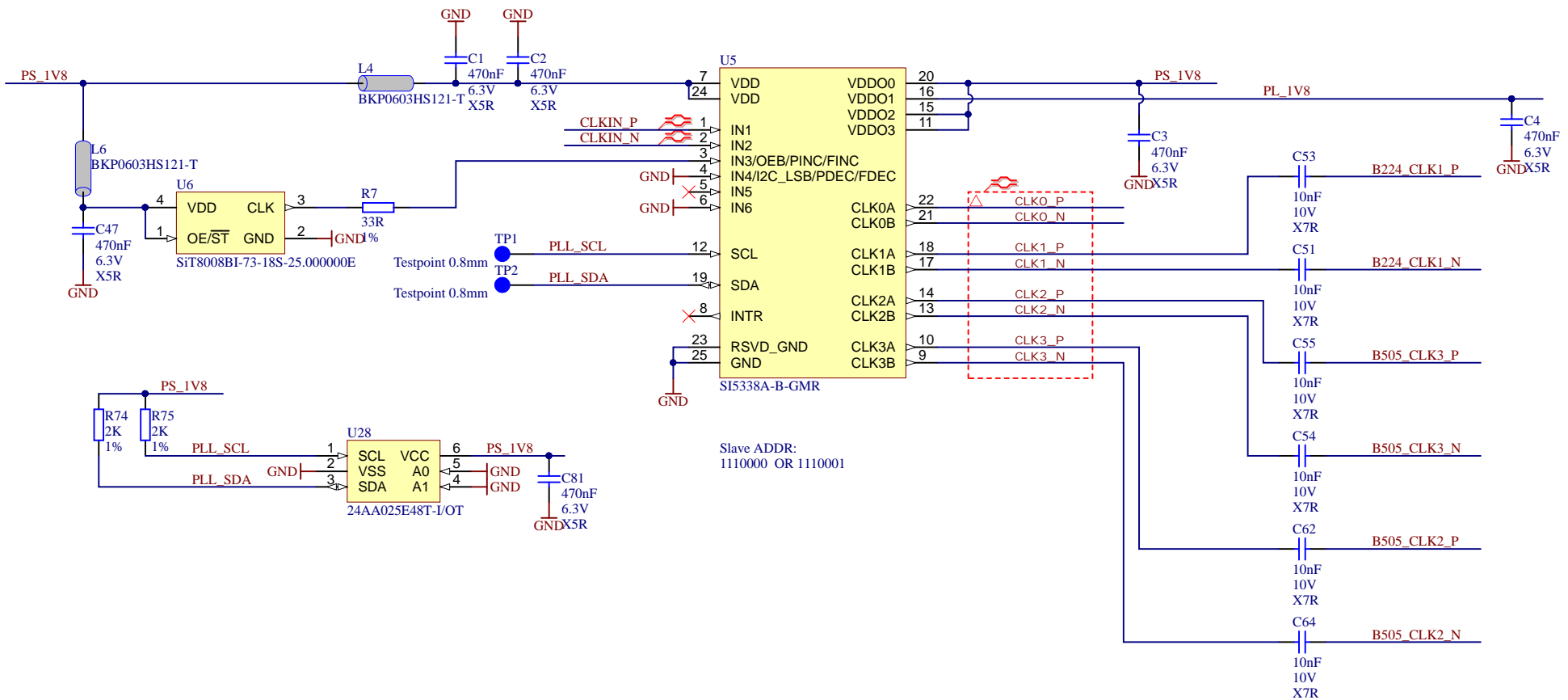
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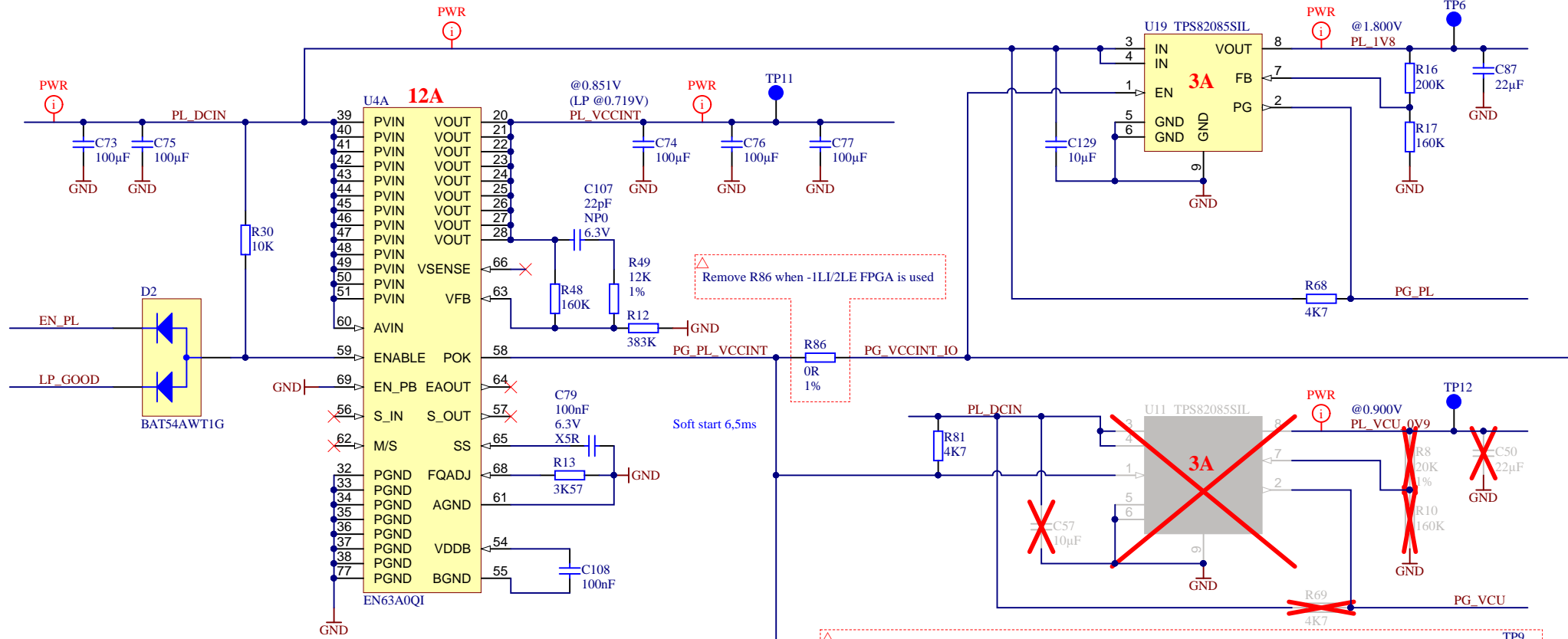
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A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page20 of 26
Filename: DDR4-RAM_4.SchDoc		



Title: TE0803 - DDR4_TERM		
A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page21 of 26
Filename: DDR4-TERM.SchDoc		



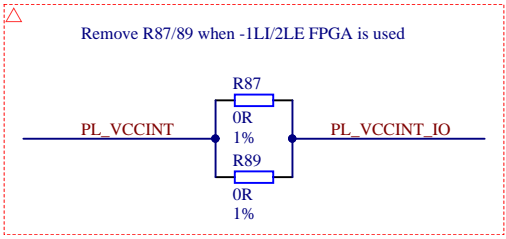
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		A4	Number: TE0803 4AE21-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: Clock.SchDoc		Page 22 of 26	



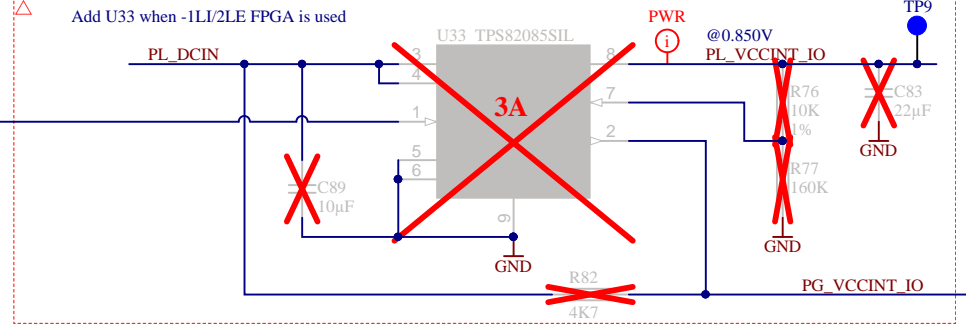
U4B

1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76

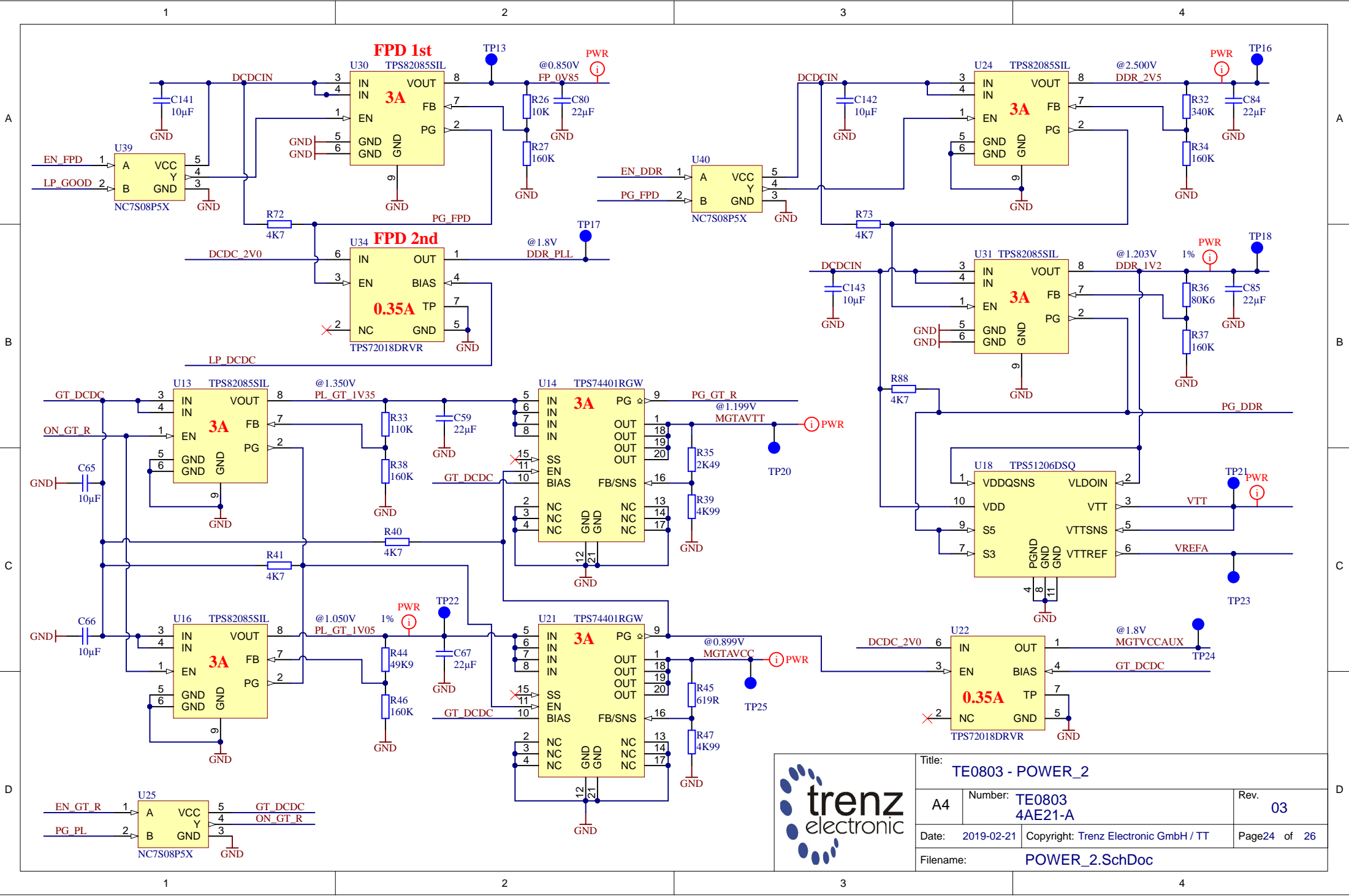
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Remove R86 when -1LI/2LE FPGA is used

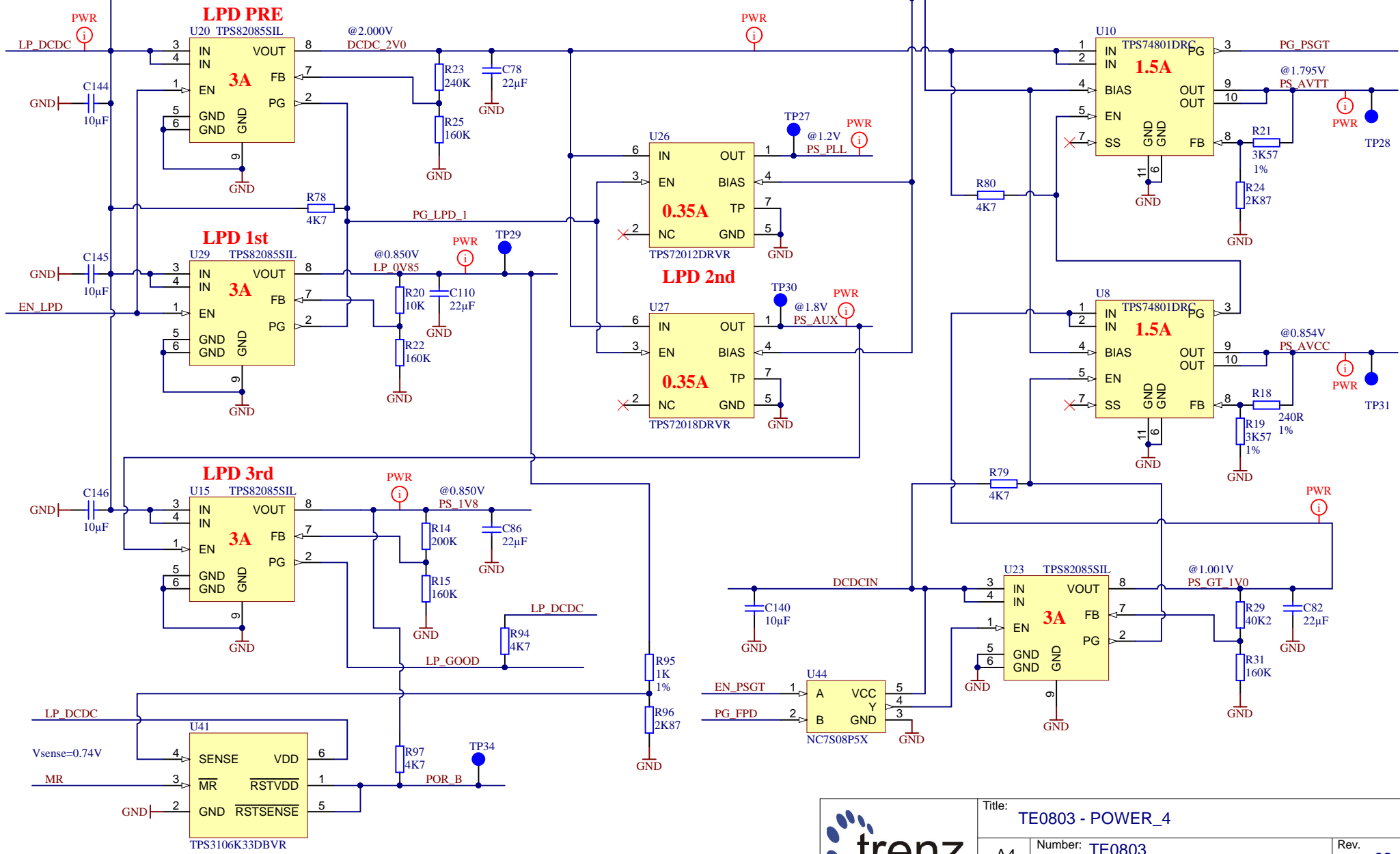


Title: TE0803 - POWER		
A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 23 of 26
Filename: POWER.SchDoc		



Title: <b>TE0803 - POWER_2</b>		
A4	Number: <b>TE0803 4AE21-A</b>	Rev. <b>03</b>
Date: <b>2019-02-21</b>	Copyright: Trenz Electronic GmbH / TT	
Filename: <b>POWER_2.SchDoc</b>		Page24 of 26





Title: TE0803 - POWER_4		
A4	Number: TE0803 4AE21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 25 of 26
Filename: POWER_4.SchDoc		

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CHANGES REV01a (20.11.2017):

- 1) VCU voltage set to 0.9V, R20 changed to 40K , PL\_VCU\_1V0 renamed to PL\_VCU\_0V9.

CHANGES REV02 (20.06.2018):

- 1) Added LDO to DDR\_PLL
- 2) All differential pairs with length matched with tolerance 0.1mm (excluding package delays)
- 3) Added MAC EEPROM U28
- 4) VPS\_MGTRAVCC set to 0.85V
- 5) Added pull-up resistors R68,R69

CHANGES REV03 (21.02.2019):

- 1) Added support of DDP DDR4
- 2) Added support of Low power FPGA (-L1/L2).
- 3) Revised testpoints
- 4) Revised J1-J4 connectors net label style

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Title: <b>TE0803 - Changes list</b>			
A4	Number: <b>TE0803 4AE21-A</b>	Rev. <b>03</b>	
Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>26</b> of <b>26</b>	
Filename: <b>Revision_Changes.SchDoc</b>			

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