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U_J1
J1.SchDoc

U_J2
J2.SchDoc

U_J3
J3.SchDoc

U_J4
J4.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

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B64.SchDoc

U_B65
B65.SchDoc

U_B66
B66.SchDoc

U_B_GT
B_GT.SchDoc

U_B_PS_GT
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PS_DDR.SchDoc

U_B_MIO
B_MIO.SchDoc

U_B_HD
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Clock.SchDoc

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CONFIG.SchDoc

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DDR4-RAM_3.SchDoc

U_DDR4-RAM_4
DDR4-RAM_4.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

U_ZU_POWER
ZU_POWER.SchDoc

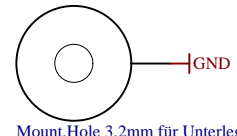
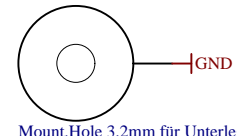
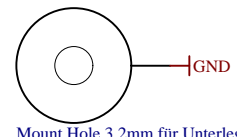
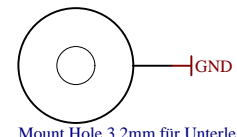
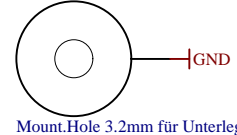
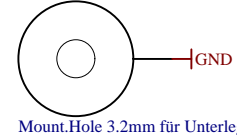
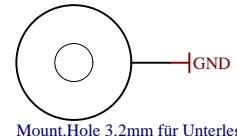
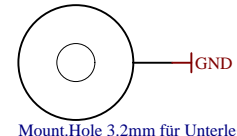
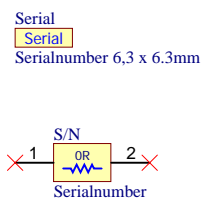
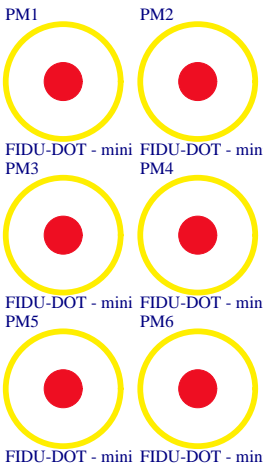
U_ZU_PS_POWER
ZU_PS_POWER.SchDoc

U_POWER
POWER.SchDoc

U_POWER_2
POWER_2.SchDoc

U_POWER_4
POWER_4.SchDoc

U_REV_CH
Revision_Changes.SchDoc



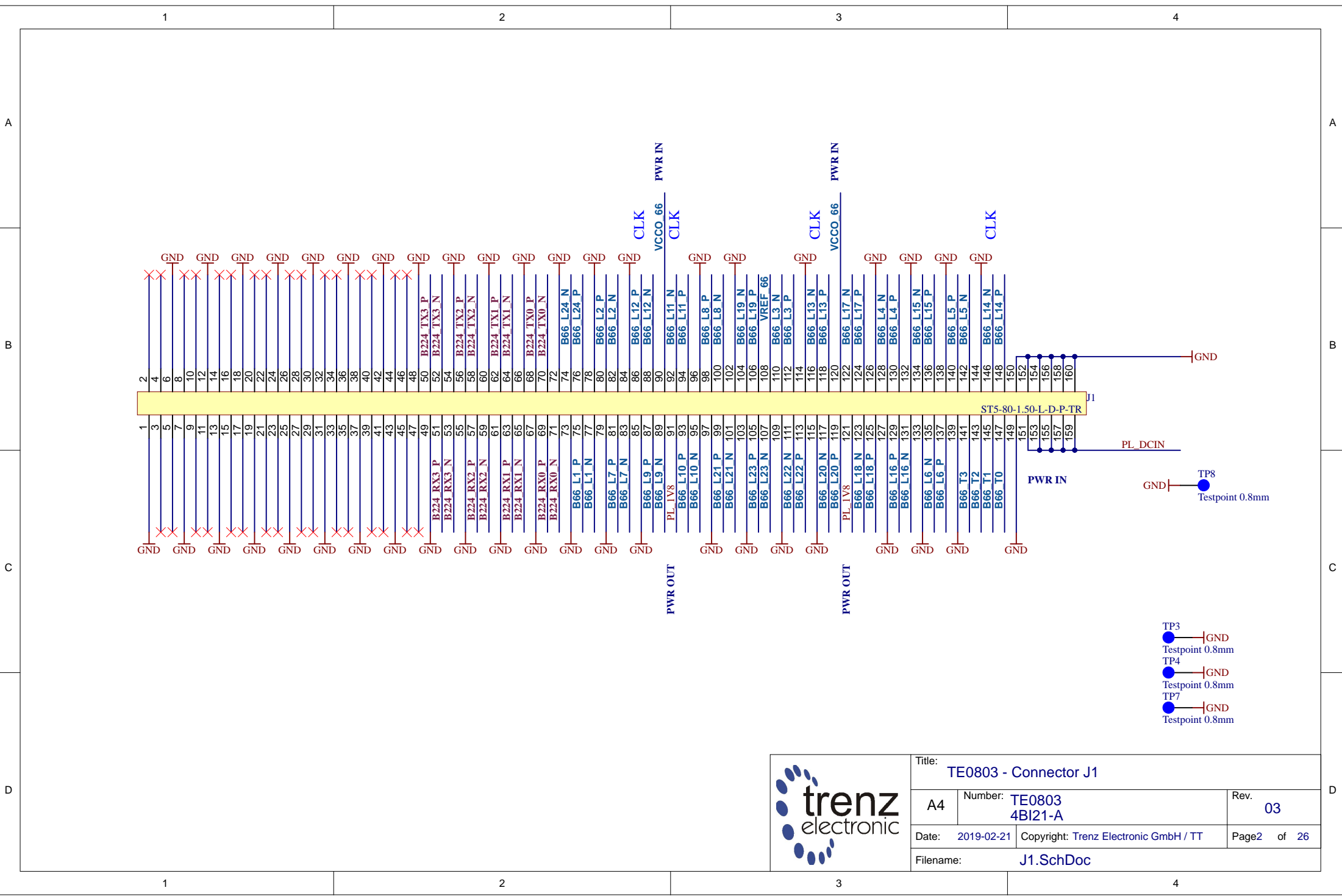
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A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page1 of 26
Filename: TE0803.SchDoc		

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Title: TE0803 - Connector J1		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page2 of 26
Filename: J1.SchDoc		

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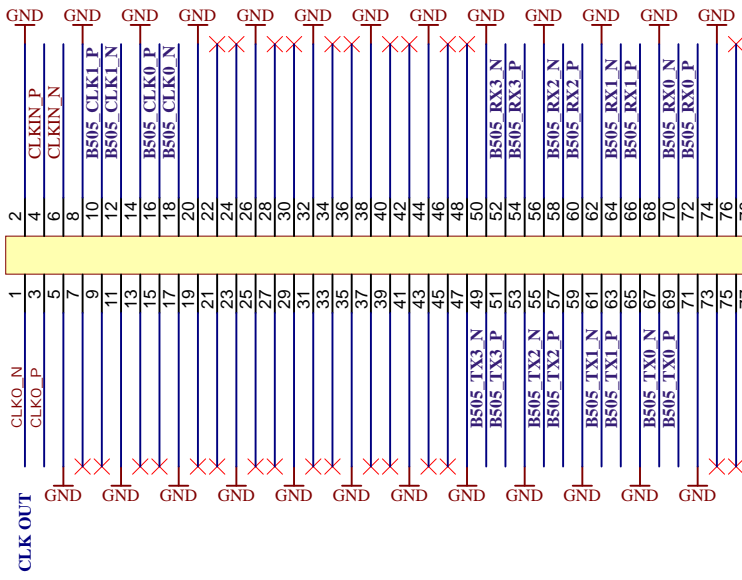
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CLKIN
CLKIN
CLKIN



(External pull-up R required)

(External pull-up R required)

(On board pull-up R)

(On board pull-up R)

(On board pull-up R)

(On board pull-up R)

(On board pull-up R)

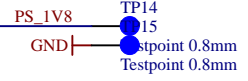
(1.2...1.5V)

PWR IN

PWR IN

LP_DCDC

DCDCIN



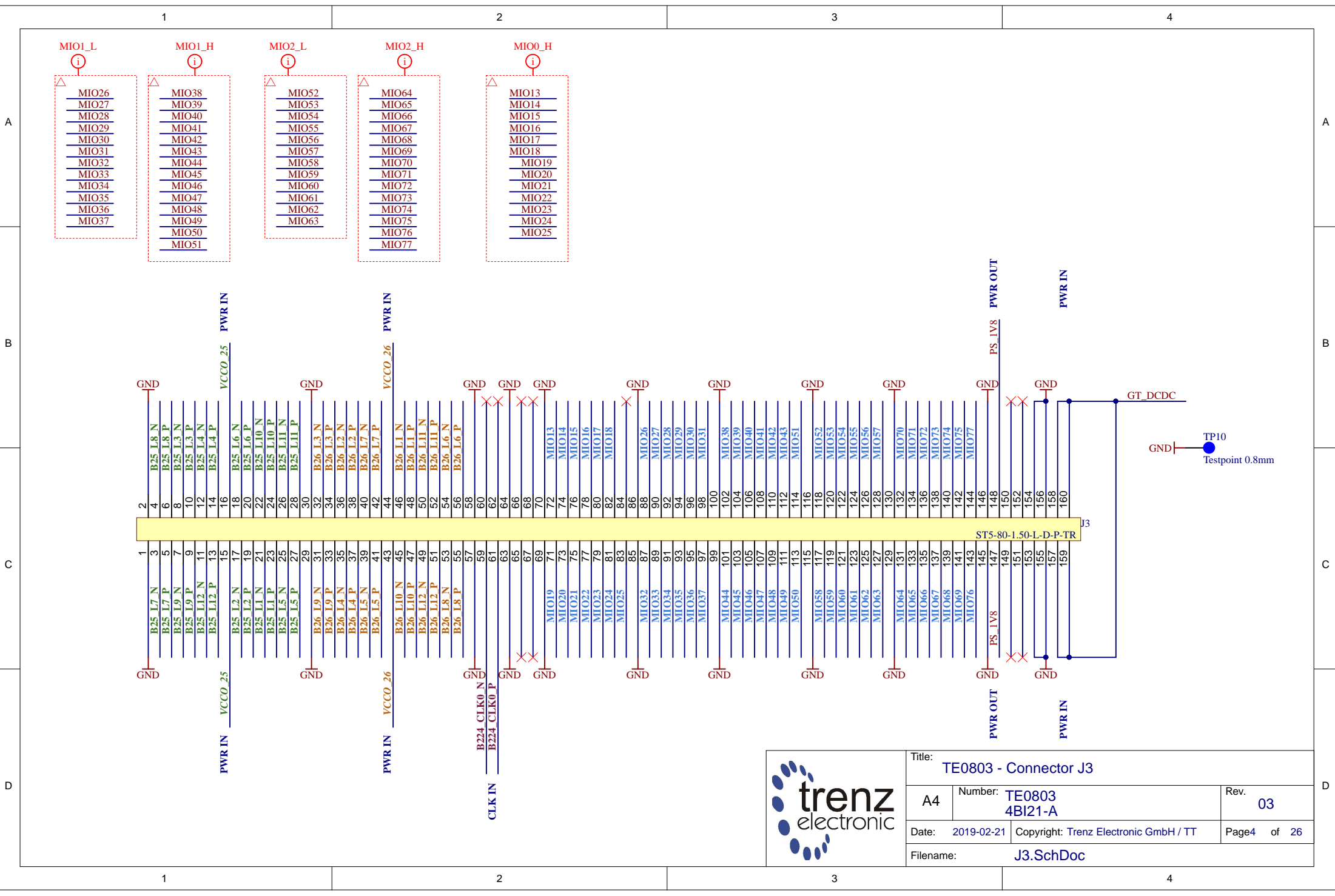
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A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page3 of 26
Filename: J2.SchDoc		

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Title: TE0803 - Connector J3		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page4 of 26
Filename: J3.SchDoc		

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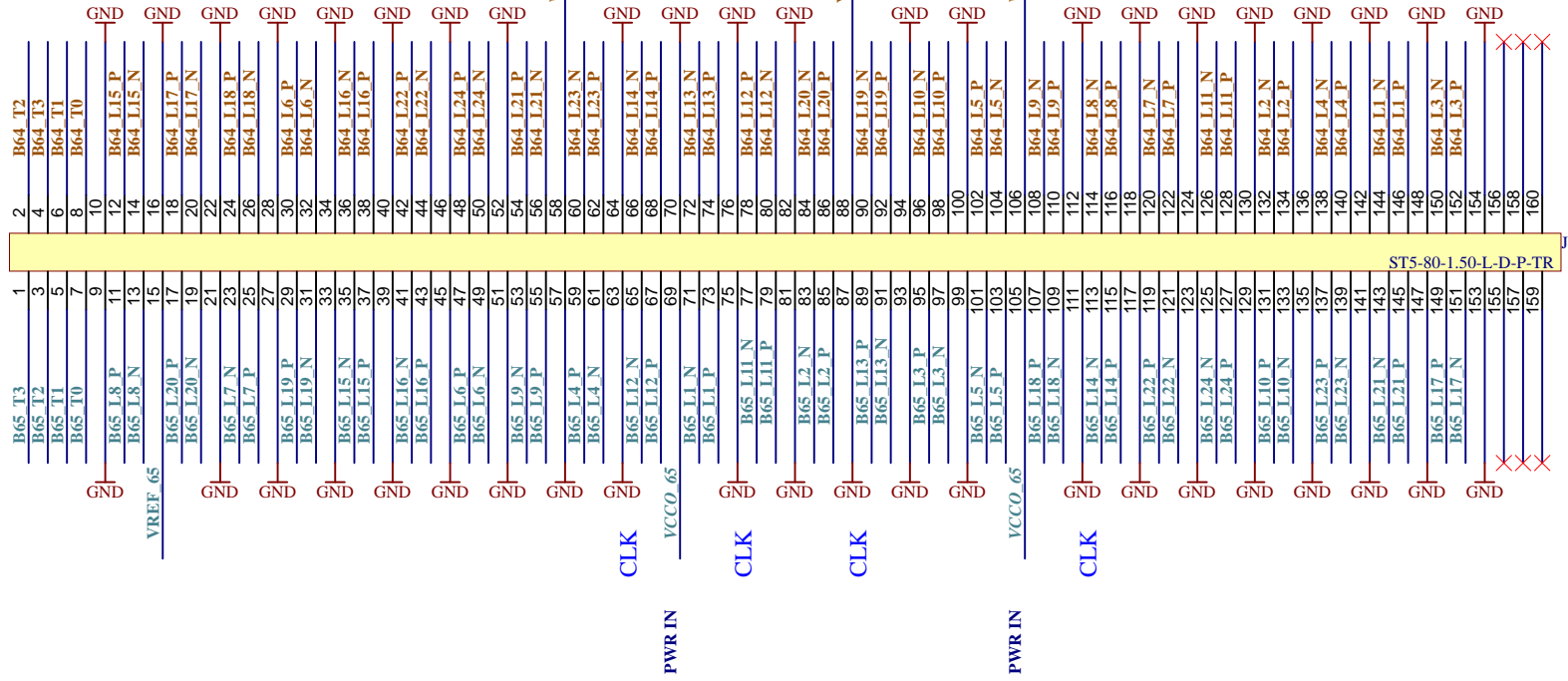

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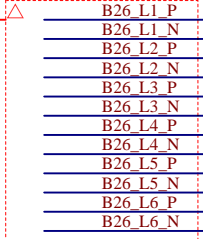
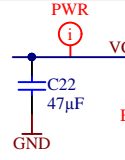
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A4	Number: TE0803 4B121-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page5 of 26
Filename: J4.SchDoc		

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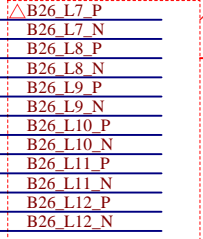
4



U1C XCZU4EG-1SFVC784I

BANK 46 HD (ZU2/3 BANK 26 HD)

F14	VCCO_46		
C15	VCCO_46		
B15	IO_L1P_AD11P_46	IO_L7P_HDGC_AD5P_46	G13
A15	IO_L1N_AD11N_46	IO_L7N_HDGC_AD5N_46	F13
B14	IO_L2P_AD10P_46	IO_L8P_HDGC_AD4P_46	F15
A14	IO_L2N_AD10N_46	IO_L8N_HDGC_AD4N_46	E15
B13	IO_L3P_AD9P_46	IO_L9P_AD3P_46	G15
A13	IO_L3N_AD9N_46	IO_L9N_AD3N_46	G14
C14	IO_L4P_AD8P_46	IO_L10P_AD2P_46	H14
C13	IO_L4N_AD8N_46	IO_L10N_AD2N_46	H13
D15	IO_L5P_HDGC_AD7P_46	IO_L11P_AD1P_46	K14
D14	IO_L5N_HDGC_AD7N_46	IO_L11N_AD1N_46	J14
E14	IO_L6P_HDGC_AD6P_46	IO_L12P_AD0P_46	L14
E13	IO_L6N_HDGC_AD6N_46	IO_L12N_AD0N_46	L13



A

A

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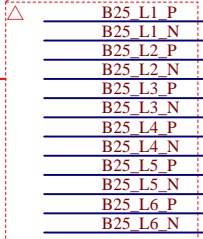
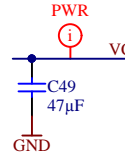
B

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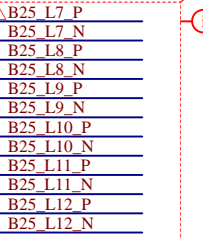
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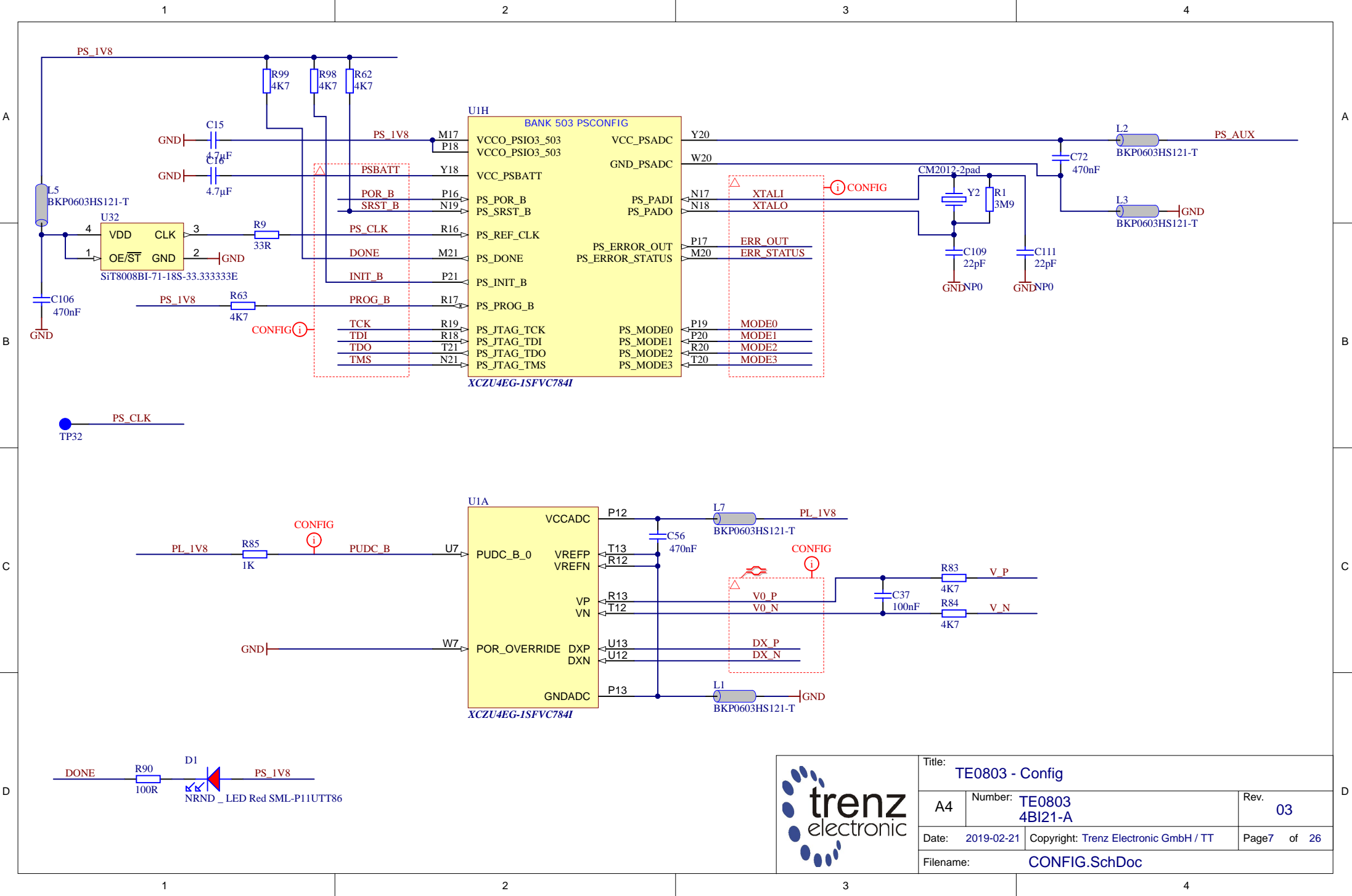
U1B

BANK 44 HD (ZU2/3 BANK 24 HD)

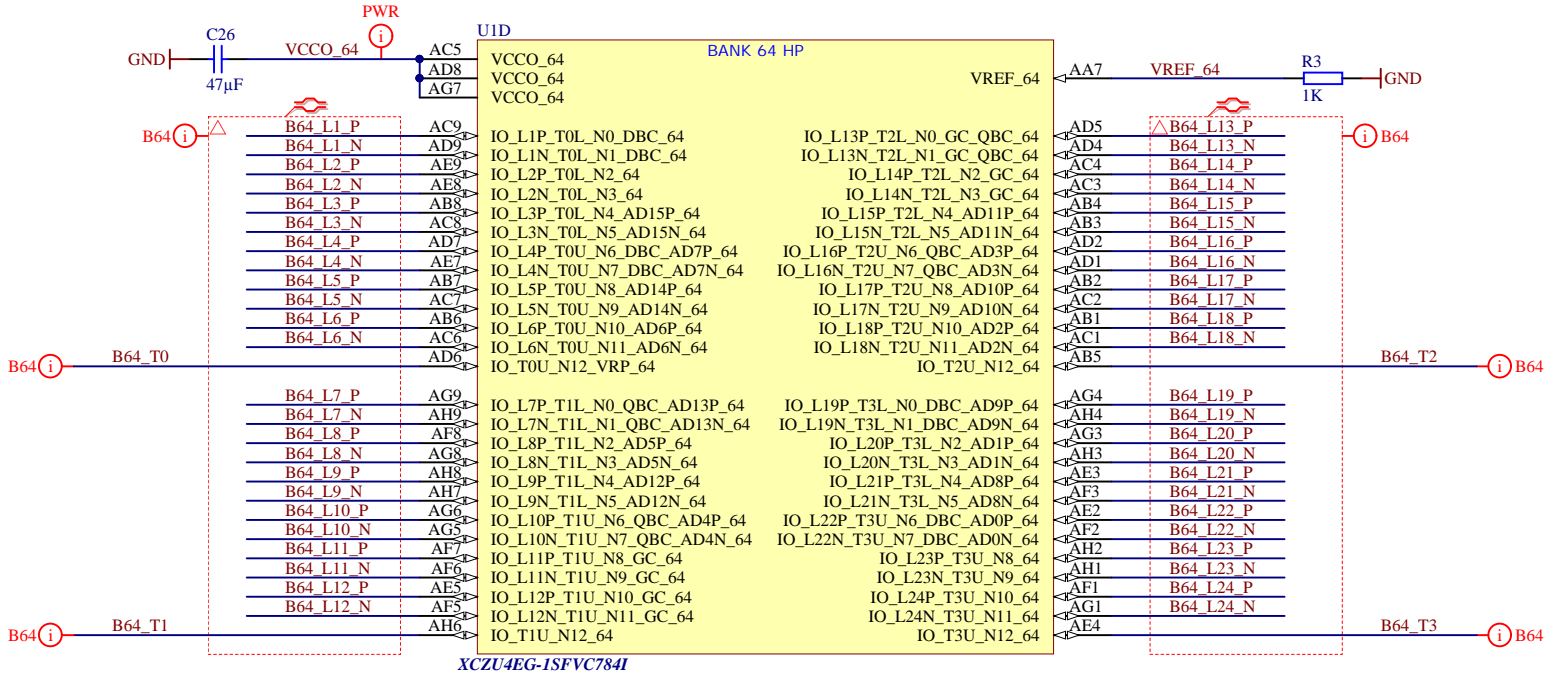
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AD13	VCCO_44		
AE15	IO_L1P_AD15P_44	IO_L7P_HDGC_44	AA13
AE14	IO_L1N_AD15N_44	IO_L7N_HDGC_44	AB13
AG14	IO_L2P_AD14P_44	IO_L8P_HDGC_44	AB15
AH14	IO_L2N_AD14N_44	IO_L8N_HDGC_44	AB14
AG13	IO_L3P_AD13P_44	IO_L9P_AD11P_44	W14
AH13	IO_L3N_AD13N_44	IO_L9N_AD11N_44	W13
AE13	IO_L4P_AD12P_44	IO_L10P_AD10P_44	Y14
AE12	IO_L4N_AD12N_44	IO_L10N_AD10N_44	Y13
AF13	IO_L5P_HDGC_44	IO_L11P_AD9P_44	W12
AD12	IO_L5N_HDGC_44	IO_L11N_AD9N_44	W11
AC14	IO_L6P_HDGC_44	IO_L12P_AD8P_44	Y12
AC13	IO_L6N_HDGC_44	IO_L12N_AD8N_44	AA12



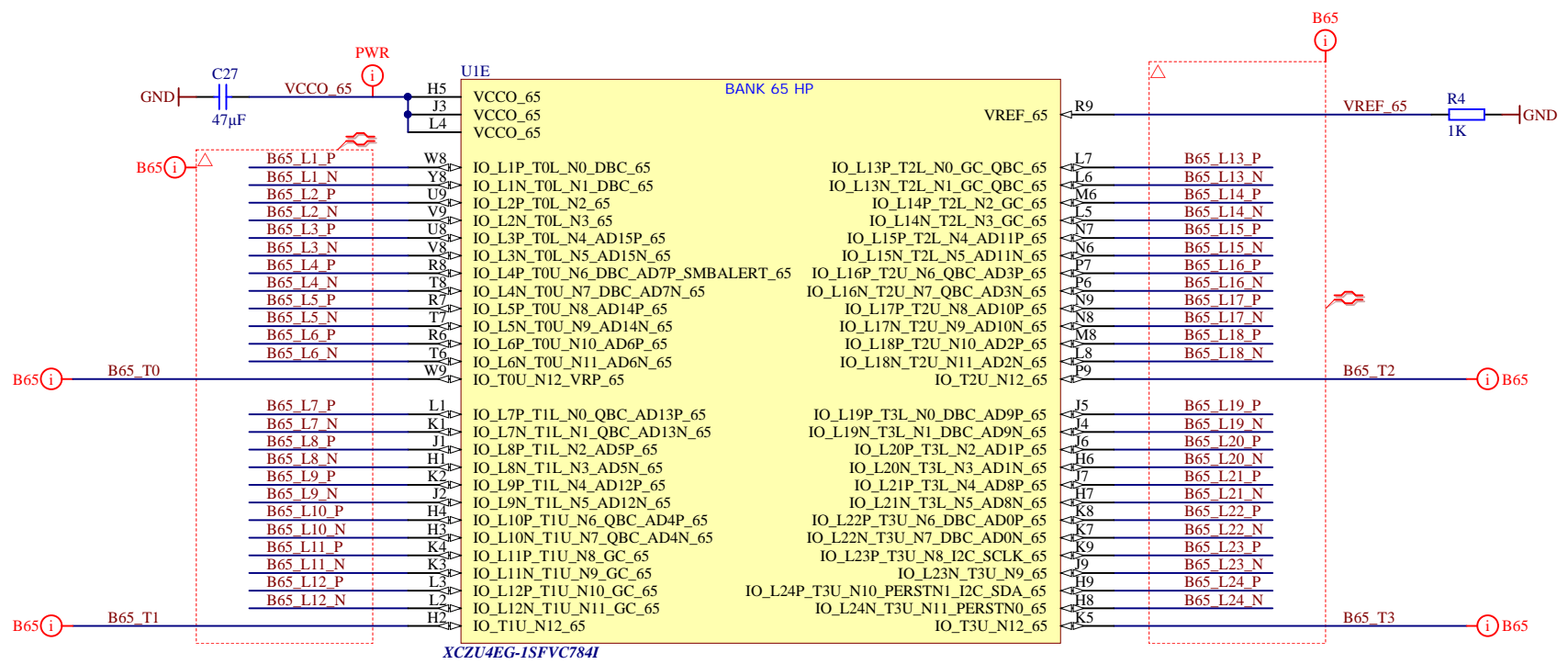
Title: TE0803 - HD Banks		
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page6 of 26
Filename: B_HD.SchDoc		



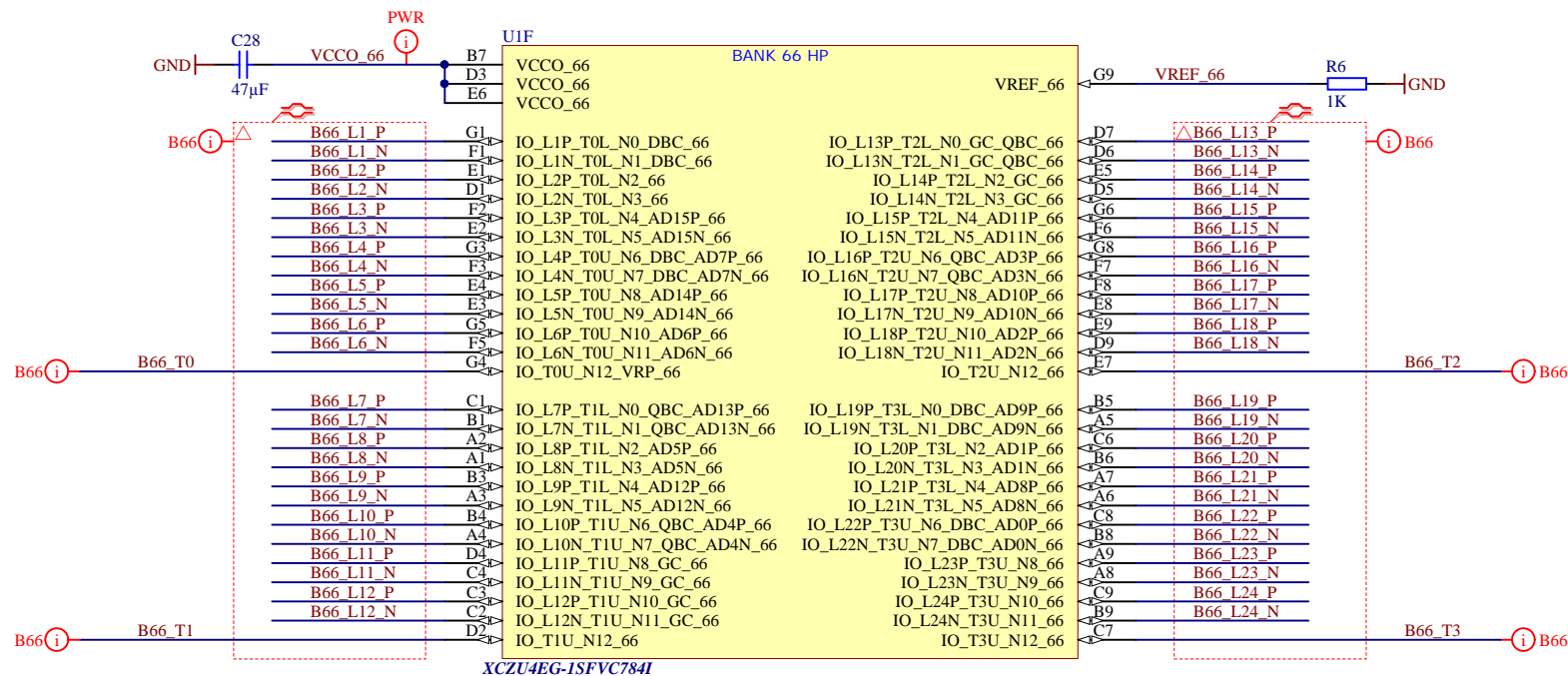
Title: TE0803 - Config		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 7 of 26
Filename: CONFIG.SchDoc		



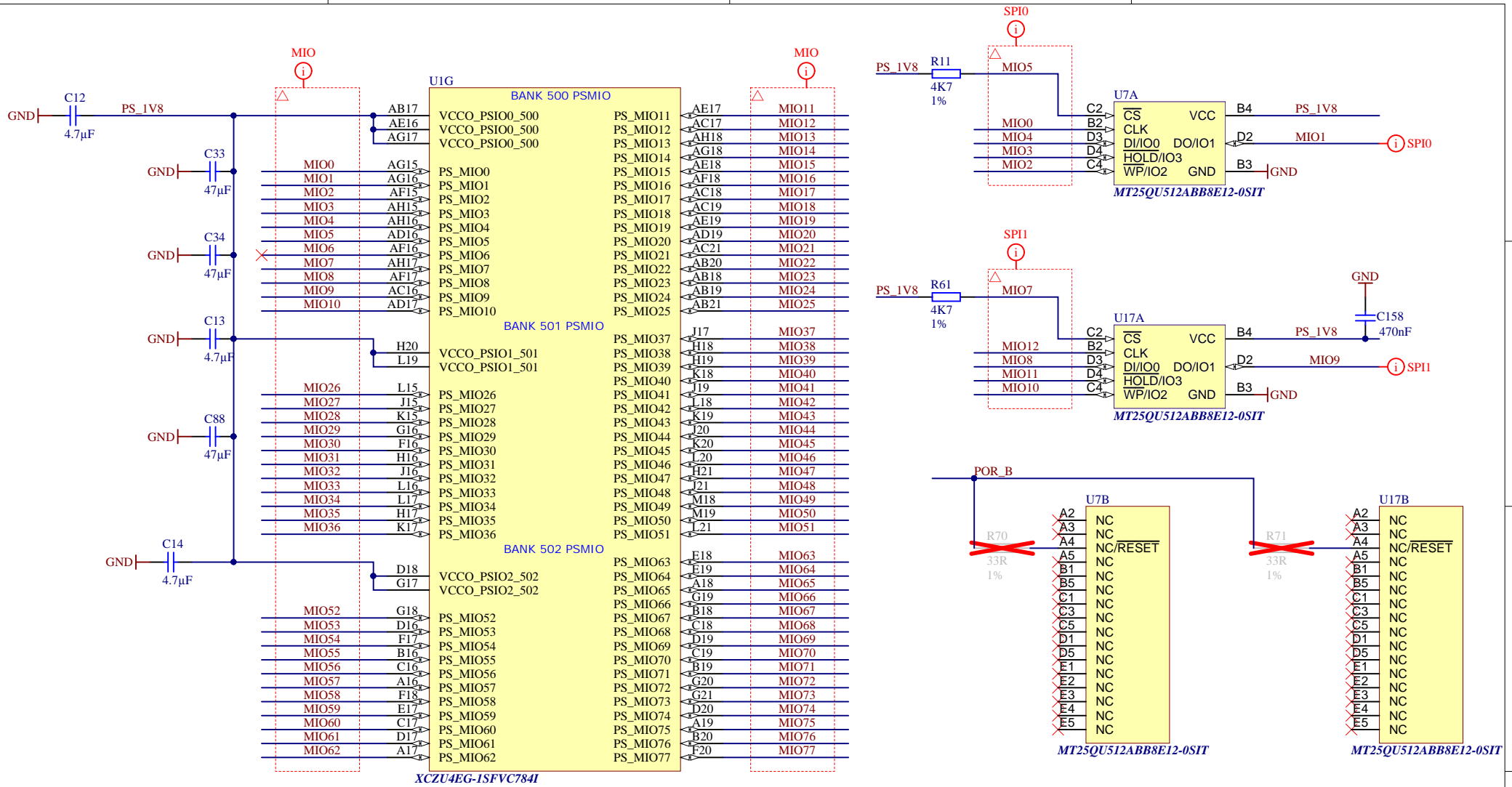
Title: TE0803 - B64		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 8 of 26
Filename: B64.SchDoc		



Title: TE0803 - B65		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 9 of 26
Filename: B65.SchDoc		



Title: TE0803 - B66		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 10 of 26
Filename: B66.SchDoc		



	Title: TE0803 - MIO Banks		
	A4	Number: TE0803 4BI21-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	
	Filename: B_MIO.SchDoc	Page 11 of 26	

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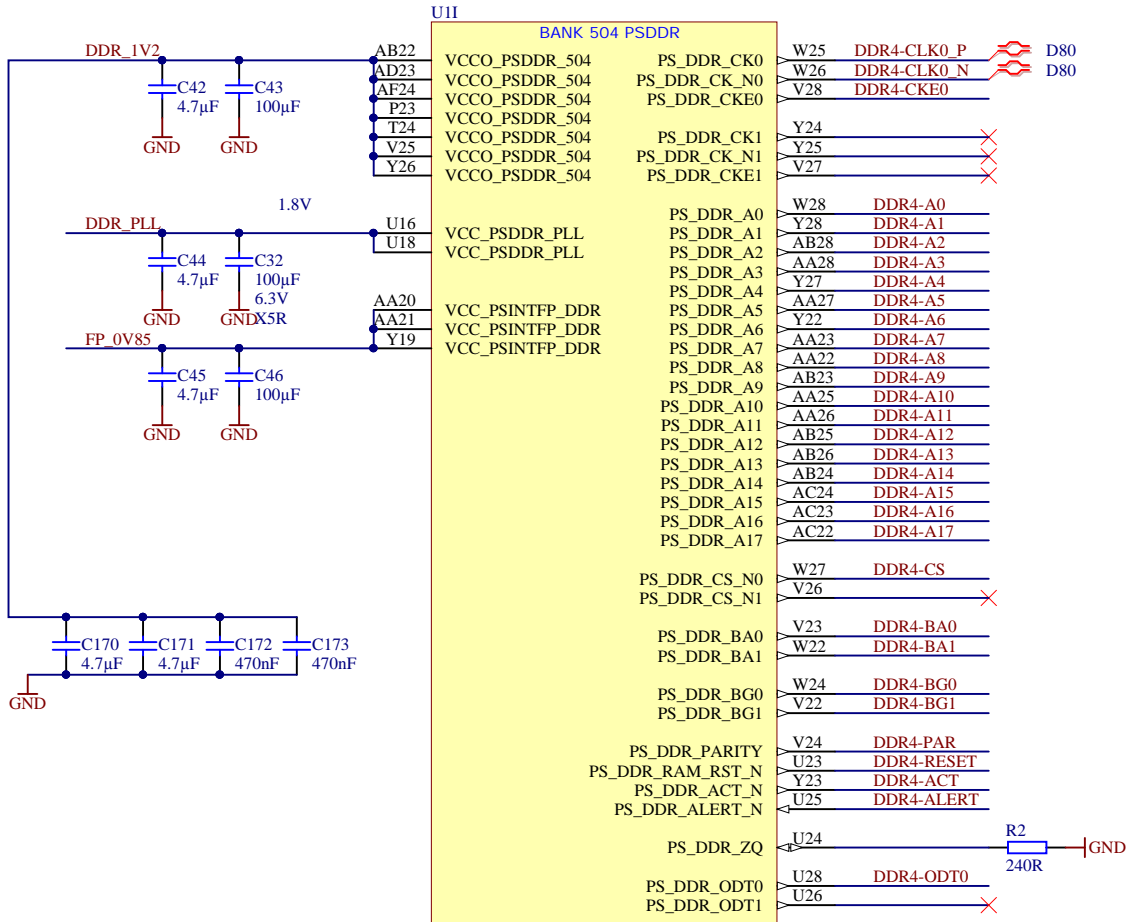
D

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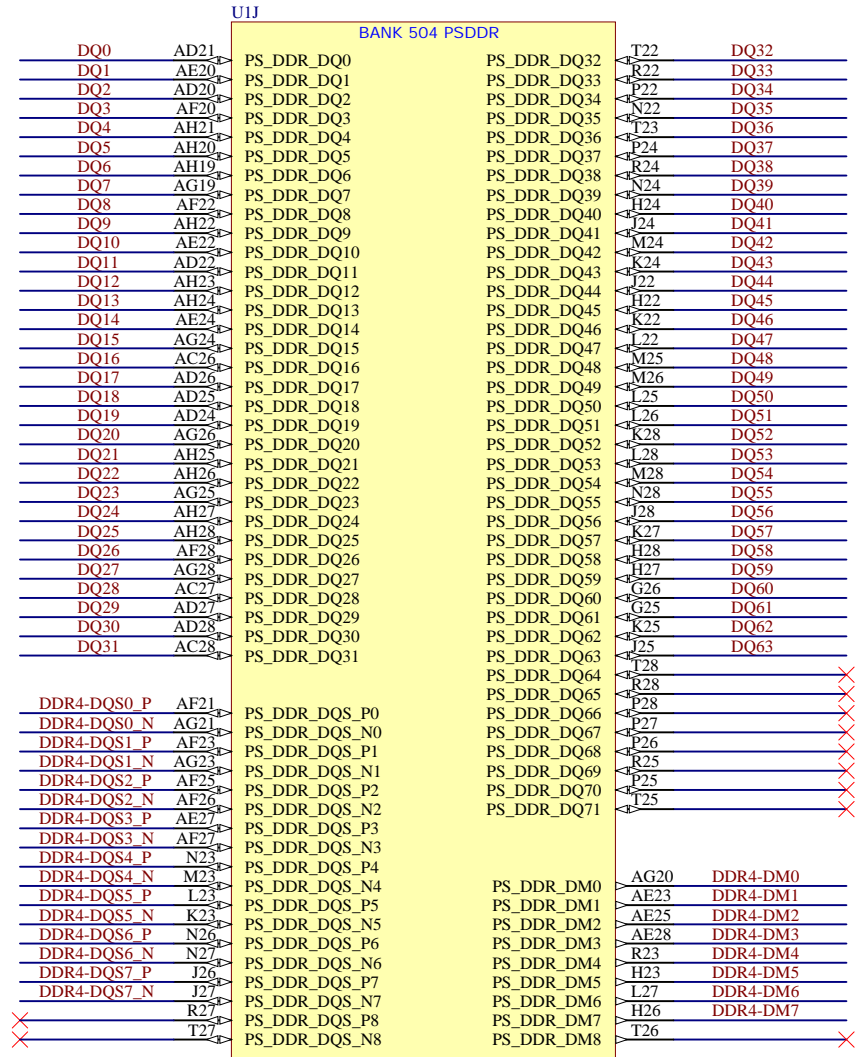
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XCZU4EG-1SFVC784I



XCZU4EG-1SFVC784I



Title: TE0803 - PS_DDR		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 12 of 26
Filename: PS_DDR.SchDoc		

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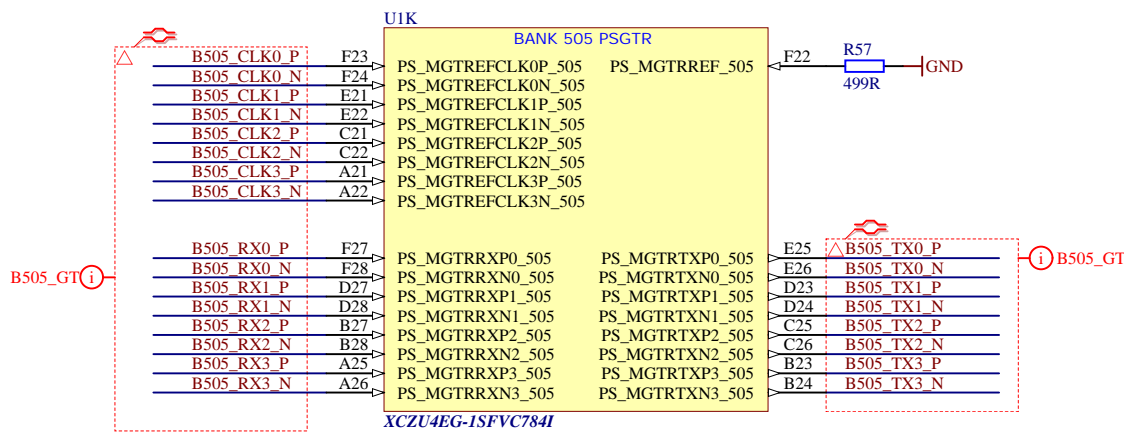
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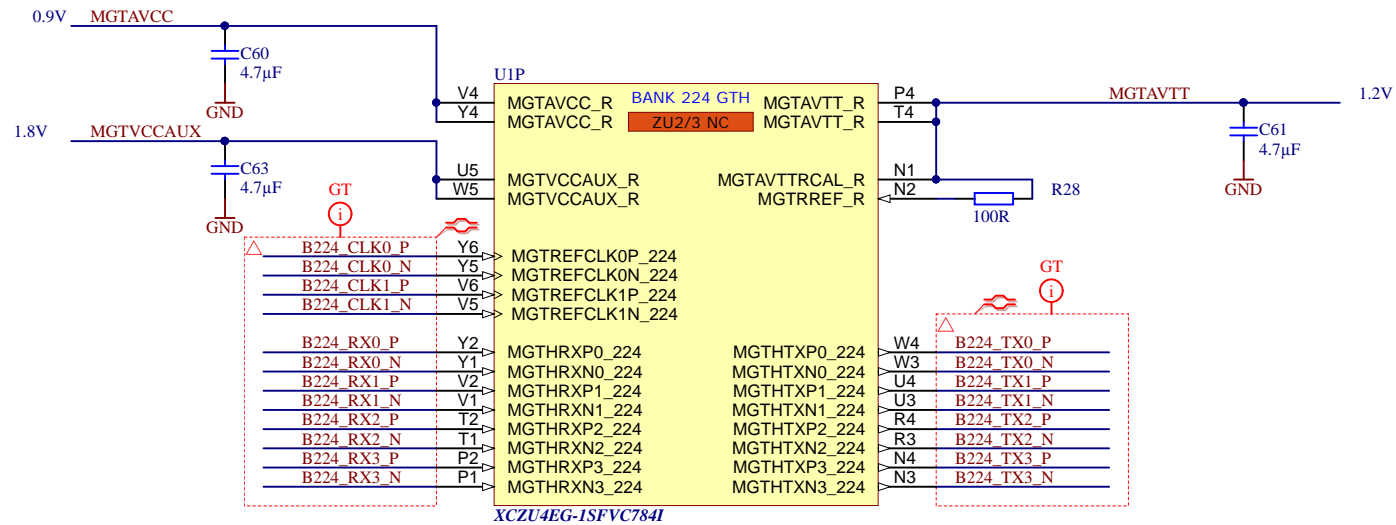
Title: TE0803 - PS_GT		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 13 of 26
Filename: B_PS_GT.SchDoc		


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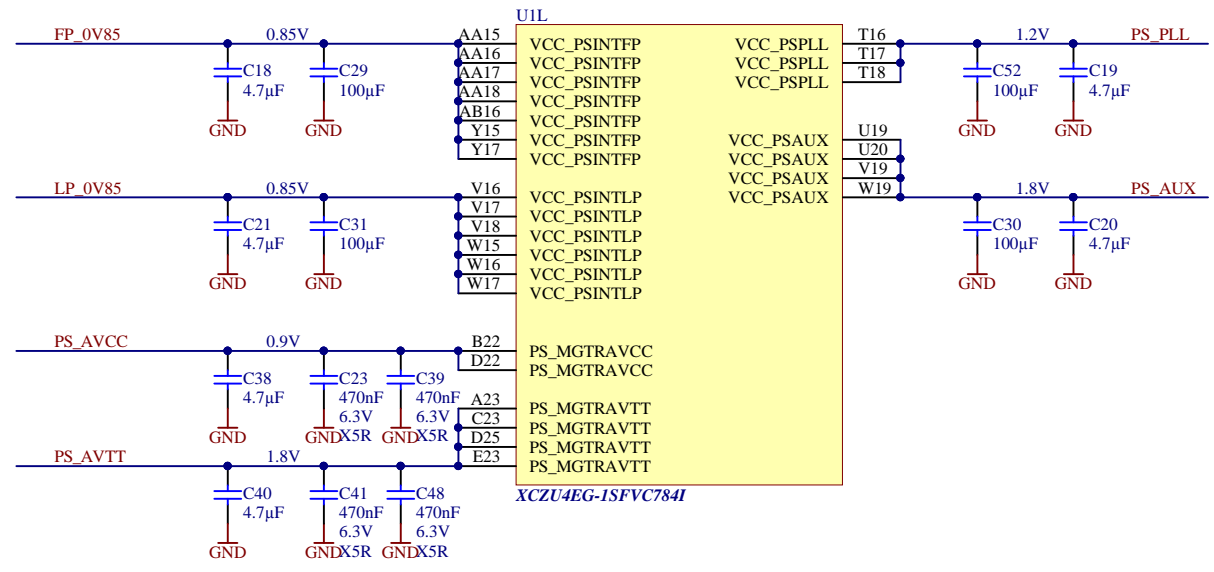
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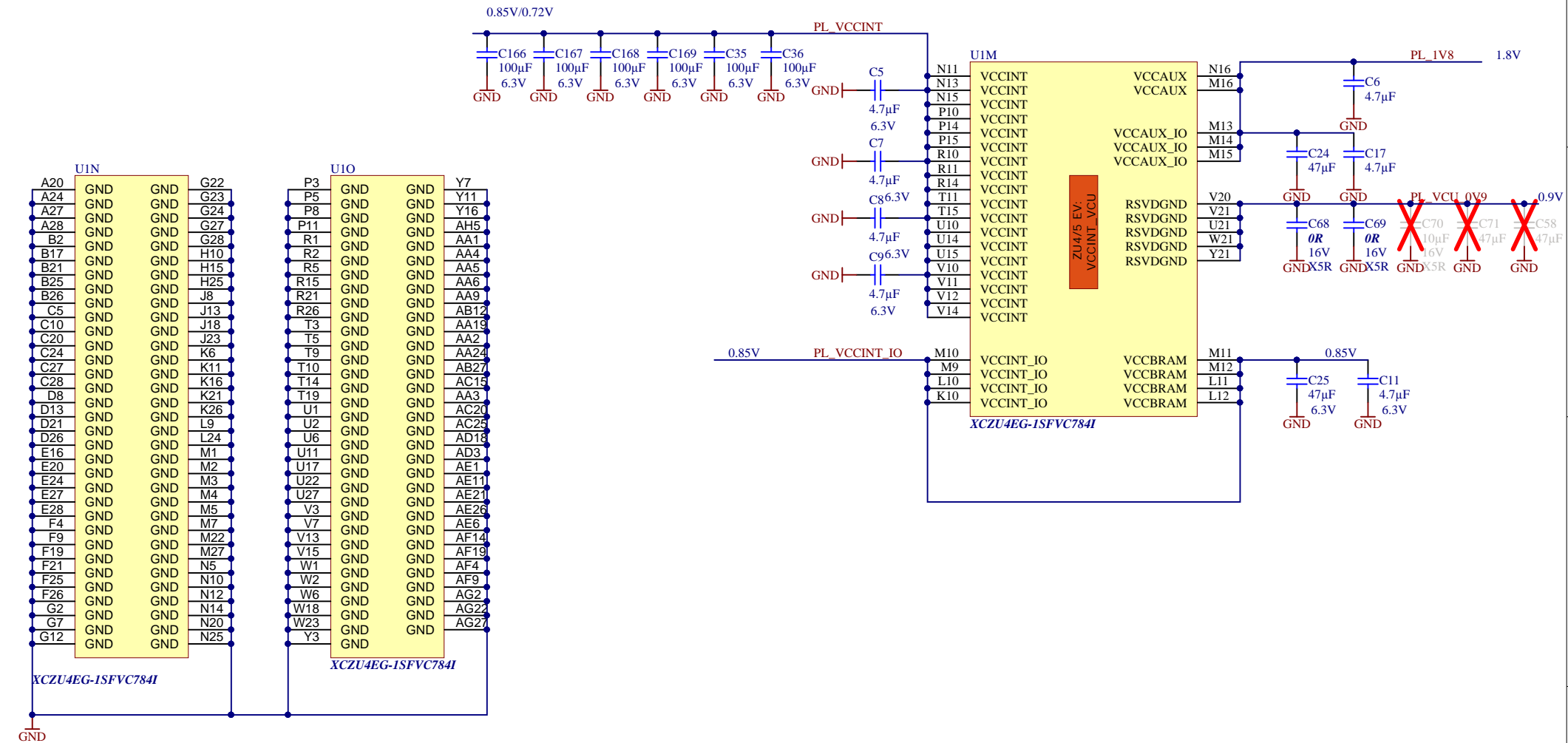
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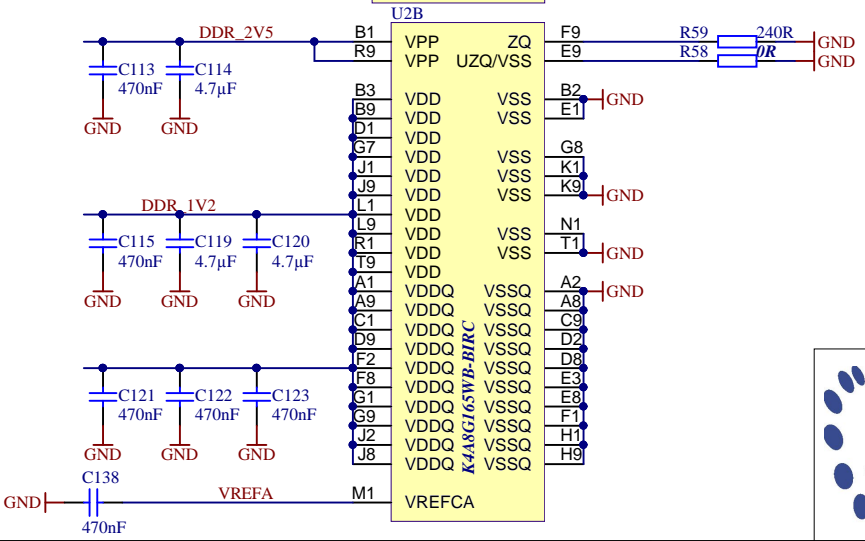
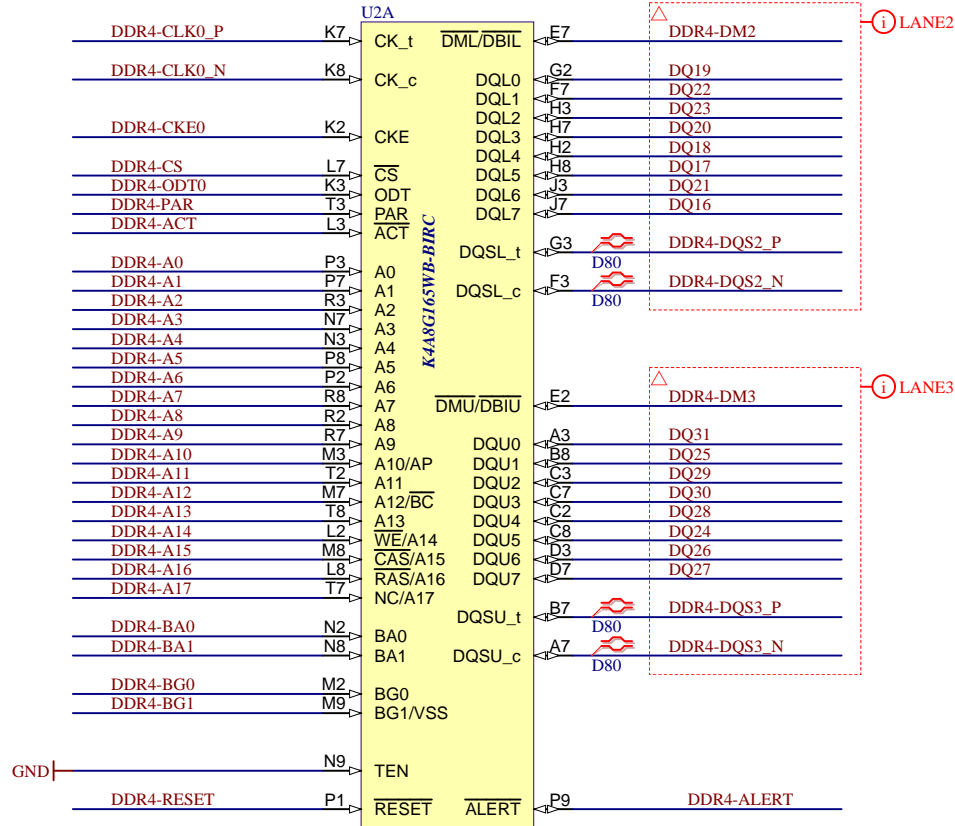

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Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: B_GT.SchDoc		Page 14 of 26	



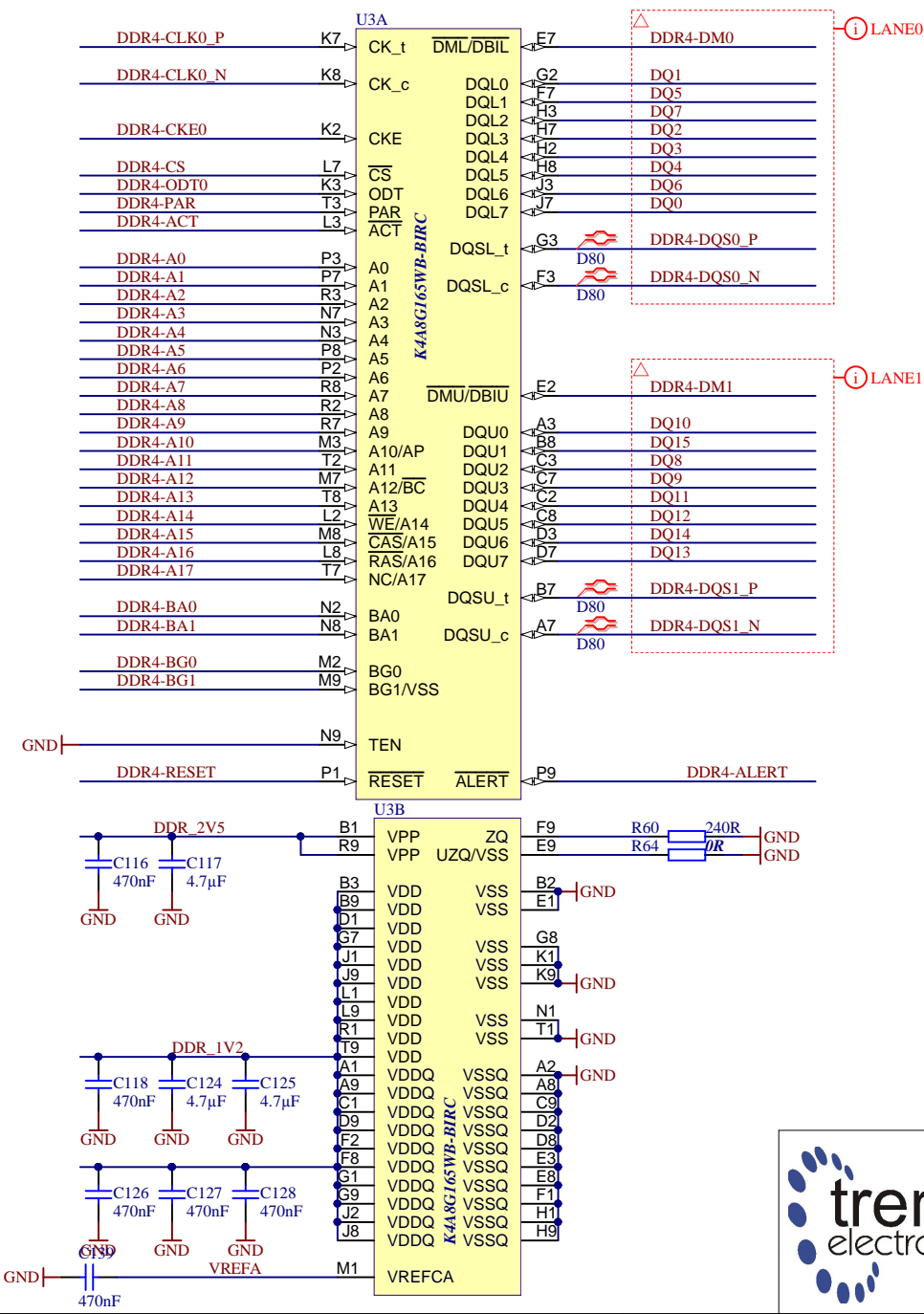
	Title: TE0803 - ZU_PS_POWER		
	A4	Number: TE0803 4BI21-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page15 of 26
	Filename: ZU_PS_POWER.SchDoc		




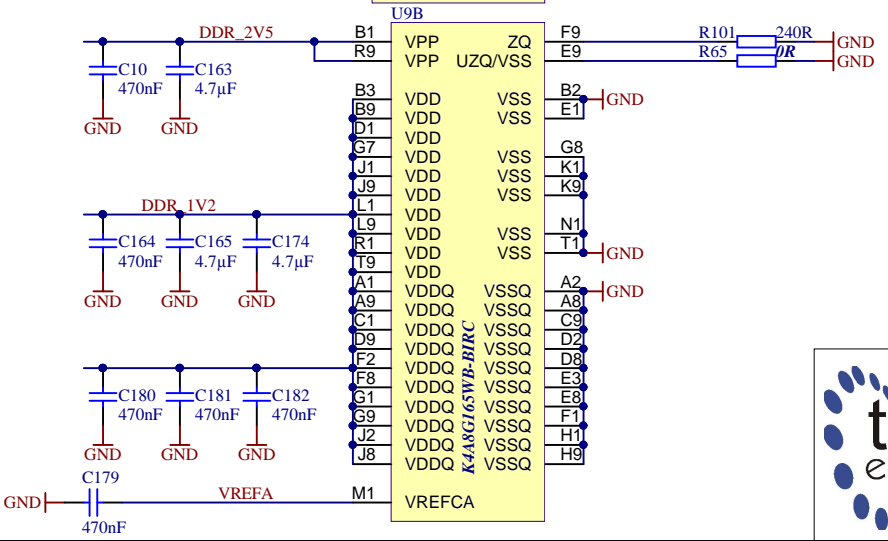
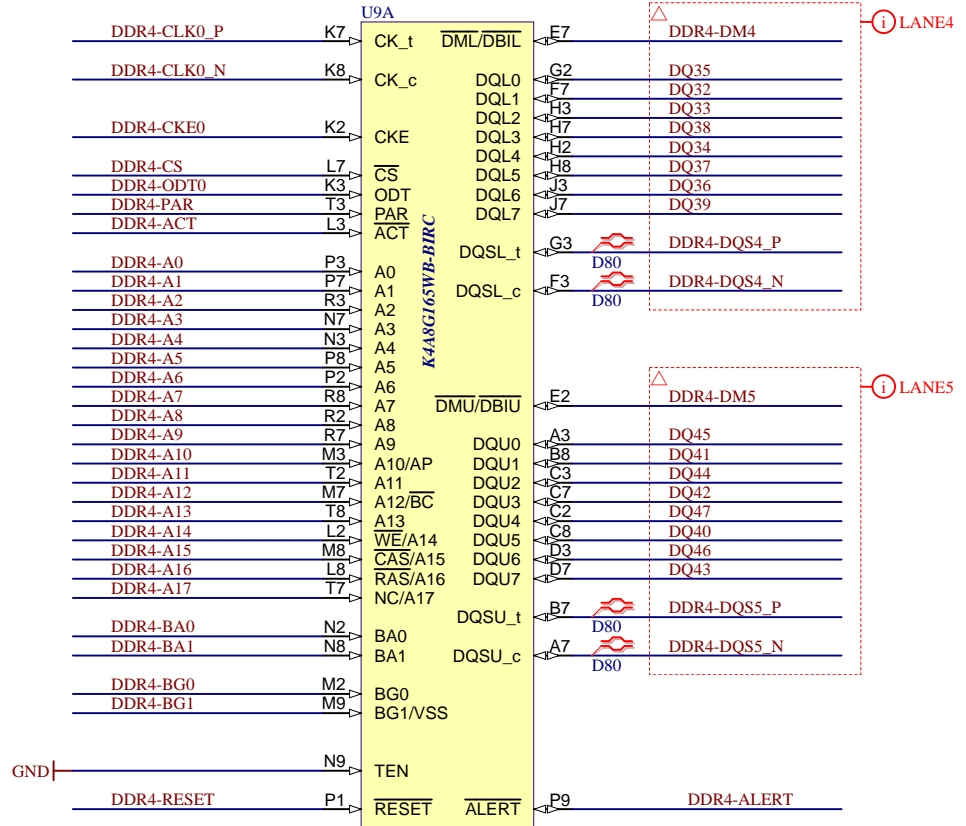
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Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: ZU_POWER.SchDoc		Page 16 of 26	

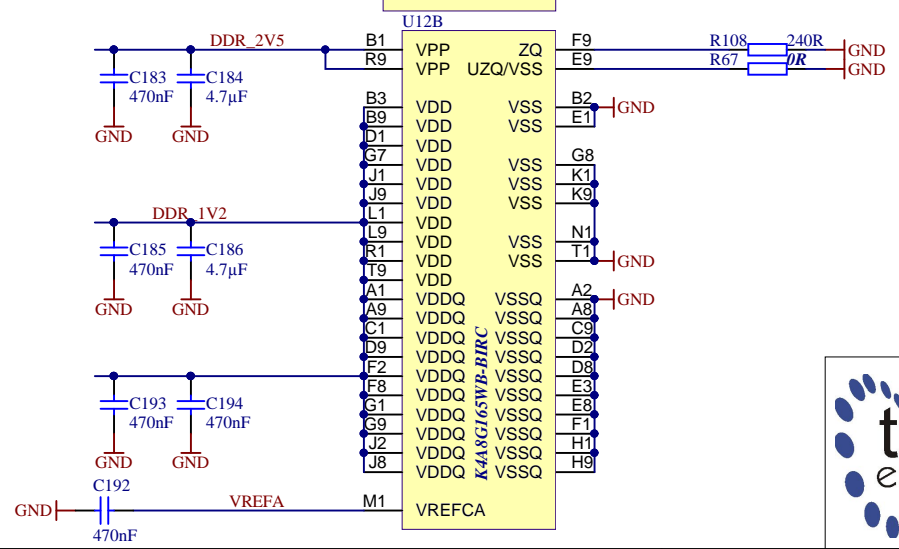
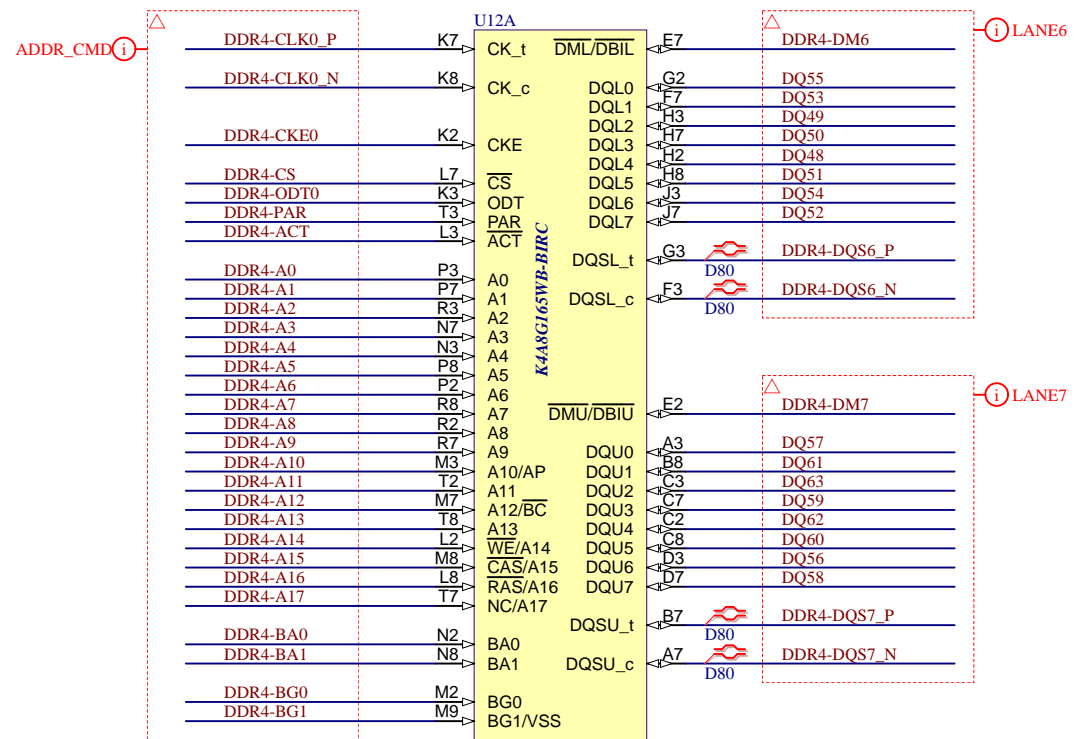
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 17 of 26
Filename: DDR4-RAM.SchDoc		



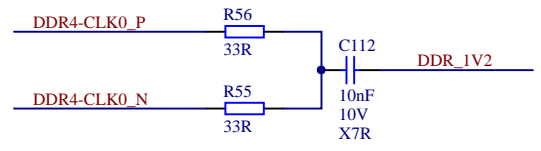
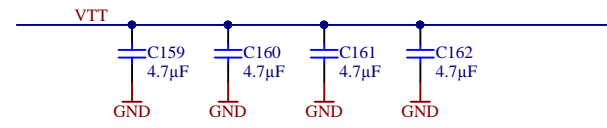
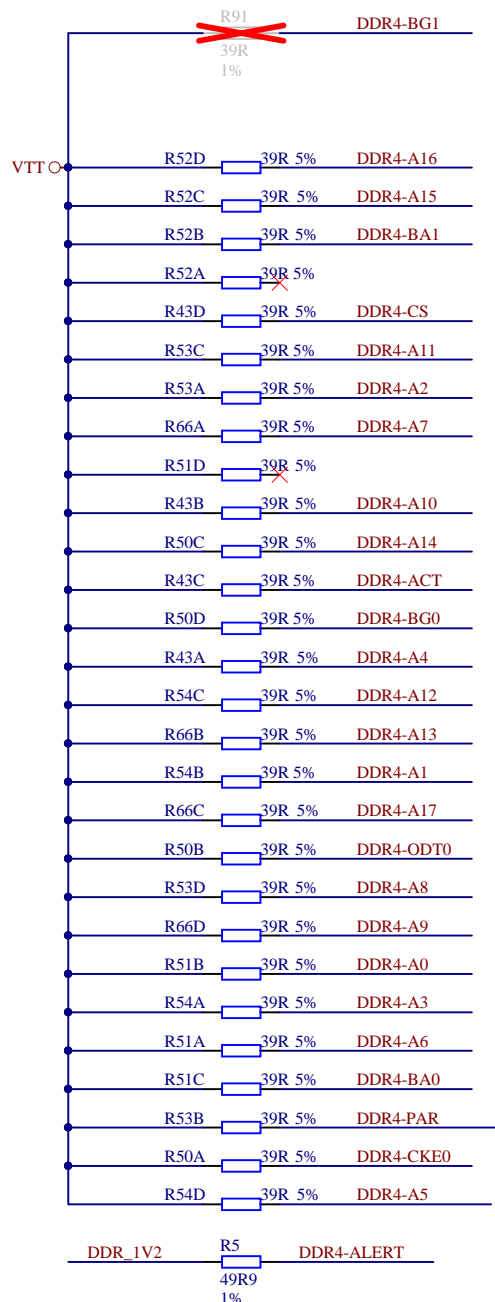
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			A4	Number: TE0803 4BI21-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT		Page 18 of 26
Filename: DDR4-RAM_2.SchDoc				



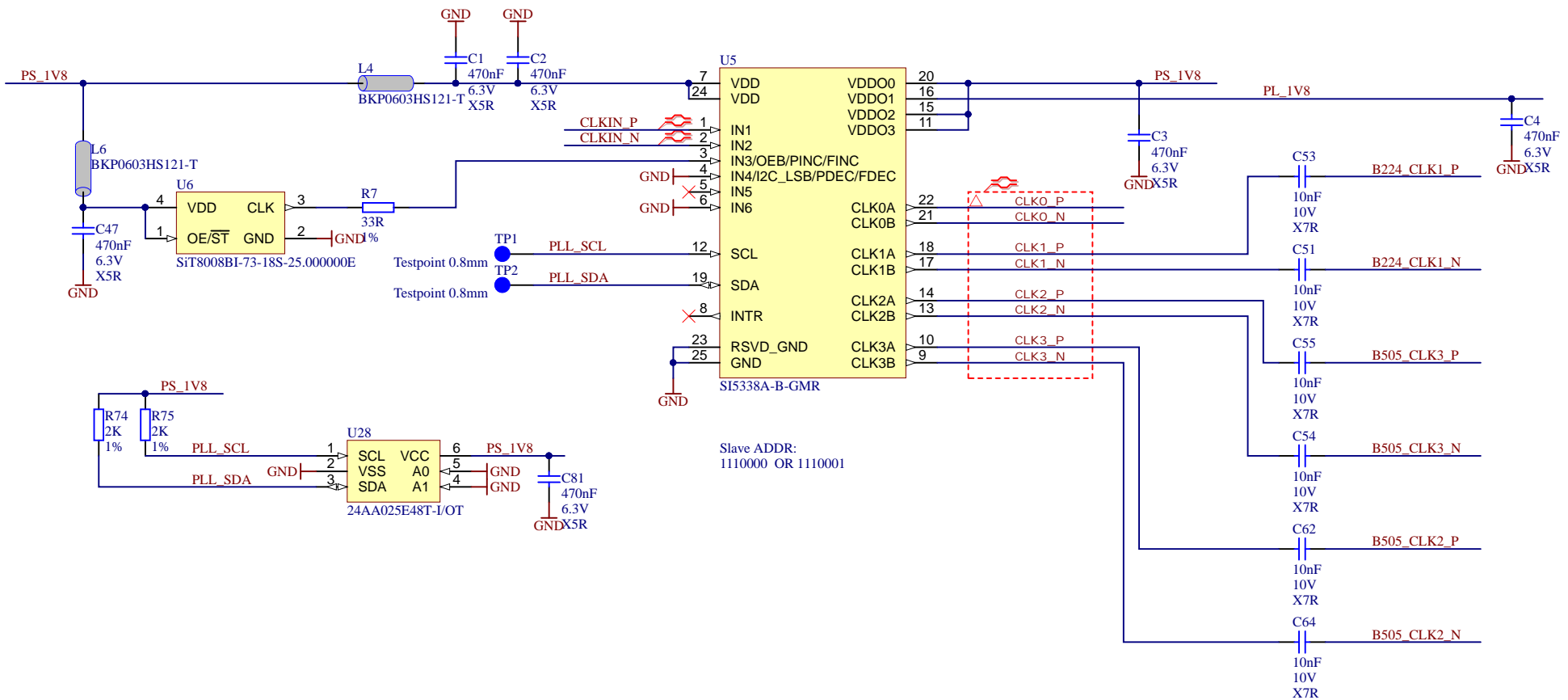
Title: TE0803 - DDR4_3_RAM		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 19 of 26
Filename: DDR4-RAM_3.SchDoc		




Title: TE0803 - DDR4_4_RAM		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page20 of 26
Filename: DDR4-RAM_4.SchDoc		

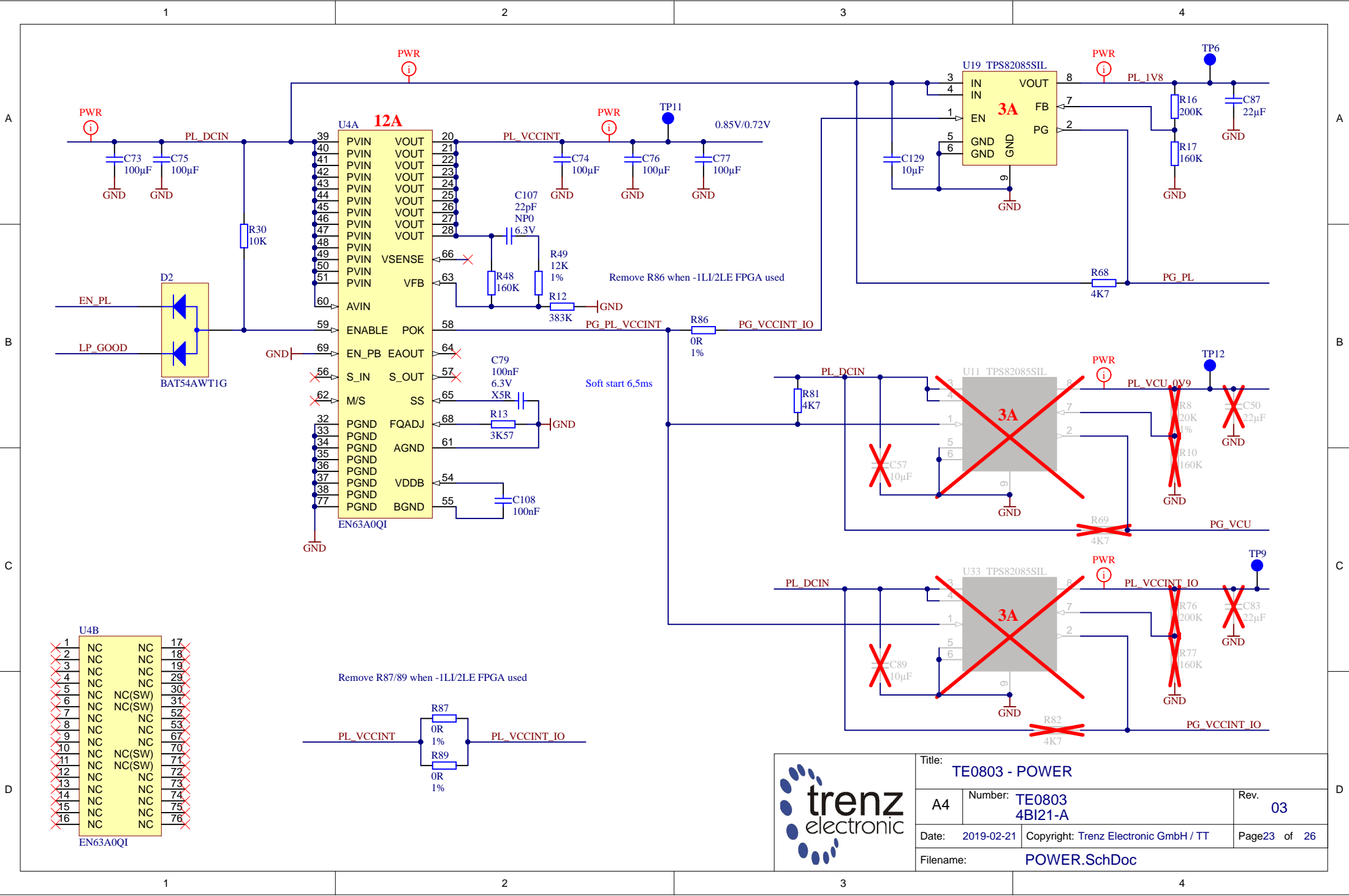


Title: TE0803 - DDR4_TERM		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page21 of 26
Filename: DDR4-TERM.SchDoc		



Slave ADDR:
1110000 OR 1110001

		Title: TE0803 - CLOCK	
		A4	Number: TE0803 4BI21-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: Clock.SchDoc		Page 22 of 26	

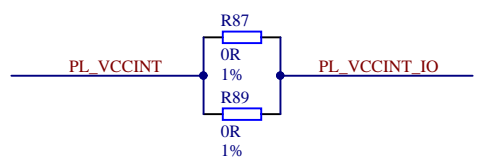


U4B

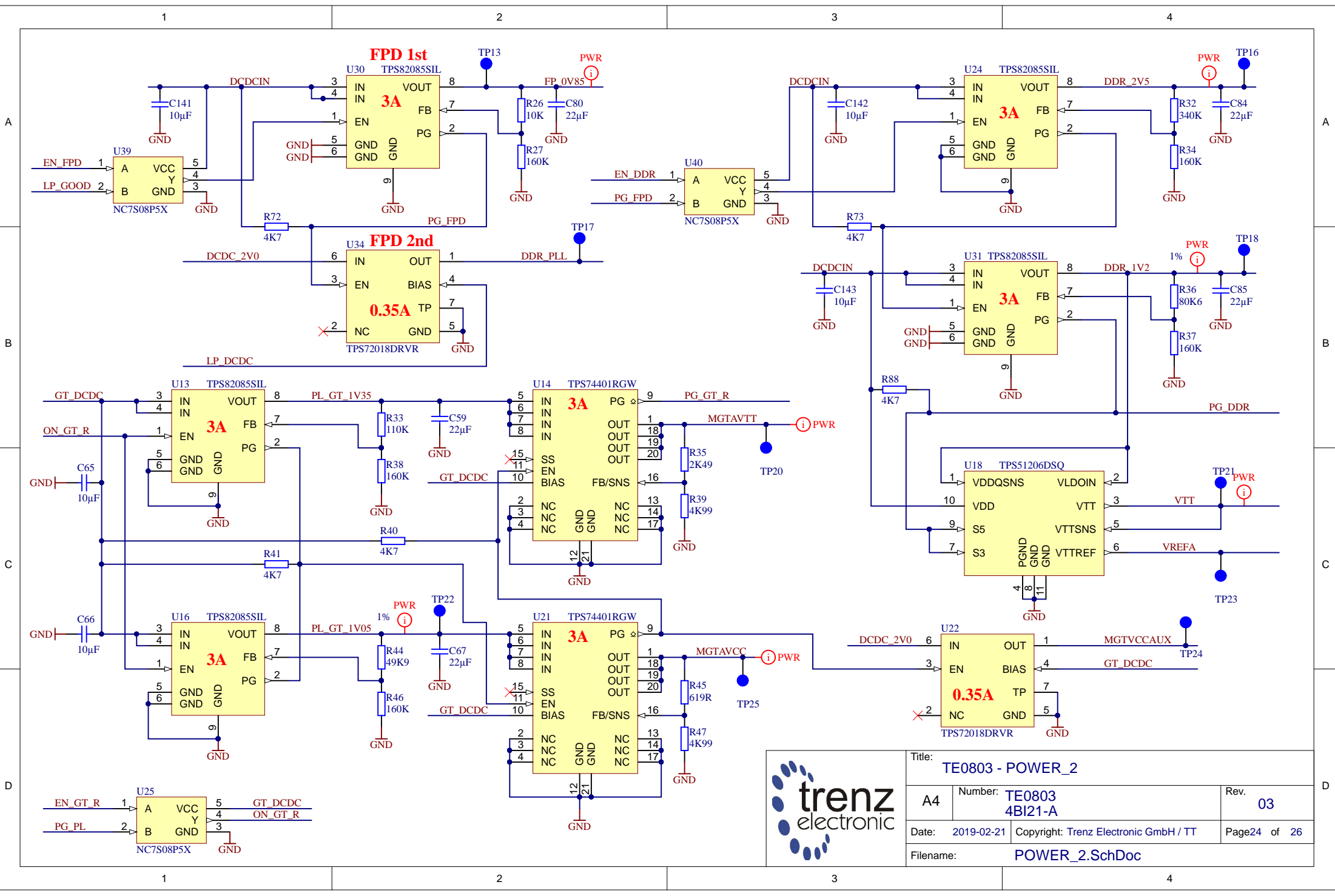
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2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76

EN63A0QI

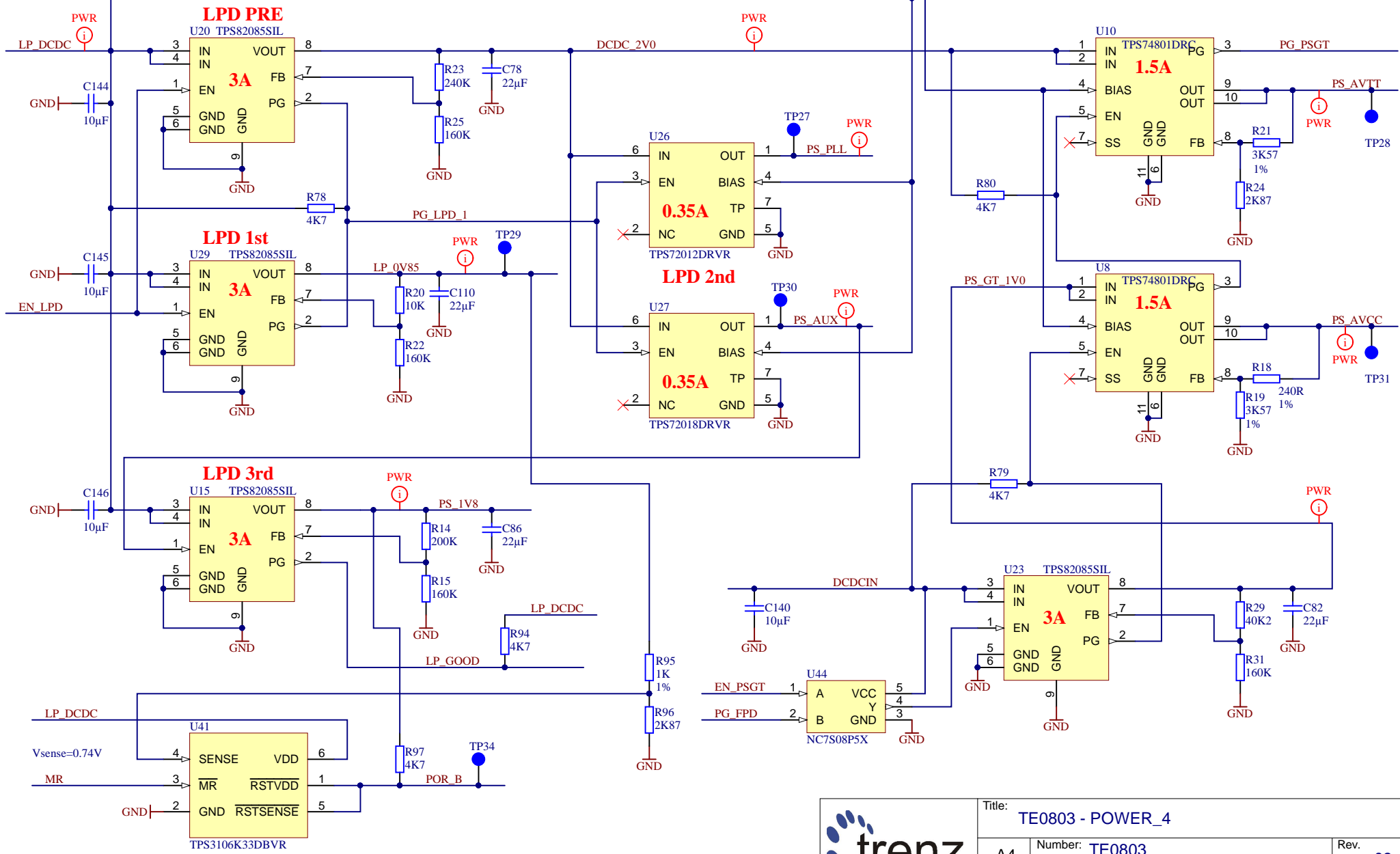
Remove R87/89 when -1L1/2LE FPGA used



Title: TE0803 - POWER		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 23 of 26
Filename: POWER.SchDoc		



Title: TE0803 - POWER_2		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page24 of 26
Filename: POWER_2.SchDoc		



Title: TE0803 - POWER_4		
A4	Number: TE0803 4BI21-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 25 of 26
Filename: POWER_4.SchDoc		

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CHANGES REV01a (20.11.2017):

- 1) VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9.

CHANGES REV02 (20.06.2018):

- 1) Added LDO to DDR_PLL
- 2) All differential pairs wath length matched with tollerance 0.1mm (excluding package delays)
- 3) Added MAC EEPROM U28
- 4) VPS_MGTRAVCC set to 0.85V
- 5) Added pull-up resistors R68,R69

CHANGES REV03 (21.02.2019):

- 1) Added support of DDP DDR4
- 2) Added support of Low power FPGA (-L1/L2).
- 3) Revised testpoints
- 4) Revised J1-J4 connectors net label style

A

A

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	Title: TE0803 - Changes list		
	A4	Number: TE0803 4BI21-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH	Page 26 of 26
	Filename: Revision_Changes.SchDoc		

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