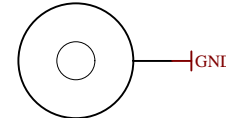


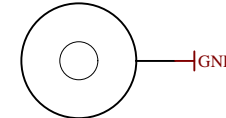
U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_DDR4-TERM DDR4-TERM.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_REV_CH Revision_Changes.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	
	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

Special notes:

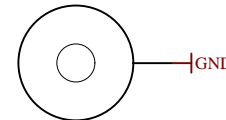
U41 Power supervisor TPS3106K33DBVR replaced by Schottky diodes SBAS70-04LT1G



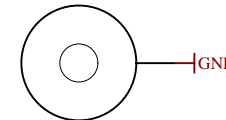
Mount.Hole 3.2mm für Unterlegscheibe



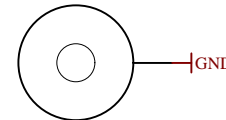
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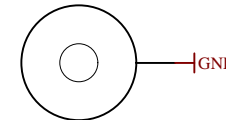
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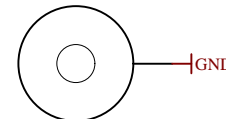
Mount.Hole 3.2mm für Unterlegscheibe



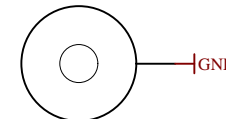
Mount.Hole 3.2mm für Unterlegscheibe



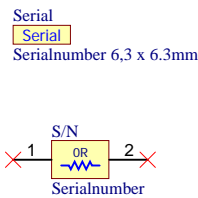
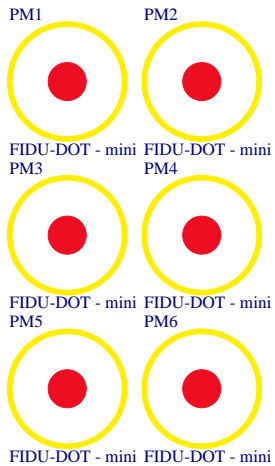
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



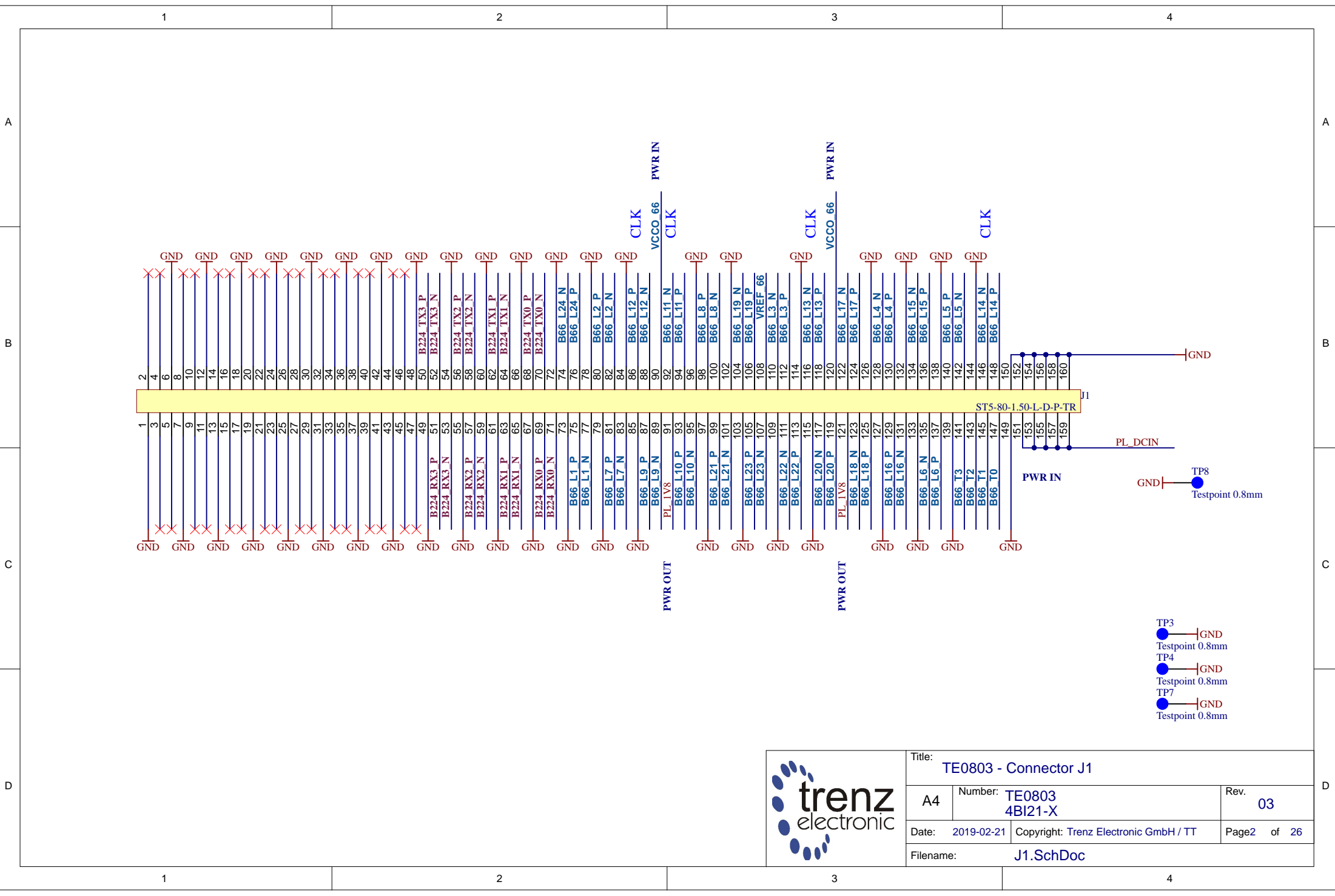
Mount.Hole 3.2mm für Unterlegscheibe



Assembly variant	4BI21-X
Created by	VY
Modified by	VY
Modified at	2019-09-16
SVN Revision	8575



Title: TE0803		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page1 of 26
Filename: TE0803.SchDoc		



Title: TE0803 - Connector J1		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page2 of 26
Filename: J1.SchDoc		

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A

A

B

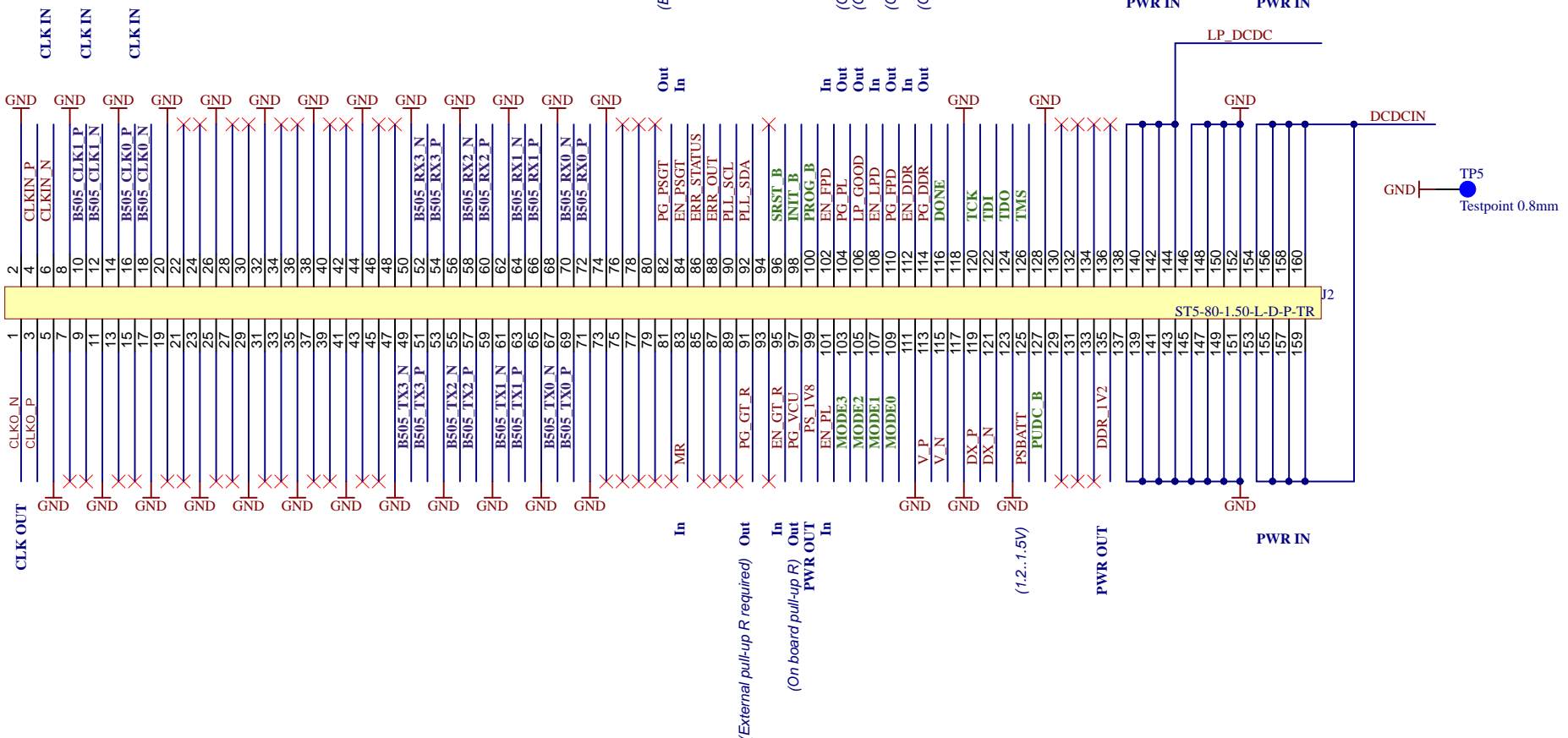
B


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D

D



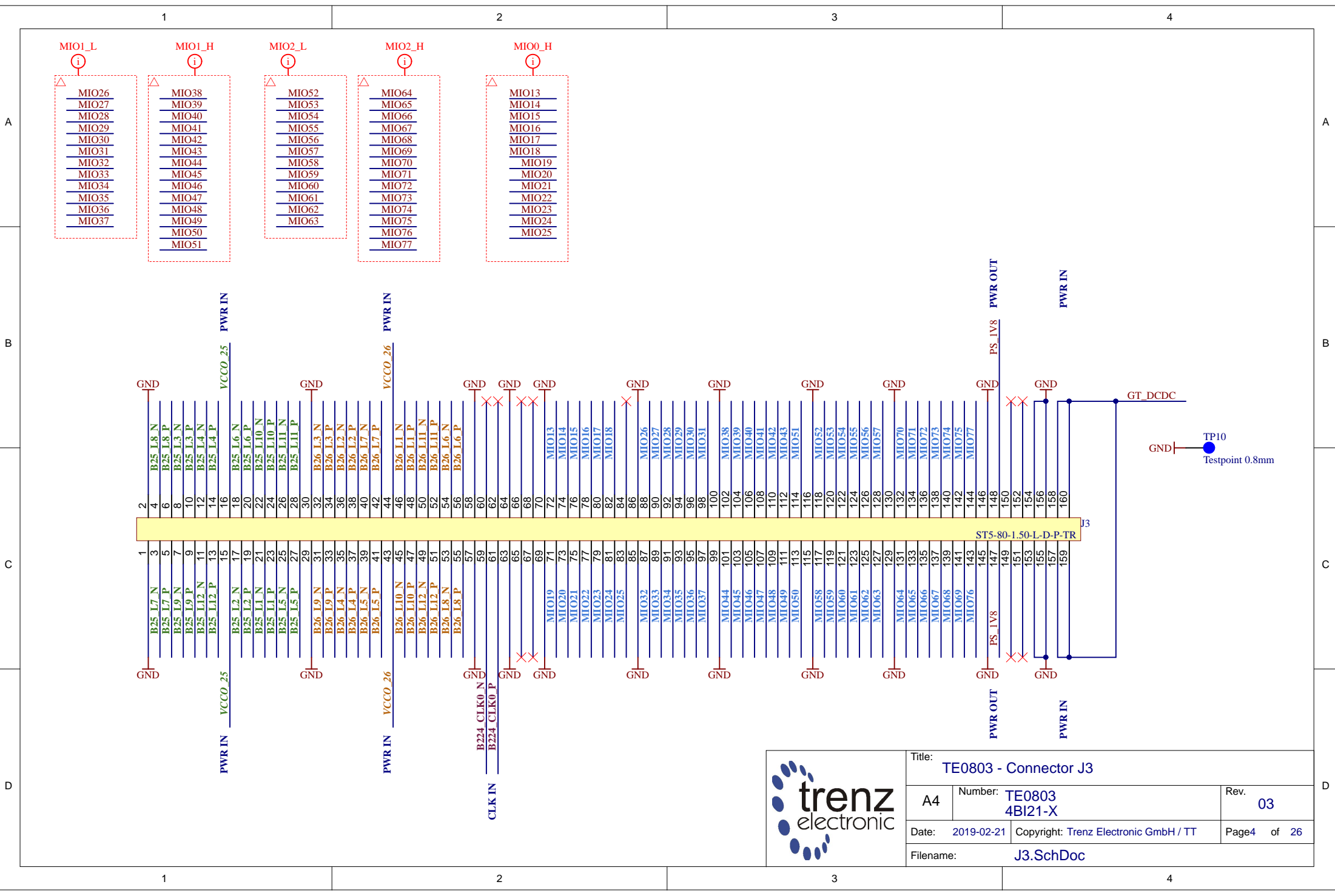
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		A4	Number: TE0803 4BI21-X
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: J2.SchDoc		Page3 of 26	

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Title: TE0803 - Connector J3		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page4 of 26
Filename: J3.SchDoc		

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A

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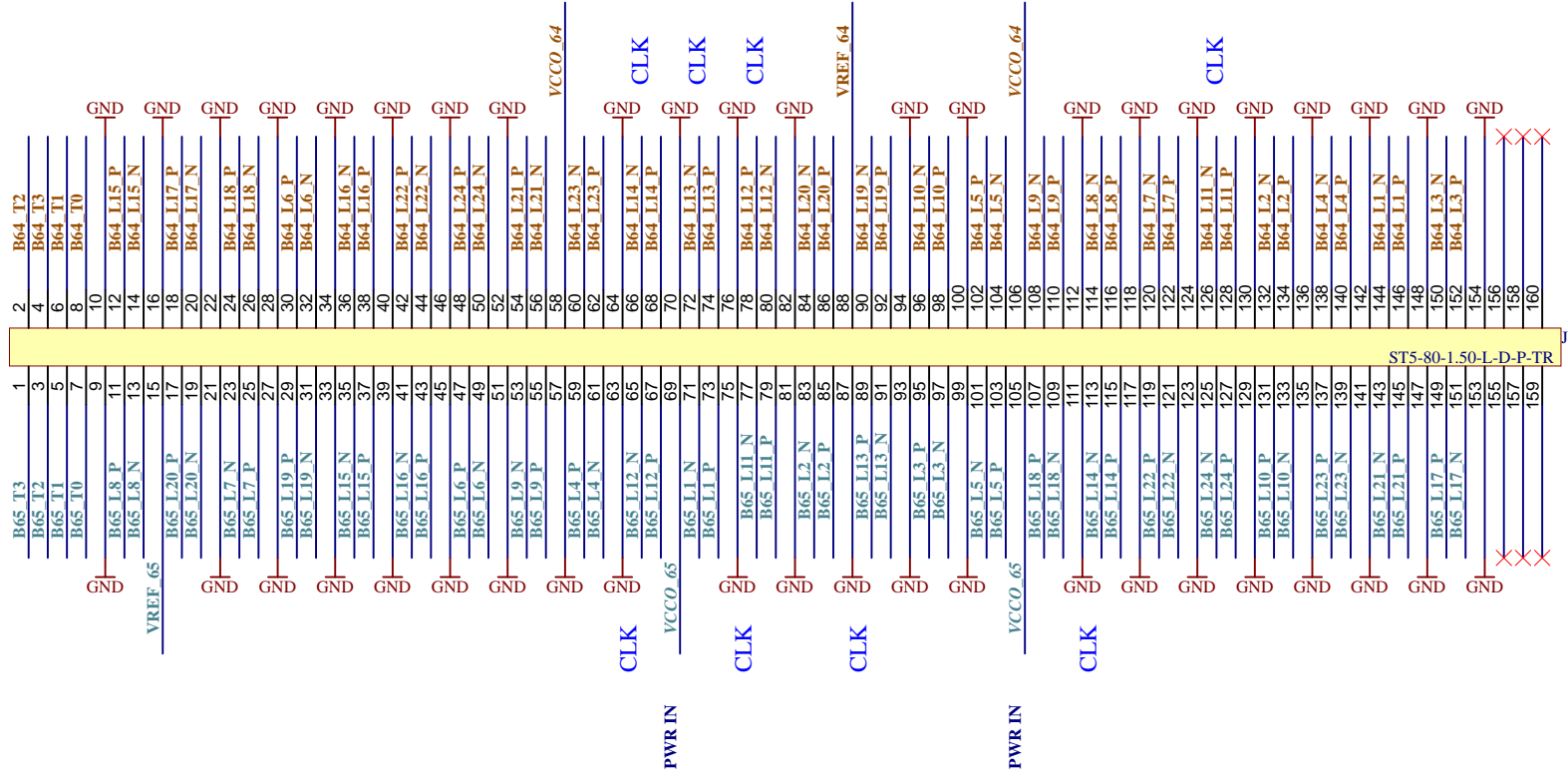
B

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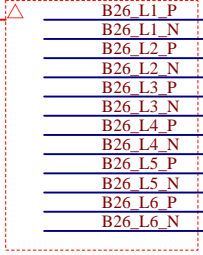
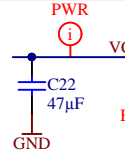
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page5 of 26
Filename: J4.SchDoc		

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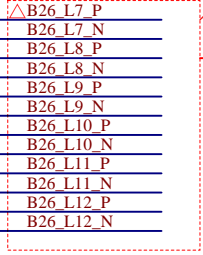
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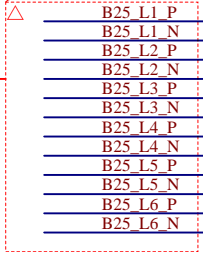
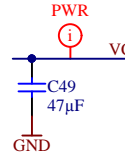
U1C XCZU4EG-1SFVC784I
BANK 46 HD (ZU2/3 BANK 26 HD)

VCCO_46	F14	VCCO_46
VCCO_46	C15	VCCO_46
IO_L1P_AD11P_46	B15	IO_L7P_HDGC_AD5P_46
IO_L1N_AD11N_46	A15	IO_L7N_HDGC_AD5N_46
IO_L2P_AD10P_46	B14	IO_L8P_HDGC_AD4P_46
IO_L2N_AD10N_46	A14	IO_L8N_HDGC_AD4N_46
IO_L3P_AD9P_46	B13	IO_L9P_AD3P_46
IO_L3N_AD9N_46	A13	IO_L9N_AD3N_46
IO_L4P_AD8P_46	C14	IO_L10P_AD2P_46
IO_L4N_AD8N_46	C13	IO_L10N_AD2N_46
IO_L5P_HDGC_AD7P_46	D15	IO_L11P_AD1P_46
IO_L5N_HDGC_AD7N_46	D14	IO_L11N_AD1N_46
IO_L6P_HDGC_AD6P_46	E14	IO_L12P_AD0P_46
IO_L6N_HDGC_AD6N_46	E13	IO_L12N_AD0N_46



BANK 43 HD (ZU2/3 BANK 44 HD)

VCCO_43	AC10	VCCO_43
VCCO_43	AG12	VCCO_43
IO_L1P_AD11P_43	AG10	IO_L7P_HDGC_AD5P_43
IO_L1N_AD11N_43	AH10	IO_L7N_HDGC_AD5N_43
IO_L2P_AD10P_43	AF11	IO_L8P_HDGC_AD4P_43
IO_L2N_AD10N_43	AG11	IO_L8N_HDGC_AD4N_43
IO_L3P_AD9P_43	AH12	IO_L9P_AD3P_43
IO_L3N_AD9N_43	AH11	IO_L9N_AD3N_43
IO_L4P_AD8P_43	AE10	IO_L10P_AD2P_43
IO_L4N_AD8N_43	AF10	IO_L10N_AD2N_43
IO_L5P_HDGC_AD7P_43	AE12	IO_L11P_AD1P_43
IO_L5N_HDGC_AD7N_43	AF12	IO_L11N_AD1N_43
IO_L6P_HDGC_AD6P_43	AC13	IO_L12P_AD0P_43
IO_L6N_HDGC_AD6N_43	AD12	IO_L12N_AD0N_43



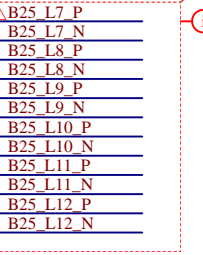
U1B
BANK 44 HD (ZU2/3 BANK 24 HD)

VCCO_44	AA14	VCCO_44
VCCO_44	AD13	VCCO_44
IO_L1P_AD15P_44	AE15	IO_L7P_HDGC_44
IO_L1N_AD15N_44	AE14	IO_L7N_HDGC_44
IO_L2P_AD14P_44	AG14	IO_L8P_HDGC_44
IO_L2N_AD14N_44	AH11	IO_L8N_HDGC_44
IO_L3P_AD13P_44	AG13	IO_L9P_AD11P_44
IO_L3N_AD13N_44	AH13	IO_L9N_AD11N_44
IO_L4P_AD12P_44	AE13	IO_L10P_AD10P_44
IO_L4N_AD12N_44	AF13	IO_L10N_AD10N_44
IO_L5P_HDGC_44	AD15	IO_L11P_AD9P_44
IO_L5N_HDGC_44	AD14	IO_L11N_AD9N_44
IO_L6P_HDGC_44	AC14	IO_L12P_AD8P_44
IO_L6N_HDGC_44	AC13	IO_L12N_AD8N_44

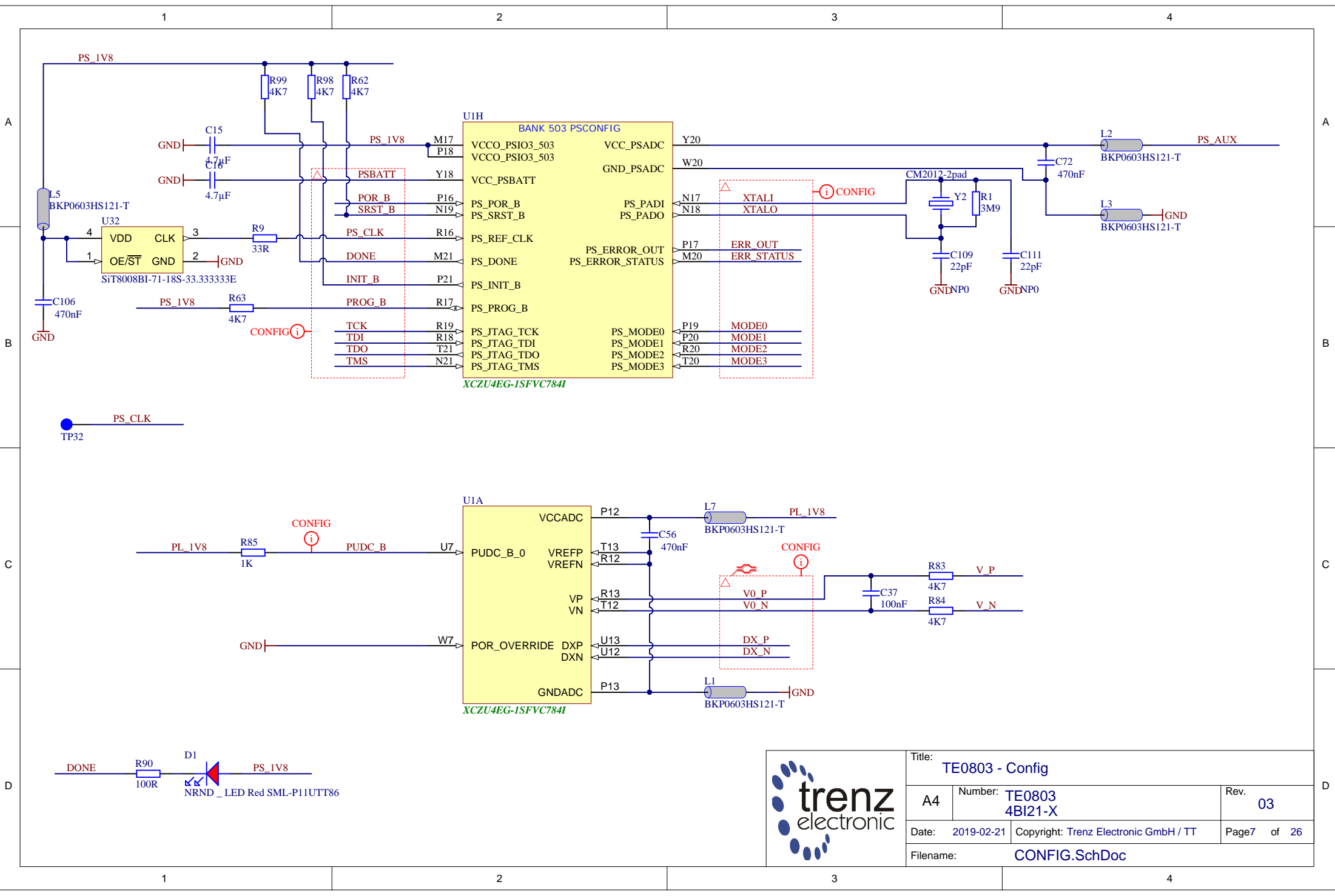


XCZU4EG-1SFVC784I
BANK 45 HD (ZU2/3 BANK 25 HD)

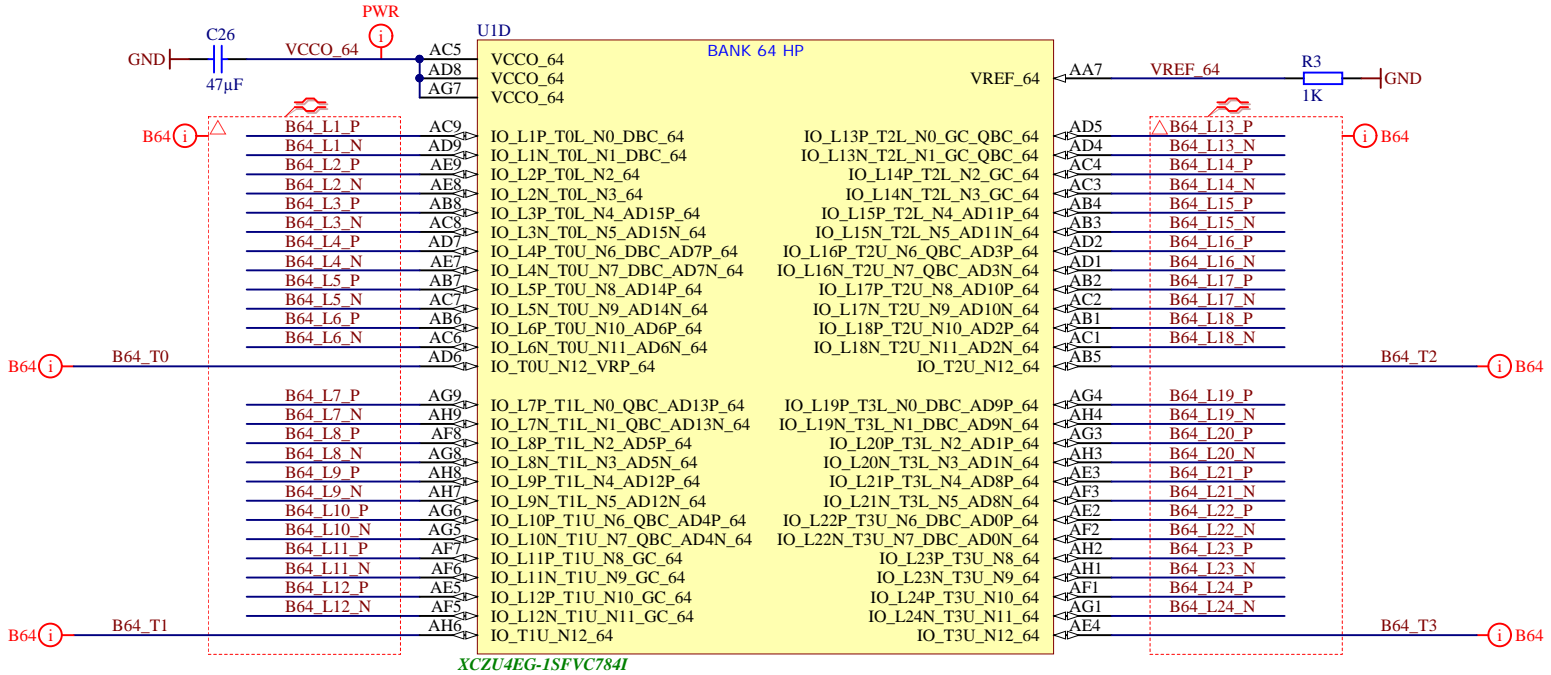
VCCO_45	B12	VCCO_45
VCCO_45	E11	VCCO_45
IO_L1P_AD15P_45	J11	IO_L7P_HDGC_45
IO_L1N_AD15N_45	J10	IO_L7N_HDGC_45
IO_L2P_AD14P_45	K13	IO_L8P_HDGC_45
IO_L2N_AD14N_45	K12	IO_L8N_HDGC_45
IO_L3P_AD13P_45	H11	IO_L9P_AD11P_45
IO_L3N_AD13N_45	G10	IO_L9N_AD11N_45
IO_L4P_AD12P_45	J12	IO_L10P_AD10P_45
IO_L4N_AD12N_45	H12	IO_L10N_AD10N_45
IO_L5P_HDGC_45	G11	IO_L11P_AD9P_45
IO_L5N_HDGC_45	F11	IO_L11N_AD9N_45
IO_L6P_HDGC_45	F12	IO_L12P_AD8P_45
IO_L6N_HDGC_45	F11	IO_L12N_AD8N_45



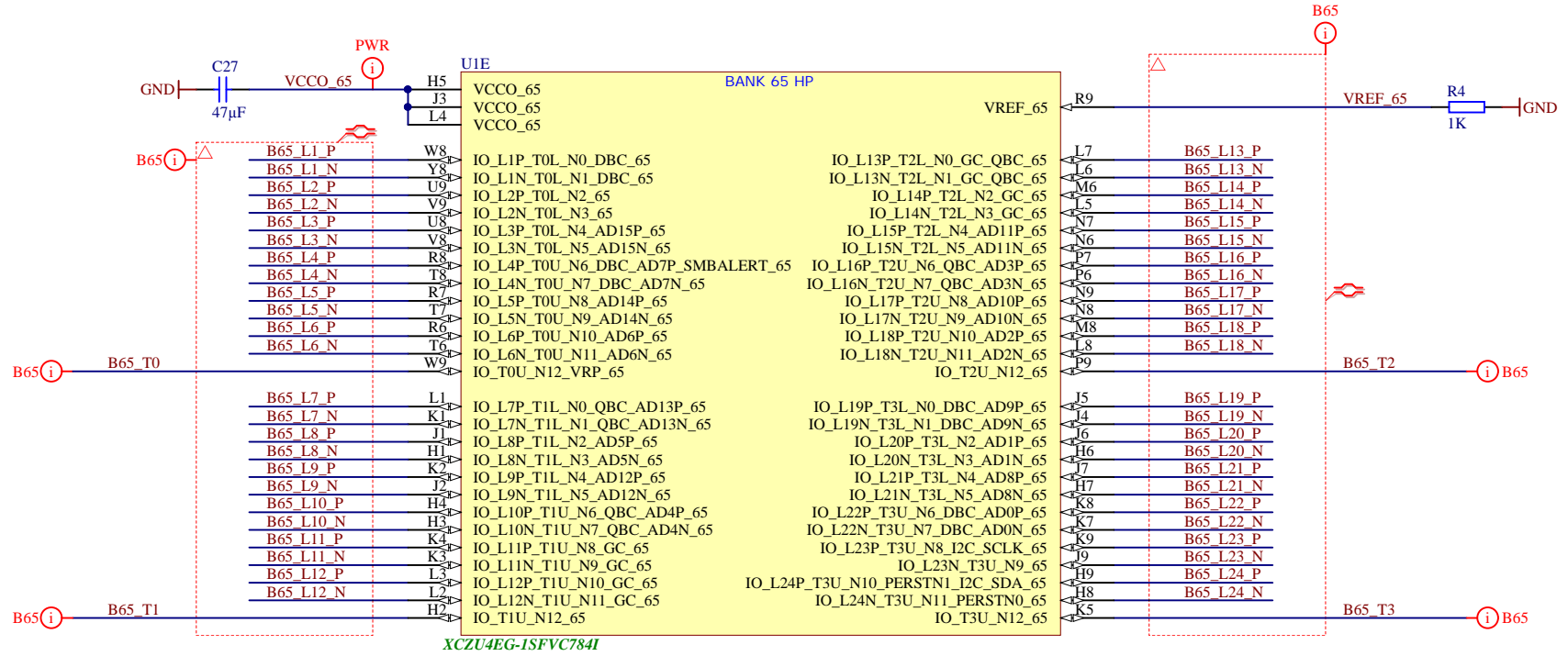
Title: TE0803 - HD Banks		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 6 of 26
Filename: B_HD.SchDoc		



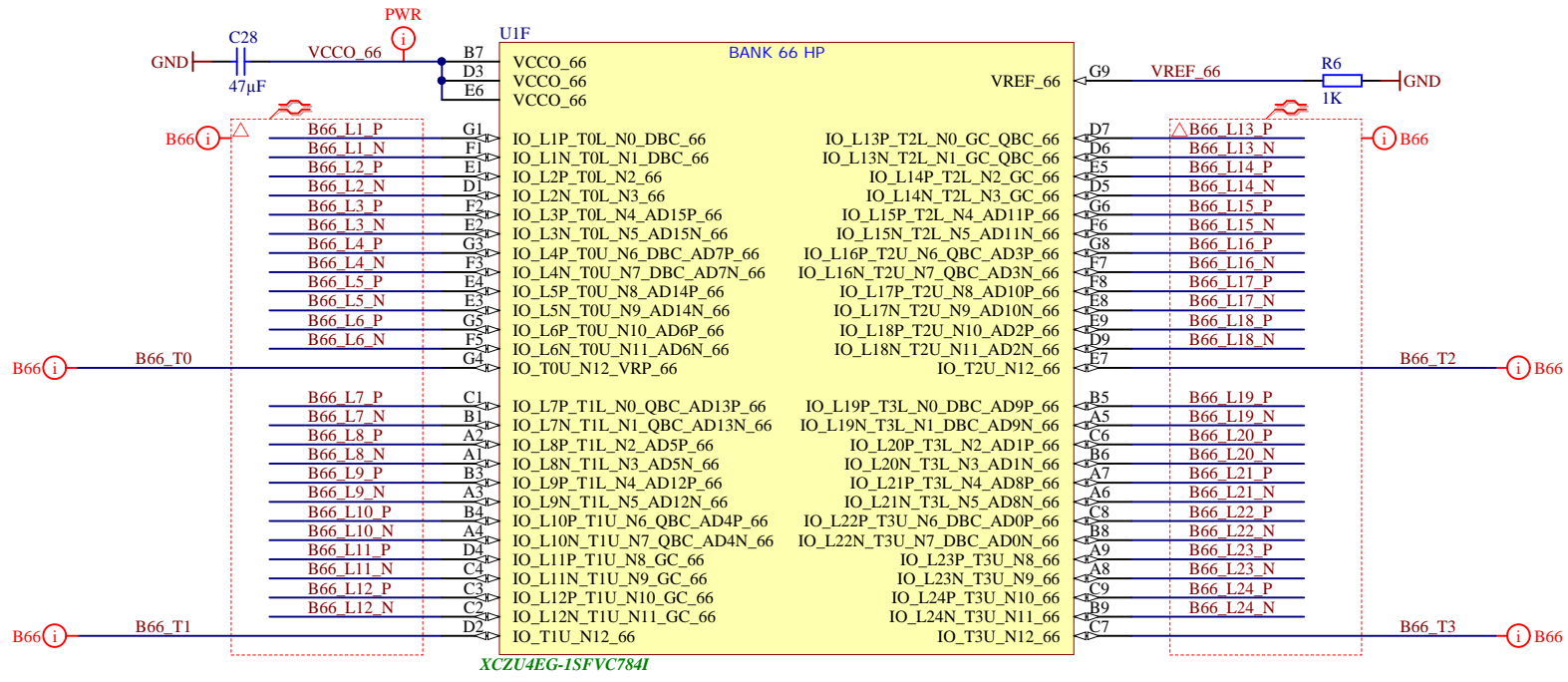
Title: TE0803 - Config		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 7 of 26
Filename: CONFIG.SchDoc		



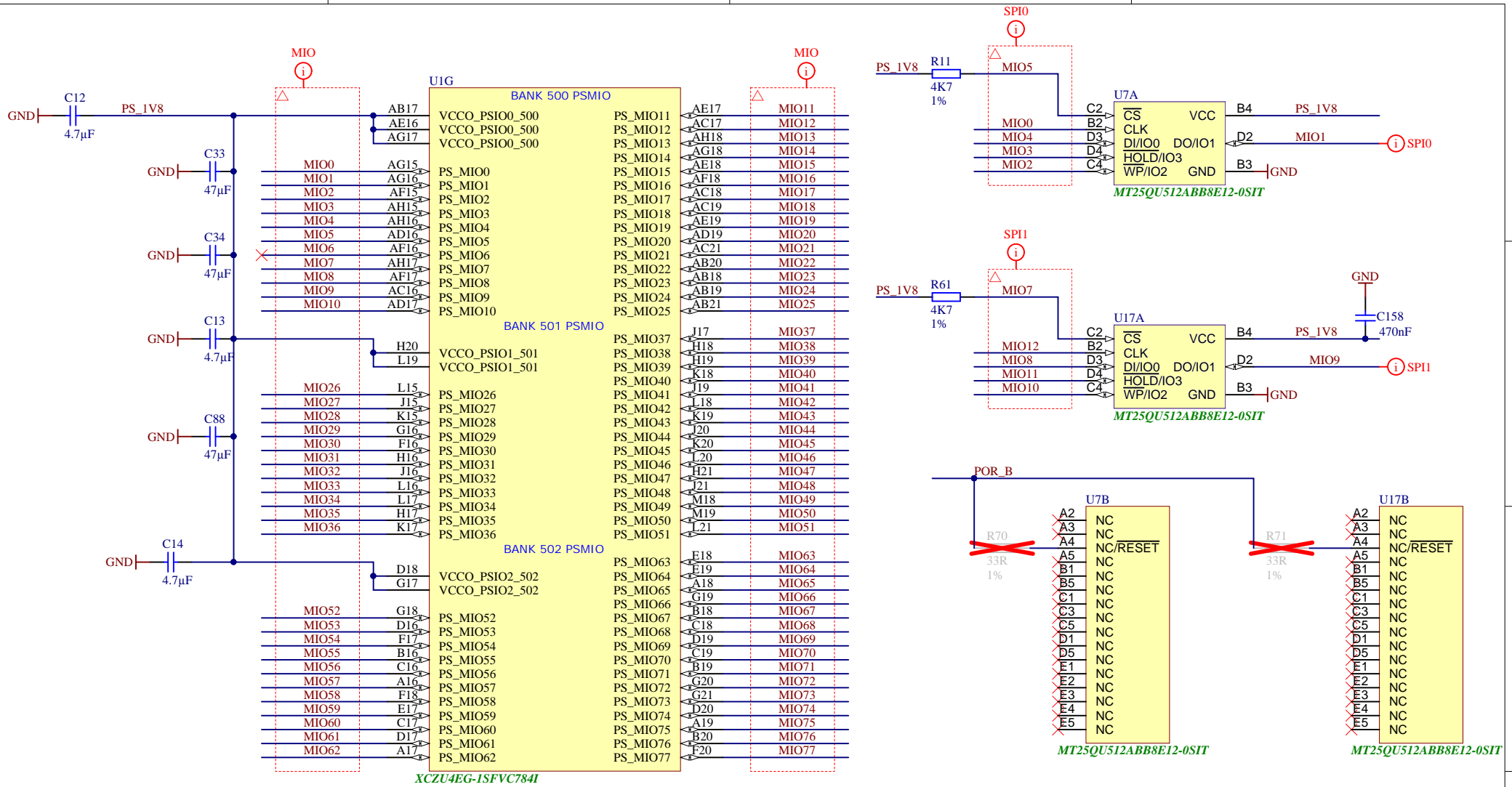
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A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 8 of 26
Filename: B64.SchDoc		




Title: TE0803 - B65		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page9 of 26
Filename: B65.SchDoc		



Title: TE0803 - B66		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 10 of 26
Filename: B66.SchDoc		



			Title: TE0803 - MIO Banks	
			A4	Number: TE0803 4BI21-X
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT		Page 11 of 26
Filename: B_MIO.SchDoc				

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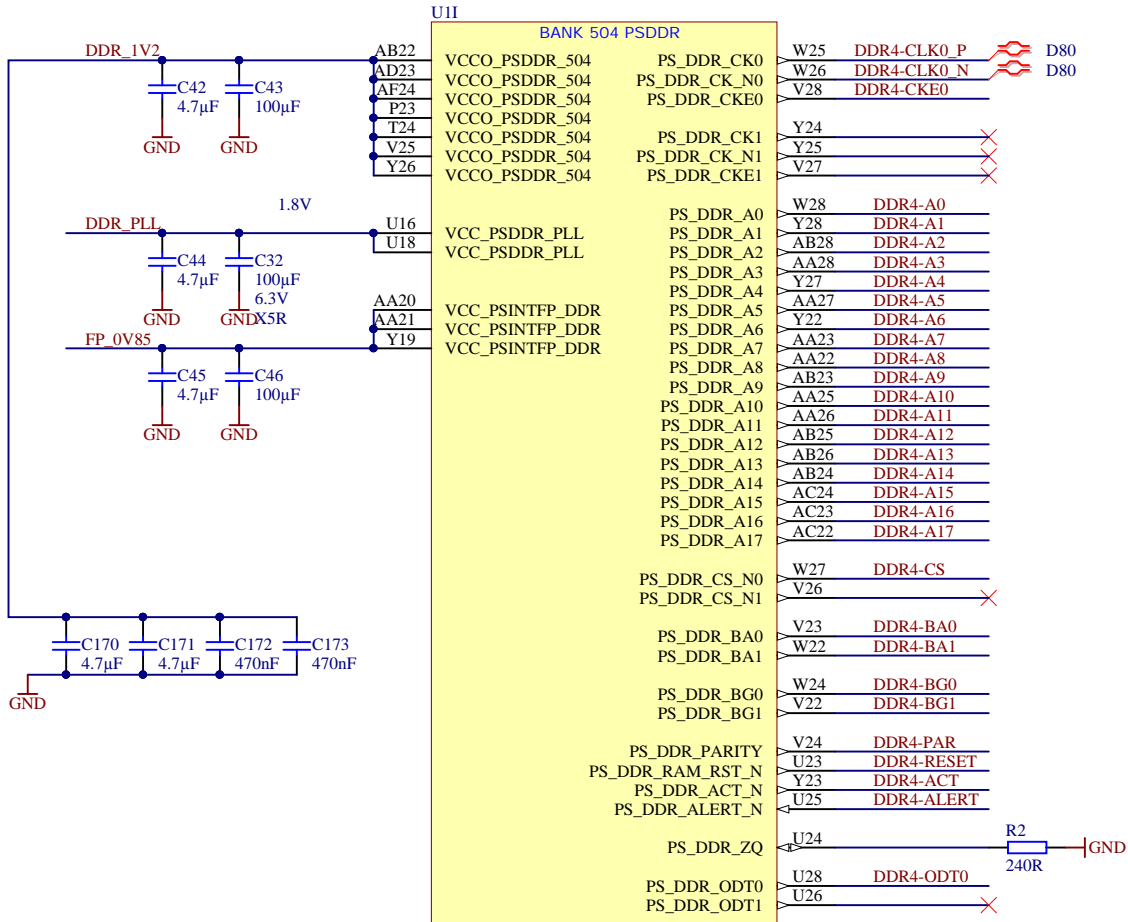
D

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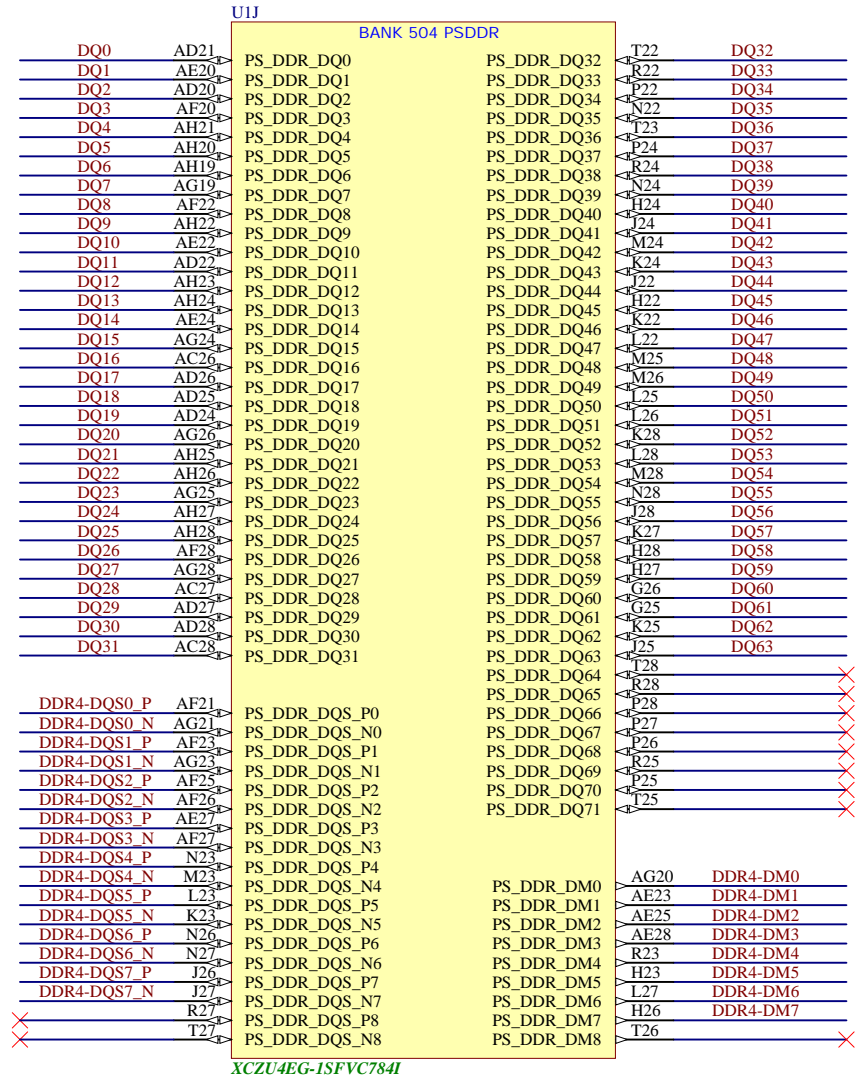
C

D



U1I		BANK 504 PSDDR	
V25	DDR4-CLK0 P	W25	DDR4-CLK0 P
W26	DDR4-CLK0 N	W26	DDR4-CLK0 N
V28	DDR4-CKE0	V28	DDR4-CKE0
Y24		Y24	
Y25		Y25	
V27		V27	
W28	DDR4-A0	W28	DDR4-A0
Y28	DDR4-A1	Y28	DDR4-A1
AB28	DDR4-A2	AB28	DDR4-A2
AA28	DDR4-A3	AA28	DDR4-A3
Y27	DDR4-A4	Y27	DDR4-A4
AA27	DDR4-A5	AA27	DDR4-A5
Y22	DDR4-A6	Y22	DDR4-A6
AA23	DDR4-A7	AA23	DDR4-A7
AA22	DDR4-A8	AA22	DDR4-A8
AB23	DDR4-A9	AB23	DDR4-A9
AA25	DDR4-A10	AA25	DDR4-A10
AA26	DDR4-A11	AA26	DDR4-A11
AB25	DDR4-A12	AB25	DDR4-A12
AB26	DDR4-A13	AB26	DDR4-A13
AB24	DDR4-A14	AB24	DDR4-A14
AC24	DDR4-A15	AC24	DDR4-A15
AC23	DDR4-A16	AC23	DDR4-A16
AC22	DDR4-A17	AC22	DDR4-A17
W27	DDR4-CS	W27	DDR4-CS
V26		V26	
V23	DDR4-BA0	V23	DDR4-BA0
W22	DDR4-BA1	W22	DDR4-BA1
W24	DDR4-BG0	W24	DDR4-BG0
V22	DDR4-BG1	V22	DDR4-BG1
V24	DDR4-PAR	V24	DDR4-PAR
U23	DDR4-RESET	U23	DDR4-RESET
Y23	DDR4-ACT	Y23	DDR4-ACT
U25	DDR4-ALERT	U25	DDR4-ALERT
U24	DDR4-ZQ	U24	DDR4-ZQ
U28	DDR4-ODT0	U28	DDR4-ODT0
U26	DDR4-ODT1	U26	DDR4-ODT1

XCZU4EG-1SFVC784I



XCZU4EG-1SFVC784I



Title: TE0803 - PS_DDR		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 12 of 26
Filename: PS_DDR.SchDoc		

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A

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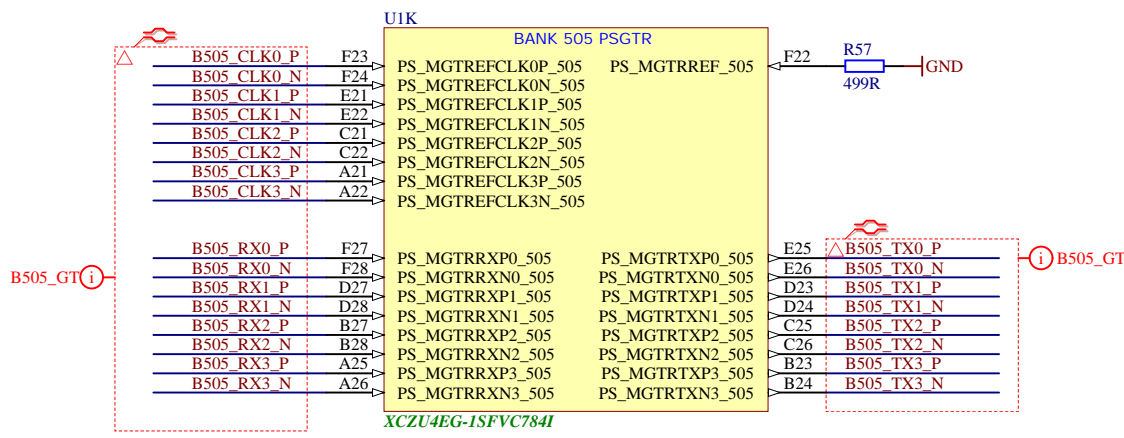
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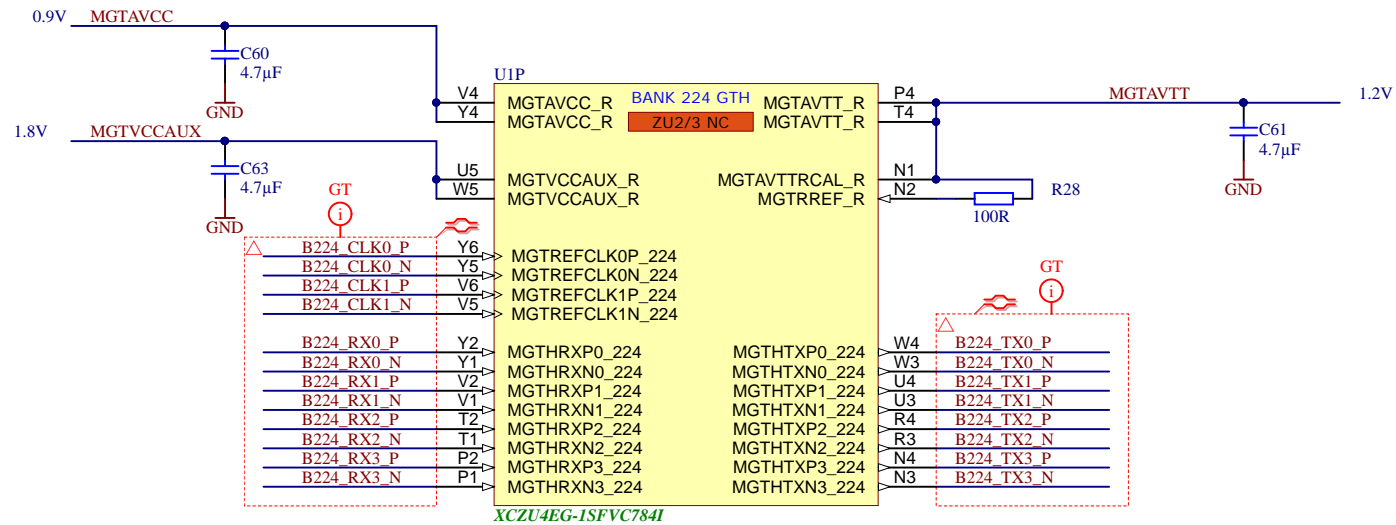
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	A4	Number: TE0803 4BI21-X	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 13 of 26
	Filename: B_PS_GT.SchDoc		


1

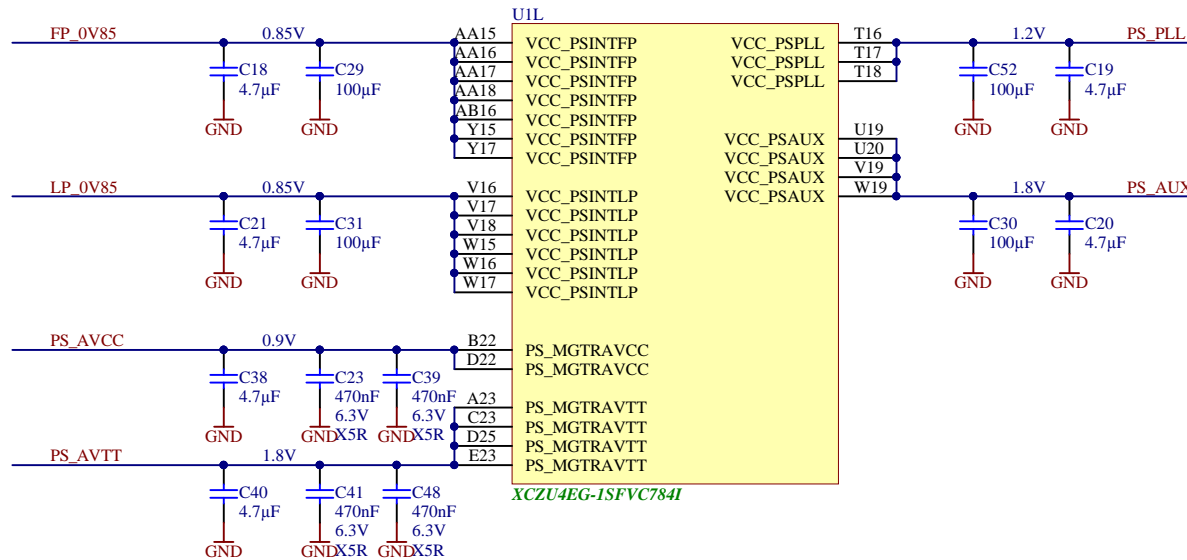
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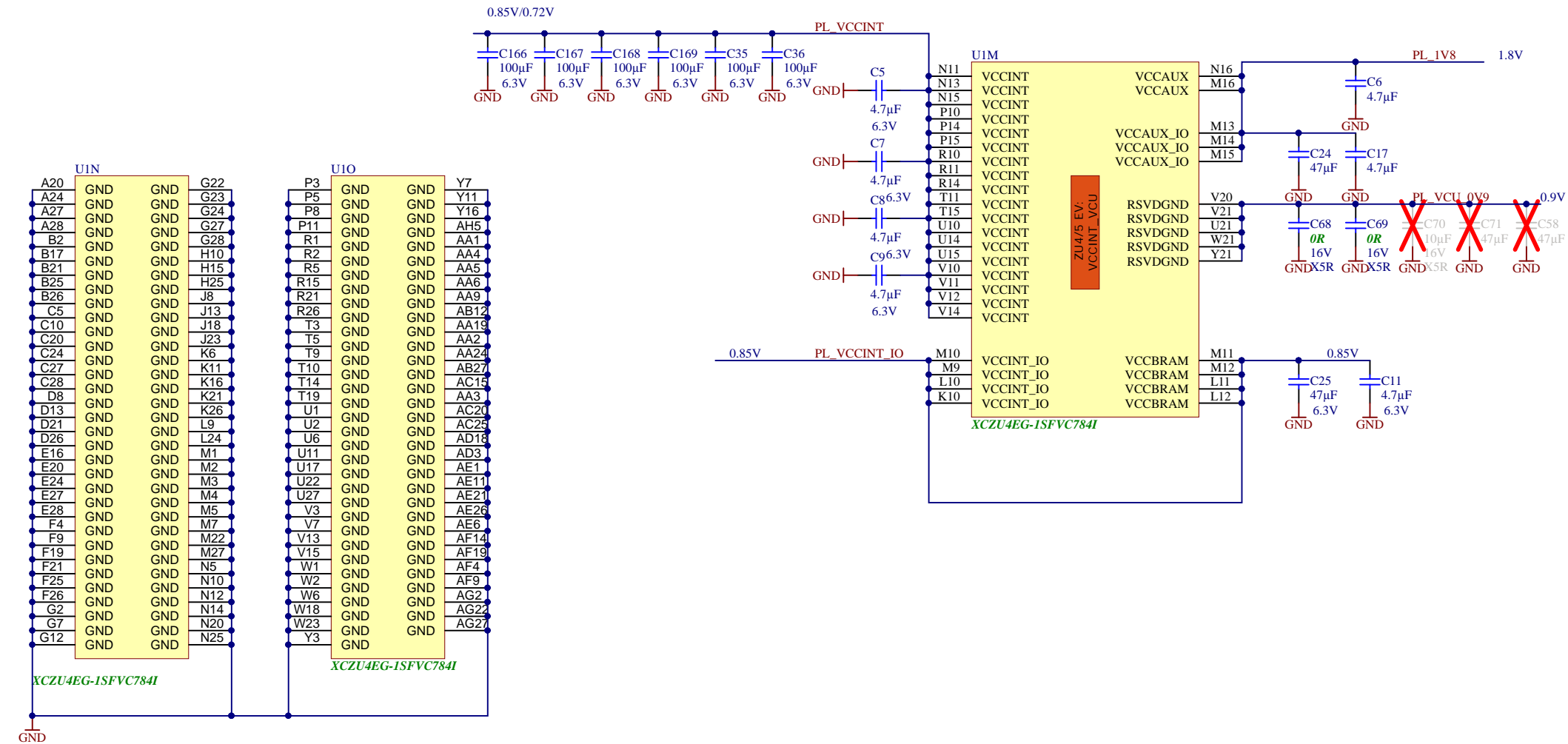
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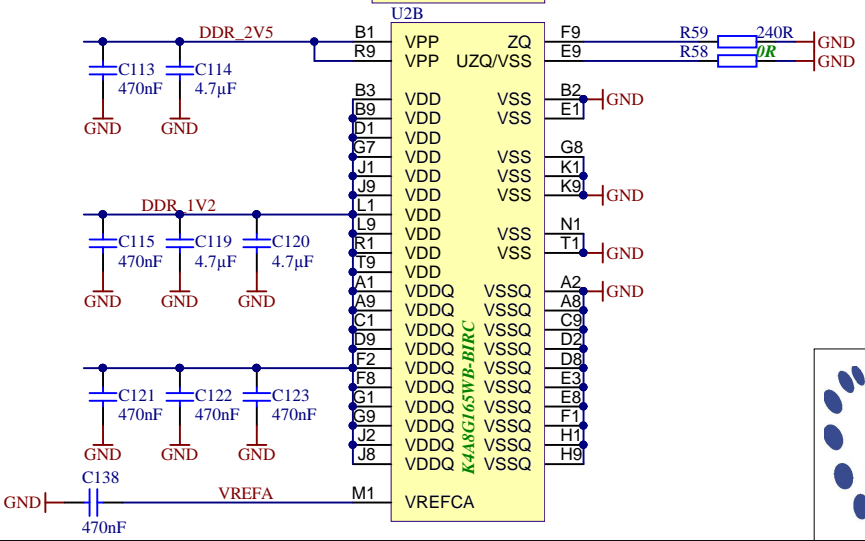
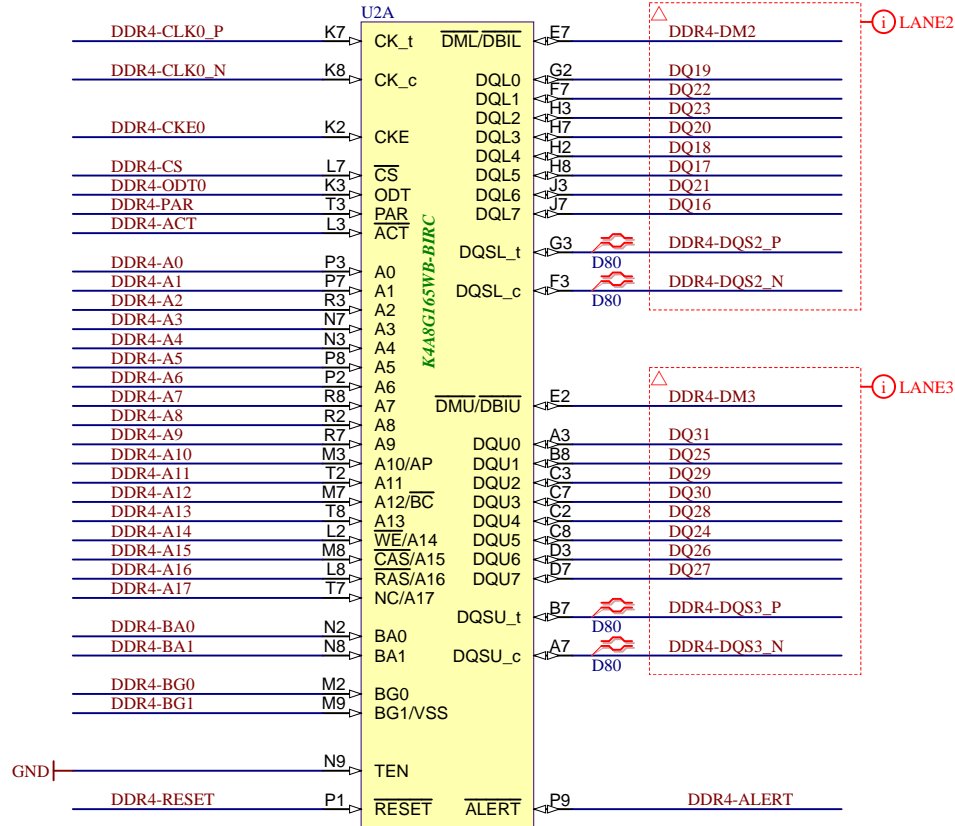
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	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 14 of 26
	Filename: B_GT.SchDoc		



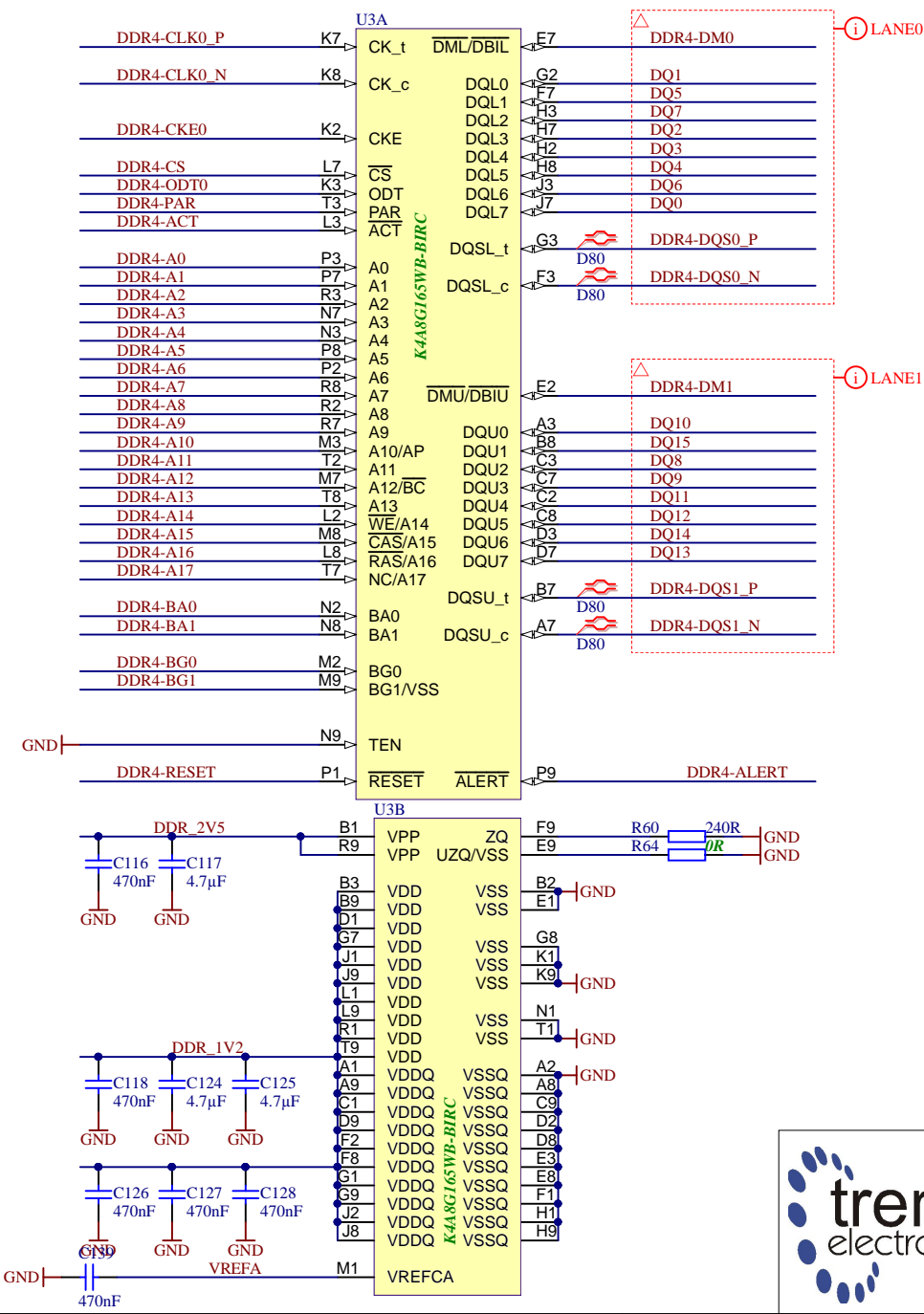

	Title: TE0803 - ZU_PS_POWER		
	A4	Number: TE0803 4BI21-X	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 15 of 26
	Filename: ZU_PS_POWER.SchDoc		



		Title: TE0803 - ZU_POWER	
		A4	Number: TE0803 4BI21-X
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: ZU_POWER.SchDoc		Page 16 of 26	



Title: TE0803 - DDR4_1_RAM		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 17 of 26
Filename: DDR4-RAM.SchDoc		

Title: TE0803 - DDR4_2_RAM		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 18 of 26
Filename: DDR4-RAM_2.SchDoc		

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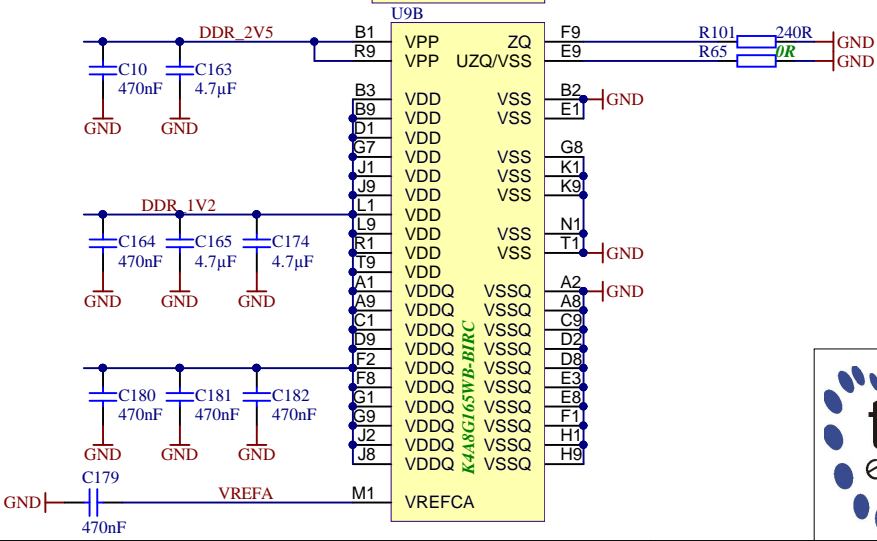
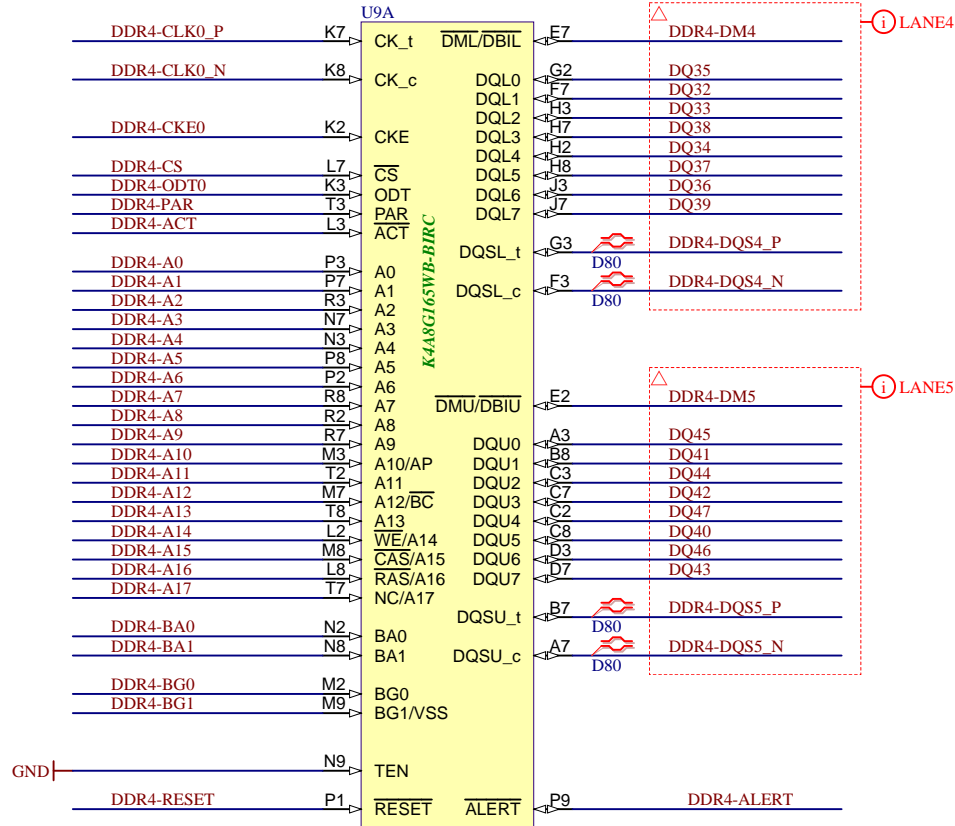

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Title: TE0803 - DDR4_3_RAM		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 19 of 26
Filename: DDR4-RAM_3.SchDoc		

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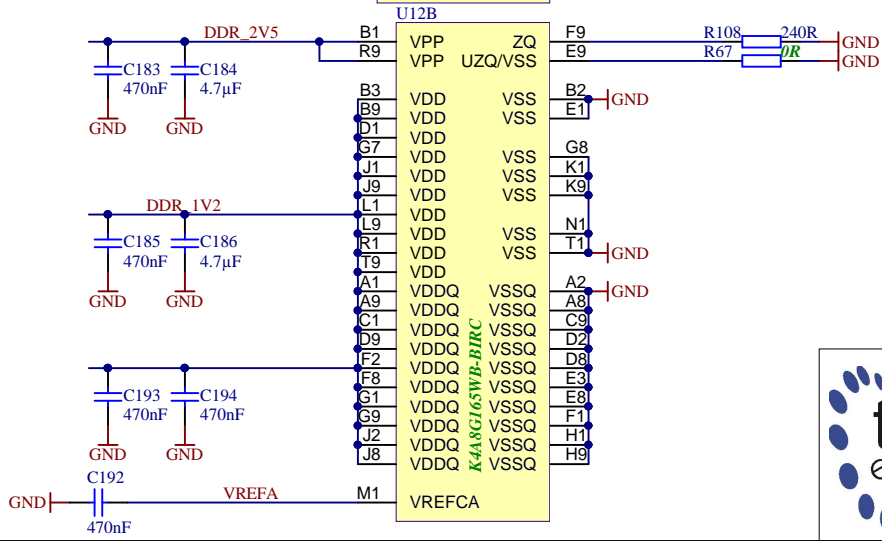
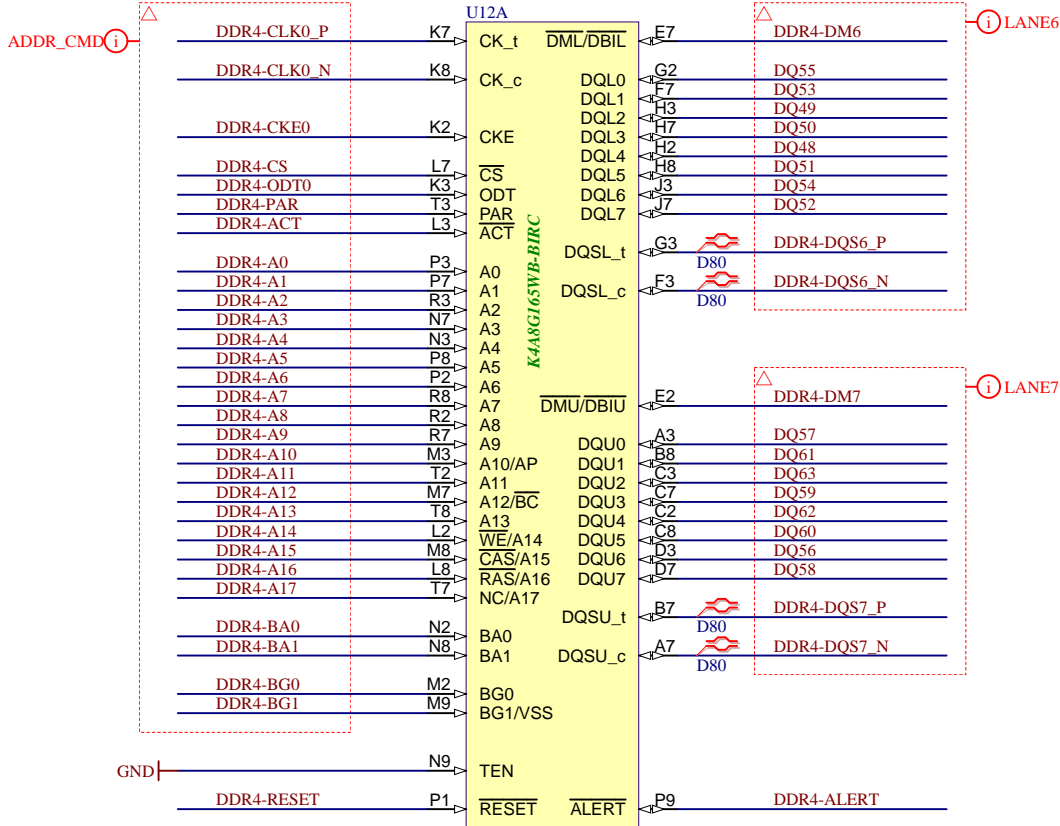
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C

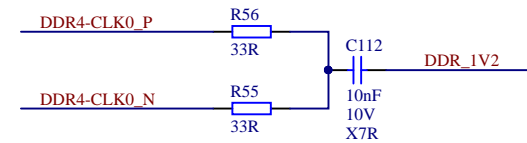
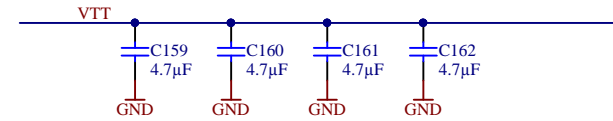
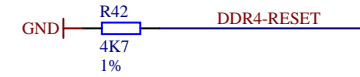
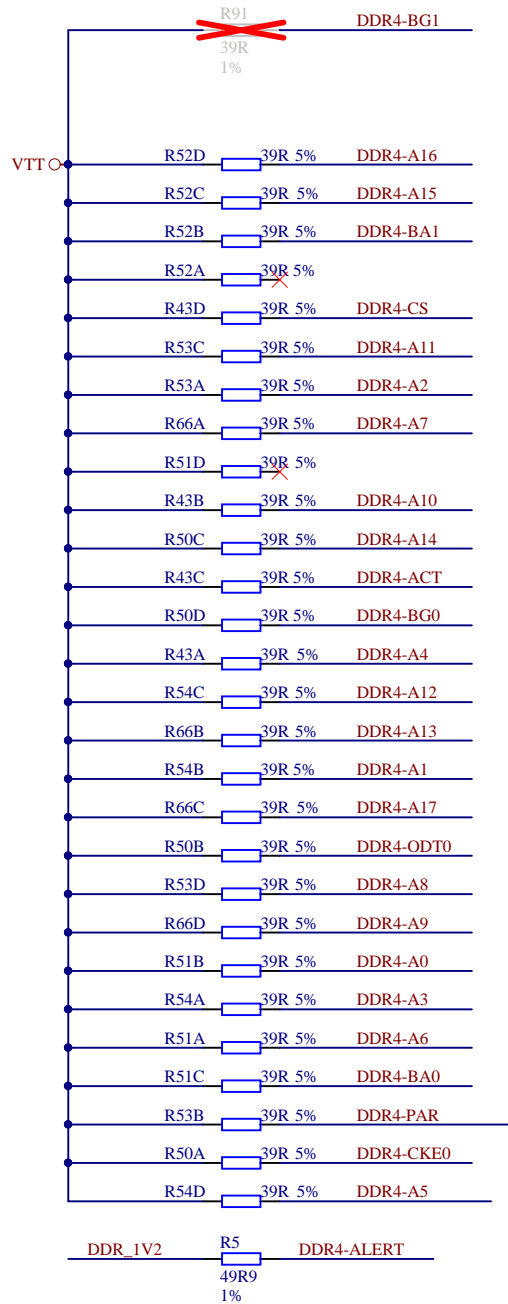
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D

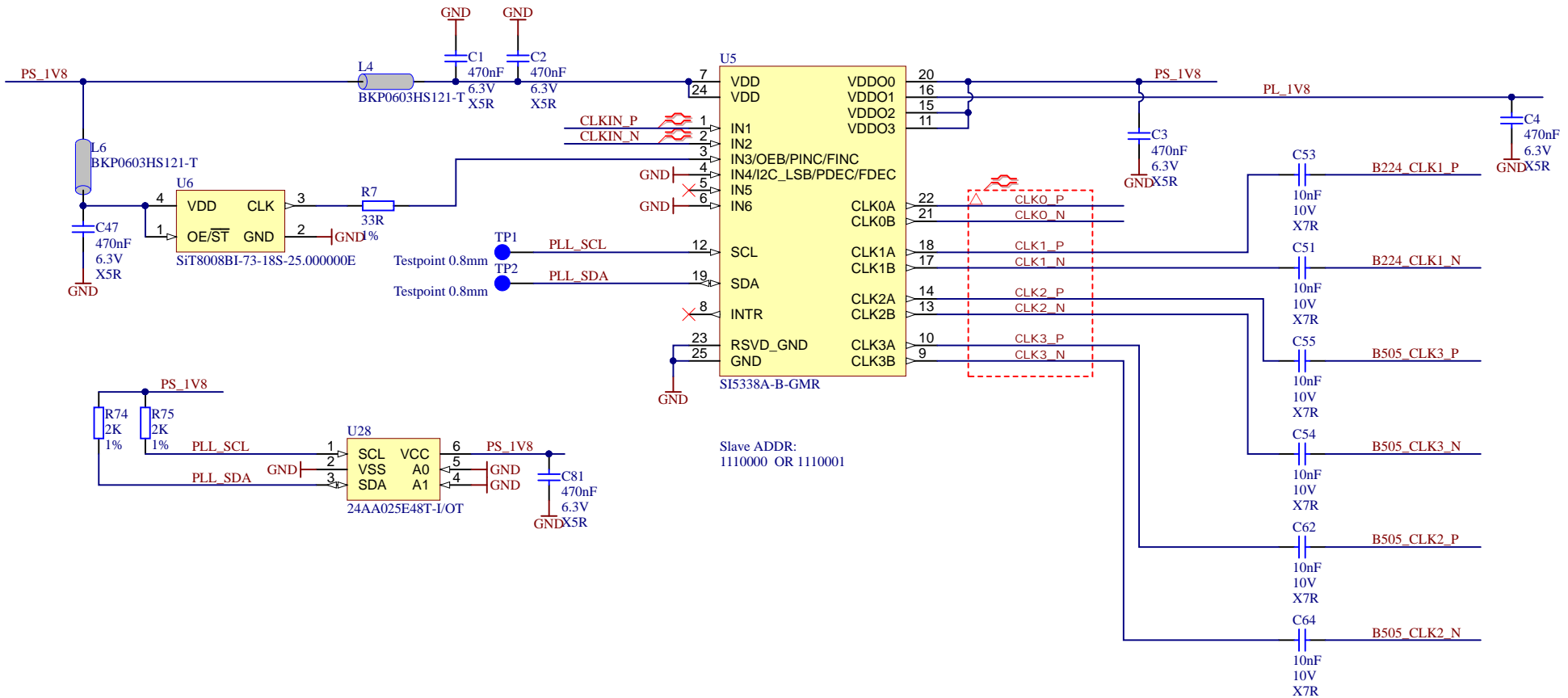
D




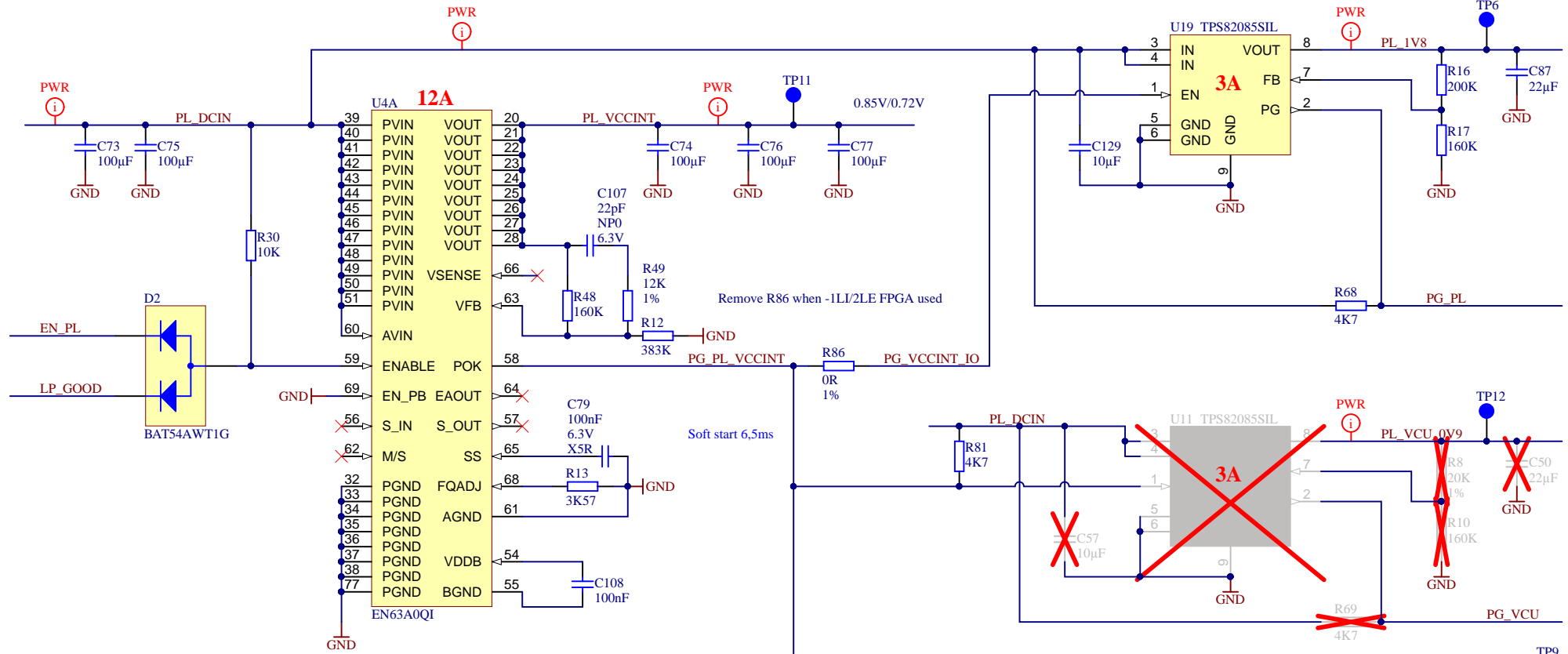
Title: TE0803 - DDR4_4_RAM		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page20 of 26
Filename: DDR4-RAM_4.SchDoc		



Title: TE0803 - DDR4_TERM		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 21 of 26
Filename: DDR4-TERM.SchDoc		



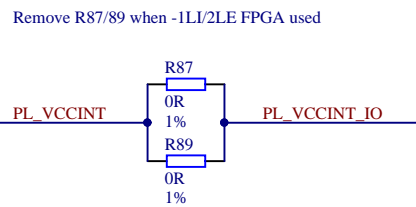
		Title: TE0803 - CLOCK	
		A4	Number: TE0803 4BI21-X
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: Clock.SchDoc		Page 22 of 26	



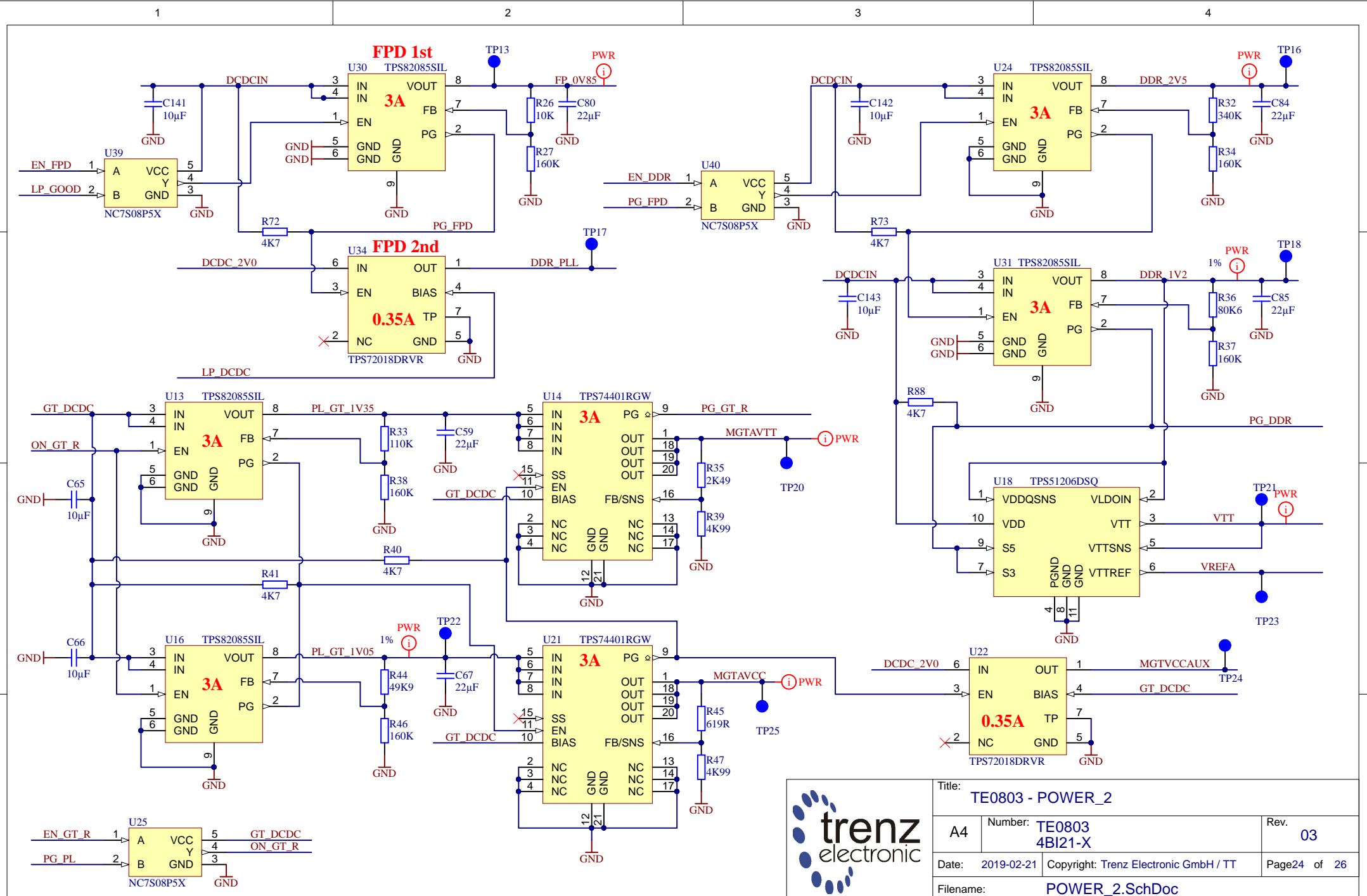
U4B

1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76

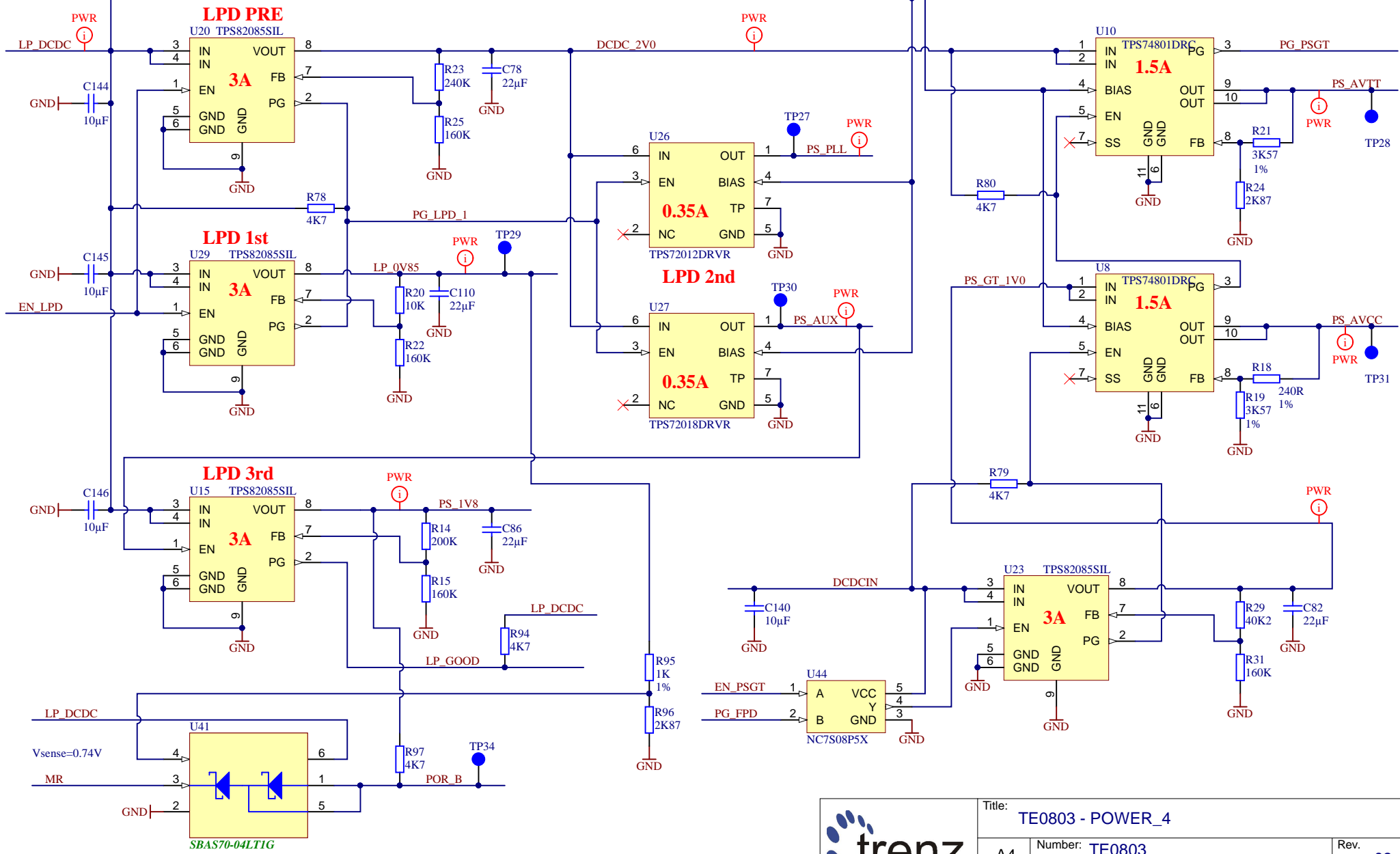
EN63A0QI



Title: TE0803 - POWER		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 23 of 26
Filename: POWER.SchDoc		



Title: TE0803 - POWER_2		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page24 of 26
Filename: POWER_2.SchDoc		



Title: TE0803 - POWER_4		
A4	Number: TE0803 4BI21-X	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 25 of 26
Filename: POWER_4.SchDoc		

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CHANGES REV01a (20.11.2017):

- 1) VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9.

CHANGES REV02 (20.06.2018):

- 1) Added LDO to DDR_PLL
- 2) All differential pairs wath length matched with tollerance 0.1mm (excluding package delays)
- 3) Added MAC EEPROM U28
- 4) VPS_MGTRAVCC set to 0.85V
- 5) Added pull-up resistors R68,R69

CHANGES REV03 (21.02.2019):

- 1) Added support of DDP DDR4
- 2) Added support of Low power FPGA (-L1/L2).
- 3) Revised testpoints
- 4) Revised J1-J4 connectors net label style

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	Title: TE0803 - Changes list		
	A4	Number: TE0803 4BI21-X	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH	Page 26 of 26
	Filename: Revision_Changes.SchDoc		

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