U_J1
J1.SchDoc

U_J2
J2.SchDoc

U_J3
J3.SchDoc

U_J4
J4.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

U_B64
B64.SchDoc

U_B65
B65.SchDoc

U_B66
B66.SchDoc

U_B_GT
B_GT.SchDoc

U_B_PS_GT
B_PS_GT.SchDoc

U_PS_DDR
PS_DDR.SchDoc

U_B_MIO
B_MIO.SchDoc

U_B_HD
B_HD.SchDoc

U_Clock
Clock.SchDoc

U_CONFIG
CONFIG.SchDoc

U_DDR4-RAM
DDR4-RAM.SchDoc

U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

U_DDR4-RAM_3
DDR4-RAM_3.SchDoc

U_DDR4-RAM_4
DDR4-RAM_4.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

U_ZU_POWER
ZU_POWER.SchDoc

U_ZU_PS_POWER
ZU_PS_POWER.SchDoc

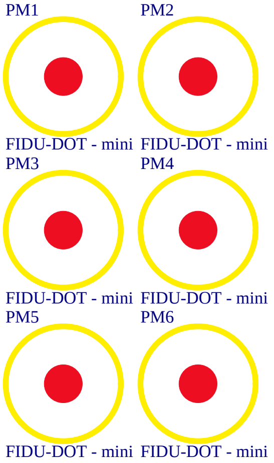
U_POWER
POWER.SchDoc

U_POWER_2
POWER_2.SchDoc

U_POWER_4
POWER_4.SchDoc

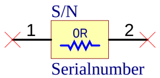
U_REV_CH
Revision_Changes.SchDoc

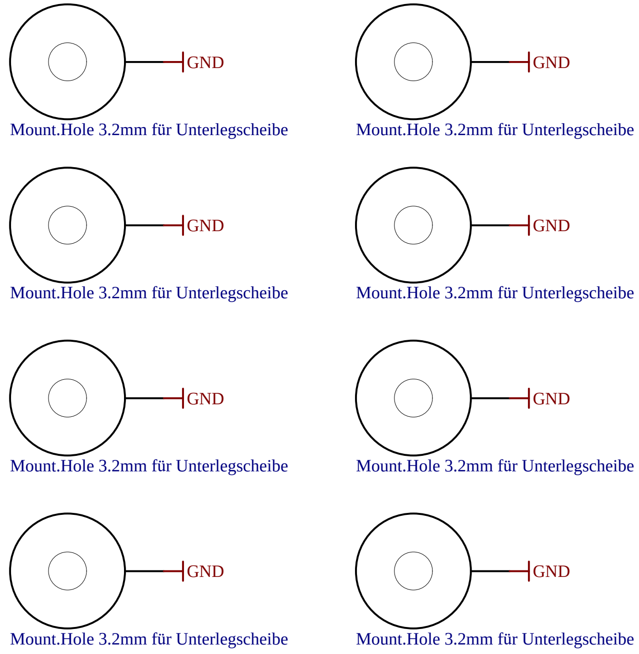
Special notes:



LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial
Serial
Serialnumber 6,3 x 6.3mm





Assembly variant	4DI21-L
Created by	VY
Modified by	VY
Modified at	2020-04-03
SVN Revision	9128 [Locally Modified]

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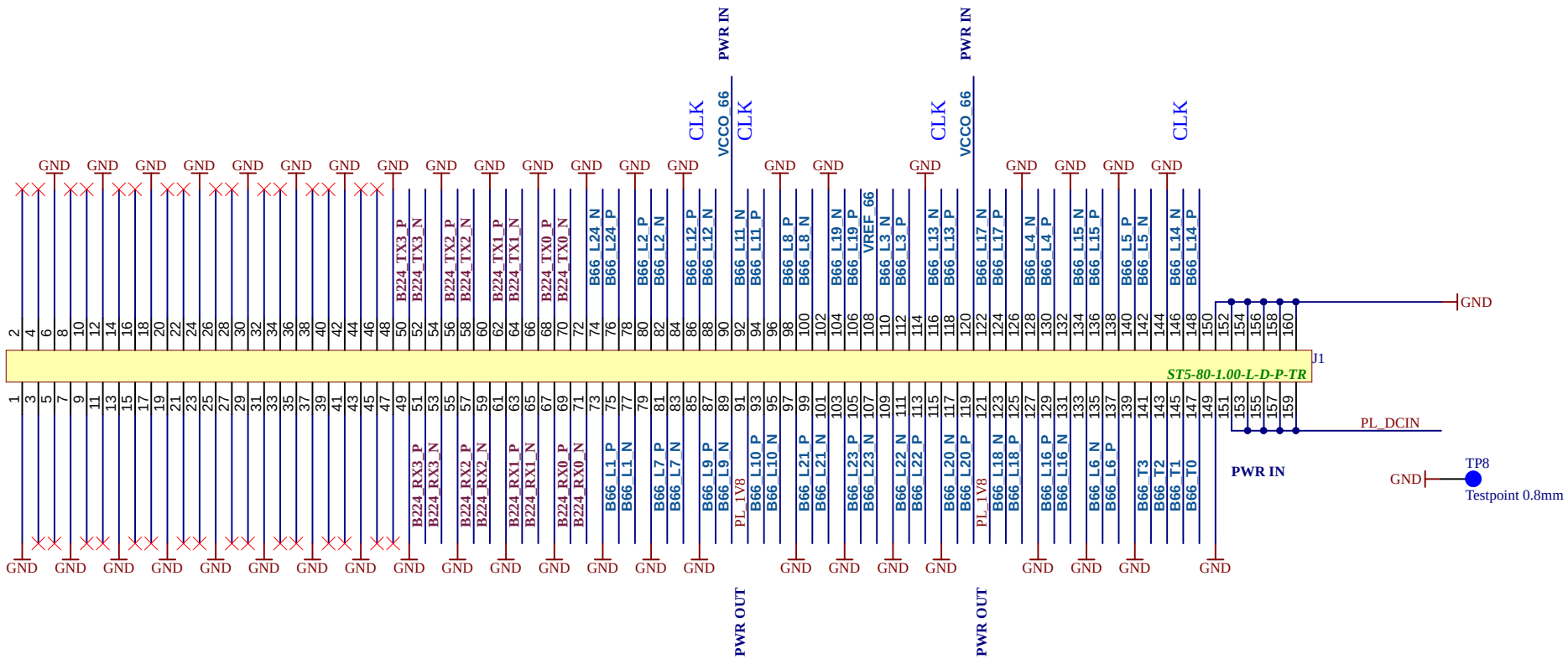
Title: TE0803			
A4	Number: TE0803 4DI21-L		Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page1 of 26
Filename: TE0803.SchDoc			



trenz electronic	Title: TE0803 - Connector J1		
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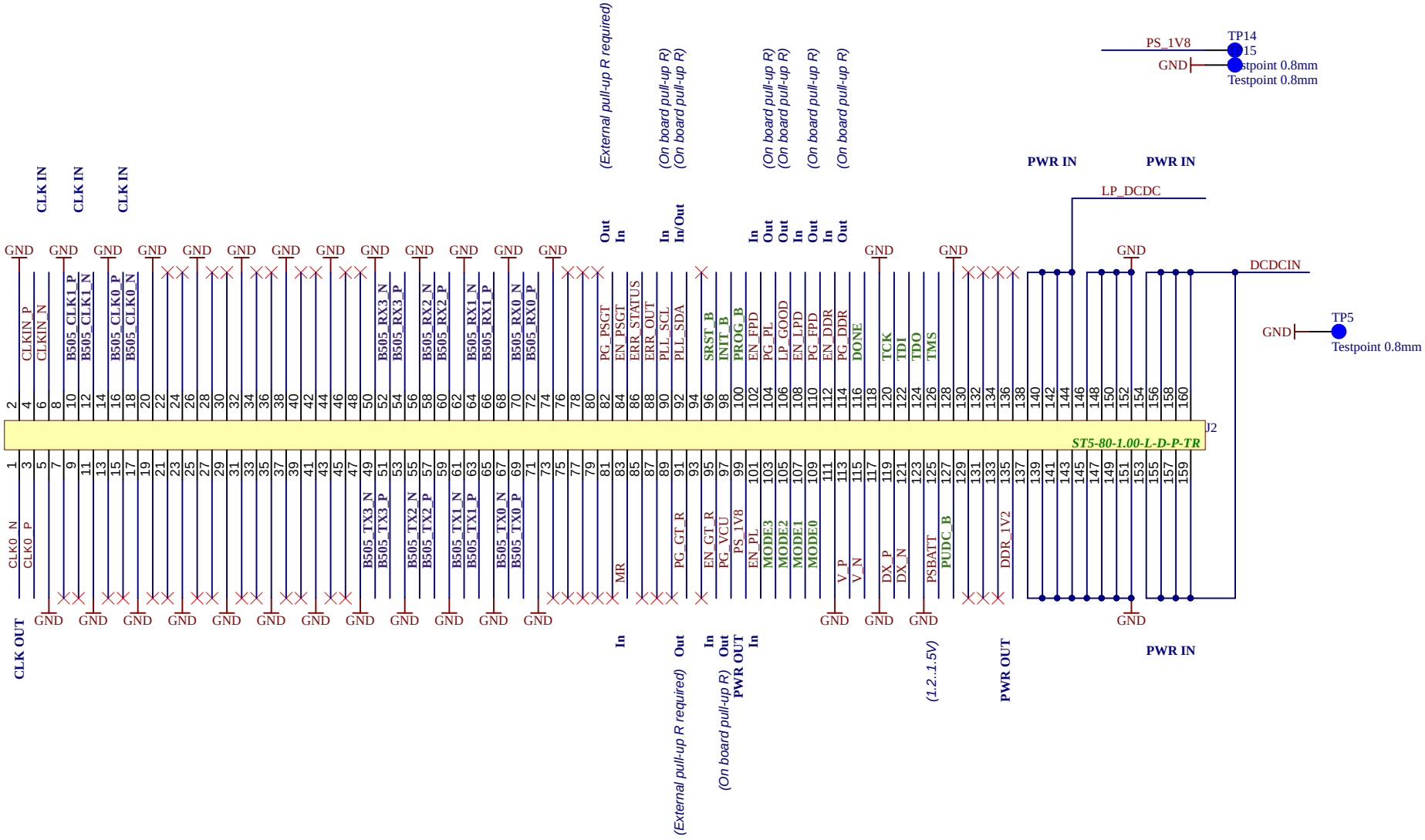
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page2 of 26
Filename: J1.SchDoc			



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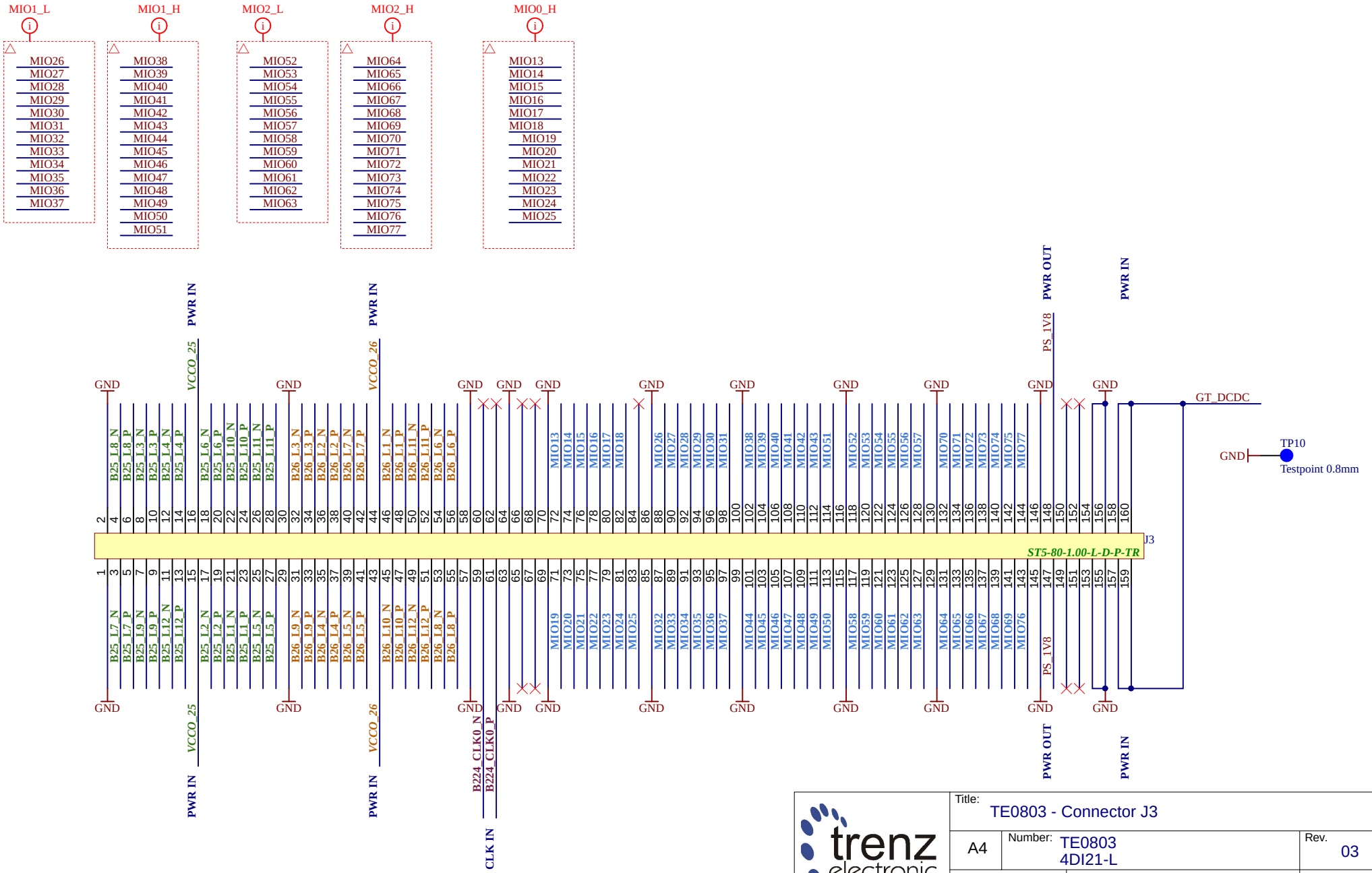
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page3 of 26
Filename: J2.SchDoc			



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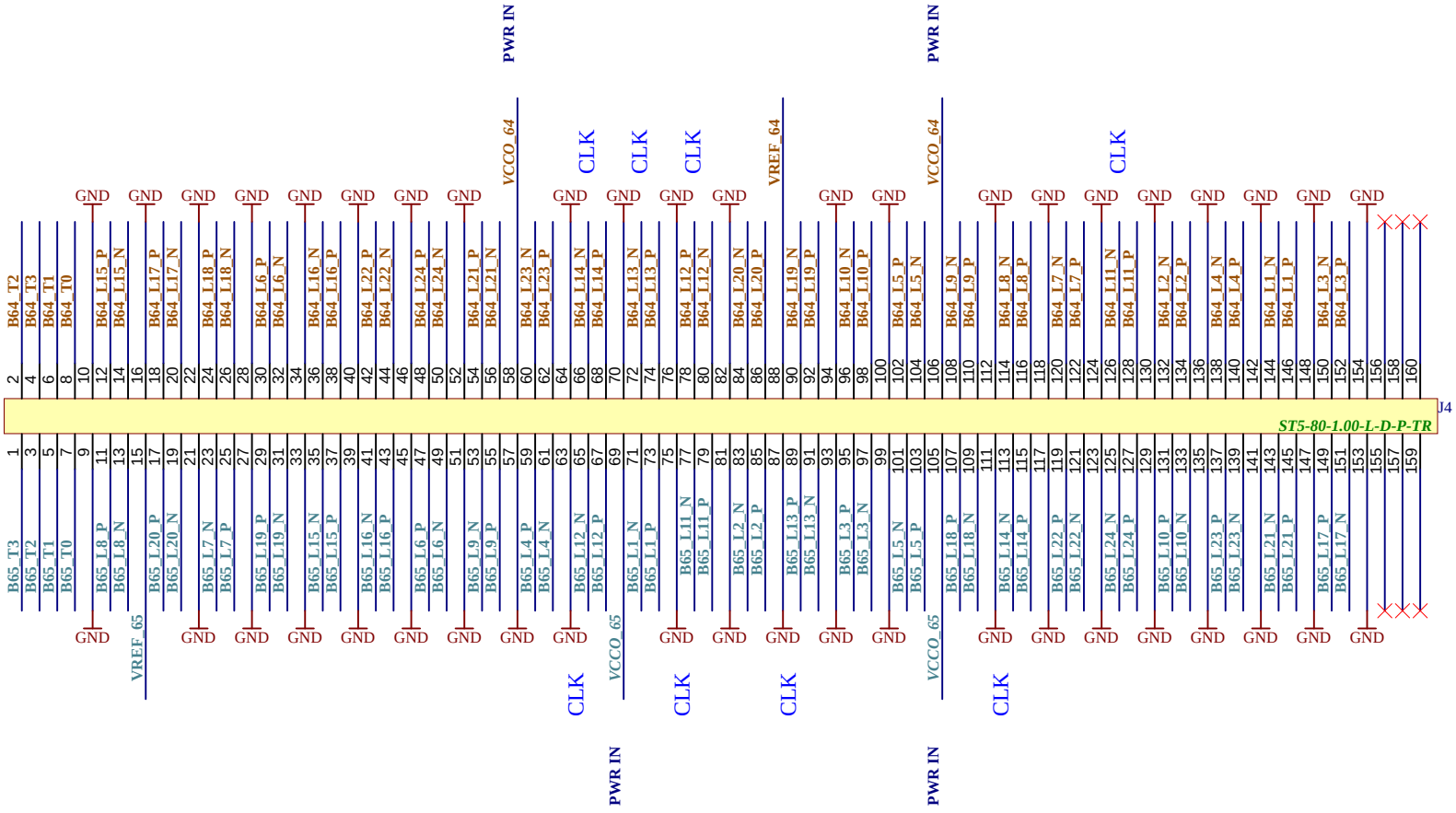
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page4 of 26
Filename: J3.SchDoc			



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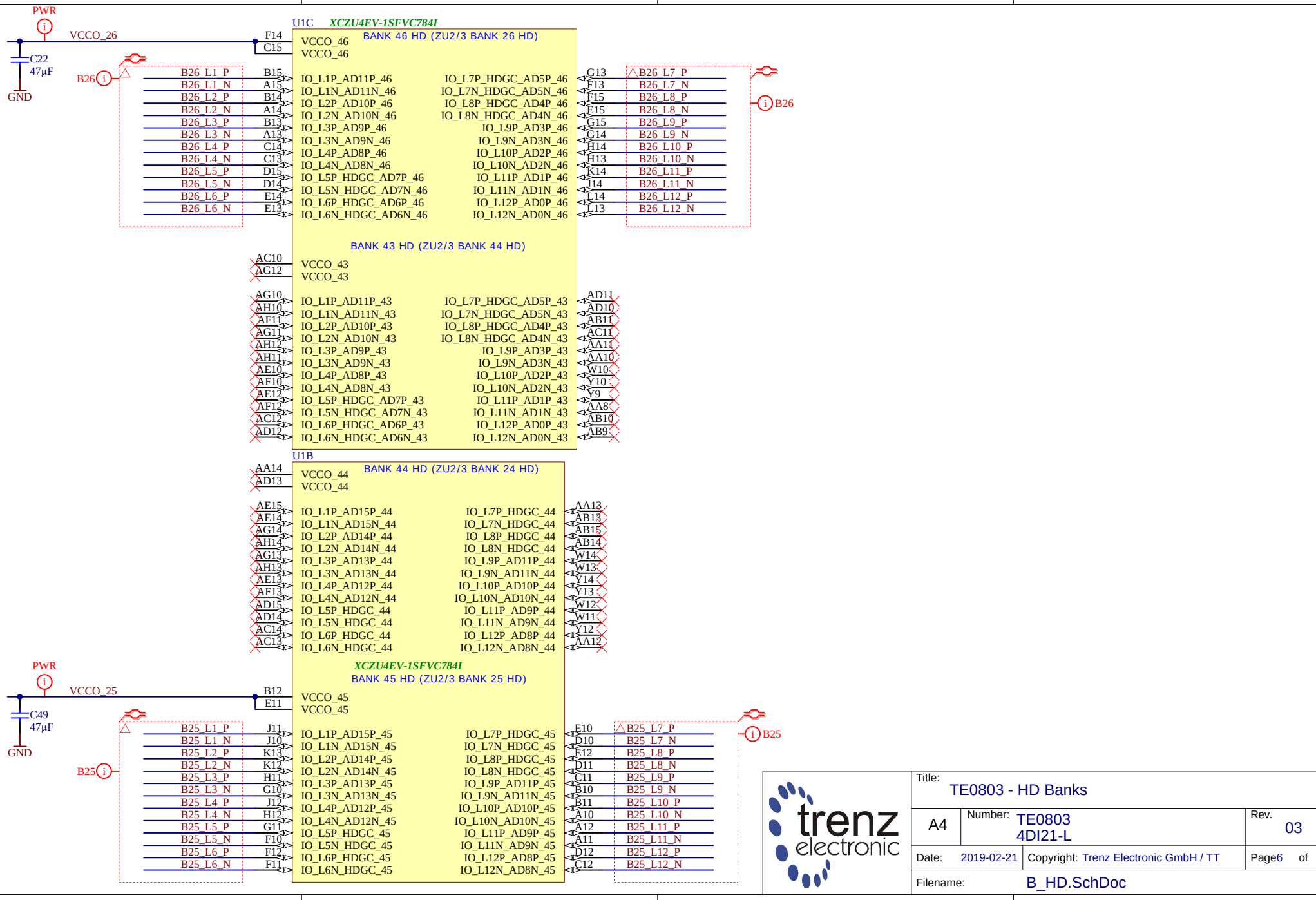
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page5 of 26
Filename: J4.SchDoc			


PWR
VCCO_26
C22
47µF
GND
U1C
XCZU4EV-1SFVC784I
BANK 46 HD (ZU2/3 BANK 26 HD)
VCCO_46
VCCO_46
IO_L1P_AD11P_46
IO_L1N_AD11N_46
IO_L2P_AD10P_46
IO_L2N_AD10N_46
IO_L3P_AD9P_46
IO_L3N_AD9N_46
IO_L4P_AD8P_46
IO_L4N_AD8N_46
IO_L5P_HDGC_AD7P_46
IO_L5N_HDGC_AD7N_46
IO_L6P_HDGC_AD6P_46
IO_L6N_HDGC_AD6N_46
IO_L7P_HDGC_AD5P_46
IO_L7N_HDGC_AD5N_46
IO_L8P_HDGC_AD4P_46
IO_L8N_HDGC_AD4N_46
IO_L9P_AD3P_46
IO_L9N_AD3N_46
IO_L10P_AD2P_46
IO_L10N_AD2N_46
IO_L11P_AD1P_46
IO_L11N_AD1N_46
IO_L12P_AD0P_46
IO_L12N_AD0N_46
B26_L1_P
B26_L1_N
B26_L2_P
B26_L2_N
B26_L3_P
B26_L3_N
B26_L4_P
B26_L4_N
B26_L5_P
B26_L5_N
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B26_L6_N
B26_L7_P
B26_L7_N
B26_L8_P
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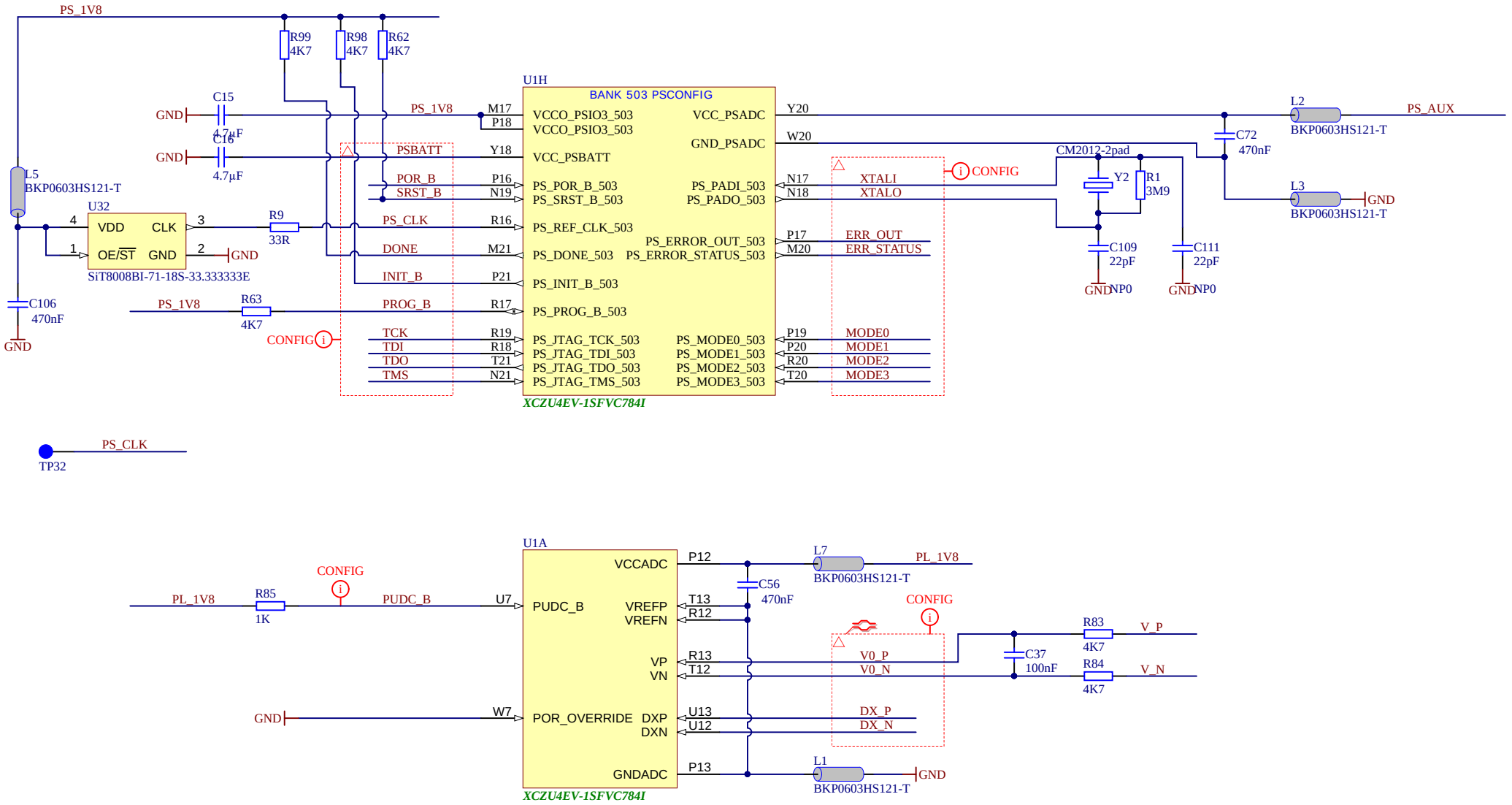
B26_L9_P
B26_L9_N
B26_L10_P
B26_L10_N
B26_L11_P
B26_L11_N
B26_L12_P
B26_L12_N
B26
BANK 43 HD (ZU2/3 BANK 44 HD)
VCCO_43
VCCO_43
IO_L1P_AD11P_43
IO_L1N_AD11N_43
IO_L2P_AD10P_43
IO_L2N_AD10N_43
IO_L3P_AD9P_43
IO_L3N_AD9N_43
IO_L4P_AD8P_43
IO_L4N_AD8N_43
IO_L5P_HDGC_AD7P_43
IO_L5N_HDGC_AD7N_43
IO_L6P_HDGC_AD6P_43
IO_L6N_HDGC_AD6N_43
IO_L7P_HDGC_AD5P_43
IO_L7N_HDGC_AD5N_43
IO_L8P_HDGC_AD4P_43
IO_L8N_HDGC_AD4N_43
IO_L9P_AD3P_43
IO_L9N_AD3N_43
IO_L10P_AD2P_43
IO_L10N_AD2N_43
IO_L11P_AD1P_43
IO_L11N_AD1N_43
IO_L12P_AD0P_43
IO_L12N_AD0N_43
U1B
BANK 44 HD (ZU2/3 BANK 24 HD)
VCCO_44
VCCO_44
IO_L1P_AD15P_44
IO_L1N_AD15N_44
IO_L2P_AD14P_44
IO_L2N_AD14N_44
IO_L3P_AD13P_44
IO_L3N_AD13N_44
IO_L4P_AD12P_44
IO_L4N_AD12N_44
IO_L5P_HDGC_44
IO_L5N_HDGC_44
IO_L6P_HDGC_44
IO_L6N_HDGC_44
IO_L7P_HDGC_44
IO_L7N_HDGC_44
IO_L8P_HDGC_44
IO_L8N_HDGC_44
IO_L9P_AD11P_44
IO_L9N_AD11N_44
IO_L10P_AD10P_44
IO_L10N_AD10N_44
IO_L11P_AD9P_44
IO_L11N_AD9N_44
IO_L12P_AD8P_44
IO_L12N_AD8N_44
XCZU4EV-1SFVC784I
BANK 45 HD (ZU2/3 BANK 25 HD)
VCCO_45
VCCO_45
IO_L1P_AD15P_45
IO_L1N_AD15N_45
IO_L2P_AD14P_45
IO_L2N_AD14N_45
IO_L3P_AD13P_45
IO_L3N_AD13N_45
IO_L4P_AD12P_45
IO_L4N_AD12N_45
IO_L5P_HDGC_45
IO_L5N_HDGC_45
IO_L6P_HDGC_45
IO_L6N_HDGC_45
IO_L7P_HDGC_45
IO_L7N_HDGC_45
IO_L8P_HDGC_45
IO_L8N_HDGC_45
IO_L9P_AD11P_45
IO_L9N_AD11N_45
IO_L10P_AD10P_45
IO_L10N_AD10N_45
IO_L11P_AD9P_45
IO_L11N_AD9N_45
IO_L12P_AD8P_45
IO_L12N_AD8N_45
B25_L1_P
B25_L1_N
B25_L2_P
B25_L2_N
B25_L3_P
B25_L3_N
B25_L4_P
B25_L4_N
B25_L5_P
B25_L5_N
B25_L6_P
B25_L6_N
B25_L7_P
B25_L7_N
B25_L8_P
B25_L8_N
B25_L9_P
B25_L9_N
B25_L10_P
B25_L10_N
B25_L11_P
B25_L11_N
B25_L12_P
B25_L12_N
B25
PWR
VCCO_25
C49
47µF
GND
trenz electronic
Title: TE0803 - HD Banks
A4
Number: TE0803 4DI21-L
Rev. 03
Date: 2019-02-21
Copyright: Trenz Electronic GmbH / TT
Page6 of 26
Filename: B_HD.SchDoc



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Title: TE0803 - Config			
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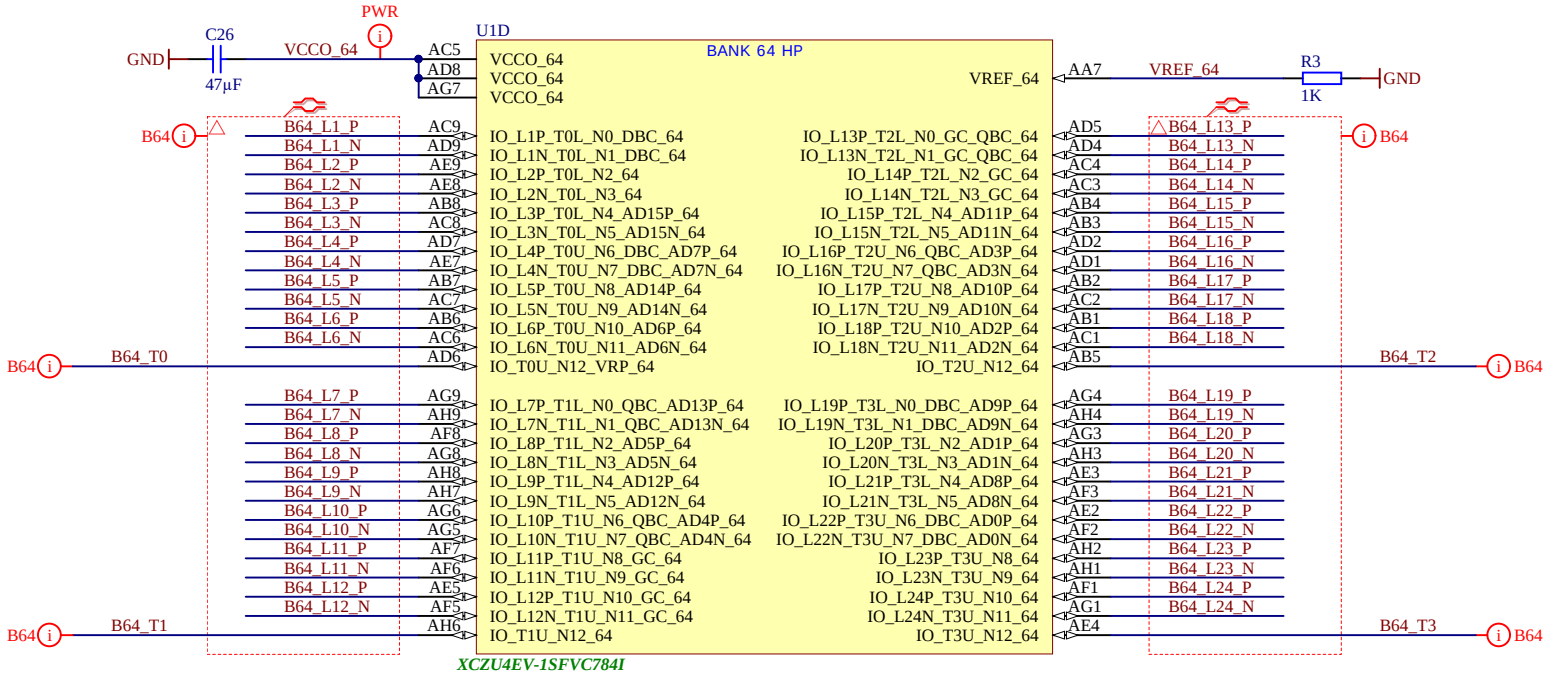
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page7 of 26
Filename: CONFIG.SchDoc			



trenz electronic	Title: TE0803 - B64		
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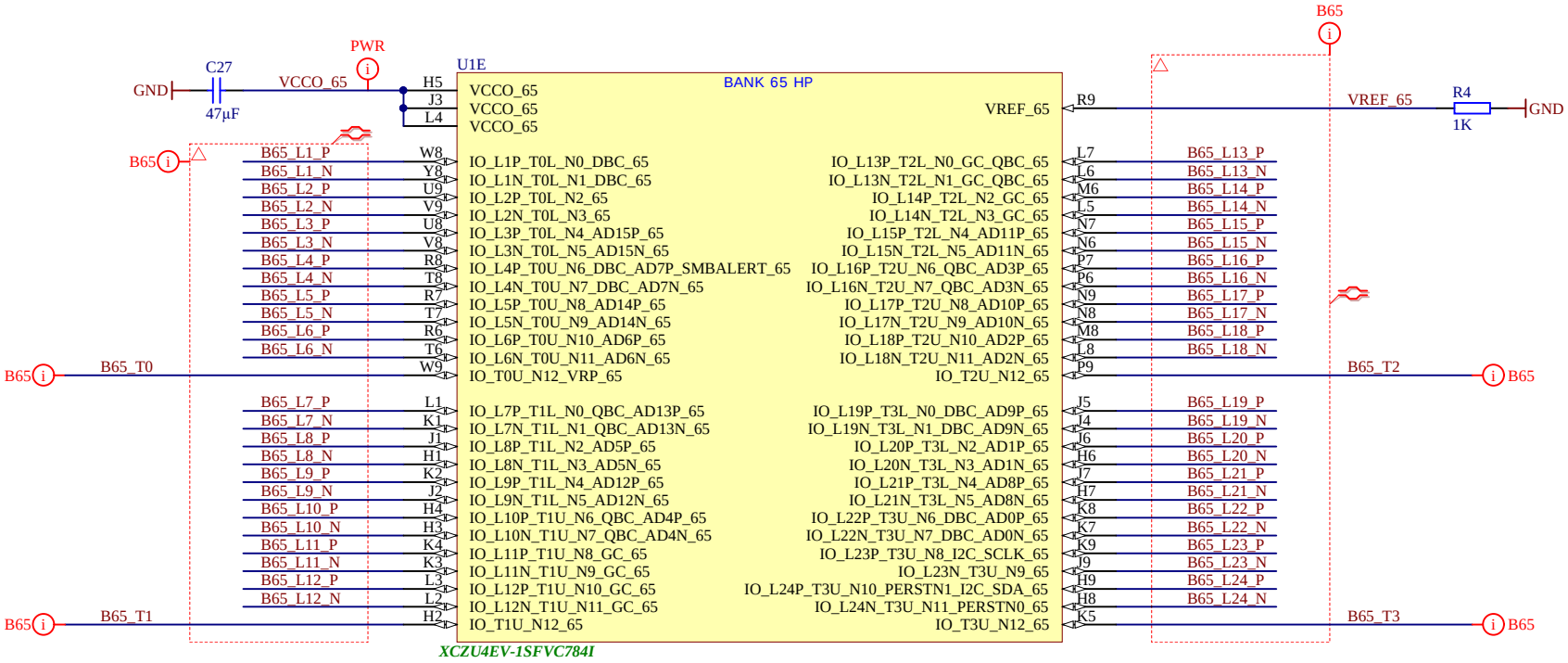
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page8 of 26
Filename: B64.SchDoc			



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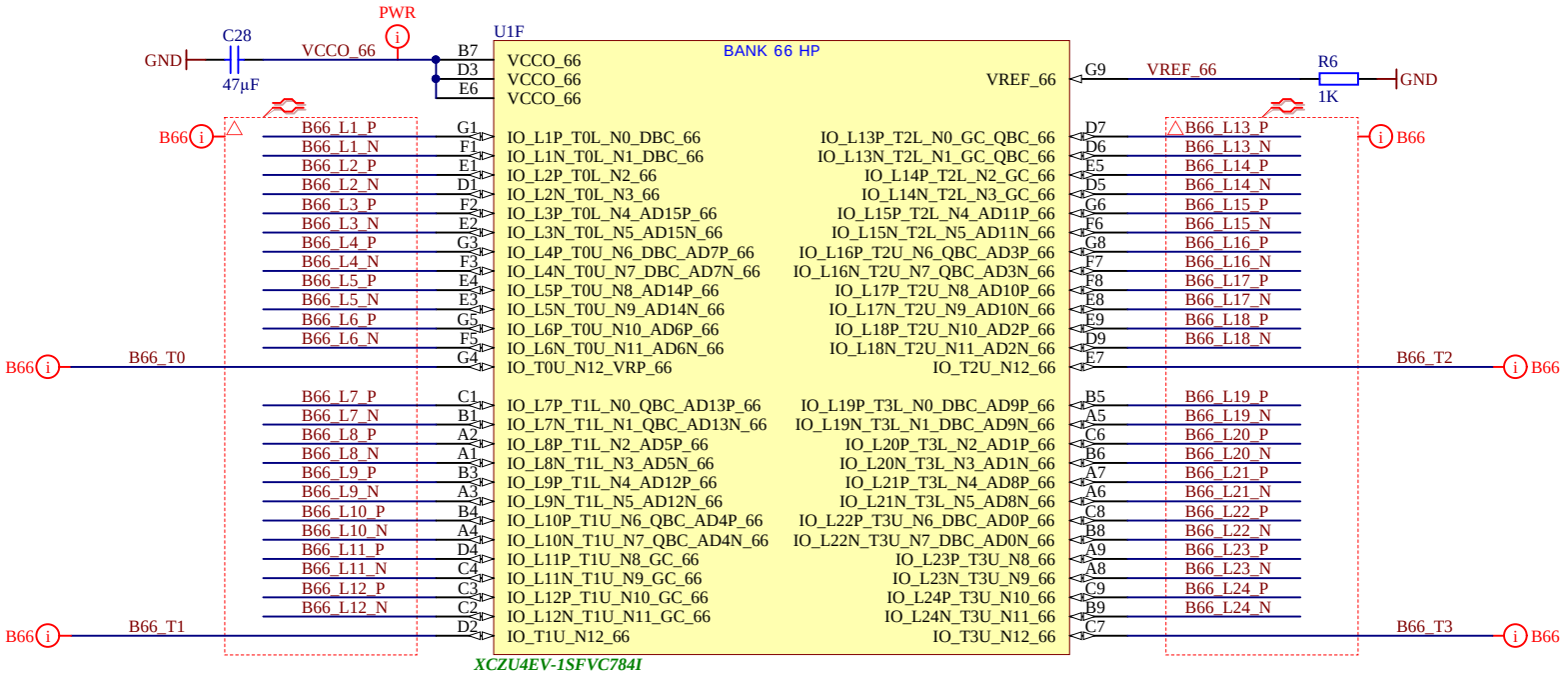
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page9 of 26
Filename: B65.SchDoc			



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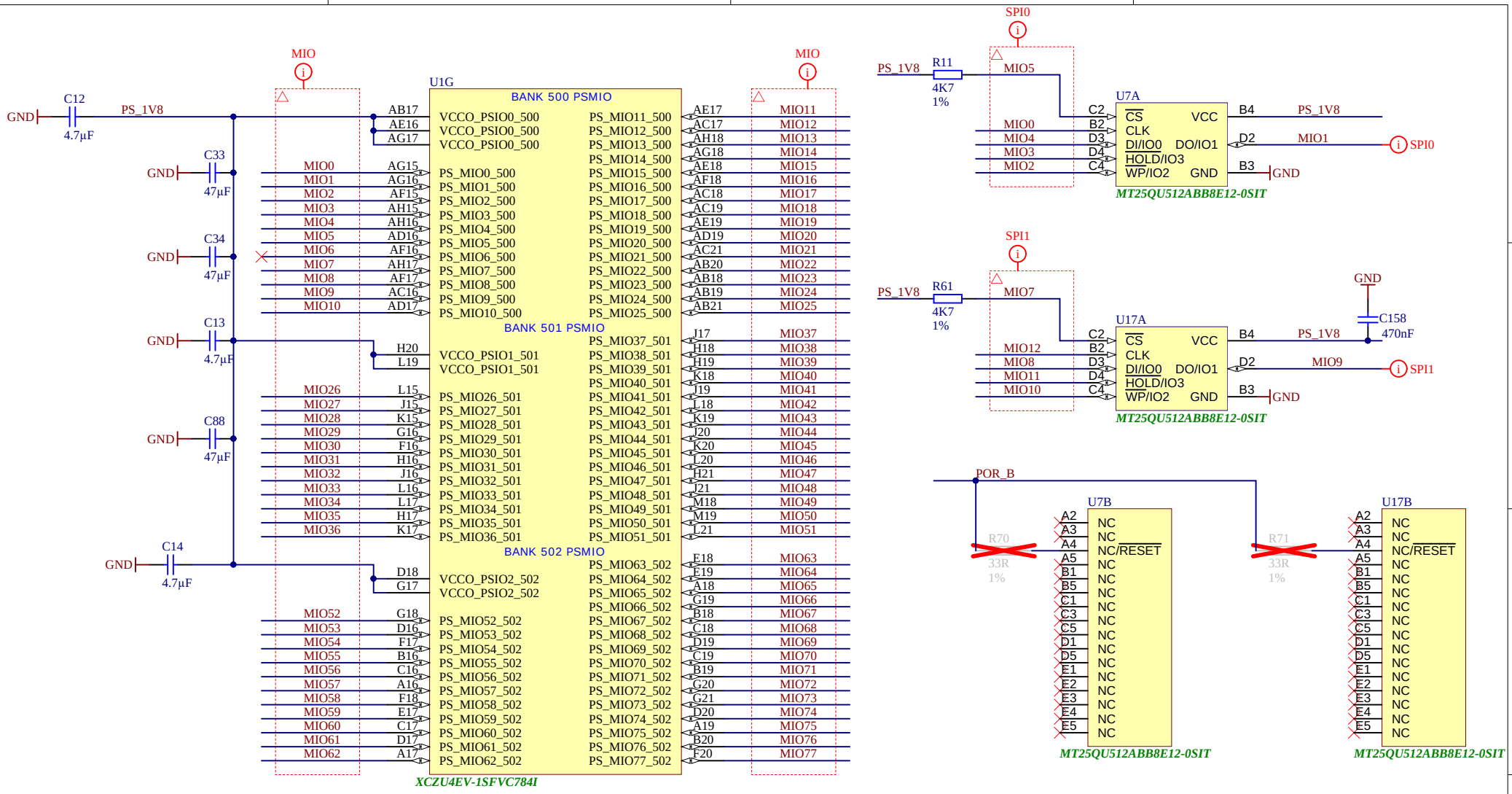
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page10 of 26
Filename: B66.SchDoc			



Title: TE0803 - MIO Banks			
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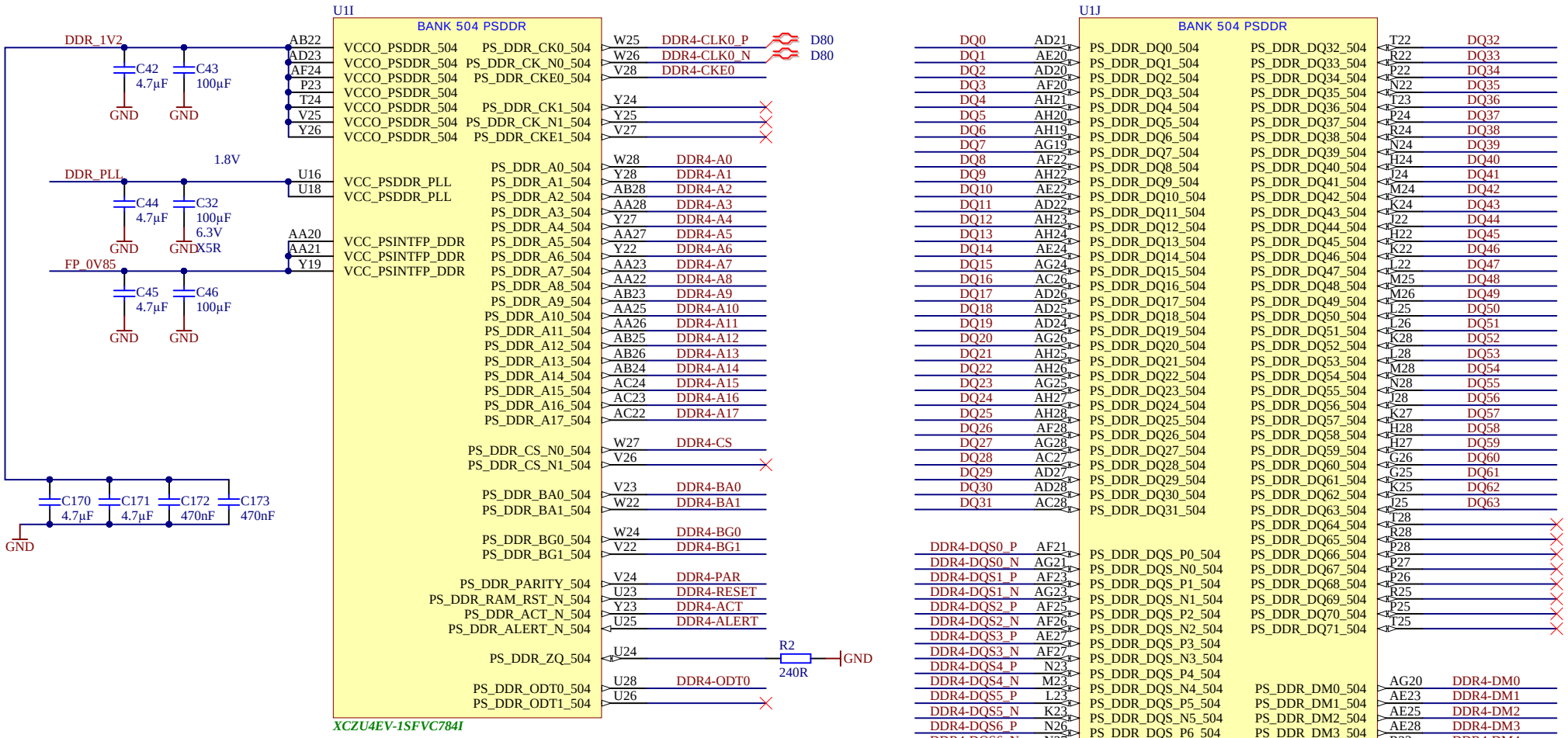
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page11 of 26
Filename: B_MIO.SchDoc			



trenz electronic	Title: TE0803 - PS_DDR		
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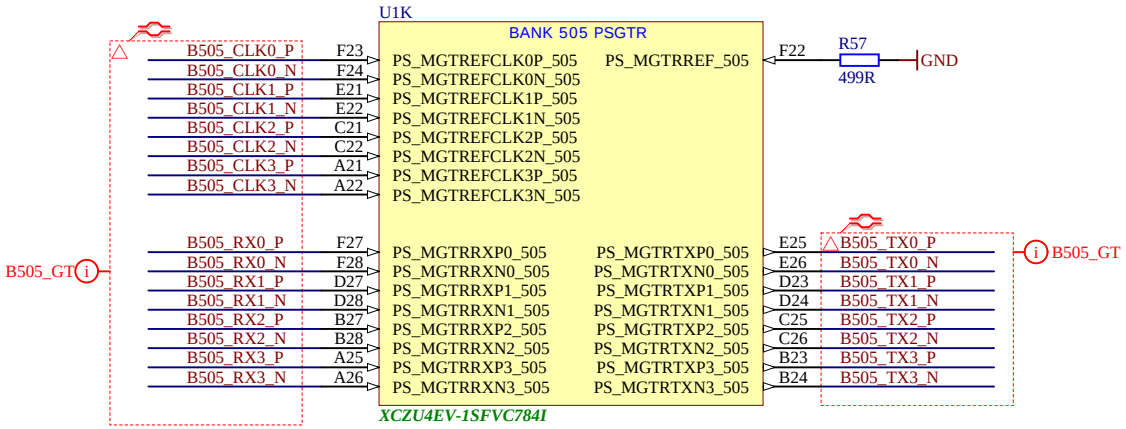
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page12 of 26
Filename: PS_DDR.SchDoc			



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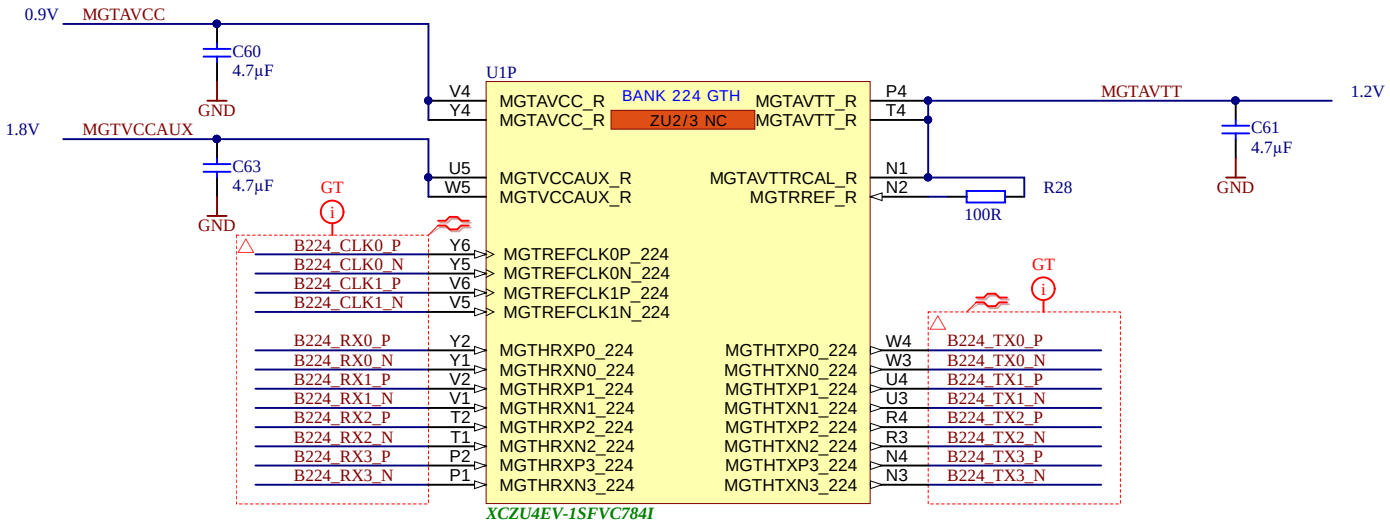
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page13 of 26
Filename: B_PS_GT.SchDoc			



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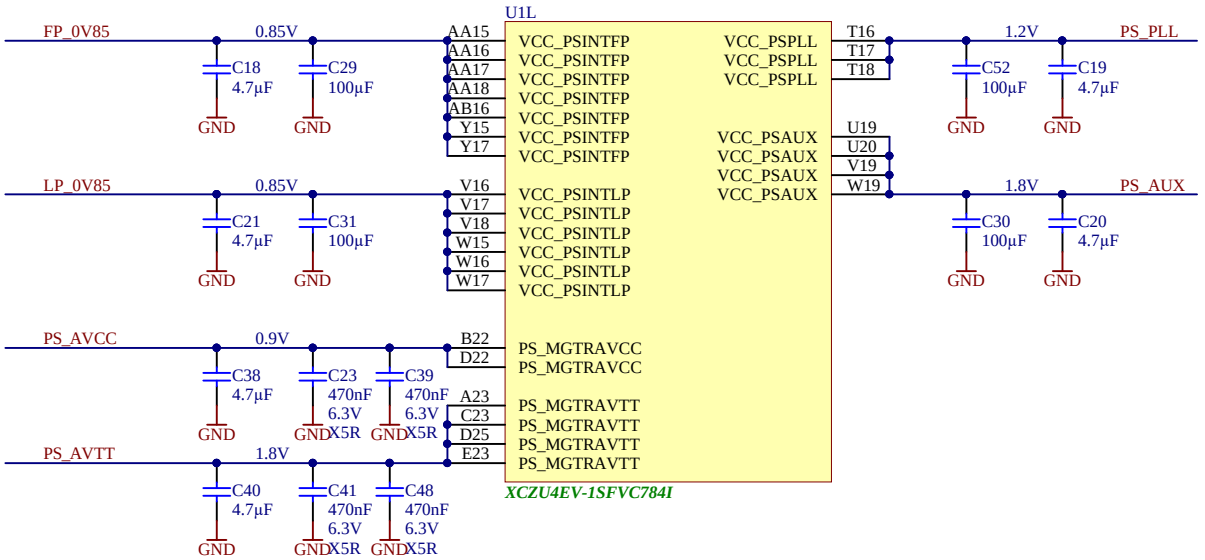
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page14 of 26
Filename: B_GT.SchDoc			



trenz electronic	Title: TE0803 - ZU_PS_POWER		
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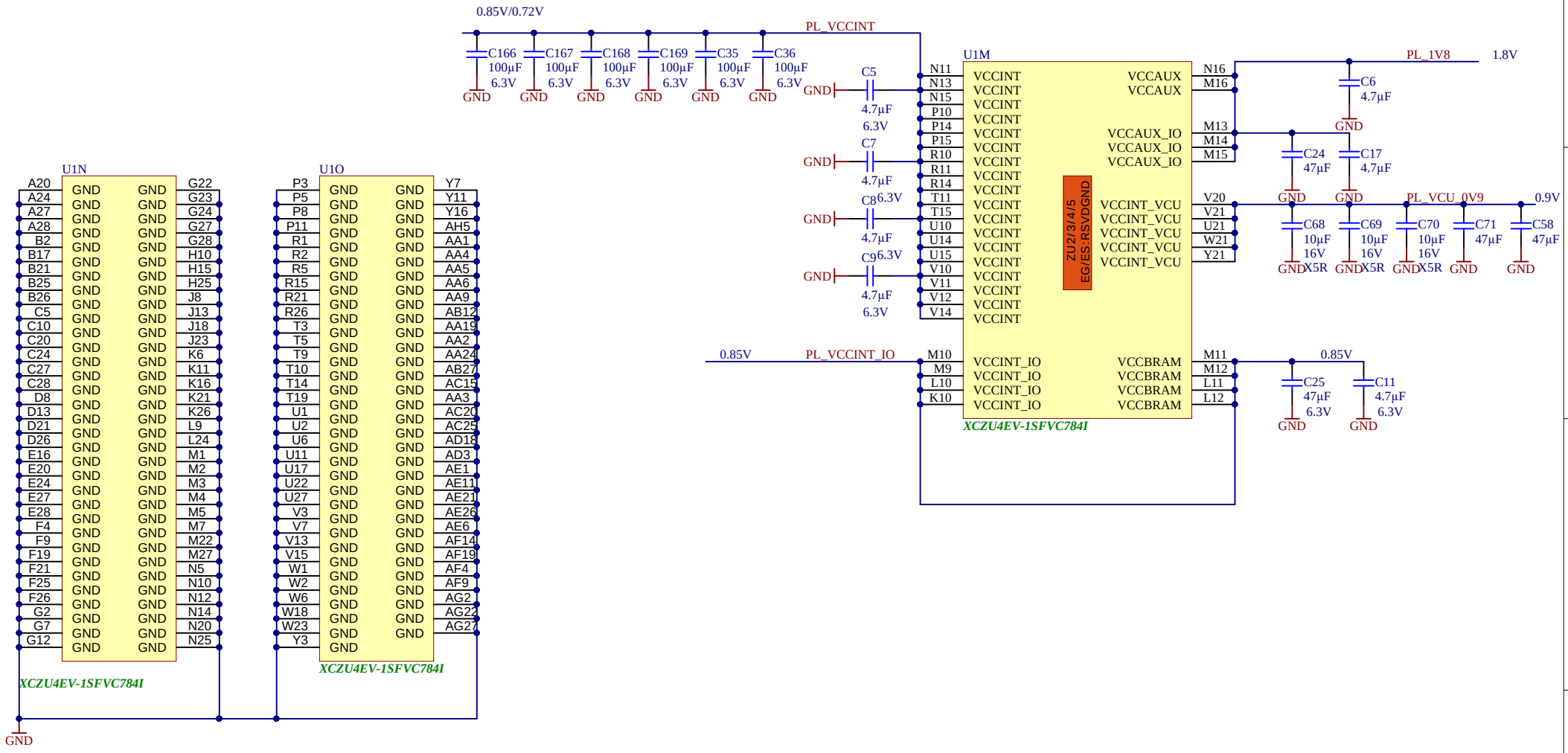
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page15 of 26
Filename: ZU_PS_POWER.SchDoc			



Title: TE0803 - ZU_POWER			
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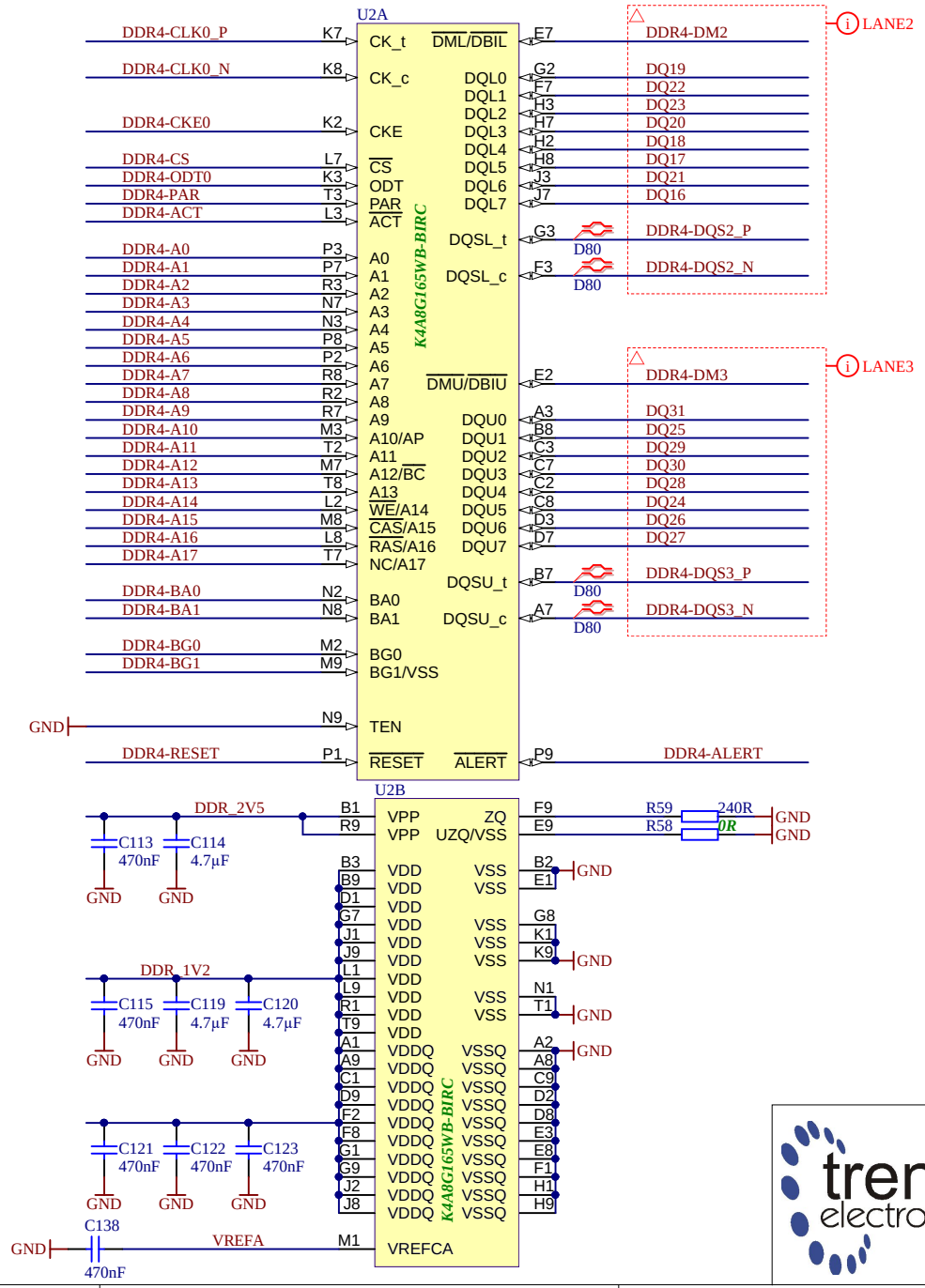
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page16 of 26
Filename: ZU_POWER.SchDoc			



Title: TE0803 - DDR4_1_RAM			
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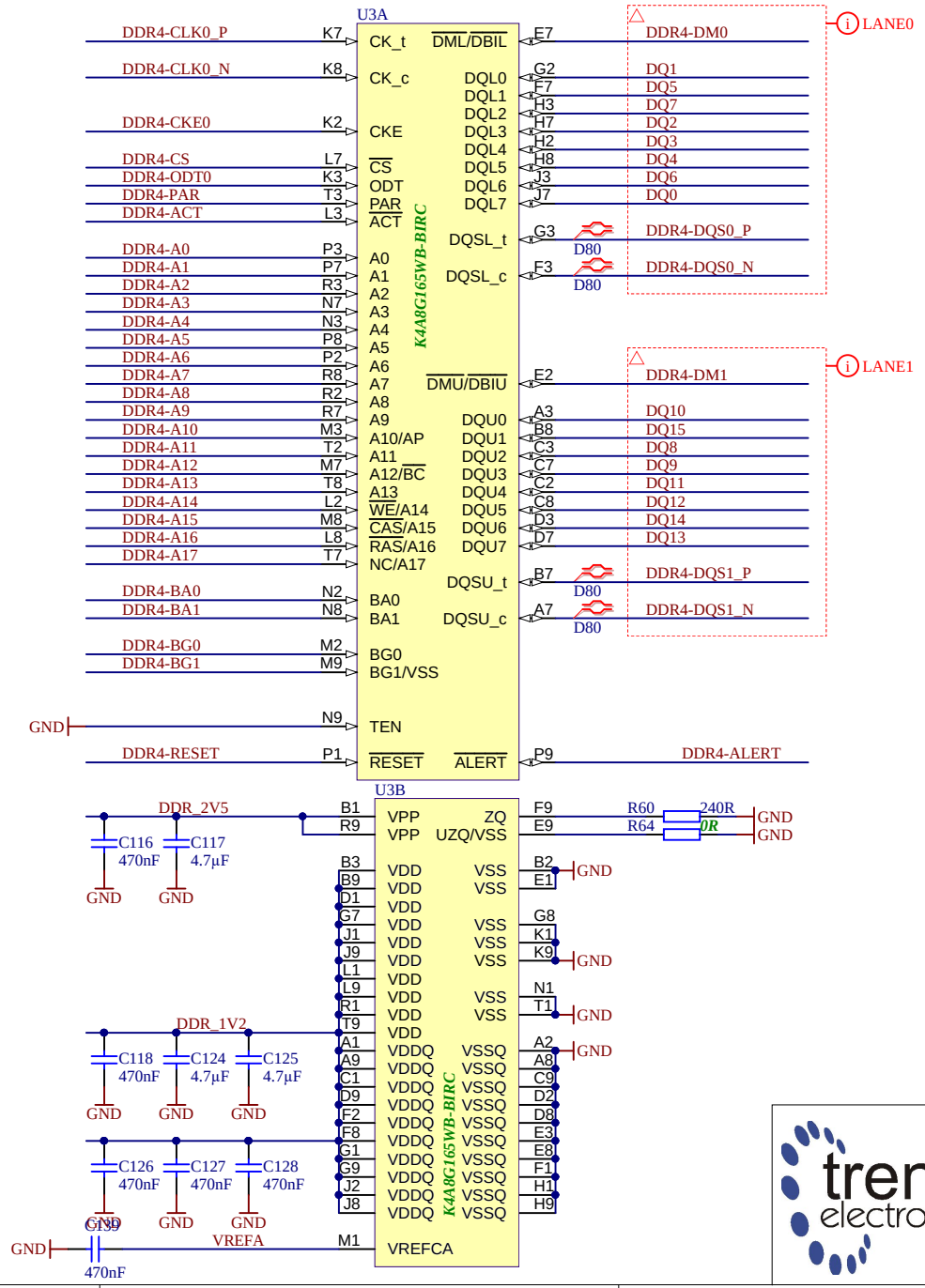
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page17 of 26
Filename: DDR4-RAM.SchDoc			



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Title: TE0803 - DDR4_2_RAM			
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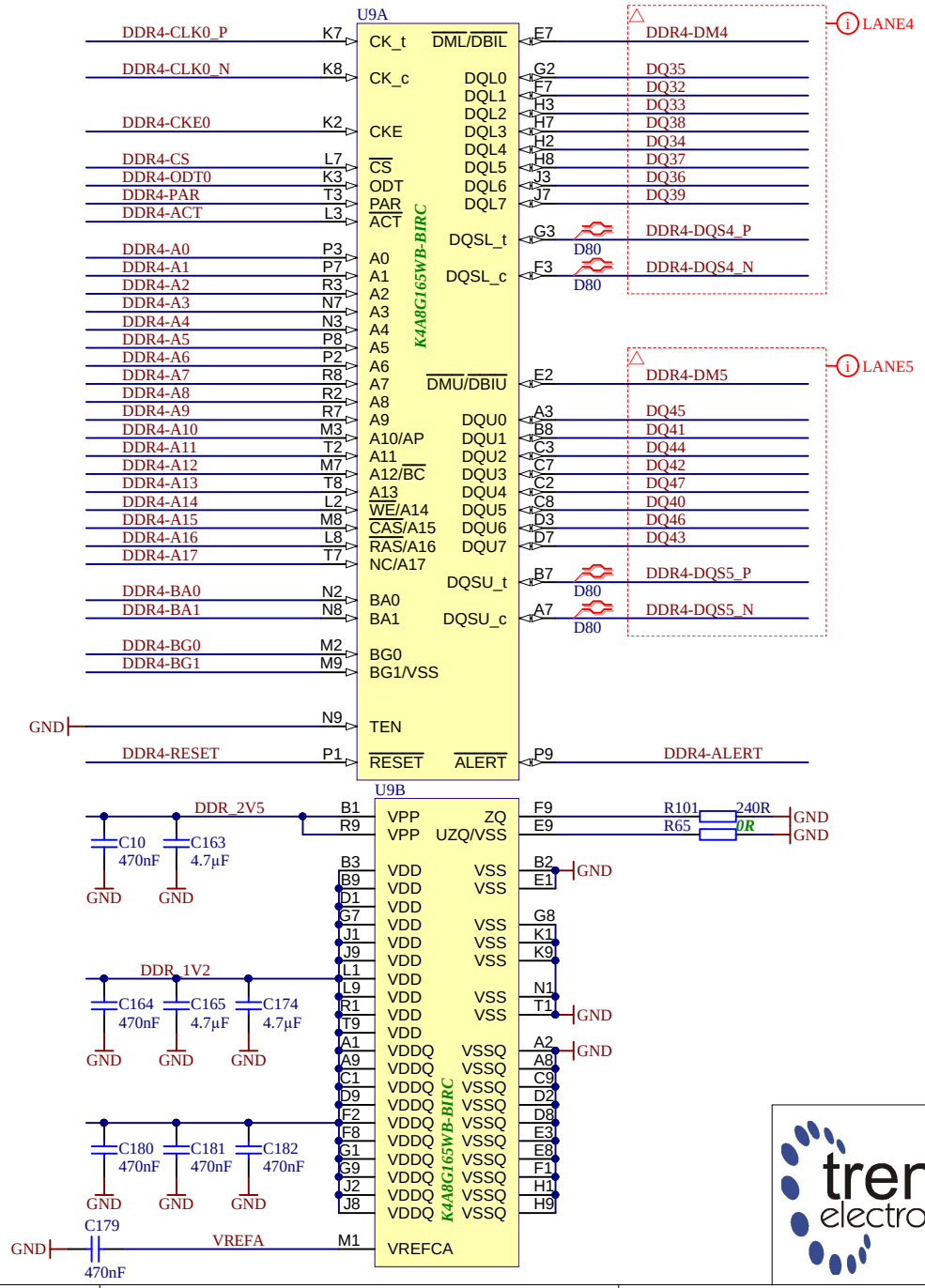
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page18 of 26
Filename: DDR4-RAM_2.SchDoc			



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Title: TE0803 - DDR4_3_RAM			
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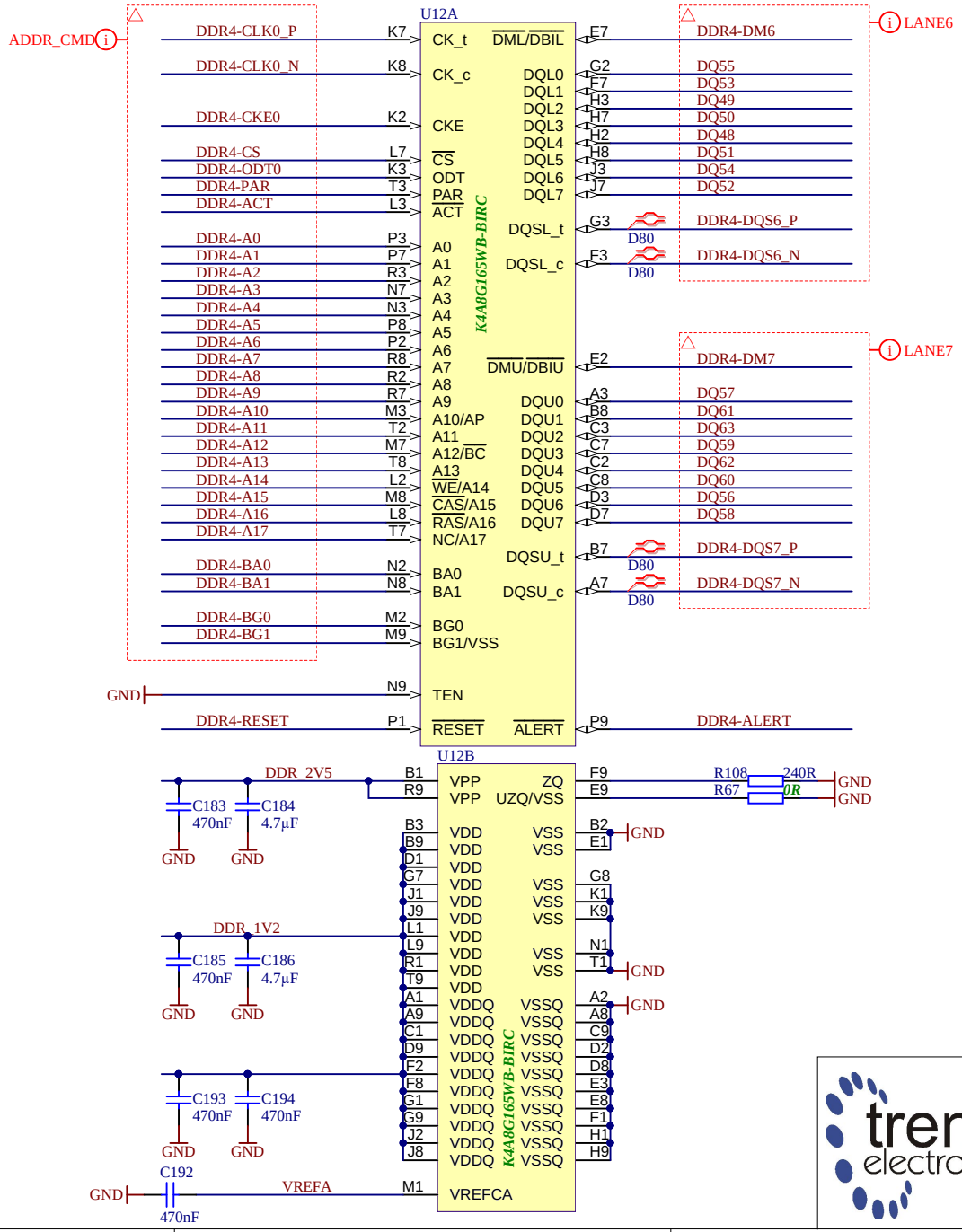
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page19 of 26
Filename: DDR4-RAM_3.SchDoc			



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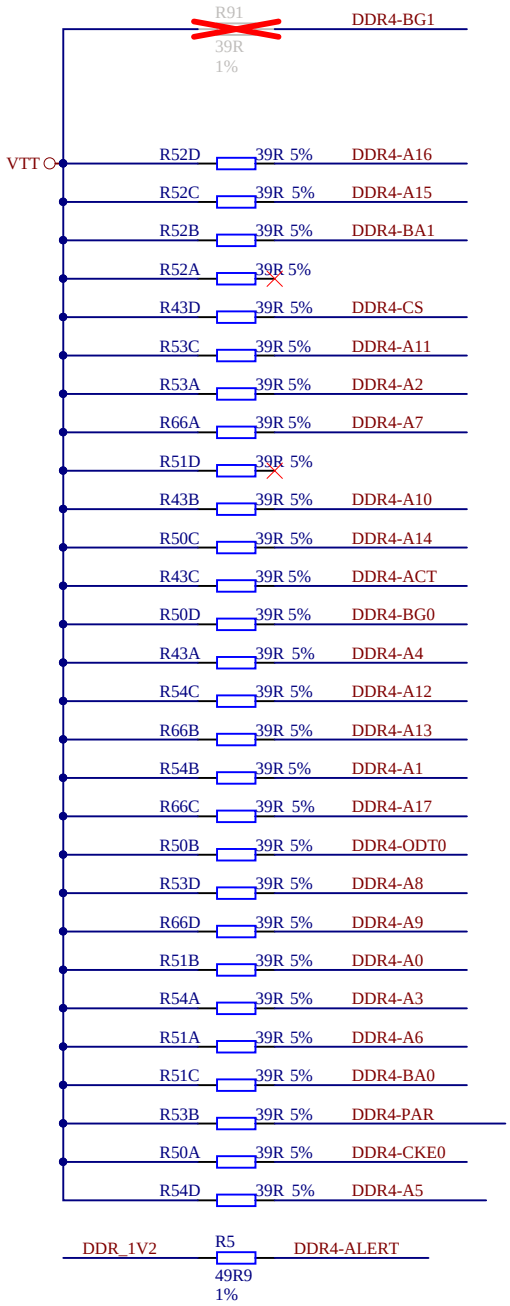
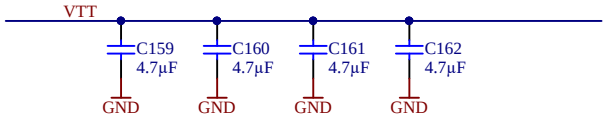
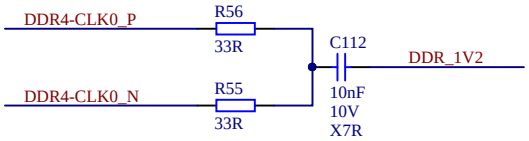
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page20 of 26
Filename: DDR4-RAM_4.SchDoc			







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Title: TE0803 - DDR4_TERM		
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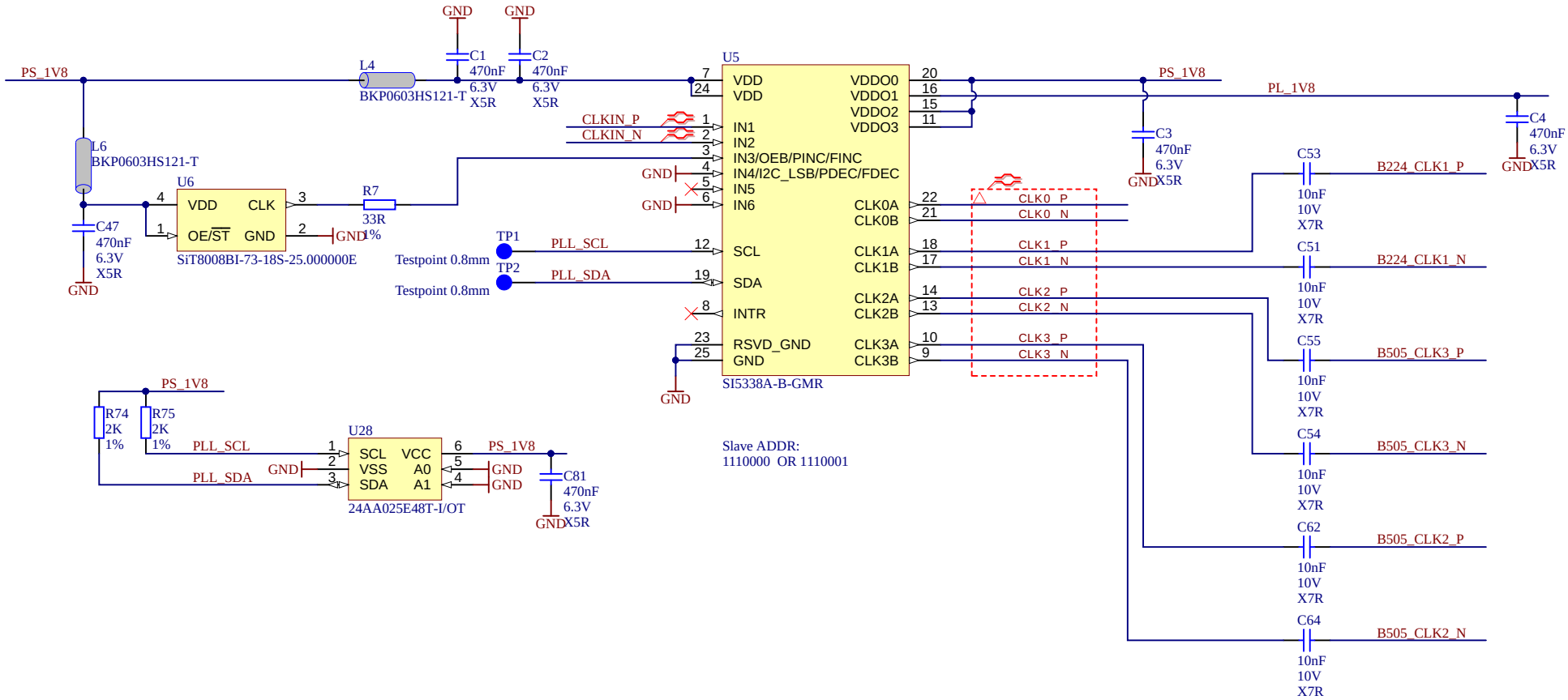
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page21 of 26
Filename: DDR4-TERM.SchDoc		



trenz electronic	Title: TE0803 - CLOCK		
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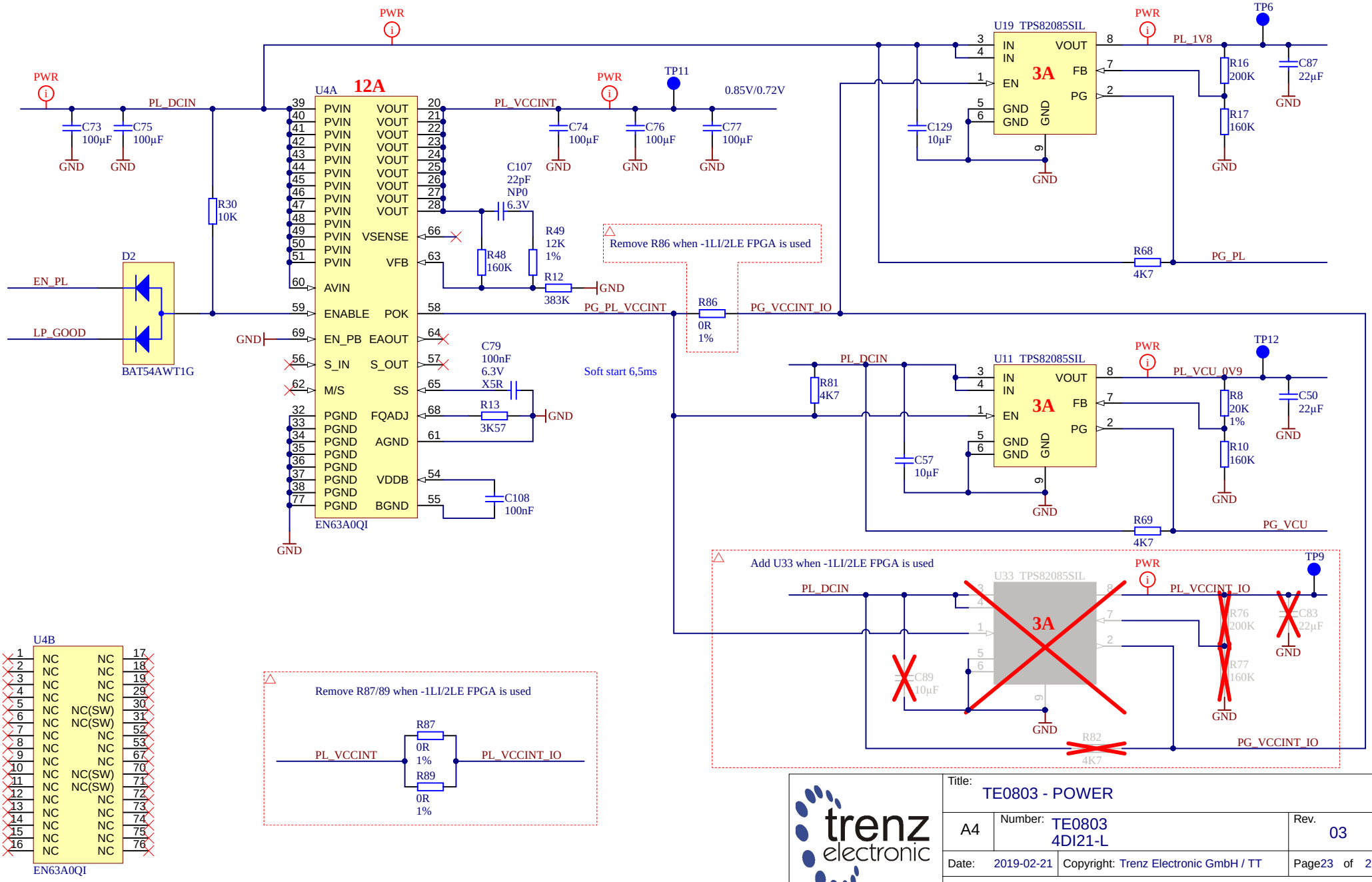
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page22 of 26
	Filename: Clock.SchDoc		



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Title: TE0803 - POWER		
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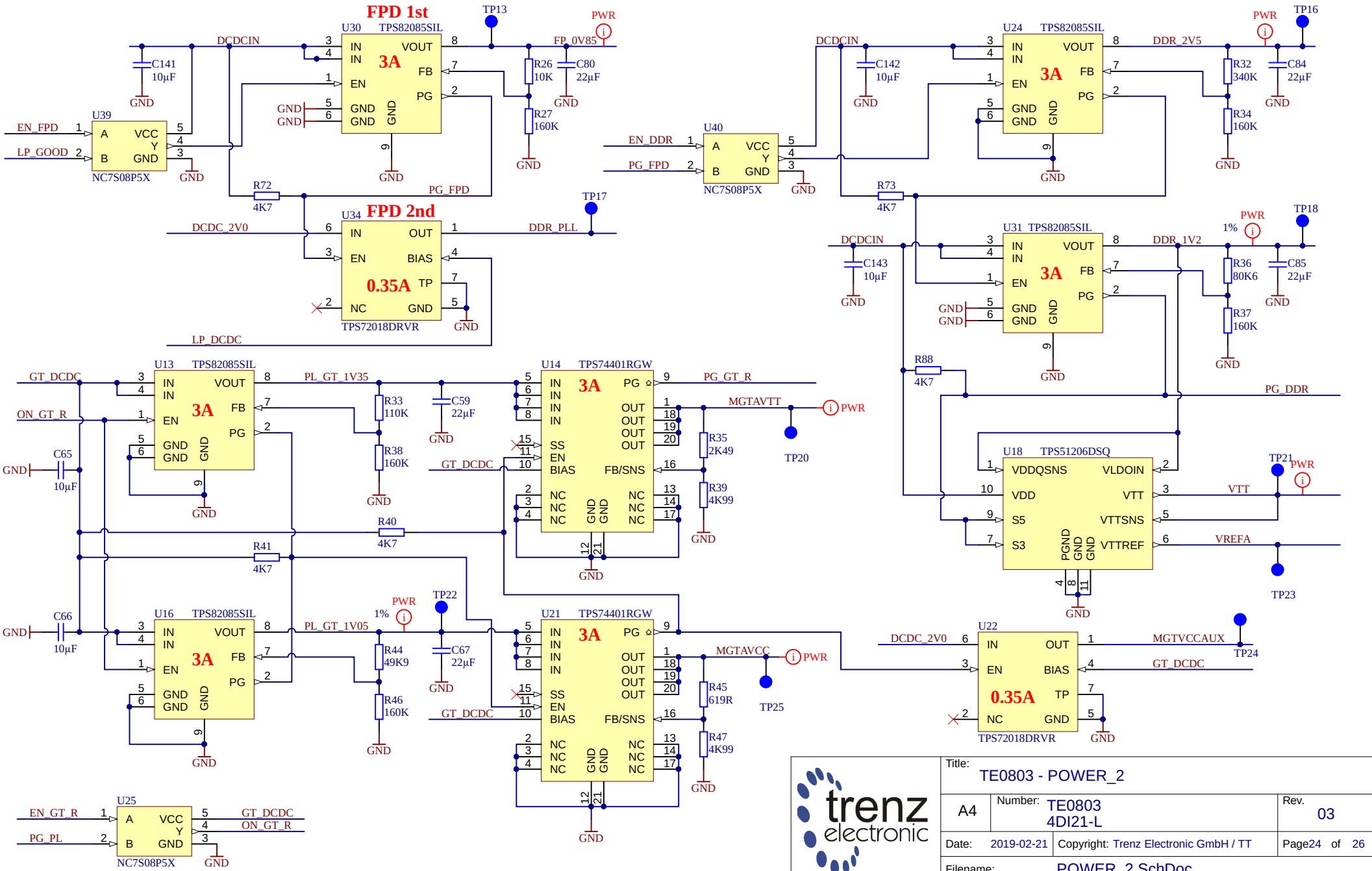
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page23 of 26
Filename: POWER.SchDoc		



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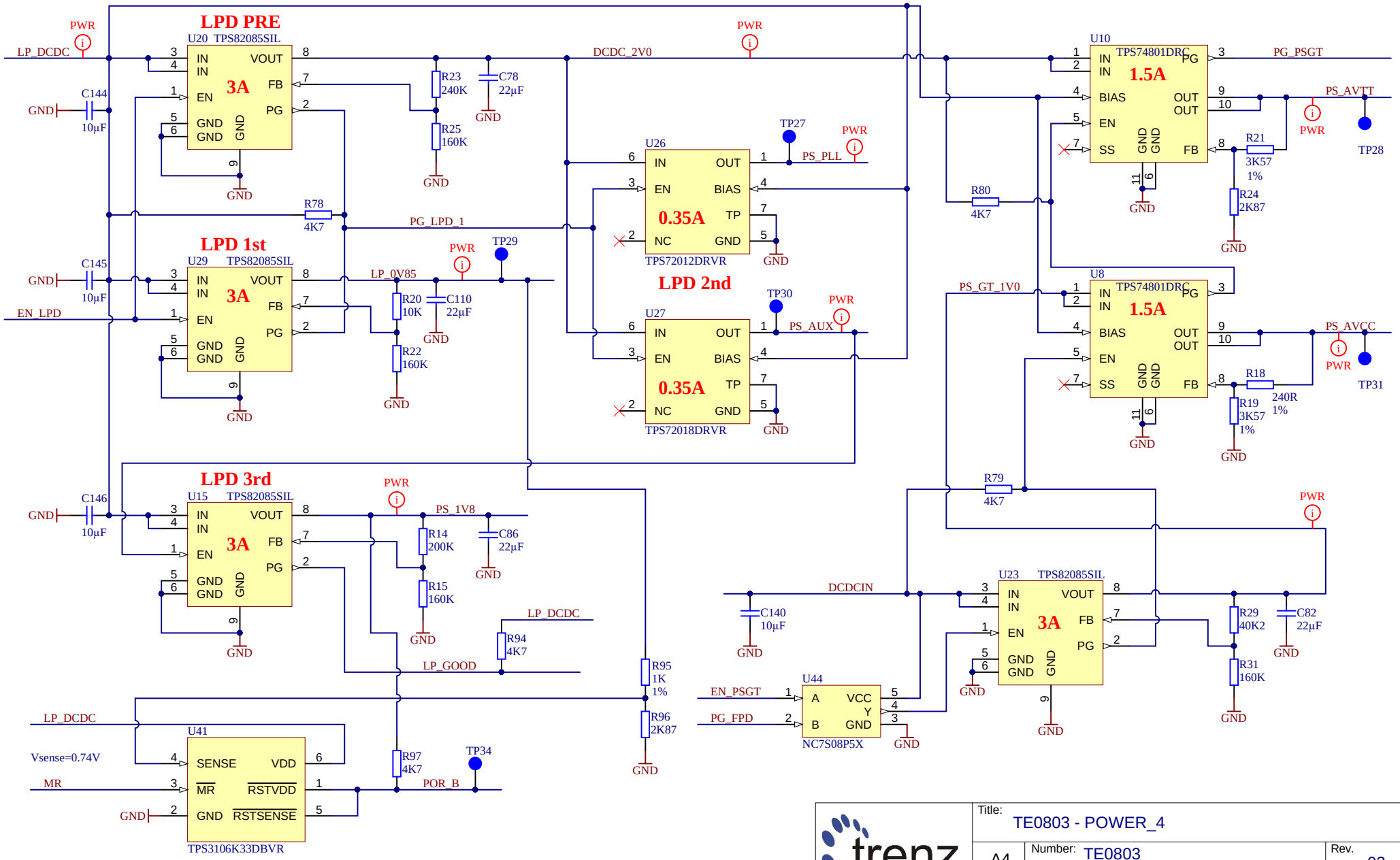
Title:	TE0803 - POWER_2		
A4	Number: TE0803 4DI21-L		Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page24 of 26
Filename:	POWER_2.SchDoc		



Title: TE0803 - POWER_4			
A4	Number: TE0803 4DI21-L		Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT		Page25 of 26
Filename: POWER_4.SchDoc			

CHANGES REV01a (20.11.2017):
---
1) VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9.

CHANGES REV02 (20.06.2018):
---
1) Added LDO to DDR_PLL
2) All differential pairs wath length matched with tollerance 0.1mm (excluding package delays)
3) Added MAC EEPROM U28
4) VPS_MGTRAVCC set to 0.85V
5) Added pull-up resistors R68,R69

CHANGES REV03 (21.02.2019):
---
1) Added support of DDP DDR4
2) Added support of Low power FPGA (-L1/L2).
3) Revised testpoints
4) Revised J1-J4 connectors net label style

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