
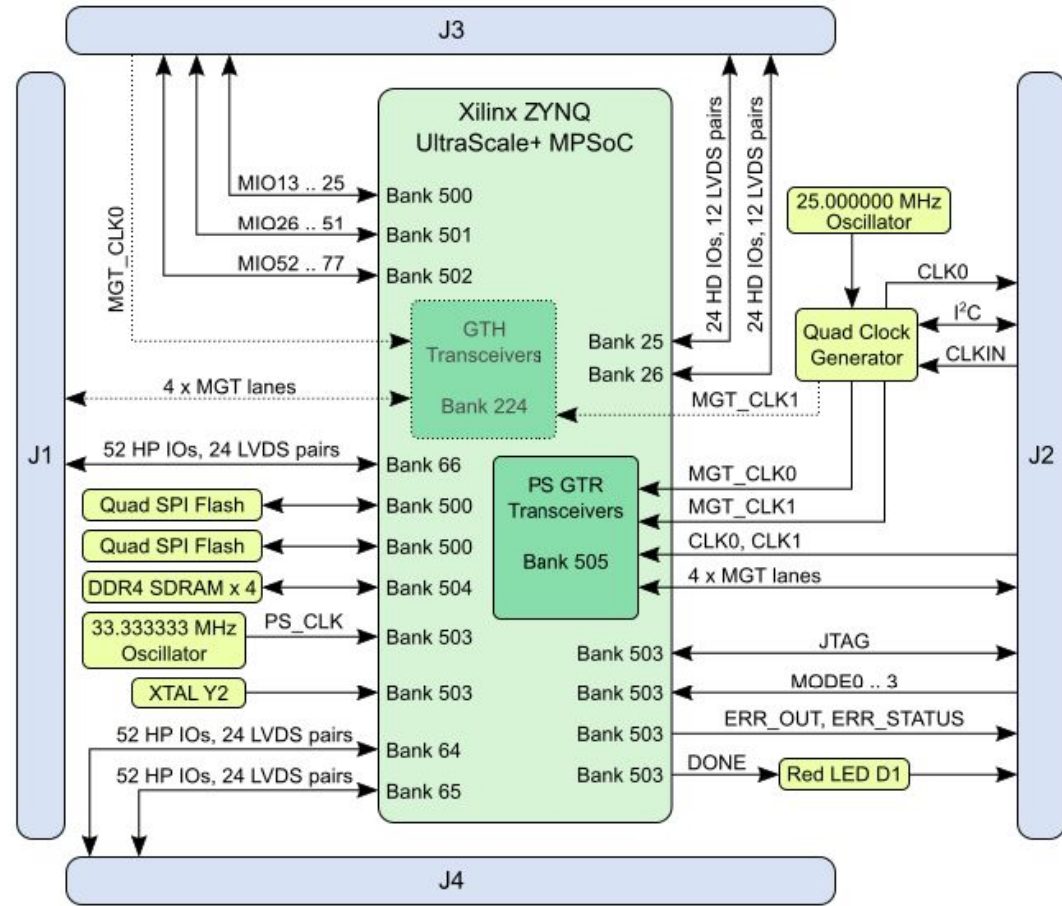



Regarding the usage of our schematics and alike documentation for Trenz module TE0803.

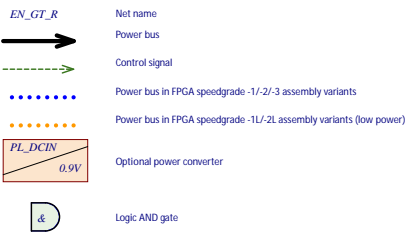
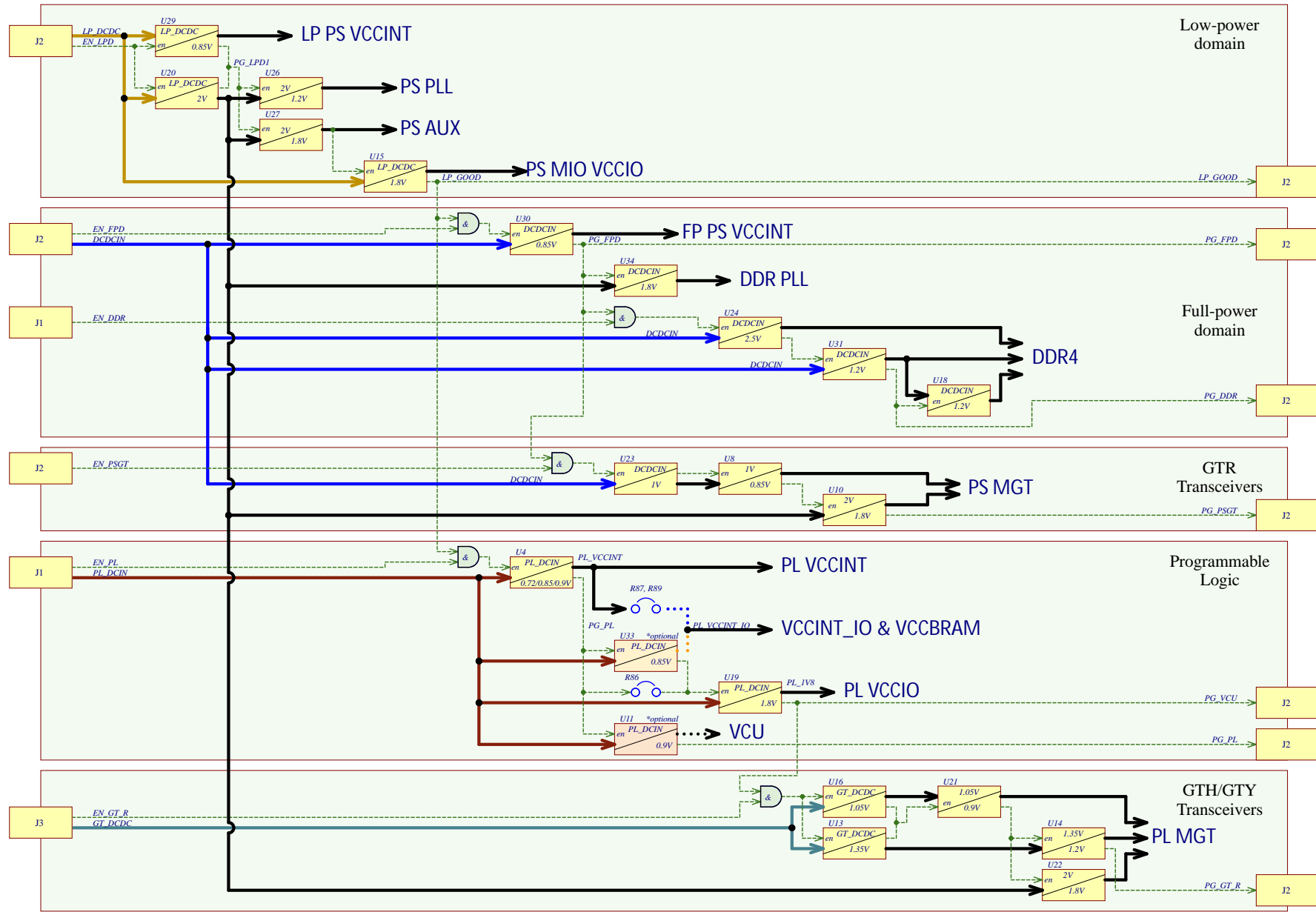
Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0803 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

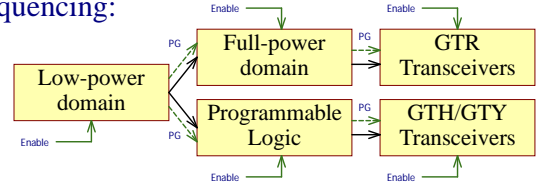
	Title: <b>TE0803</b>		
	A4	Number: <b>TE0803 2AE11-AZ</b>	Rev. <b>04</b>
	Date: <b>2021-01-19</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>1</b> of <b>30</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		



		Title: TE0803 - System Overview	
		A4	Number: TE0803 2AE11-AZ
Date: 2021-01-19		Copyright: 2015 Trenz Electronic GmbH	
Filename: TE0803-Overview.SchDoc		Page 2 of 30	



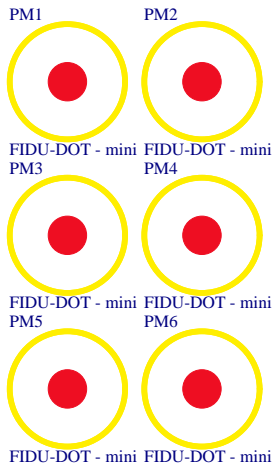
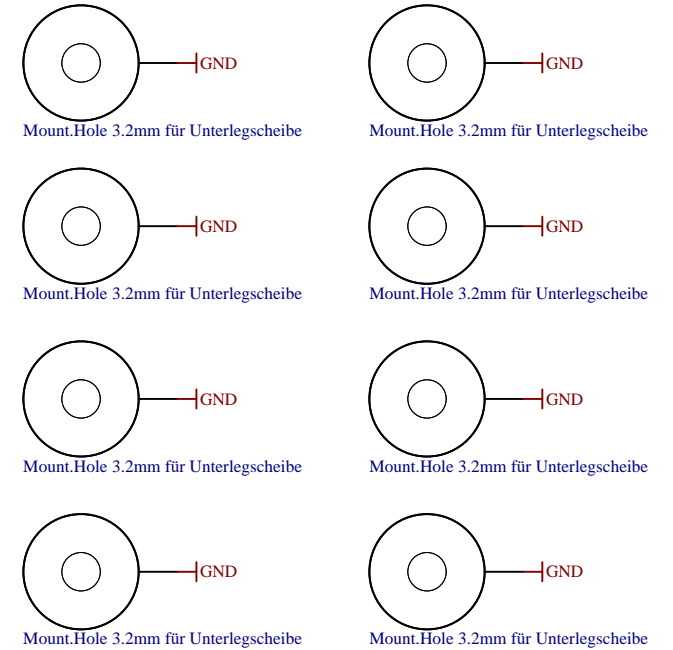
**Power-on sequencing:**



Title: TE0803 - Power Diagram		
A3	Number: TE0803 2AE11-AZ	Rev. 04
Datum: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 3 of 30
Filename: Power_Diagram.SchDoc		

U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_LN Legal Notices Modules.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_1 POWER_1.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_REV_CH Revision Changes.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	U_OVERVIEW TE0803-Overview.SchDoc
U_PD Power_Diagram.SchDoc	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

Special notes:




MECH1  
TE Address Overlay  
LOGO ADDRESS

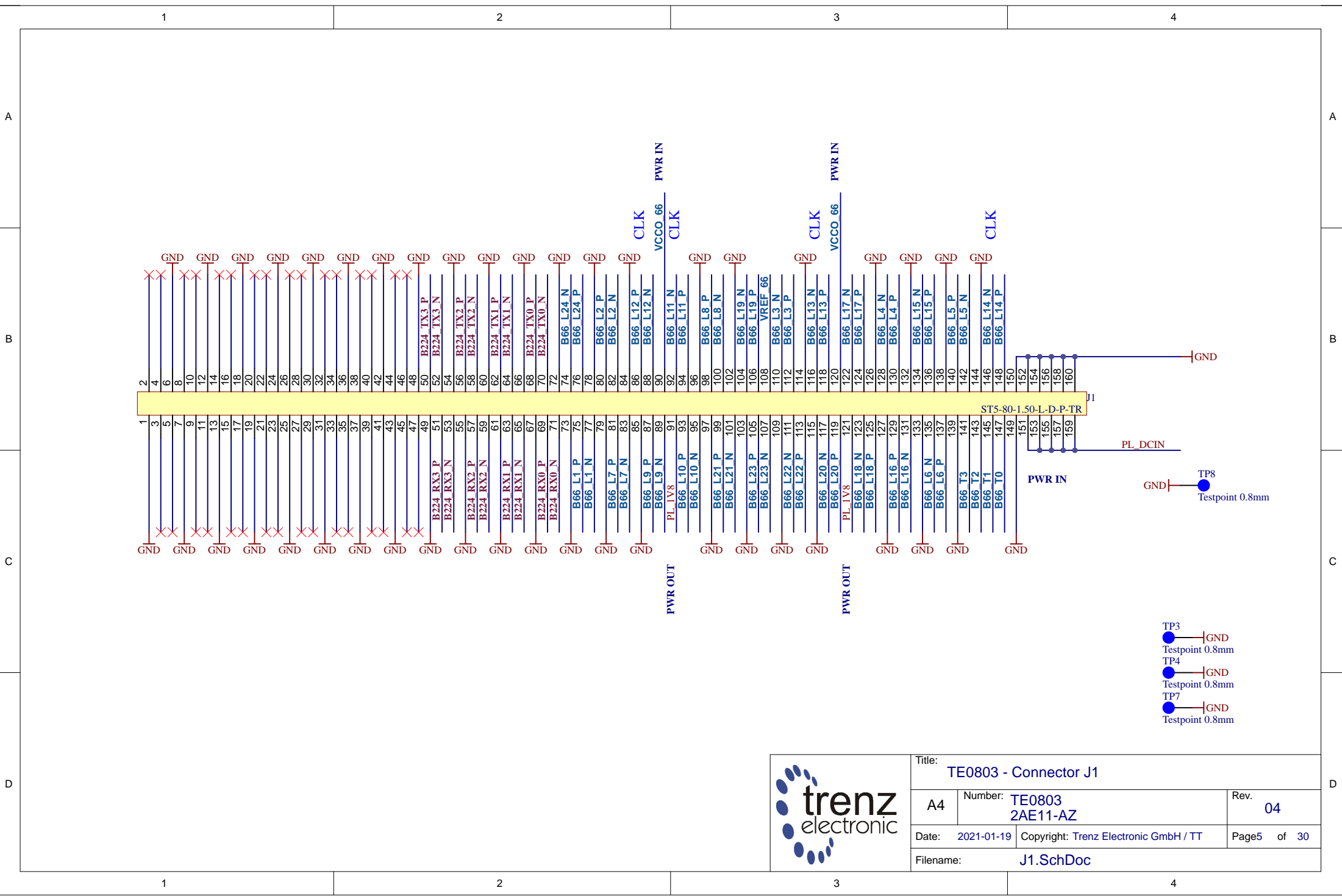
LOGO1  
TE Logo PRINT Layer  
LOGO PRINT

Serial  
Serial  
Serialnumber 6,3 x 6.3mm

Assembly variant	2AE11-AZ
Created by	VT
Modified by	VT
Modified at	2022-12-14
SVN Revision	11196

			Title: TE0803	
			A4	Number: TE0803 2AE11-AZ
Date: 2021-01-19		Copyright: Trenz Electronic GmbH / TT		Page4 of 30
Filename: TE0803.SchDoc				





Title: TE0803 - Connector J1		
A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page5 of 30
Filename: J1.SchDoc		

1

2

3

4

A

A

B

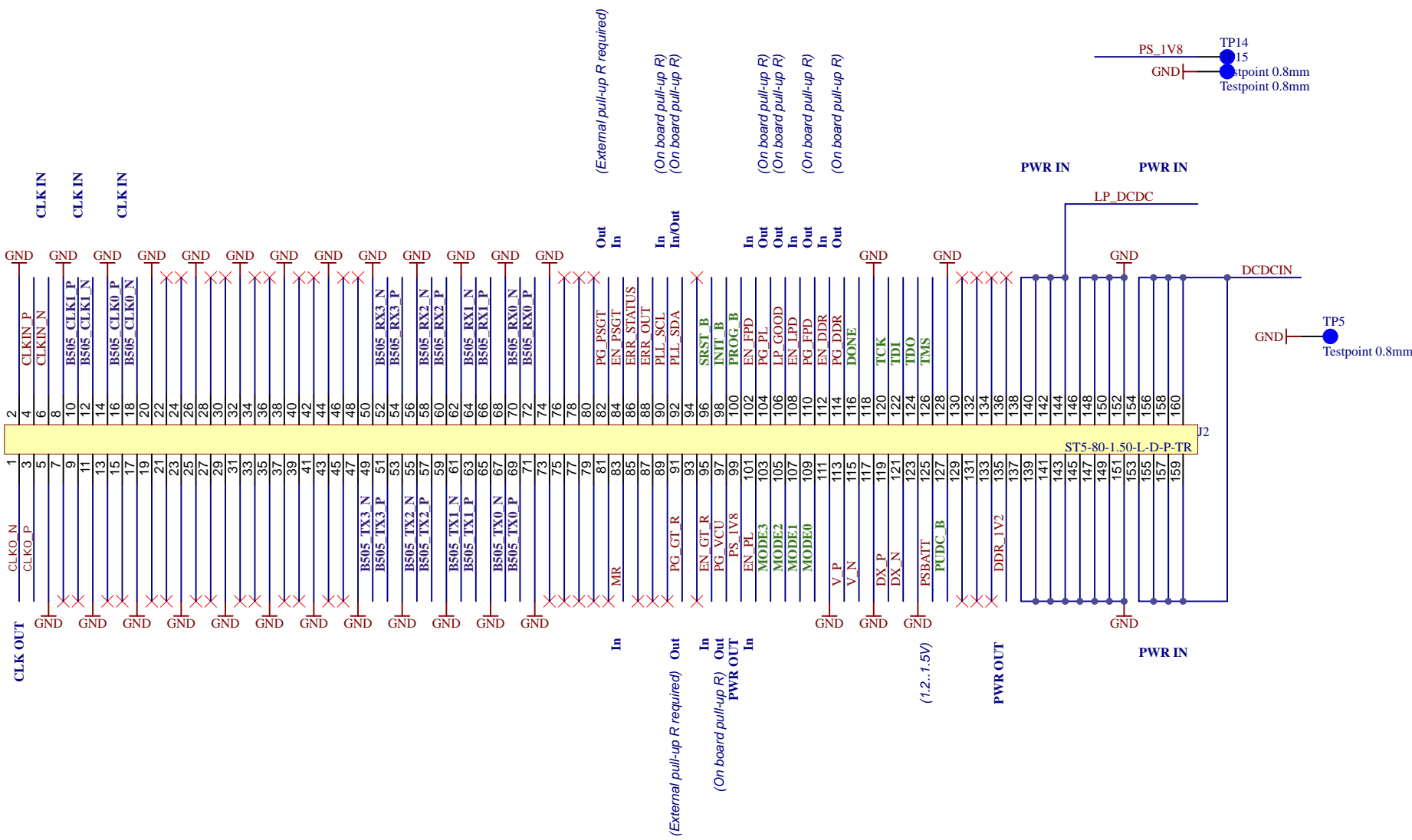

B

C

C

D

D

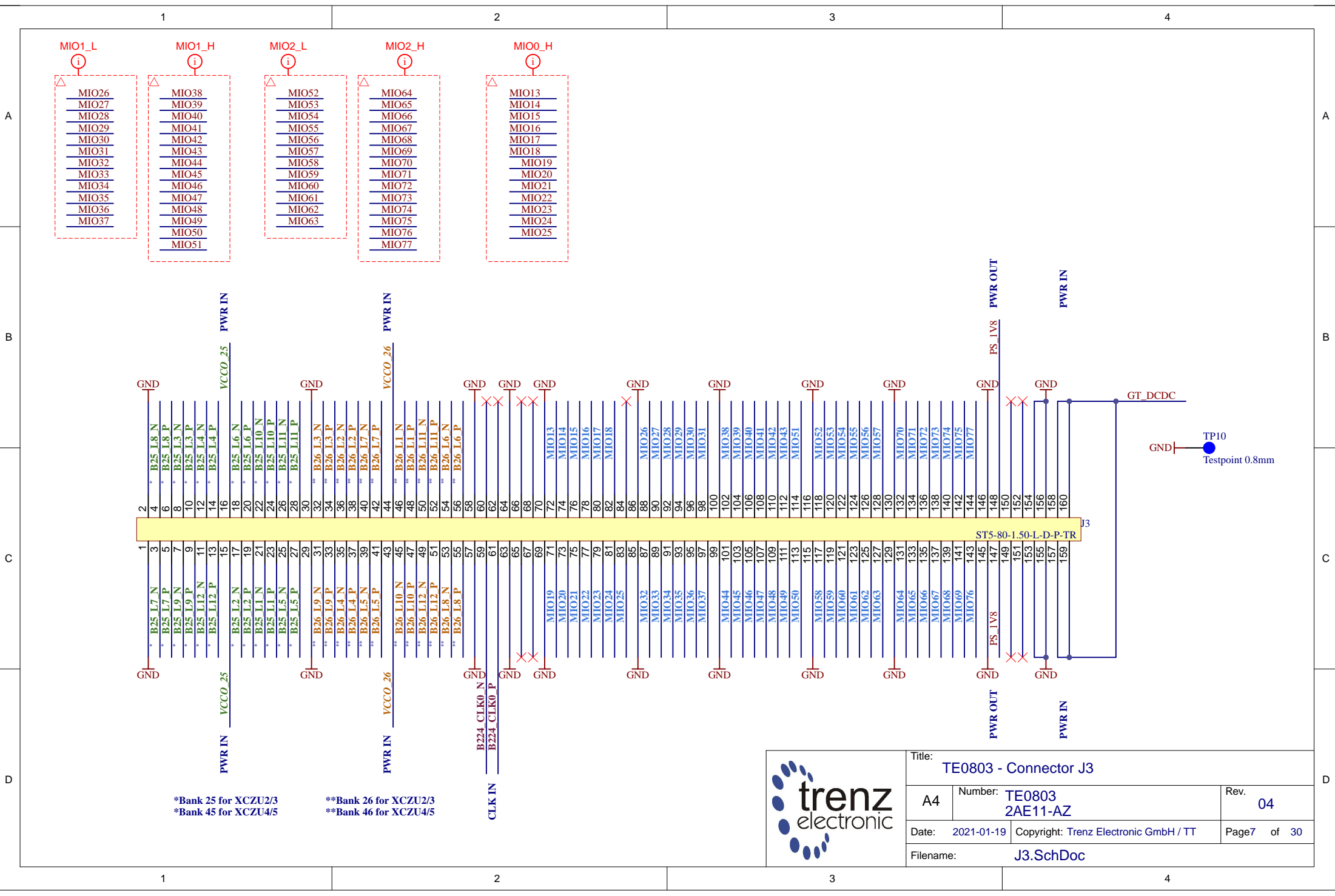
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A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 6 of 30
Filename: J2.SchDoc		

1

2

3

4



\*Bank 25 for XCZU2/3  
\*Bank 45 for XCZU4/5

\*\*Bank 26 for XCZU2/3  
\*\*Bank 46 for XCZU4/5



Title: TE0803 - Connector J3		
A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 7 of 30
Filename: J3.SchDoc		

1

2

3

4

A

A

B

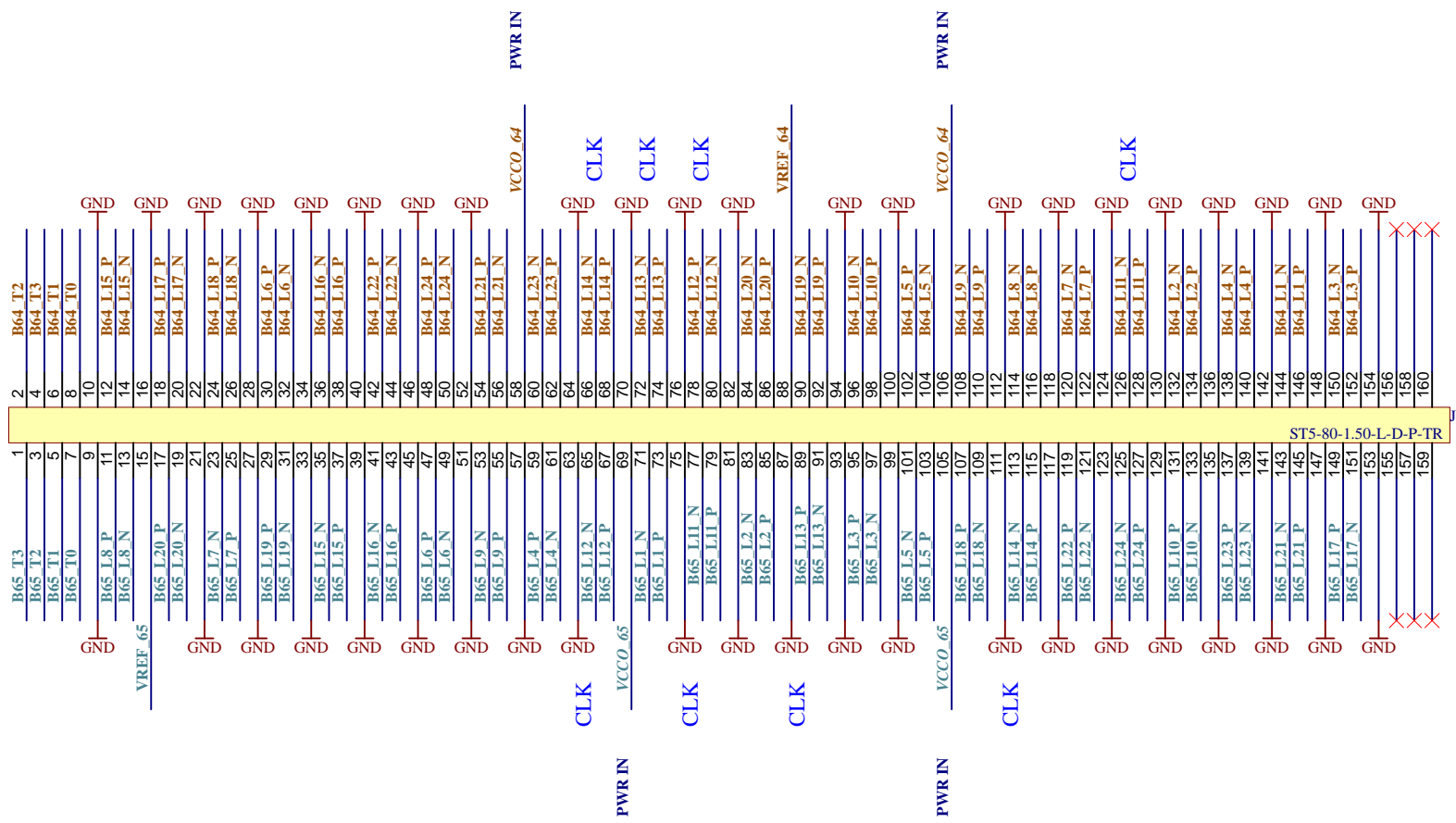
B

C

C

D

D



1

2

3

4



Title: TE0803 - Connector J4		
A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page8 of 30
Filename: J4.SchDoc		

1

2

3

4

A

A

B

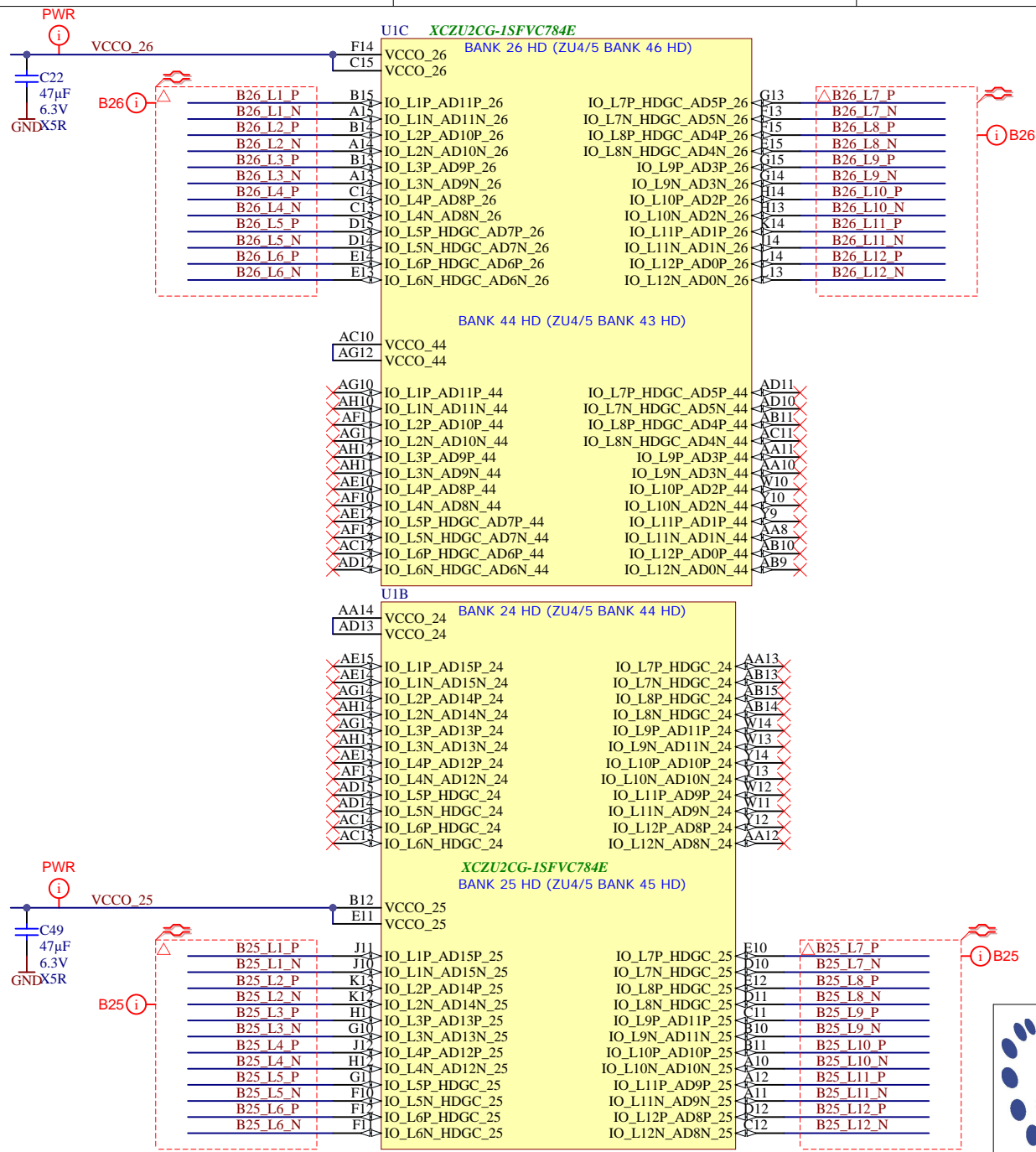
B

C

C

D

D



Title: TE0803 - HD Banks		
A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page9 of 30
Filename: B_HD.SchDoc		

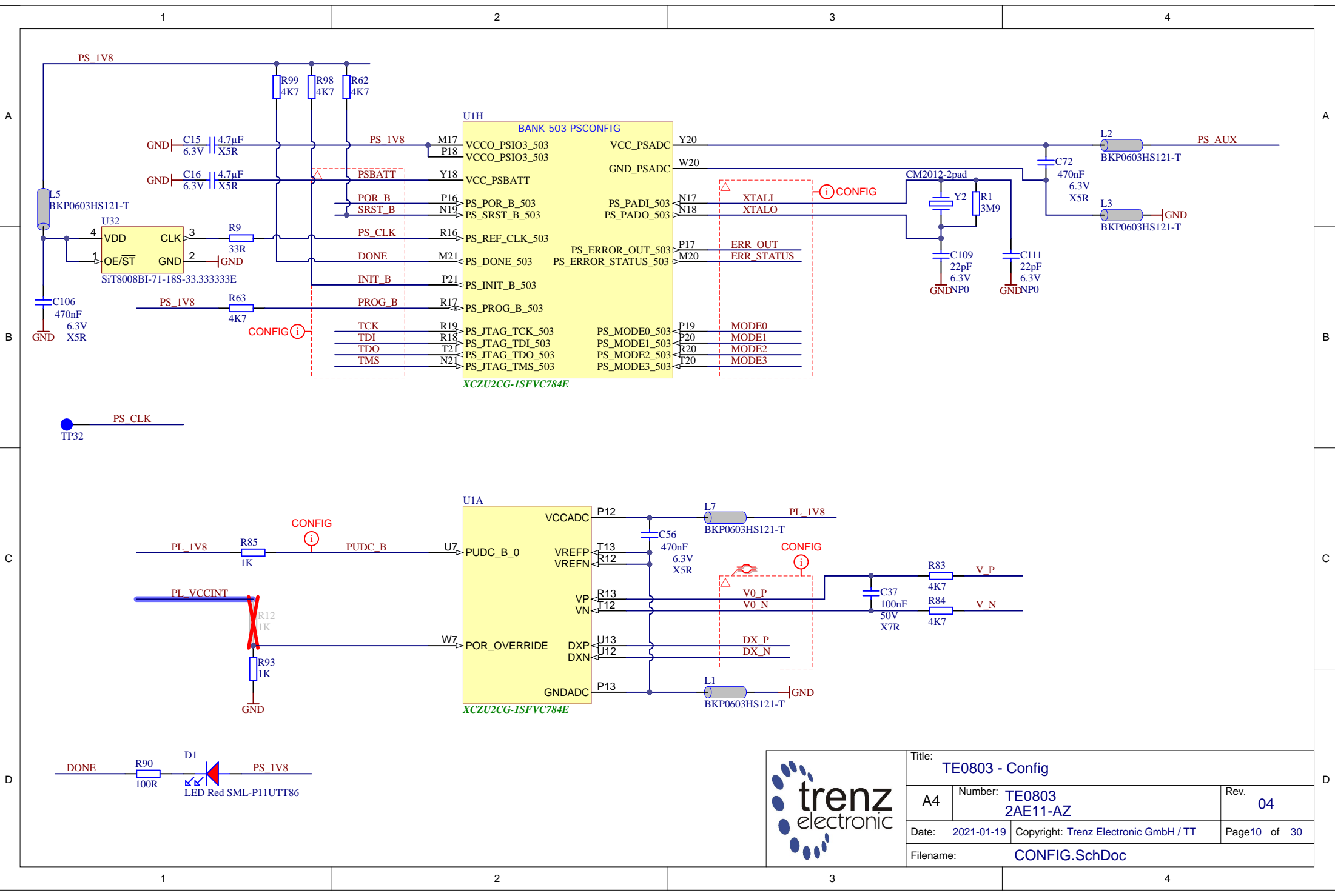
1

2

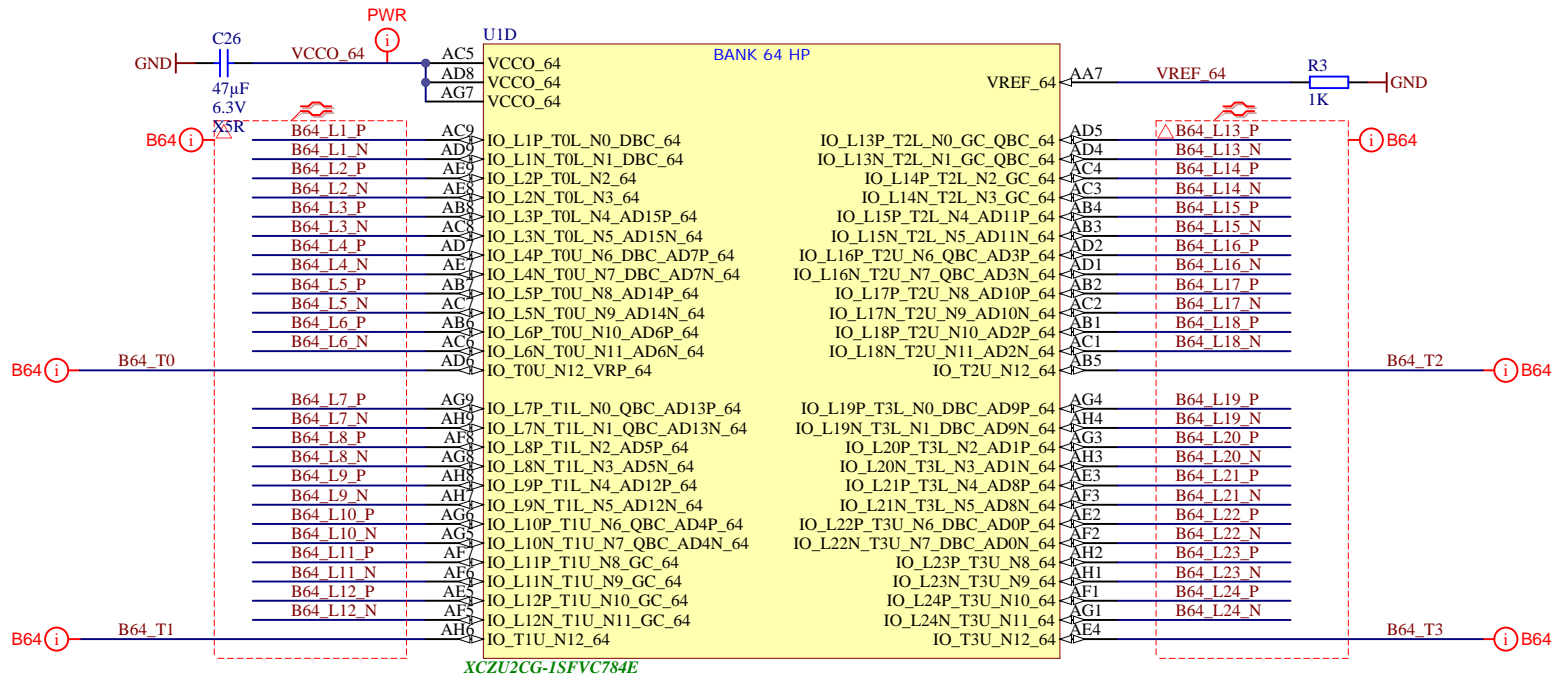
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4

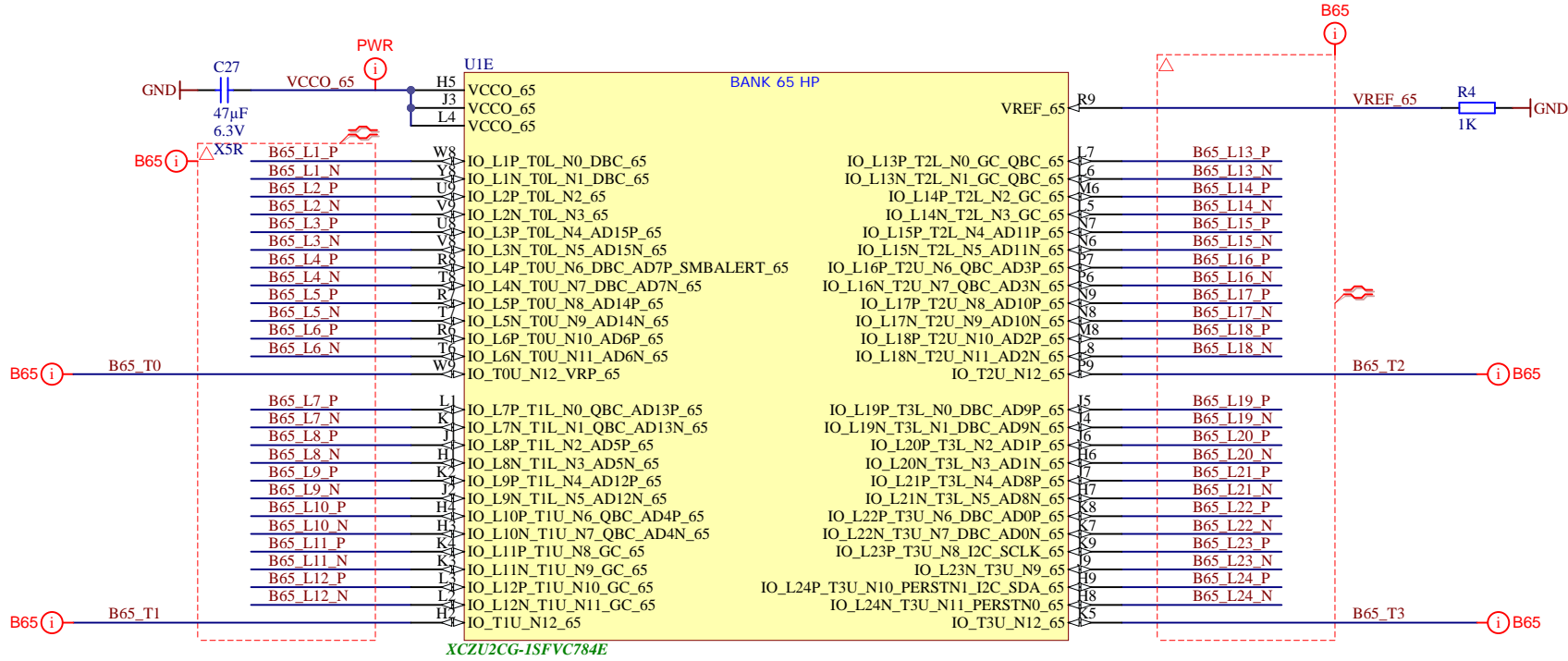




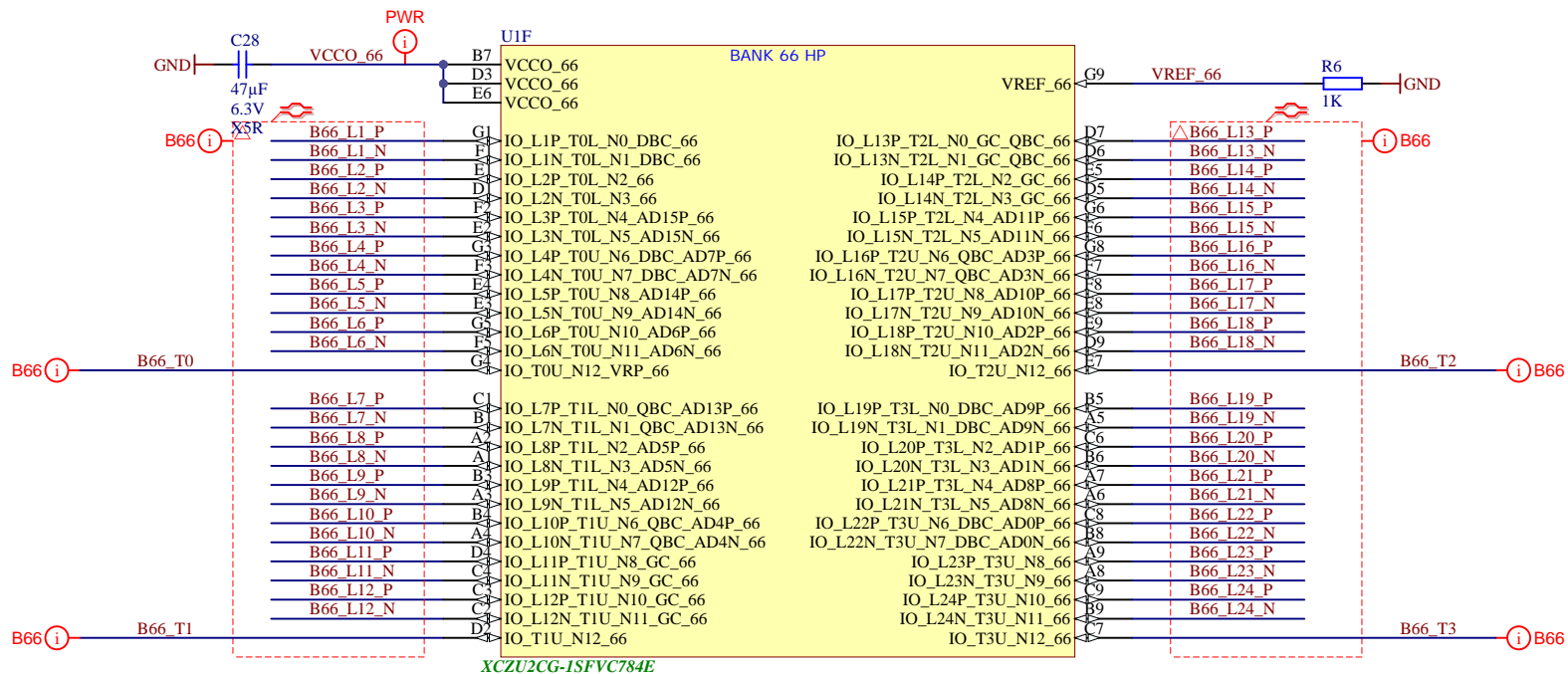
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A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 10 of 30
Filename: CONFIG.SchDoc		



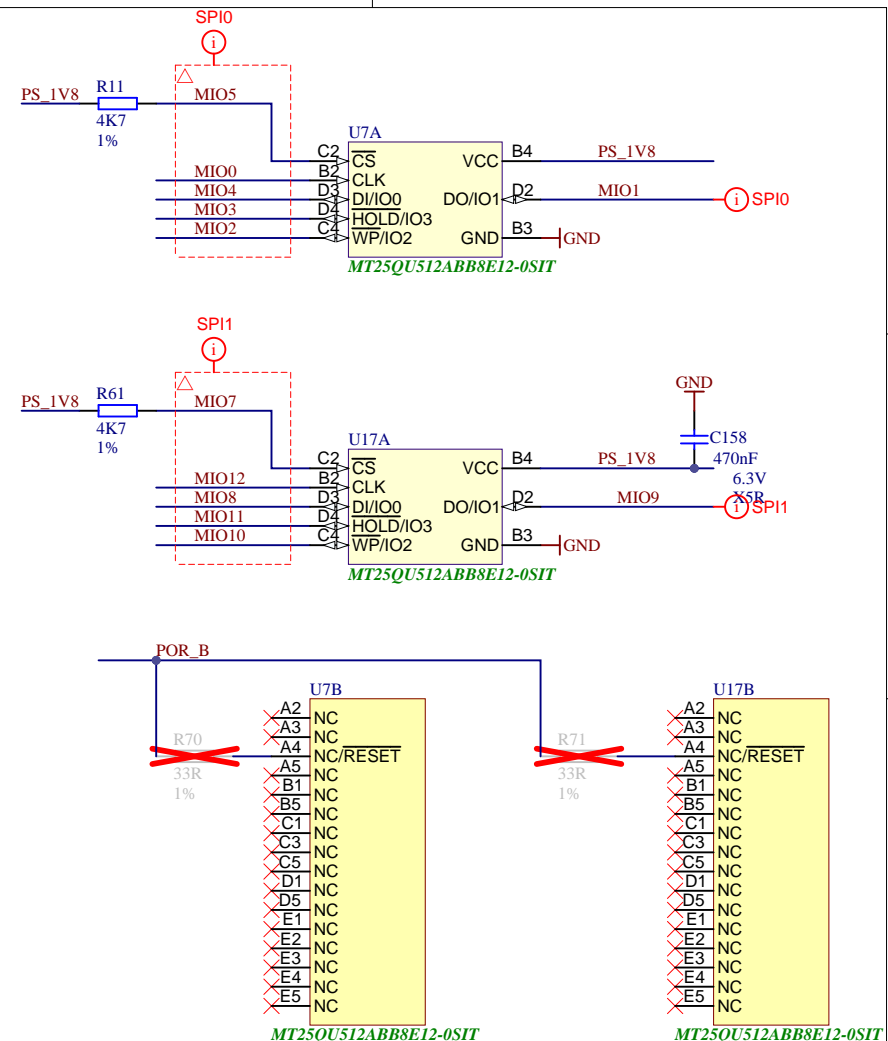
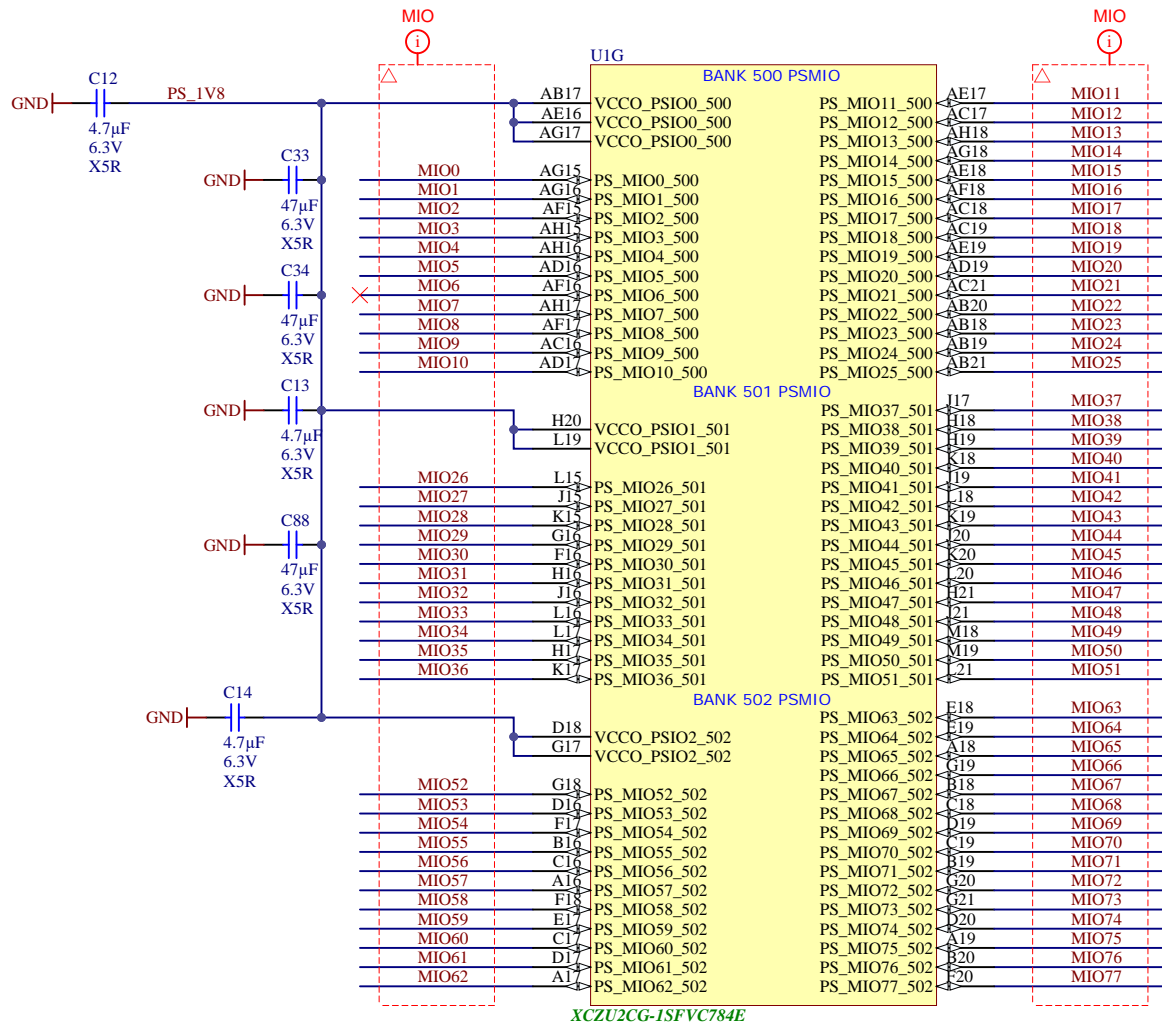
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A4	Number: <b>TE0803 2AE11-AZ</b>	Rev. <b>04</b>
Date: <b>2021-01-19</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>11</b> of <b>30</b>
Filename: <b>B64.SchDoc</b>		



Title: <b>TE0803 - B65</b>		
A4	Number: <b>TE0803 2AE11-AZ</b>	Rev. <b>04</b>
Date: <b>2021-01-19</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>12</b> of <b>30</b>
Filename: <b>B65.SchDoc</b>		



	Title: <b>TE0803 - B66</b>		
	A4	Number: <b>TE0803 2AE11-AZ</b>	Rev. <b>04</b>
	Date: <b>2021-01-19</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>13</b> of <b>30</b>
	Filename: <b>B66.SchDoc</b>		



	Title: <b>TE0803 - MIO Banks</b>	
	A4	Number: <b>TE0803 2AE11-AZ</b>
	Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT
	Filename: <b>B_MIO.SchDoc</b>	Page 14 of 30

1

2

3

4

1

2

3

4



A

A

B

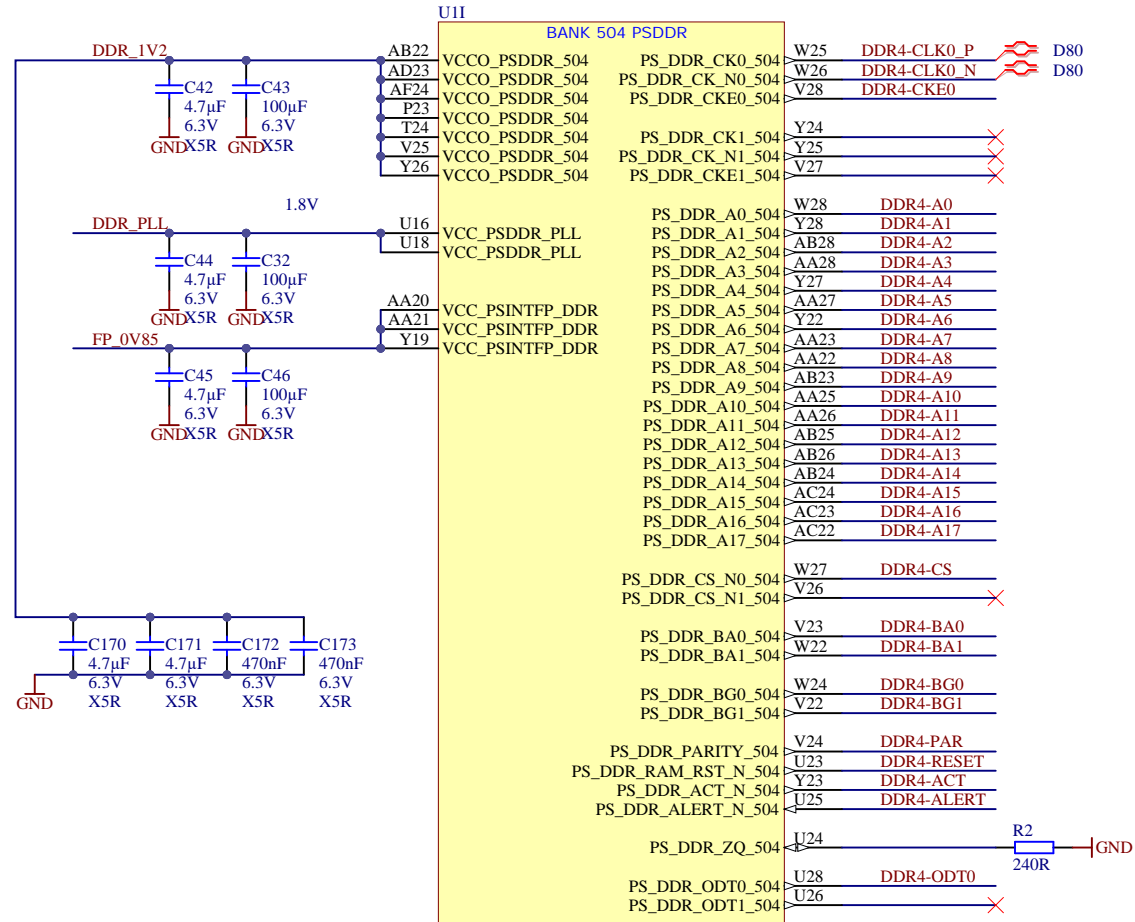
B

C

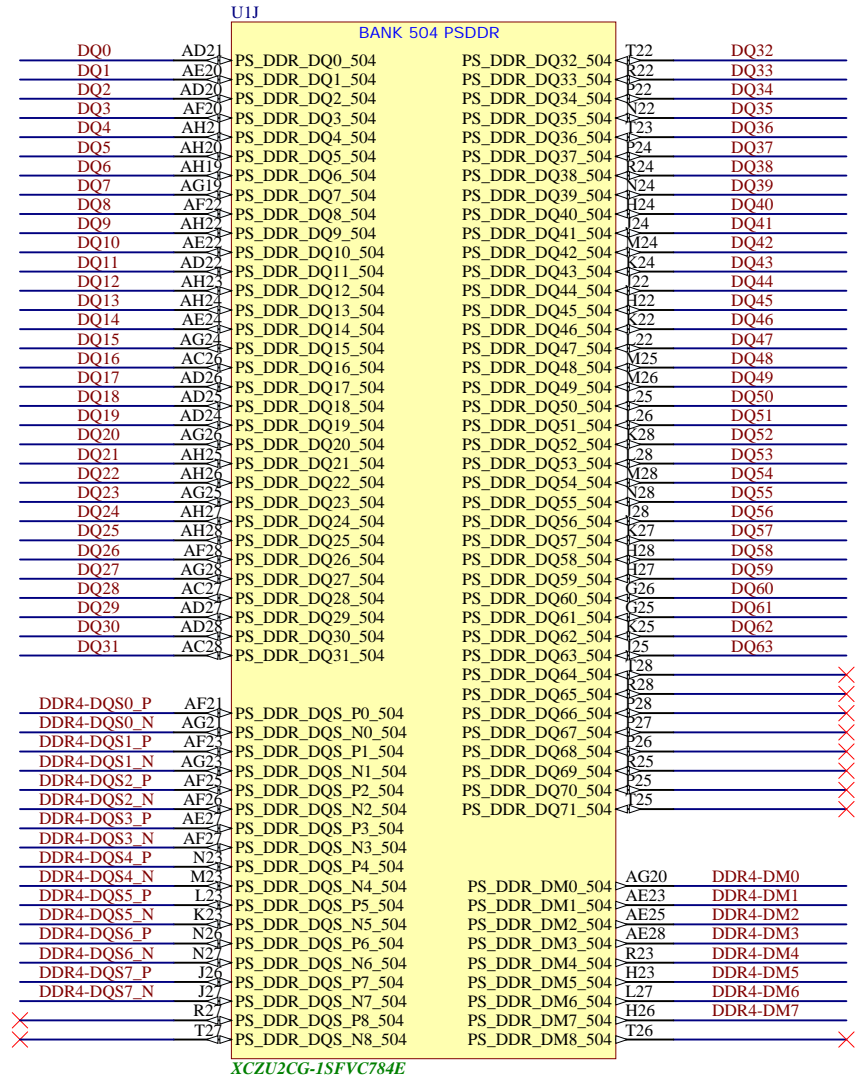
C

D

D



XCZU2CG-1SFVC784E



XCZU2CG-1SFVC784E



Title: TE0803 - PS_DDR		
A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 15 of 30
Filename: PS_DDR.SchDoc		

1

2

3

4

A

A

B

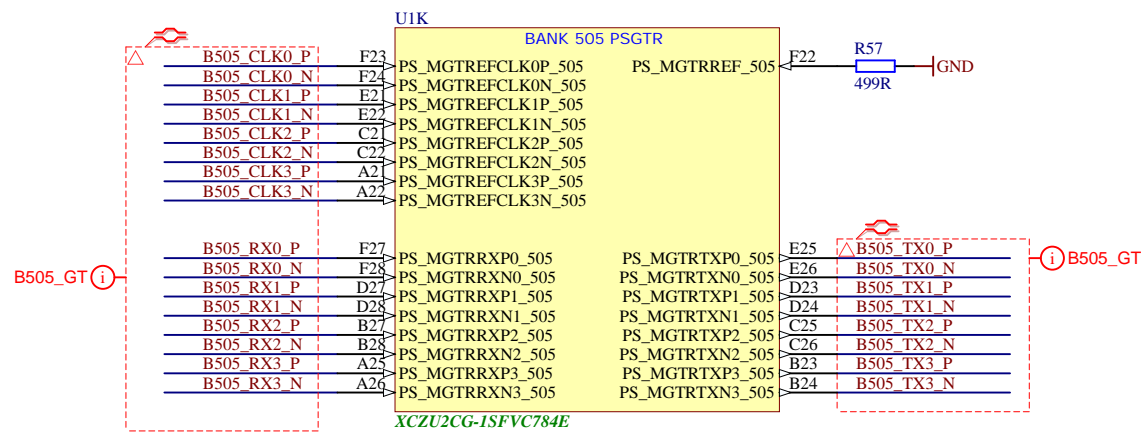
B

C

C

D

D



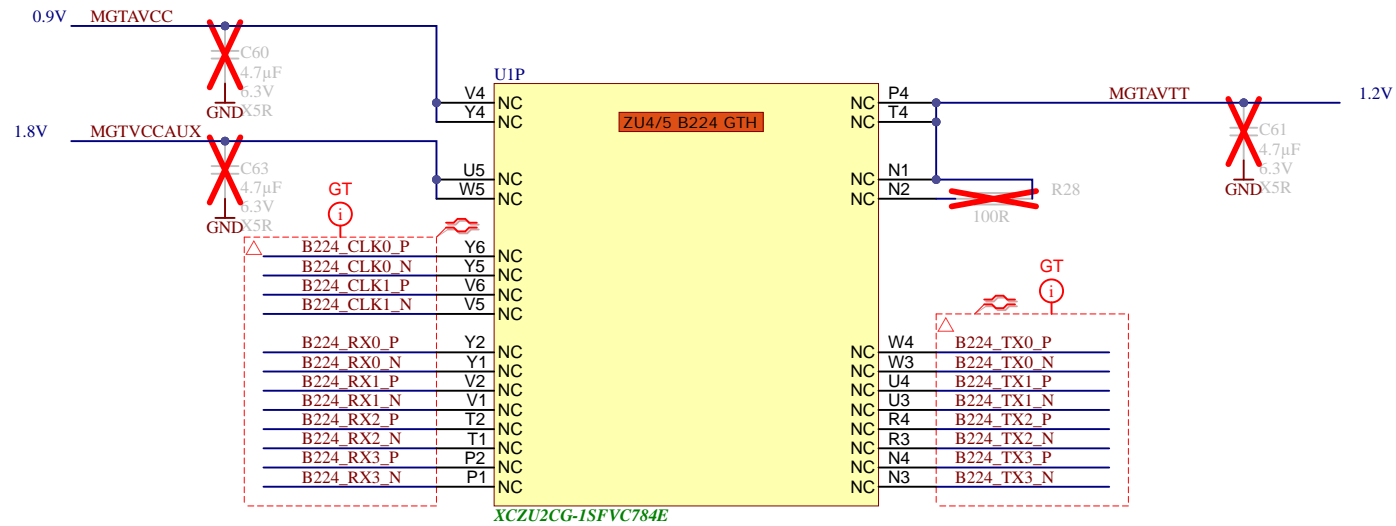
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A4	Number: <b>TE0803 2AE11-AZ</b>	Rev. <b>04</b>
Date: <b>2021-01-19</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>16</b> of <b>30</b>
Filename: <b>B_PS_GT.SchDoc</b>		


1

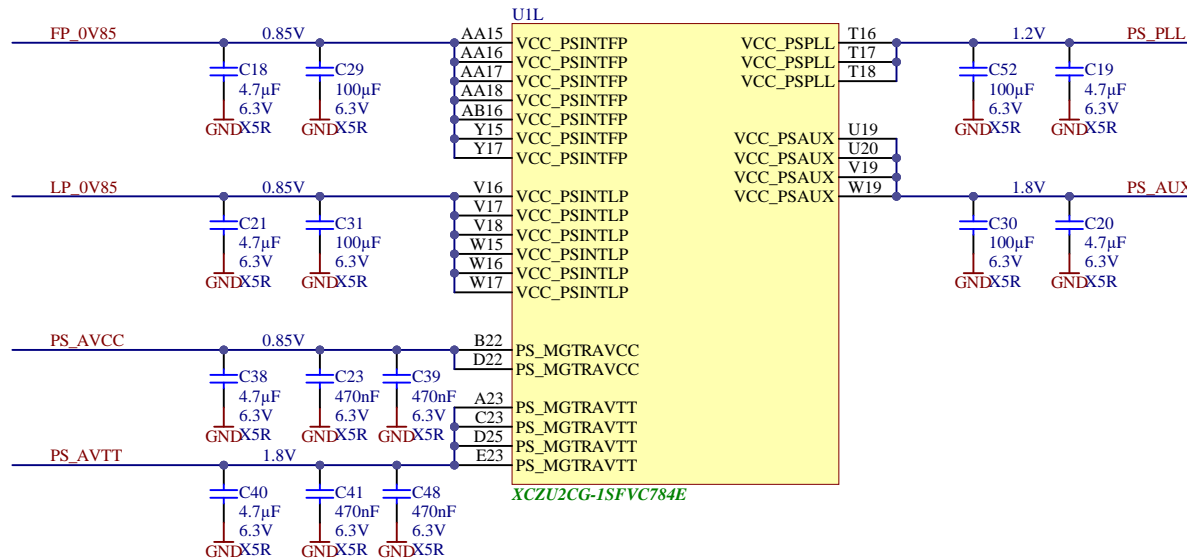
2

3

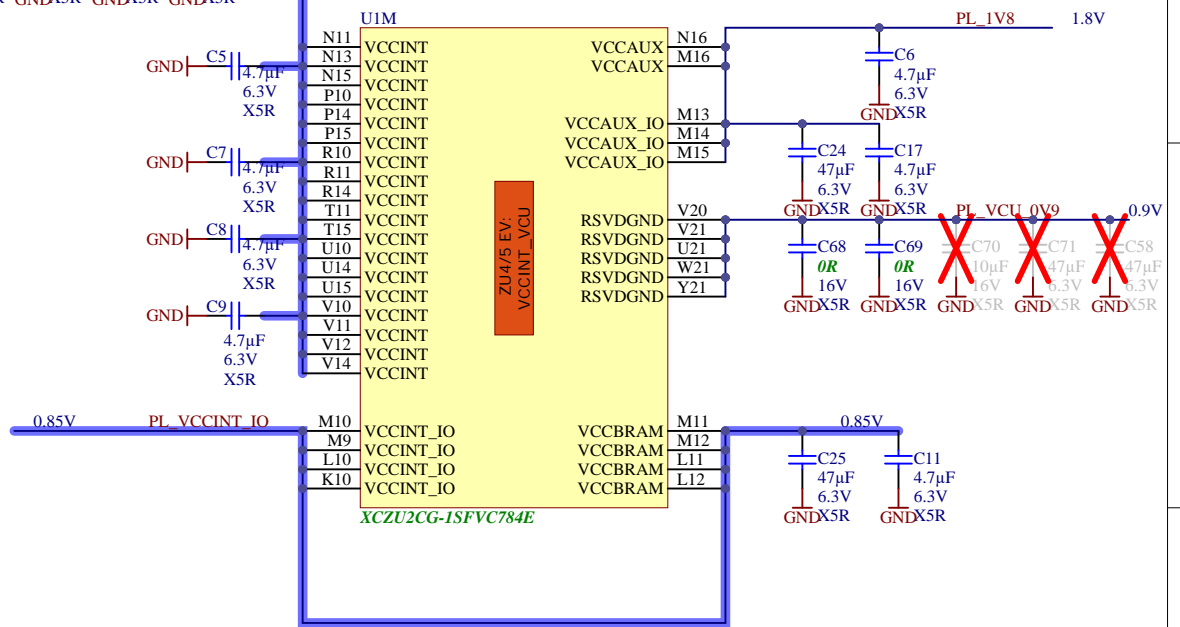
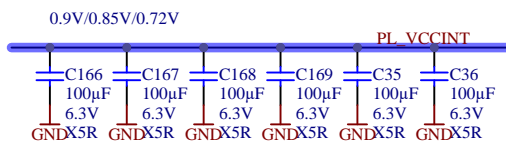
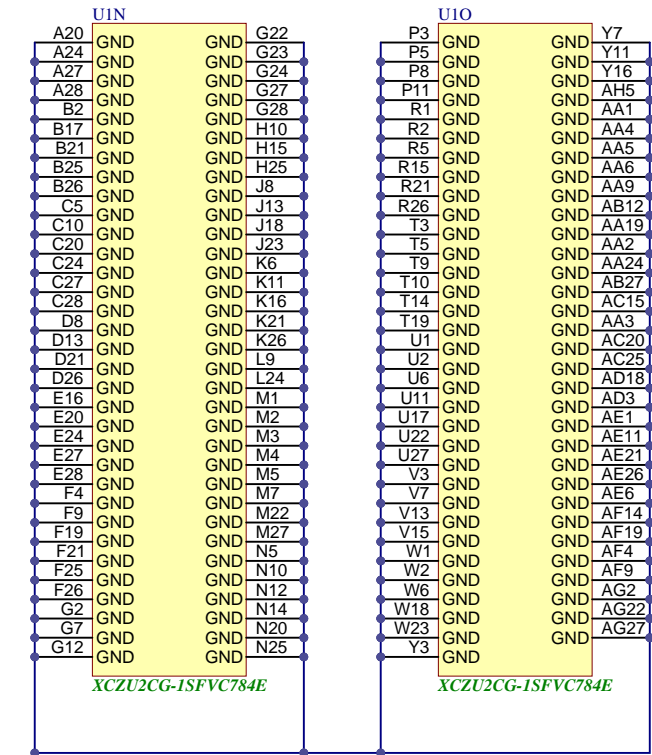
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		Title: TE0803 - B224GTH	
		A4	Number: TE0803 2AE11-AZ
Date: 2021-01-19		Copyright: Trenz Electronic GmbH / TT	
Filename: B_GT.SchDoc		Page17 of 30	



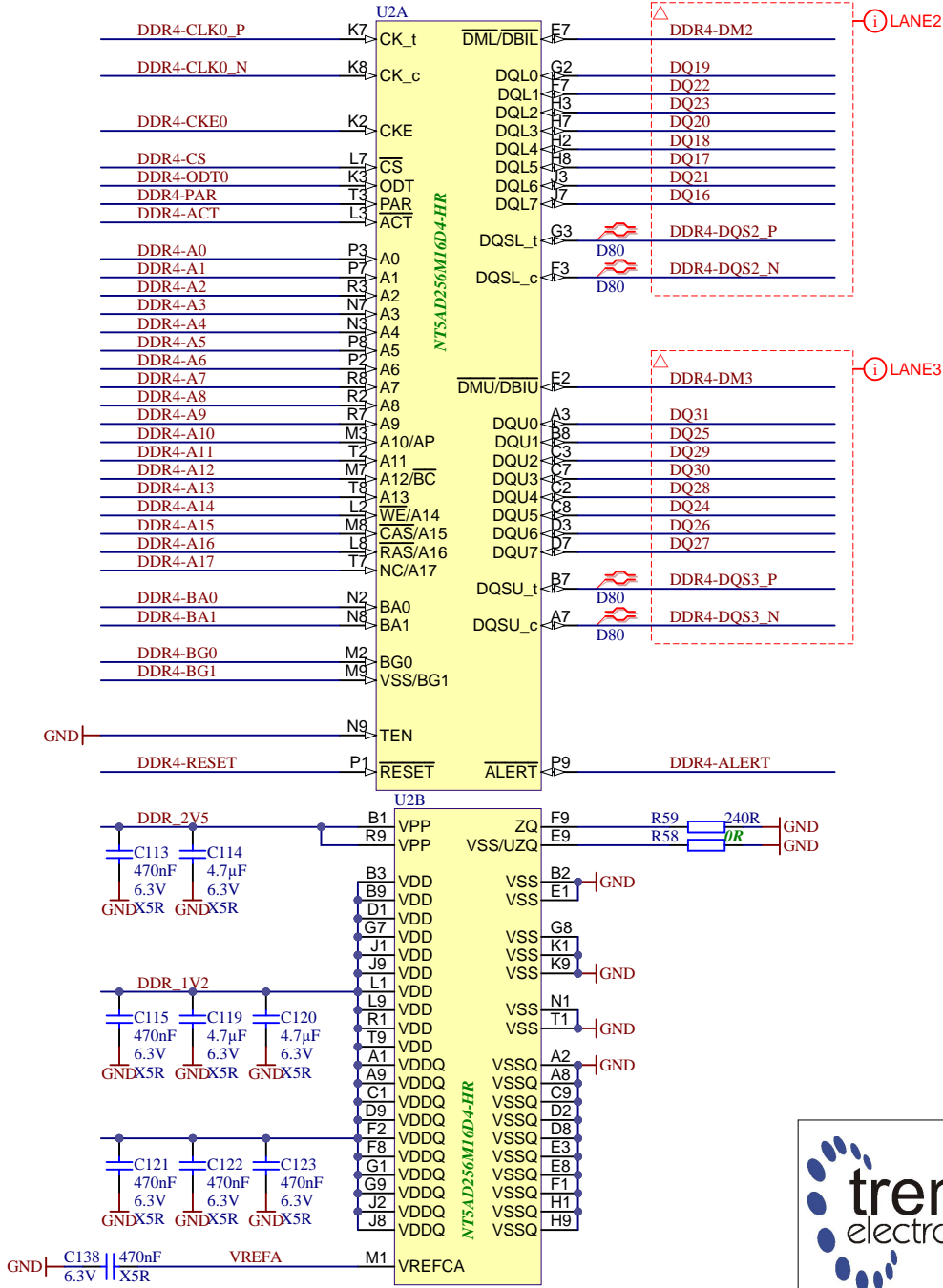
	Title: TE0803 - ZU_PS_POWER		
	A4	Number: TE0803 2AE11-AZ	Rev. 04
	Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 18 of 30
	Filename: ZU_PS_POWER.SchDoc		



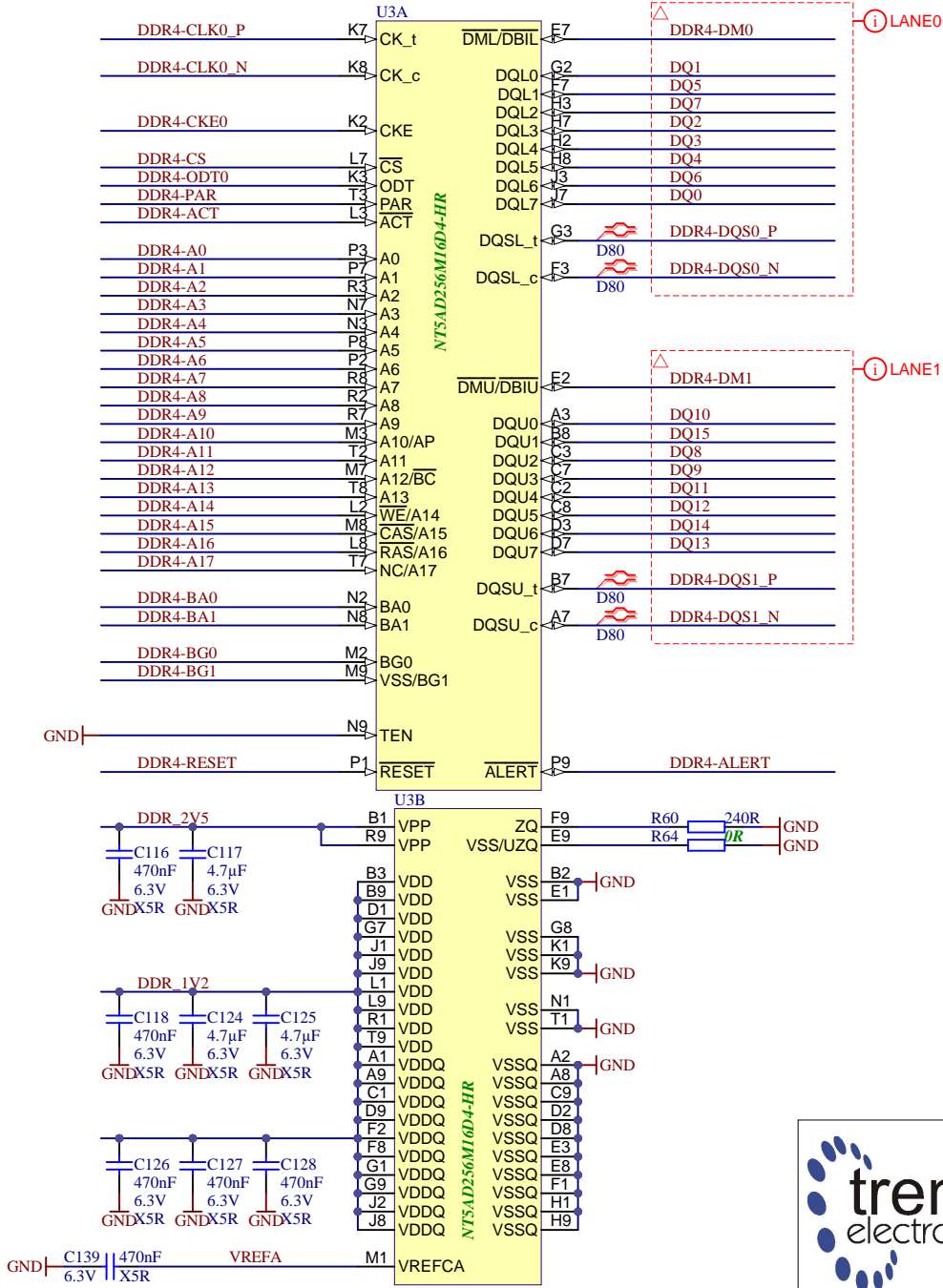
Title: TE0803 - ZU\_POWER

A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 19 of 30
Filename: ZU_POWER.SchDoc		

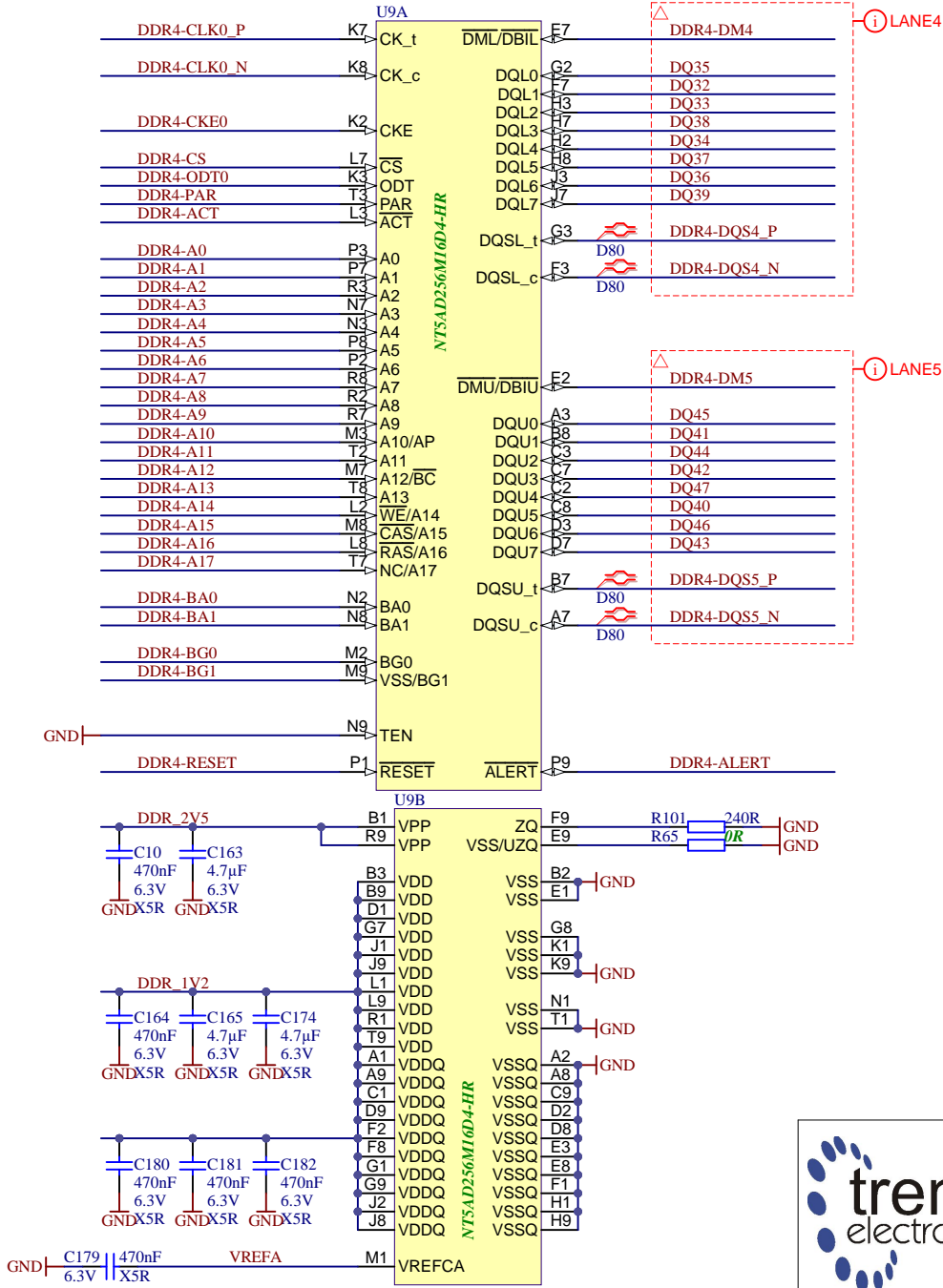




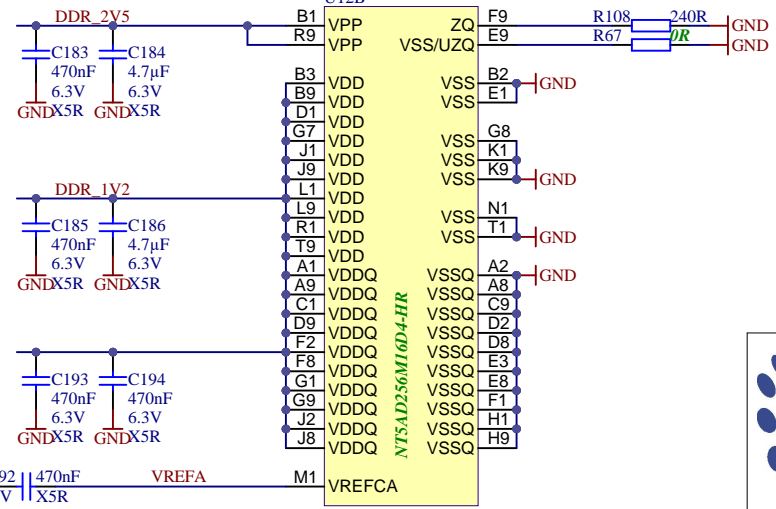
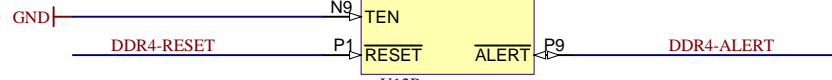
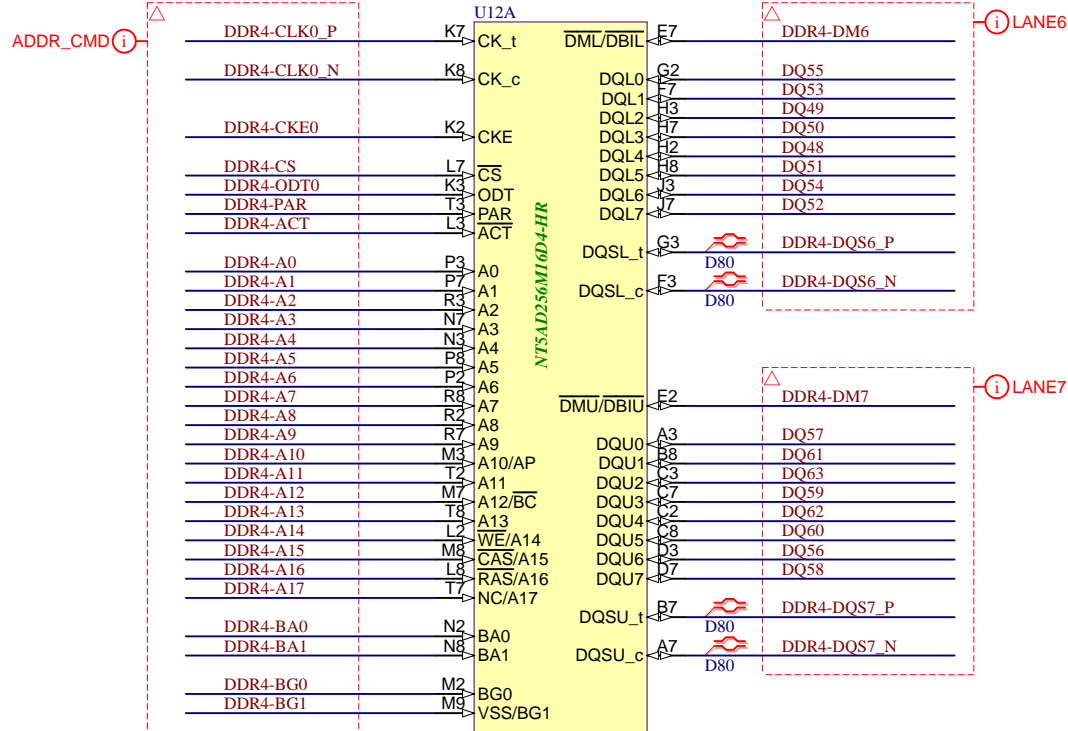
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A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page20 of 30
Filename: DDR4-RAM.SchDoc		



Title: TE0803 - DDR4_2_RAM		
A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page21 of 30
Filename: DDR4-RAM_2.SchDoc		



Title: TE0803 - DDR4_3_RAM		
A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 22 of 30
Filename: DDR4-RAM_3.SchDoc		



Title: TE0803 - DDR4_4_RAM		
A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page23 of 30
Filename: DDR4-RAM_4.SchDoc		

A

A

B

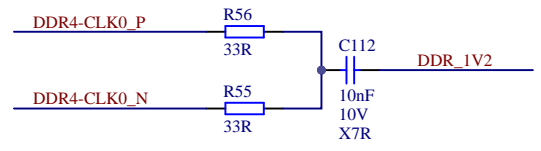
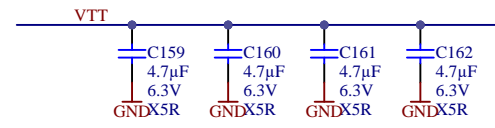
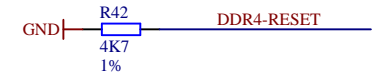
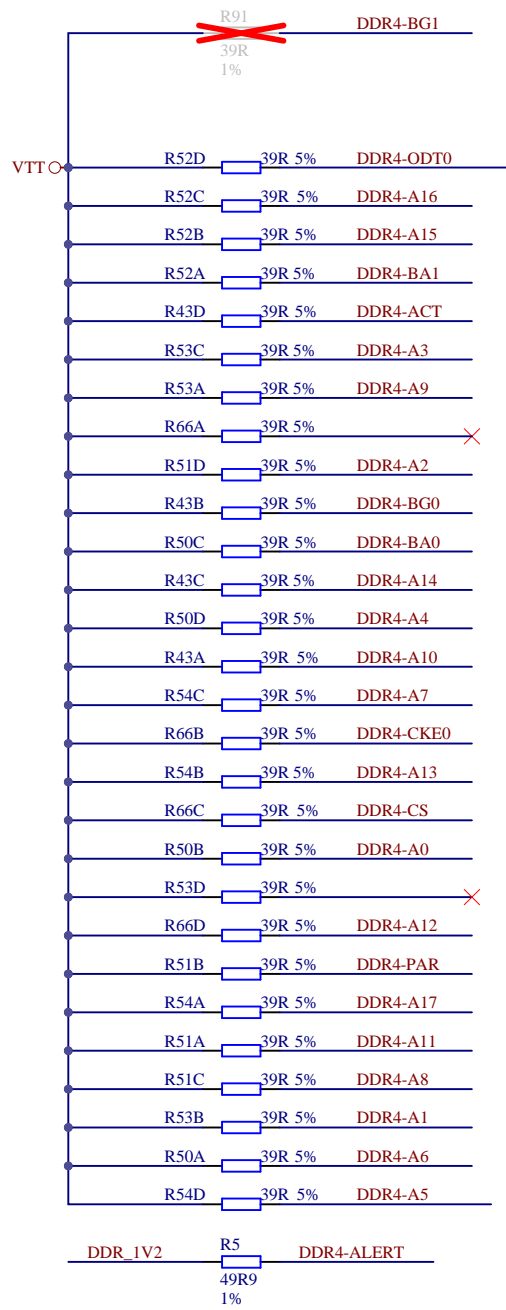
B

C

C

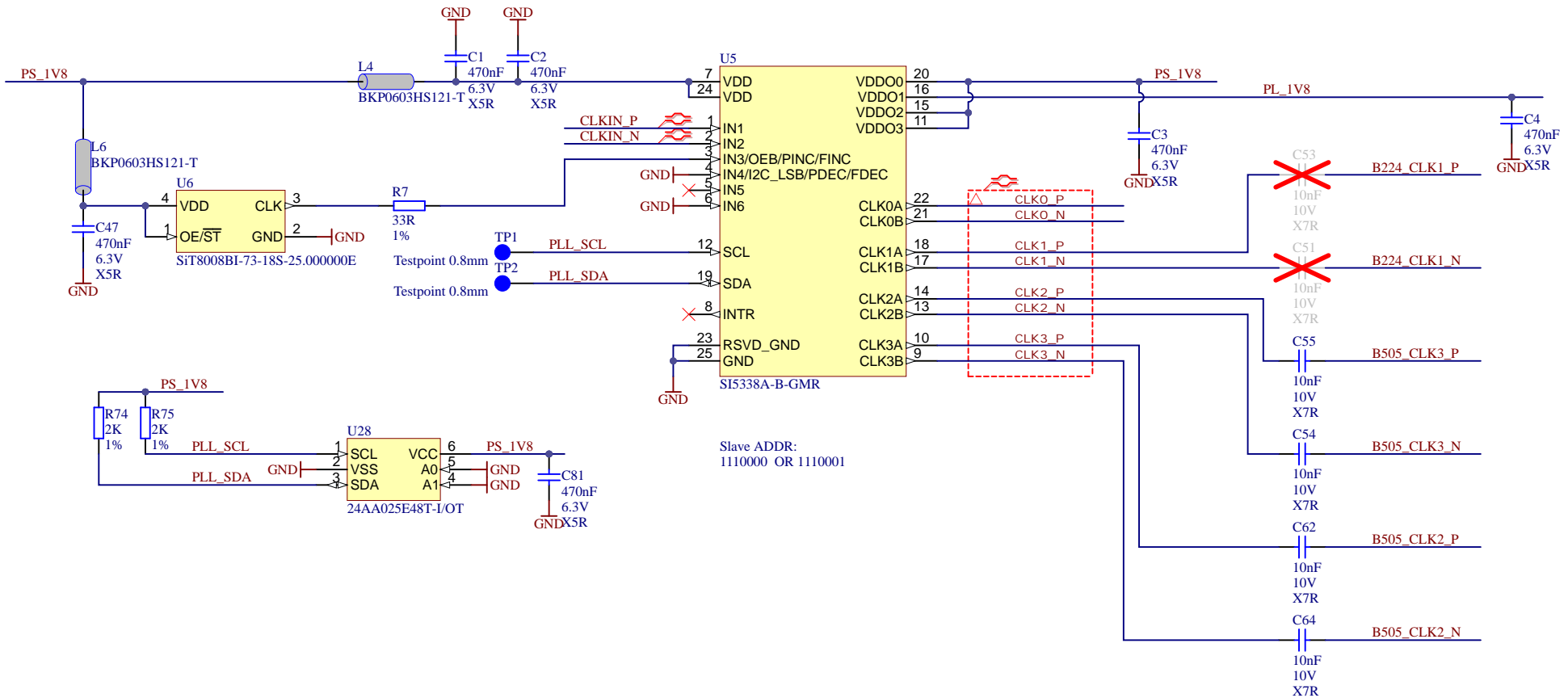
D


D



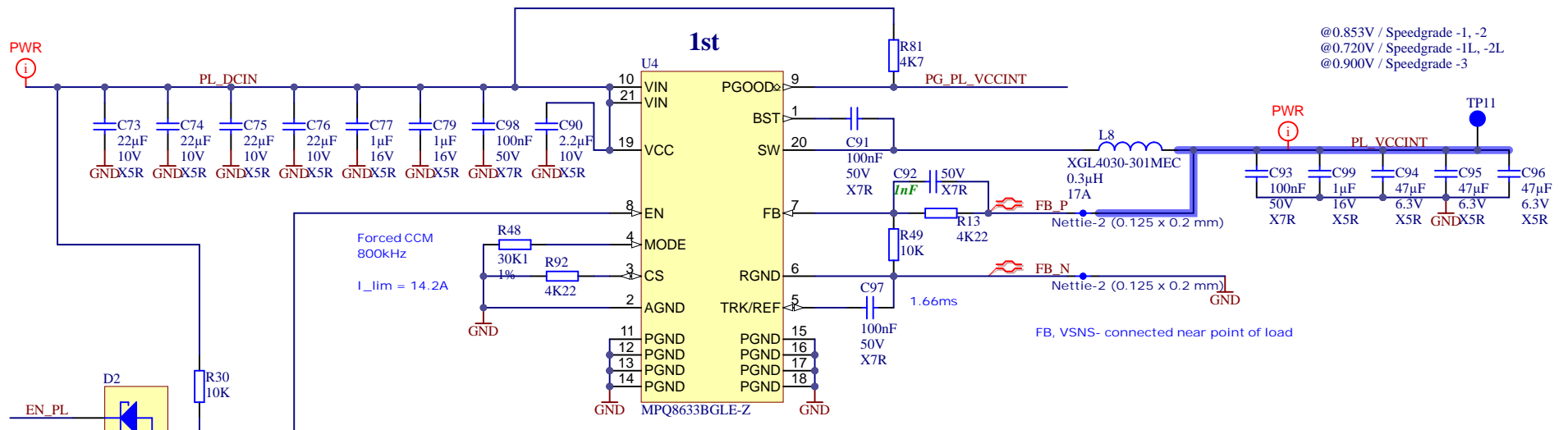
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A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page24 of 30
Filename: DDR4-TERM.SchDoc		





		Title: TE0803 - CLOCK	
		A4	Number: TE0803 2AE11-AZ
Date: 2021-01-19		Copyright: Trenz Electronic GmbH / TT	
Filename: Clock.SchDoc		Page 25 of 30	

# PL VCCINT



@0.853V / Speedgrade -1, -2  
 @0.720V / Speedgrade -1L, -2L  
 @0.900V / Speedgrade -3

Forced CCM  
 800kHz  
 I\_lim = 14.2A

FB, VSNS- connected near point of load

FPGA Speed grade:		
-1L1 / -2LE	R13 - 2K, R49 - 10K	PL_VCCINT = 0.720V
-1 / -2	R13 - 4K22, R49 - 10K	PL_VCCINT = 0.853V
-3E	R13 - 10K, R49 - 20K	PL_VCCINT = 0.900V

U4 pin compatible with  
 -- TPS548A28 (15A)  
 -- TPS548B28 (20A)  
 -- TPS54JA20 (12A)  
 -- MPQ8633B (20A)

**U4 can be either TPS548A28RWW or MPQ8633BGL-E-Z which is up to Trenz Electronic GmbH.**

	Title: TE0803 - POWER	
	A4	Number: TE0803 2AE11-AZ
	Date: 2021-01-19	Rev. 04
	Copyright: Trenz Electronic GmbH / TT	Page 26 of 30
Filename: POWER.SchDoc		

1

2

3

4

A

A

B

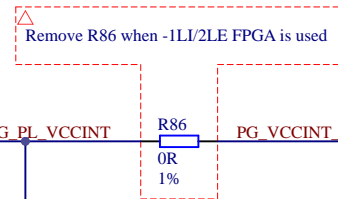
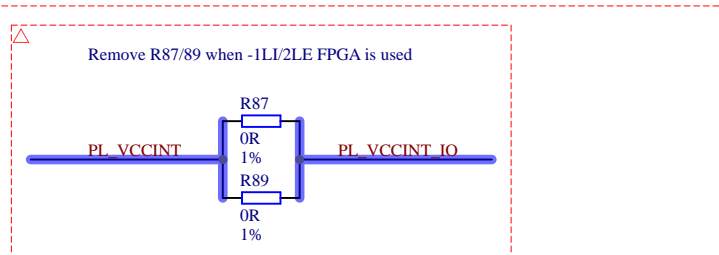
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C

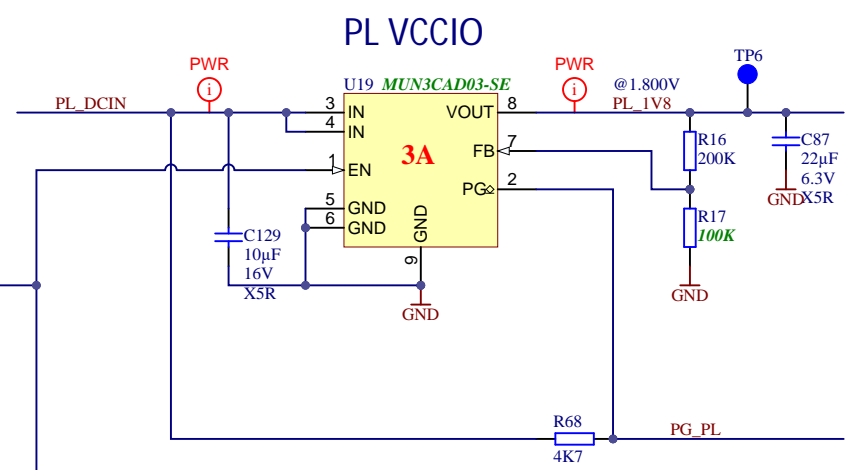
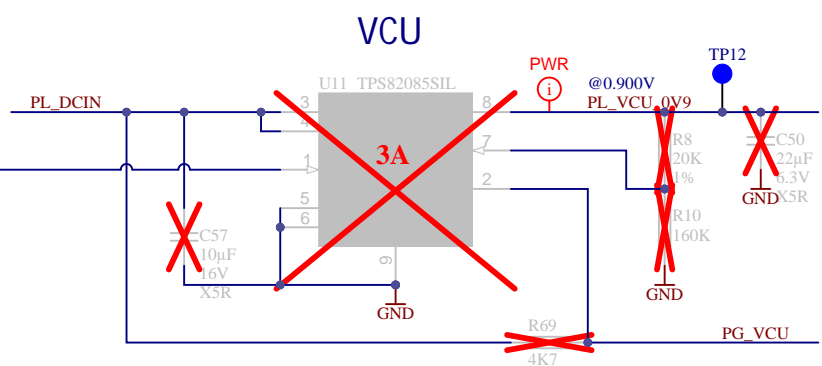
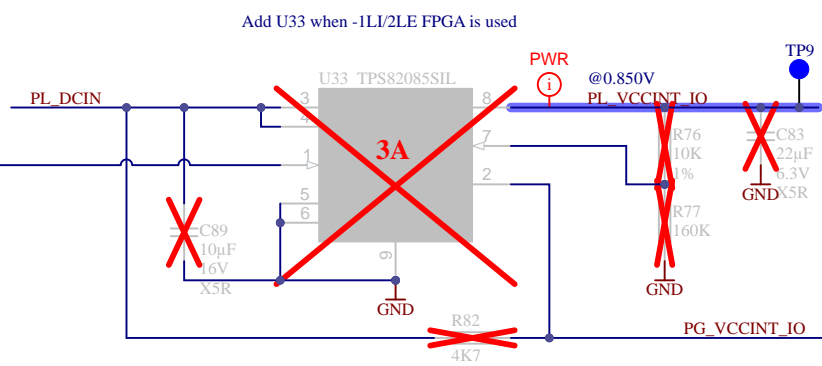
C

D

D



### VCCINT\_IO & VCCBRAM



Title: TE0803 - POWER		
A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 27 of 30
Filename: POWER_1.SchDoc		

1

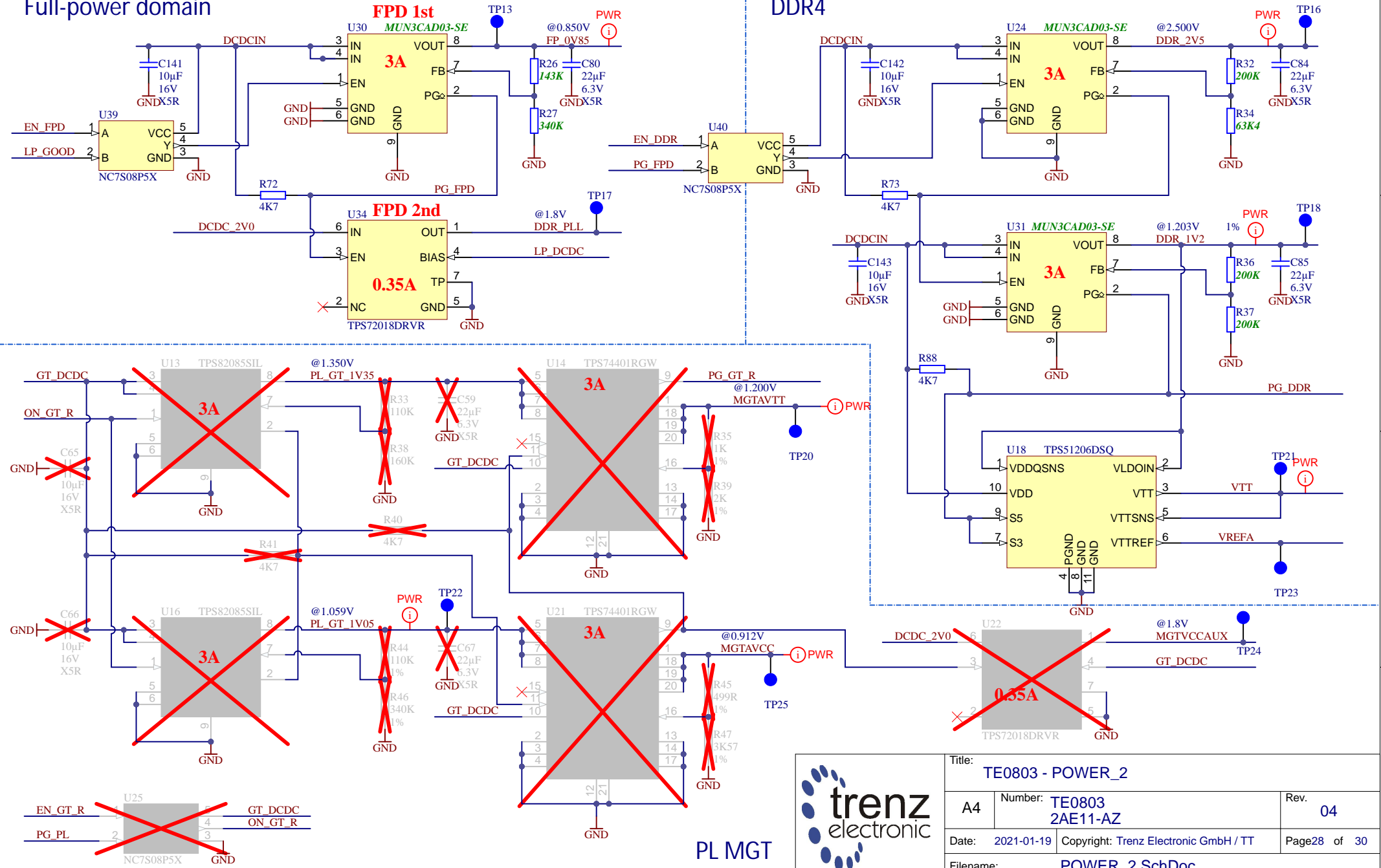
2

3

4

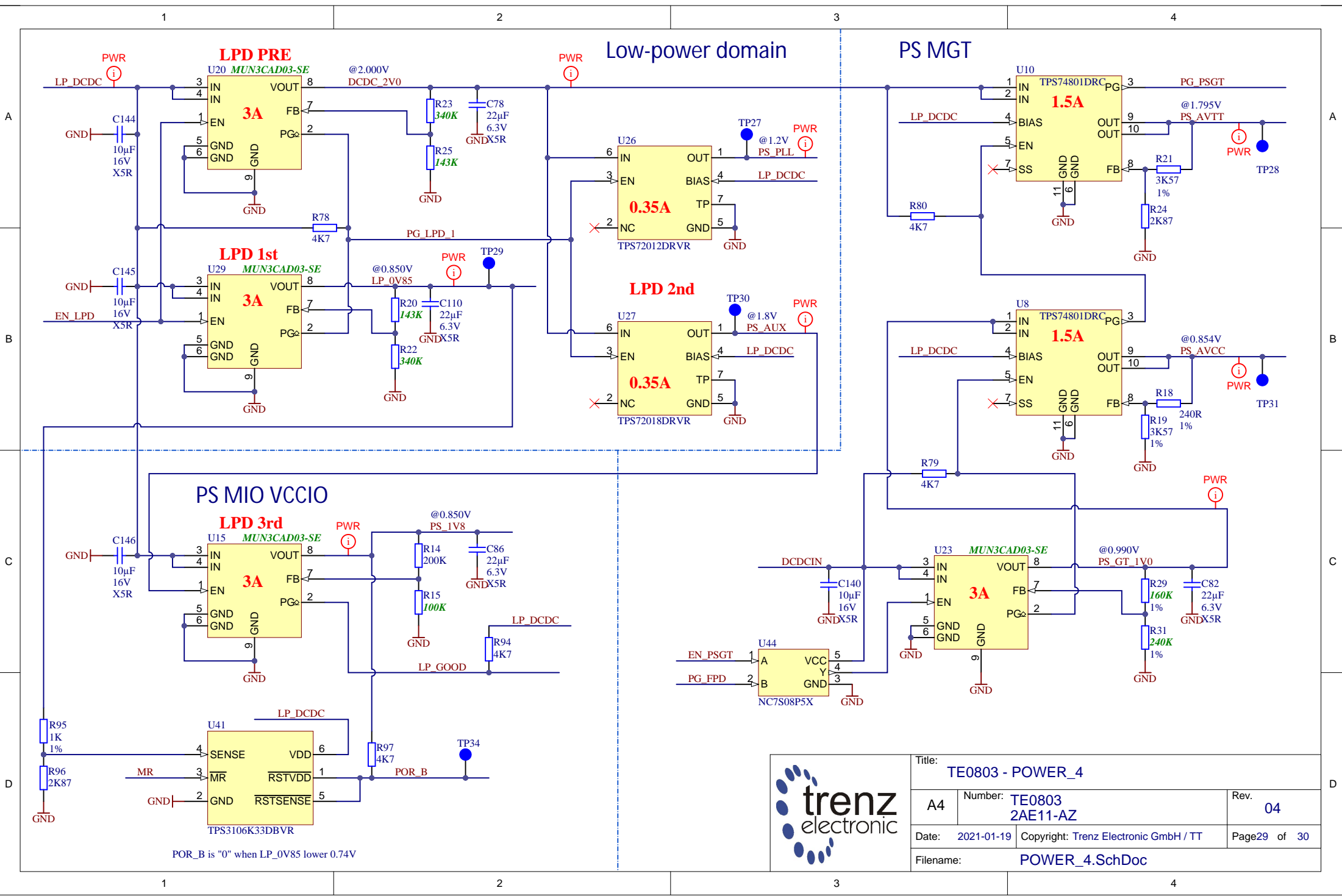
# Full-power domain

# DDR4



Title: <b>TE0803 - POWER_2</b>		
A4	Number: <b>TE0803 2AE11-AZ</b>	Rev. <b>04</b>
Date: <b>2021-01-19</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>28</b> of <b>30</b>
Filename: <b>POWER_2.SchDoc</b>		

PL MGT




POR\_B is "0" when LP\_0V85 lower 0.74V



Title: TE0803 - POWER_4		
A4	Number: TE0803 2AE11-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 29 of 30
Filename: POWER_4.SchDoc		

REV	DATE	Description	
-01		Initial revision	VT
-01a	20.11.2017	1. VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9;	VT
-02	20.06.2018	1. Added LDO to DDR_PLL 2. All differential pairs with length matched with tolerance 0.1mm (excluding package delays) 3. Added MAC EEPROM U28 4. VPS_MGTRAVCC set to 0.85V 5. Added pull-up resistors R68,R69	VT
-03	21.02.2019	1. Added support of DDP DDR4 2. Added support of Low power FPGA (-L1/L2). 3. Revised testpoints 4. Revised J1-J4 connectors net label style	VY
-04	15.12.2020	1. Revised PL_VCCINT power supply. EN63A0QI replaced by TPS548A28RWWR. PCB: revised routing and components placement; 2. Added support of wide SDRAM DDR4 packages. PCB: revised routing and components placement; 3. Added option to select POR_OVERRIDE level (R12 and R93) 4. VCCO pins if unused Bank 44 connected together. Same for unused Bank 24 (UG583 recommendation) 5. PCB: updated signal trace lengths. 6. PCB: updated silkscreen. Added company address, CE and WEEE symbols; 7. PCB: added module orientation rectangle pointer 8. Changed resistors value of R29, R31, R35, R39, R44-R47 (BOM optimization) 9. Removed traceability part (Obsolete component)	VY
-04	23.02.2022	10. Changed capacitor C92 for all variants from 100 nF to 1 nF.	ED
-04	08.06.2023	11. U4 can be either TPS548A28RWWR or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.	VY

				Title: <b>TE0803 - Revision History</b>	
				A4	Number: <b>TE0803 2AE11-AZ</b>
Date: <b>2021-01-19</b>		Copyright: <b>Trenz Electronic GmbH</b>		Page <b>30</b> of <b>30</b>	
Drawn by: <b>VY</b>			Filename: <b>Revision Changes.SchDoc</b>		