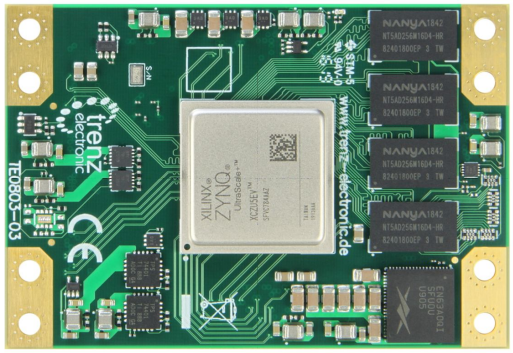

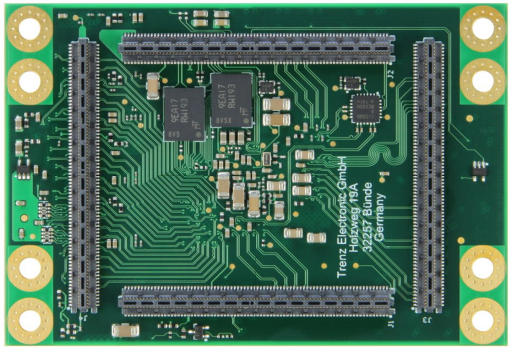

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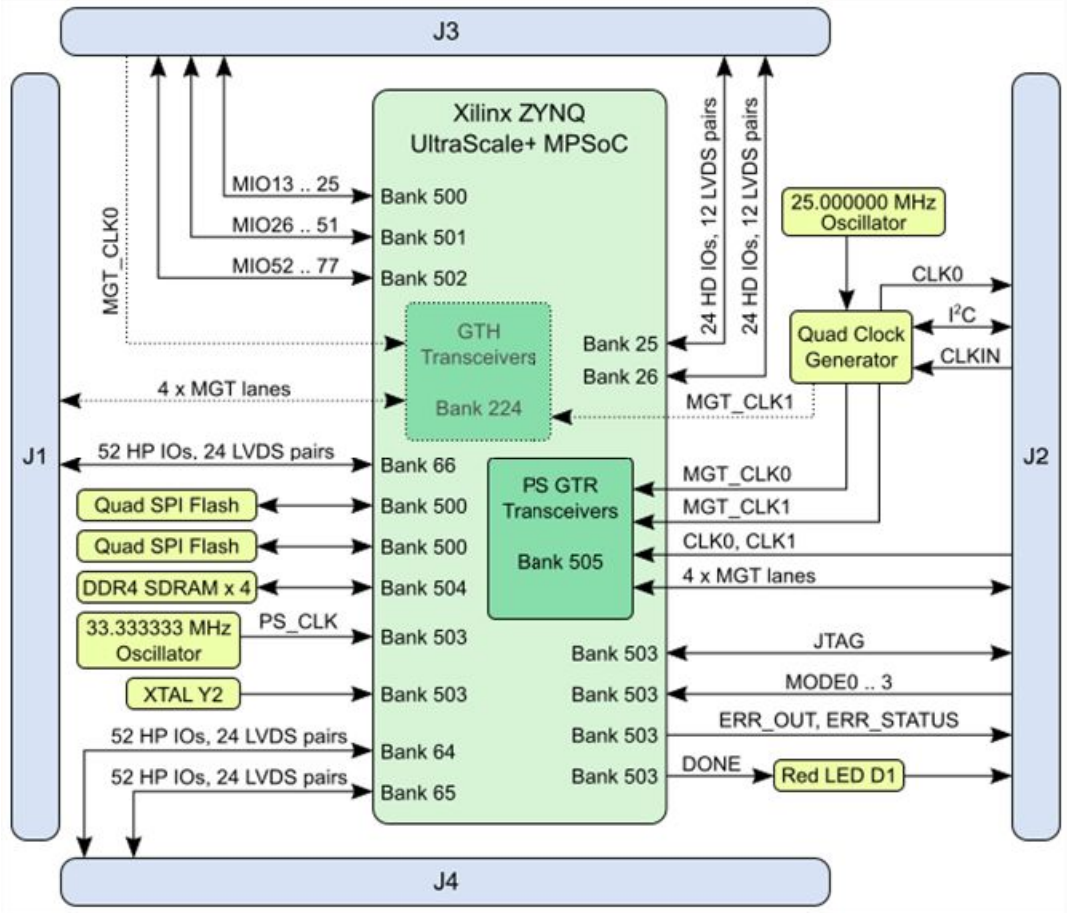
Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TE0803		
	A4	Number: TE0803 5DI21-A	Rev. 04
	Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 1 of 30
	Filename: Legal Notices Modules.SchDoc		



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Title: TE0803 - System Overview		
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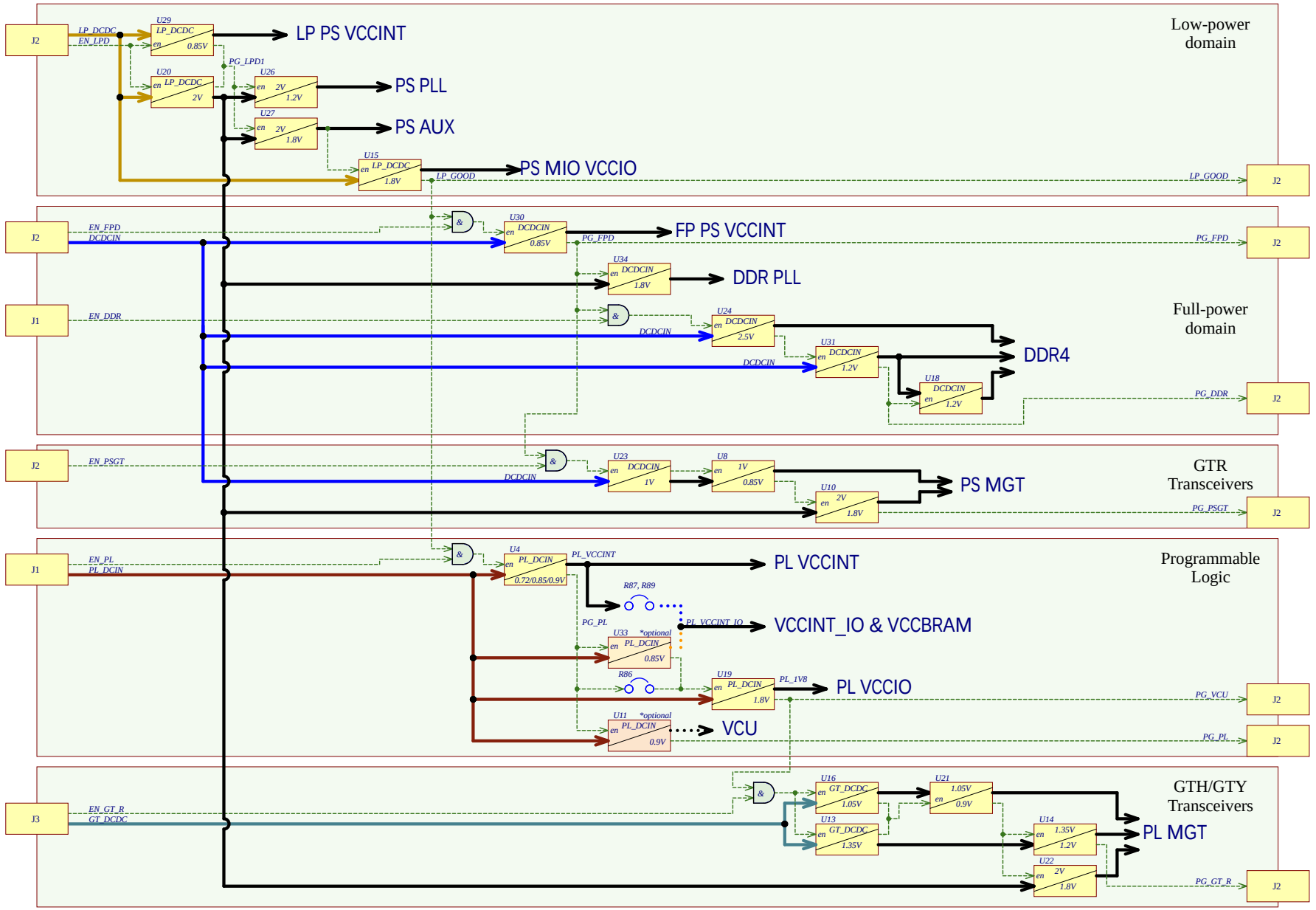
Date: 2021-01-19	Copyright: 2015 Trenz Electronic GmbH	Page 2 of 30
Filename: TE0803-Overview.SchDoc		



EN_GT_R — Net name

Power bus

Control signal

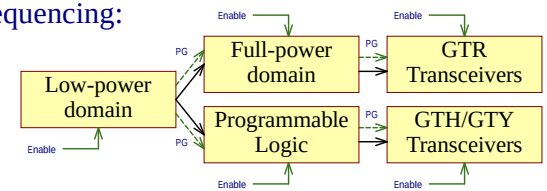
Power bus in FPGA speedgrade -1/-2/-3 assembly variants

Power bus in FPGA speedgrade -1L/-2L assembly variants (low power)

PL_DCIN 0.9V — Optional power converter

& — Logic AND gate

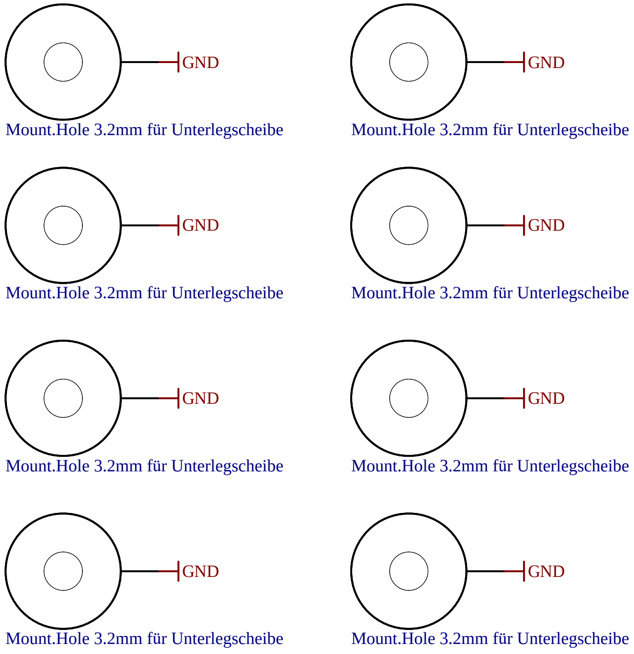
Power-on sequencing:

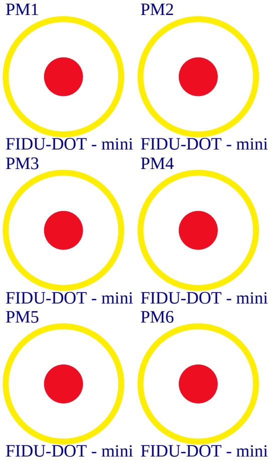


Title: TE0803 - Power Diagram			
A3	Nummer: TE0803 5DI21-A		Rev. 04
Datum: 2021-01-19	Copyright:Trenz Electronic GmbH / TT		Page 3 of 30
Filename: Power_Diagram.SchDoc			

U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_LN Legal Notices Modules.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_1 POWER_1.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_REV_CH Revision Changes.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	U_OVERVIEW TE0803-Overview.SchDoc
U_PD Power_Diagram.SchDoc	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

Special notes:





MECH1
TE Address Overlay
LOGO ADDRESS

LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial
Serial
Serialnumber 6,3 x 6.3mm

Assembly variant	5DI21-A
Created by	
Modified by	
Modified at	
SVN Revision	11196

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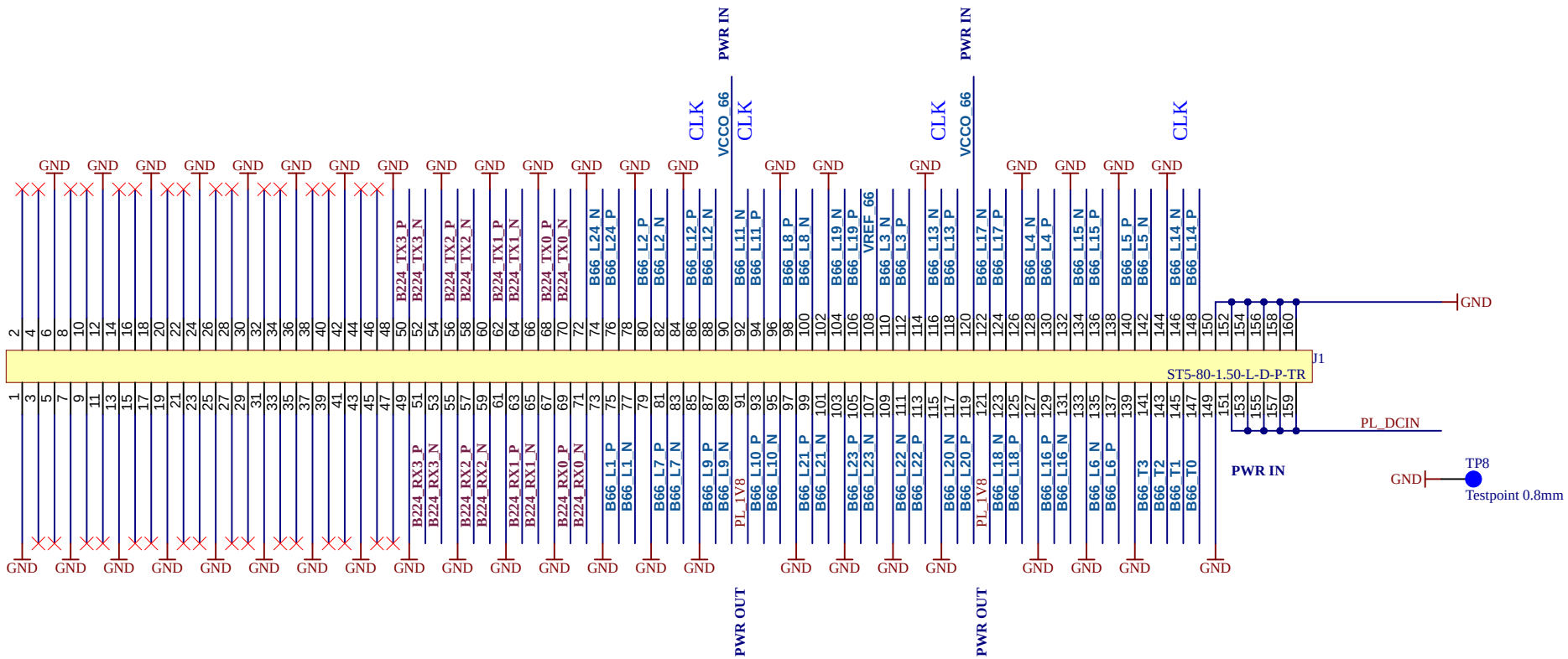
Title: TE0803			
A4	Number: TE0803 5DI21-A		Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page4 of 30
Filename: TE0803.SchDoc			



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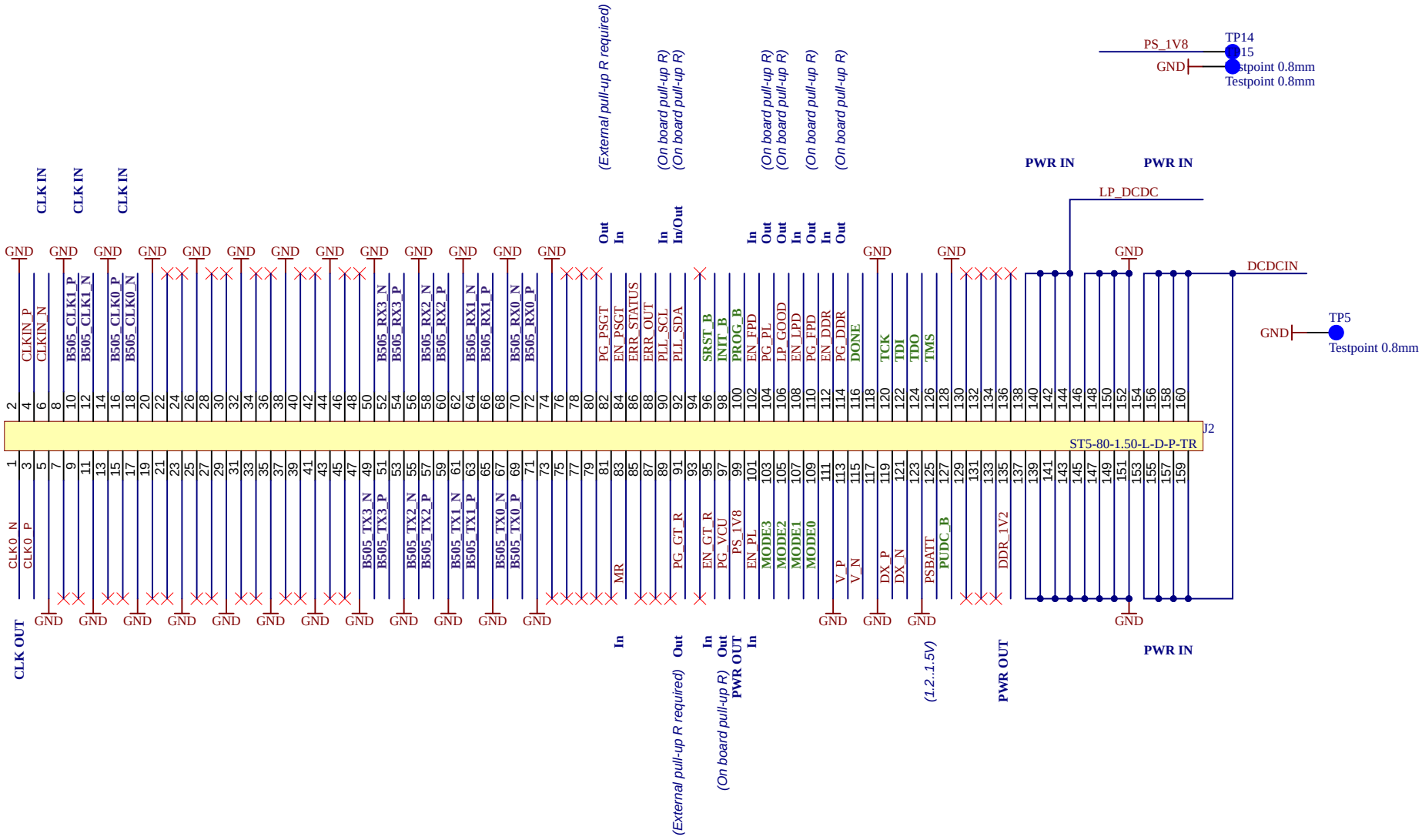
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page5 of 30
Filename: J1.SchDoc			



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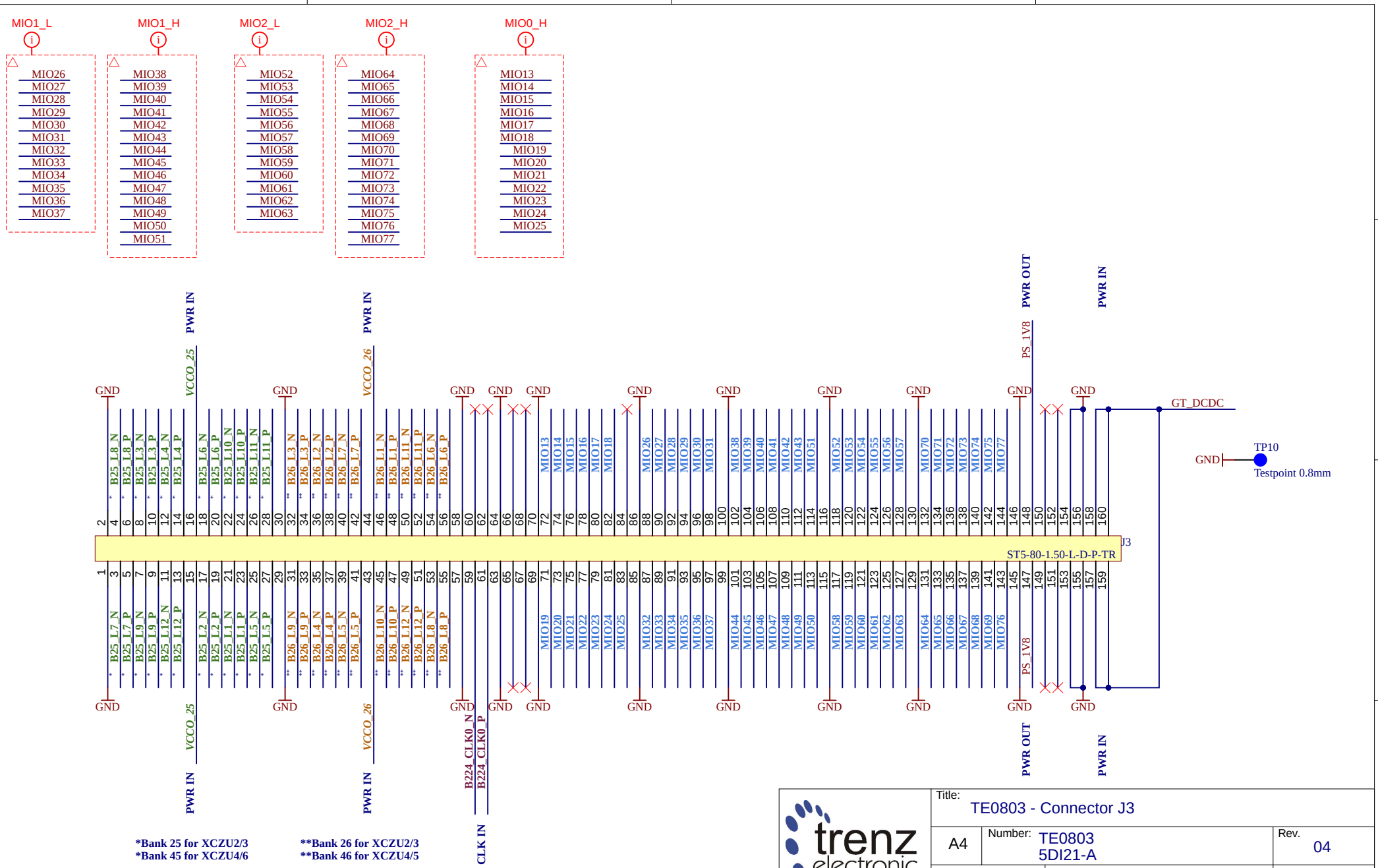
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page6 of 30
Filename: J2.SchDoc			



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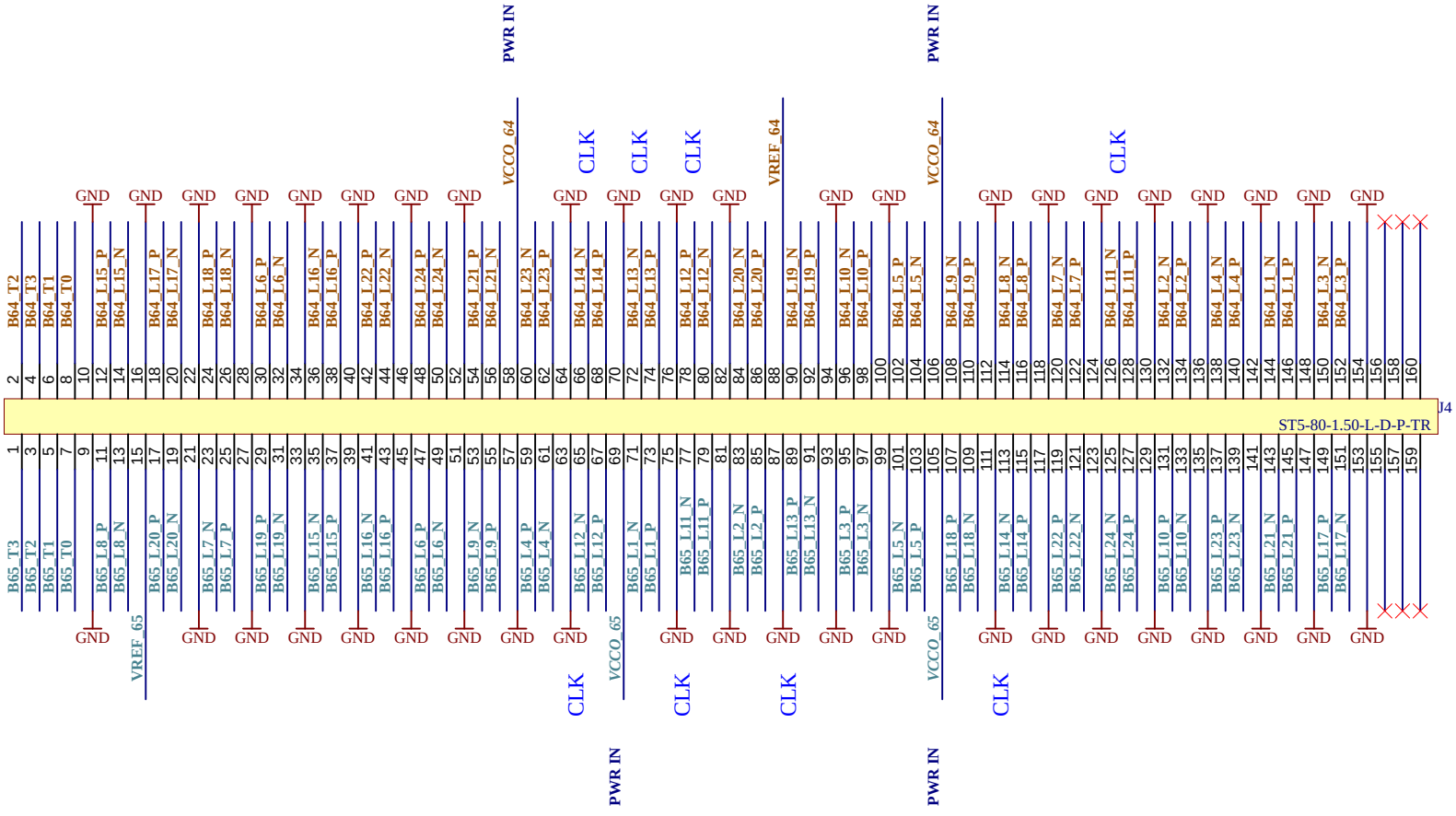
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page7 of 30
Filename: J3.SchDoc			



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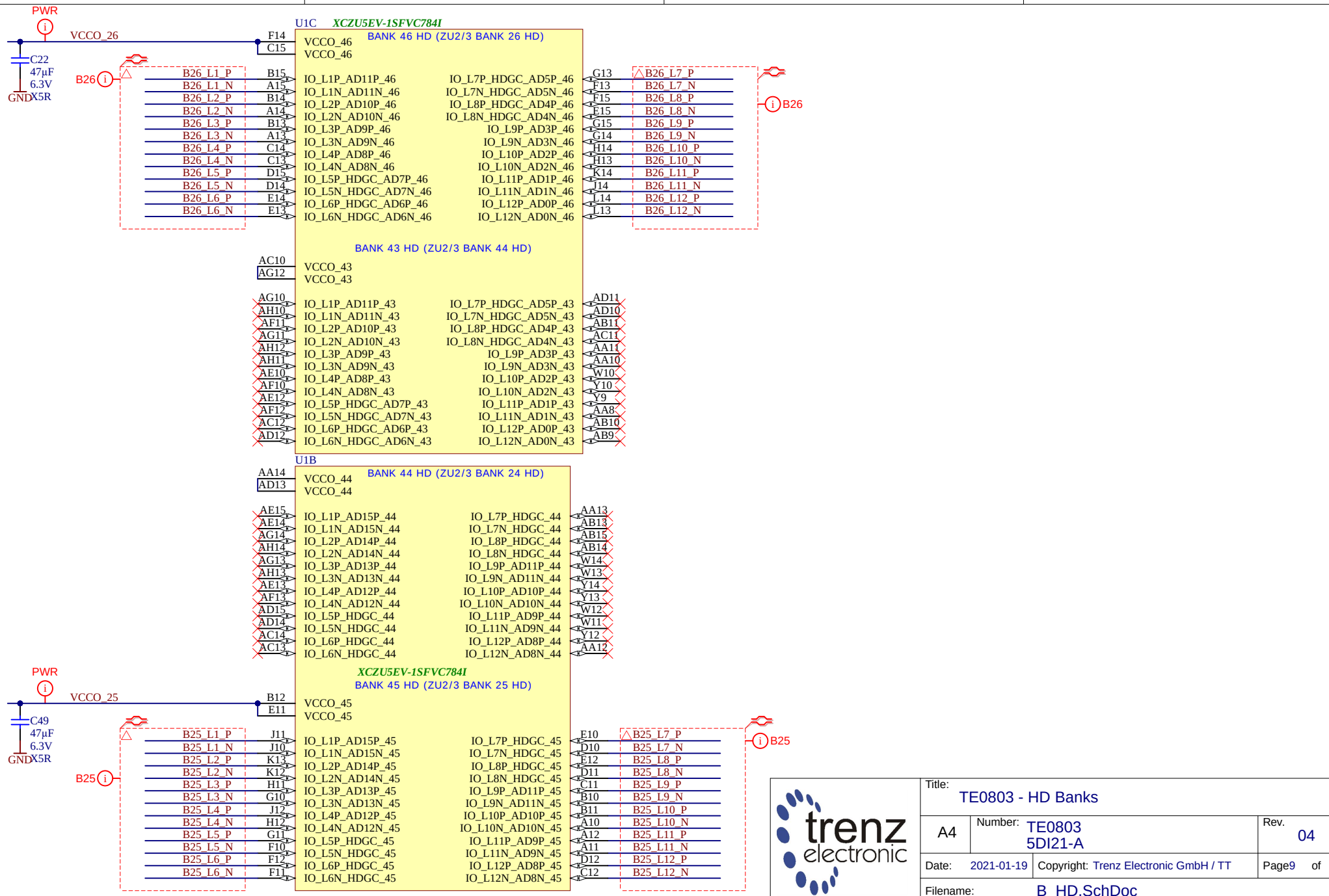
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page 8 of 30
Filename: J4.SchDoc			


PWR
VCCO_26
C22
47µF
6.3V
GND X5R
U1C
XCZU5EV-1SFVC784I
BANK 46 HD (ZU2/3 BANK 26 HD)
VCCO_46
VCCO_46
IO_L1P_AD11P_46
IO_L1N_AD11N_46
IO_L2P_AD10P_46
IO_L2N_AD10N_46
IO_L3P_AD9P_46
IO_L3N_AD9N_46
IO_L4P_AD8P_46
IO_L4N_AD8N_46
IO_L5P_HDGC_AD7P_46
IO_L5N_HDGC_AD7N_46
IO_L6P_HDGC_AD6P_46
IO_L6N_HDGC_AD6N_46
IO_L7P_HDGC_AD5P_46
IO_L7N_HDGC_AD5N_46
IO_L8P_HDGC_AD4P_46
IO_L8N_HDGC_AD4N_46
IO_L9P_AD3P_46
IO_L9N_AD3N_46
IO_L10P_AD2P_46
IO_L10N_AD2N_46
IO_L11P_AD1P_46
IO_L11N_AD1N_46
IO_L12P_AD0P_46
IO_L12N_AD0N_46
B26_L1_P
B26_L1_N
B26_L2_P
B26_L2_N
B26_L3_P
B26_L3_N
B26_L4_P
B26_L4_N
B26_L5_P
B26_L5_N
B26_L6_P
B26_L6_N
B26_L7_P
B26_L7_N
B26_L8_P
B26_L8_N
B26_L9_P
B26_L9_N
B26_L10_P
B26_L10_N
B26_L11_P
B26_L11_N
B26_L12_P
B26_L12_N
B26
BANK 43 HD (ZU2/3 BANK 44 HD)
VCCO_43
VCCO_43
IO_L1P_AD11P_43
IO_L1N_AD11N_43
IO_L2P_AD10P_43
IO_L2N_AD10N_43
IO_L3P_AD9P_43
IO_L3N_AD9N_43
IO_L4P_AD8P_43
IO_L4N_AD8N_43
IO_L5P_HDGC_AD7P_43
IO_L5N_HDGC_AD7N_43
IO_L6P_HDGC_AD6P_43
IO_L6N_HDGC_AD6N_43
IO_L7P_HDGC_AD5P_43
IO_L7N_HDGC_AD5N_43
IO_L8P_HDGC_AD4P_43
IO_L8N_HDGC_AD4N_43
IO_L9P_AD3P_43
IO_L9N_AD3N_43
IO_L10P_AD2P_43
IO_L10N_AD2N_43
IO_L11P_AD1P_43
IO_L11N_AD1N_43
IO_L12P_AD0P_43
IO_L12N_AD0N_43
U1B
BANK 44 HD (ZU2/3 BANK 24 HD)
VCCO_44
VCCO_44
IO_L1P_AD15P_44
IO_L1N_AD15N_44
IO_L2P_AD14P_44
IO_L2N_AD14N_44
IO_L3P_AD13P_44
IO_L3N_AD13N_44
IO_L4P_AD12P_44
IO_L4N_AD12N_44
IO_L5P_HDGC_44
IO_L5N_HDGC_44
IO_L6P_HDGC_44
IO_L6N_HDGC_44
IO_L7P_HDGC_44
IO_L7N_HDGC_44
IO_L8P_HDGC_44
IO_L8N_HDGC_44
IO_L9P_AD11P_44
IO_L9N_AD11N_44
IO_L10P_AD10P_44
IO_L10N_AD10N_44
IO_L11P_AD9P_44
IO_L11N_AD9N_44
IO_L12P_AD8P_44
IO_L12N_AD8N_44
XCZU5EV-1SFVC784I
BANK 45 HD (ZU2/3 BANK 25 HD)
VCCO_45
VCCO_45
IO_L1P_AD15P_45
IO_L1N_AD15N_45
IO_L2P_AD14P_45
IO_L2N_AD14N_45
IO_L3P_AD13P_45
IO_L3N_AD13N_45
IO_L4P_AD12P_45
IO_L4N_AD12N_45
IO_L5P_HDGC_45
IO_L5N_HDGC_45
IO_L6P_HDGC_45
IO_L6N_HDGC_45
IO_L7P_HDGC_45
IO_L7N_HDGC_45
IO_L8P_HDGC_45
IO_L8N_HDGC_45
IO_L9P_AD11P_45
IO_L9N_AD11N_45
IO_L10P_AD10P_45
IO_L10N_AD10N_45
IO_L11P_AD9P_45
IO_L11N_AD9N_45
IO_L12P_AD8P_45
IO_L12N_AD8N_45
B25_L1_P
B25_L1_N
B25_L2_P
B25_L2_N
B25_L3_P
B25_L3_N
B25_L4_P
B25_L4_N
B25_L5_P
B25_L5_N
B25_L6_P
B25_L6_N
B25_L7_P
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B25_L9_N
B25_L10_P
B25_L10_N
B25_L11_P
B25_L11_N
B25_L12_P
B25_L12_N
B25
PWR
VCCO_25
C49
47µF
6.3V
GND X5R
B25
trenz electronic
Title: TE0803 - HD Banks
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Number: TE0803 5DI21-A
Rev. 04
Date: 2021-01-19
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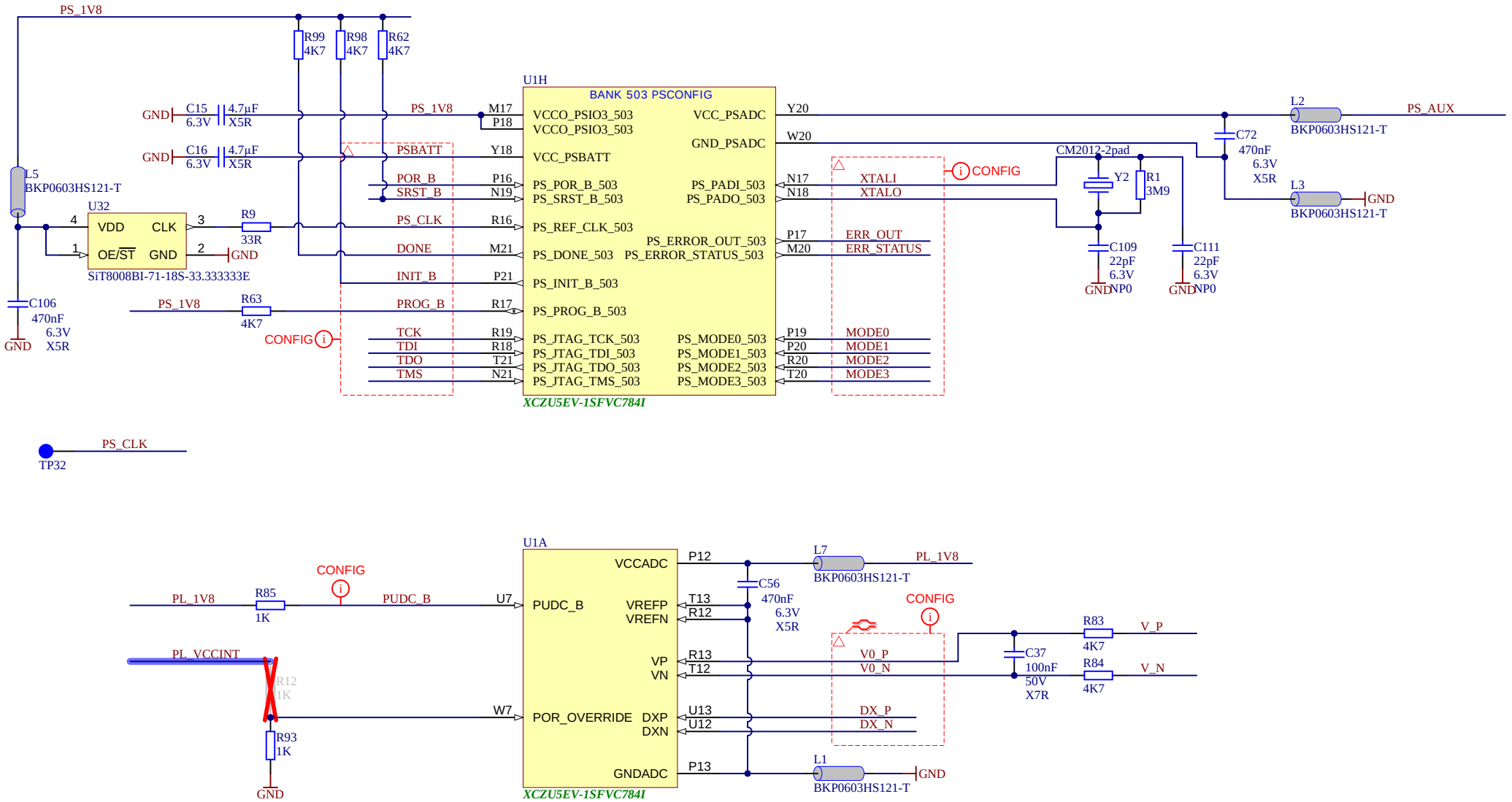
Page9 of 30
Filename: B_HD.SchDoc



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Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page10 of 30
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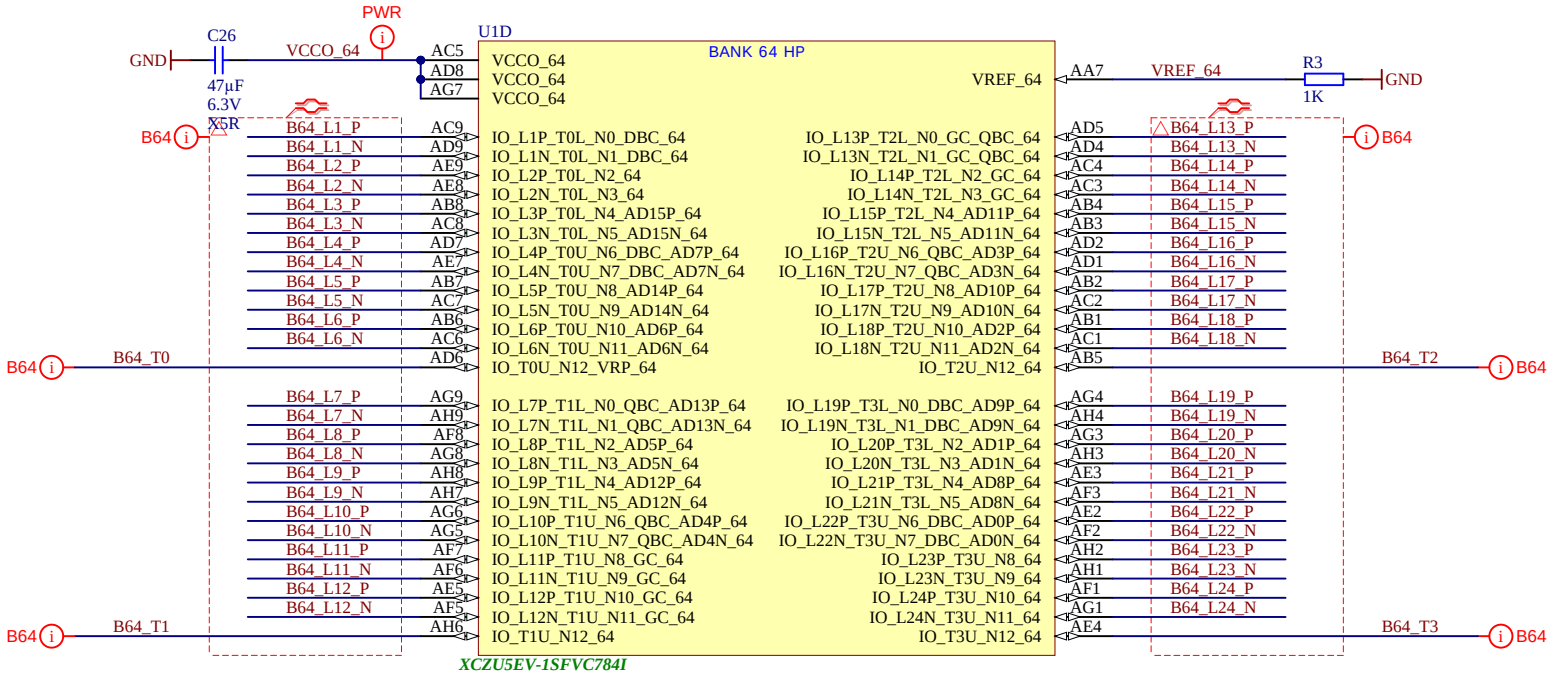

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Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page11 of 30
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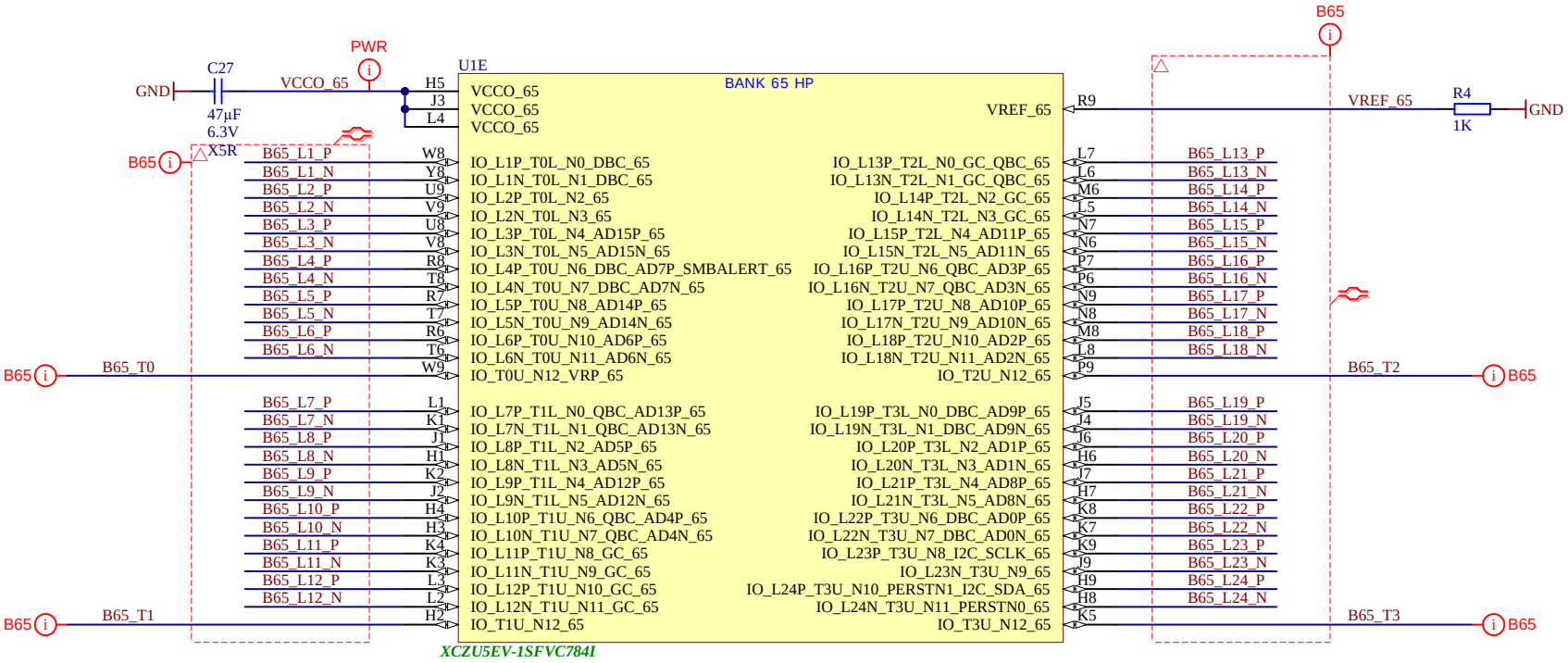

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Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page12 of 30
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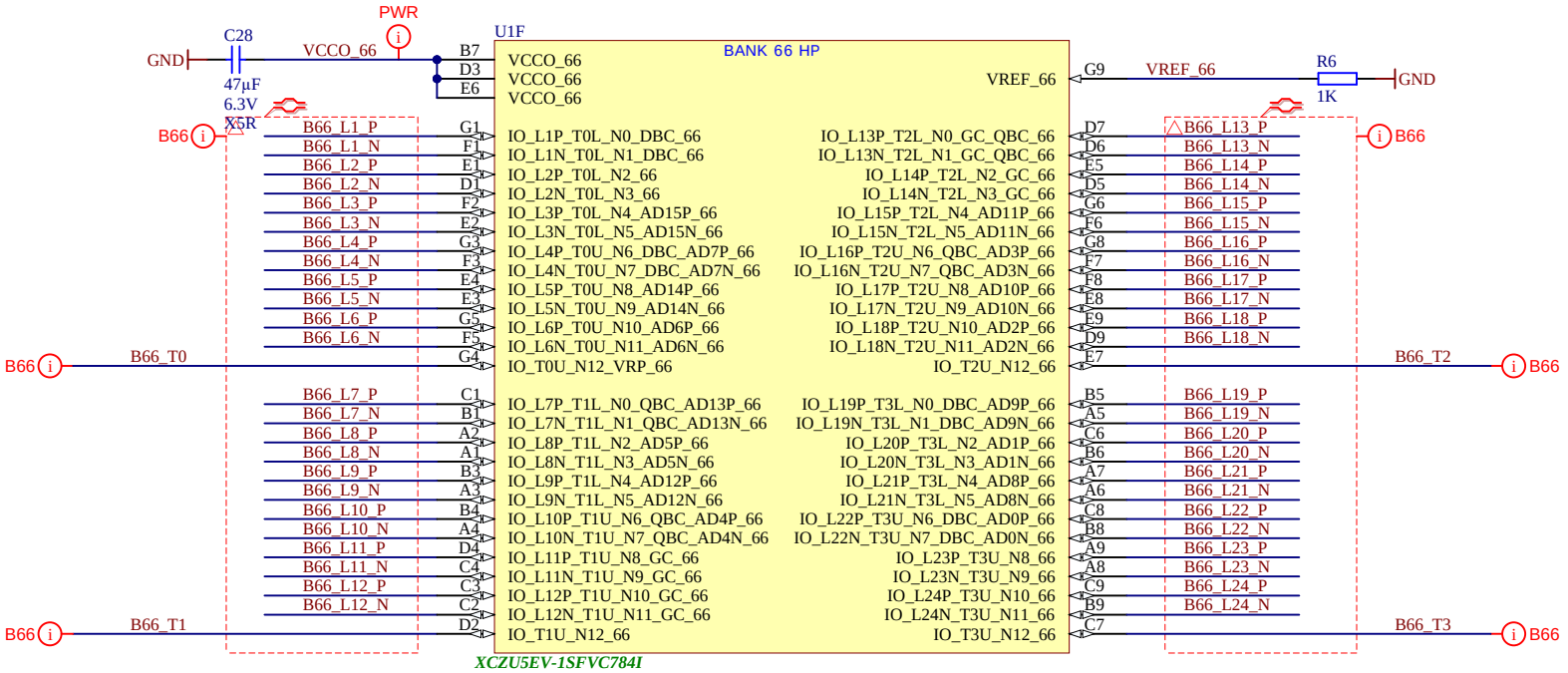

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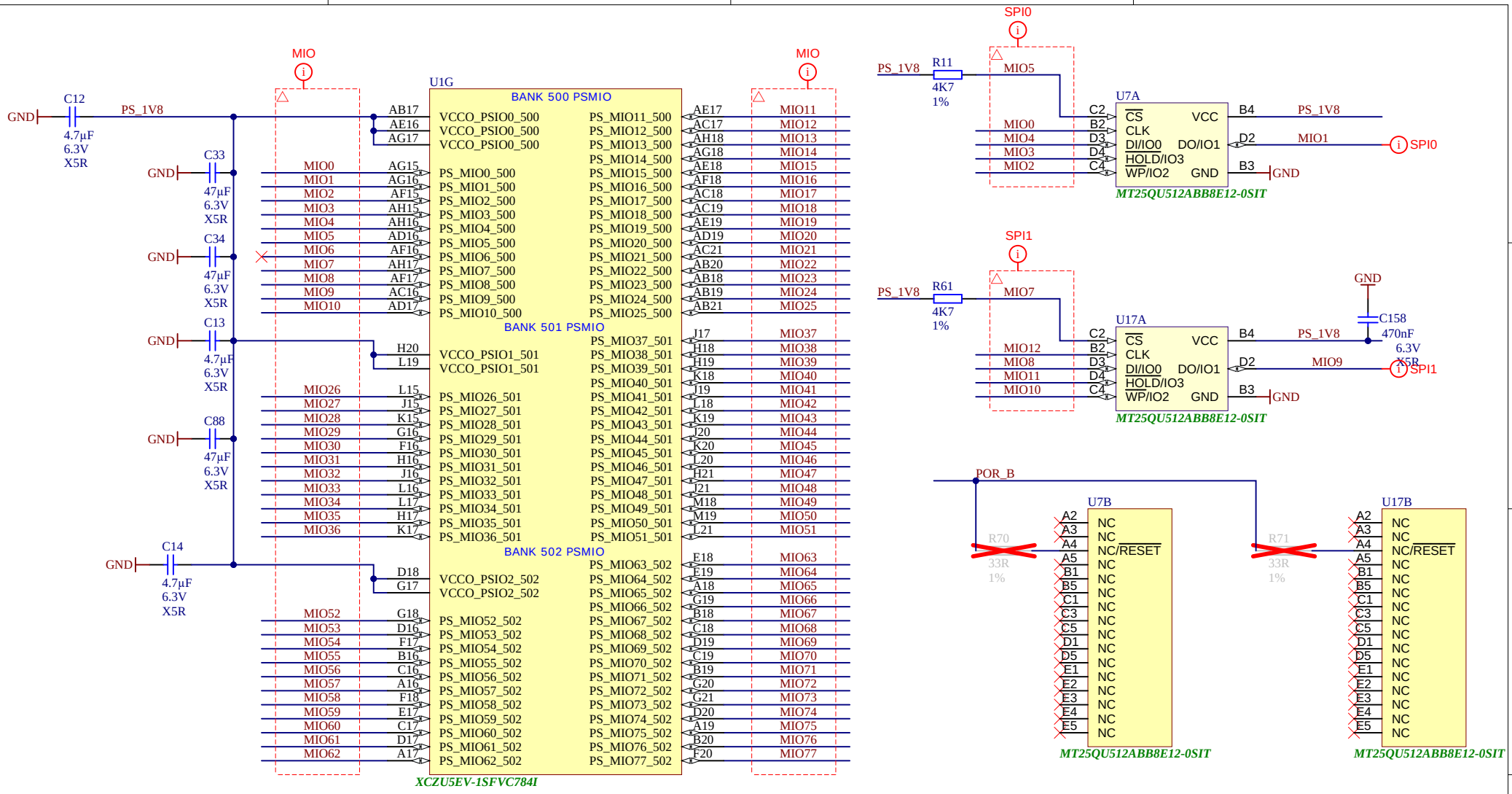
	Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page13 of 30
	Filename: B66.SchDoc		



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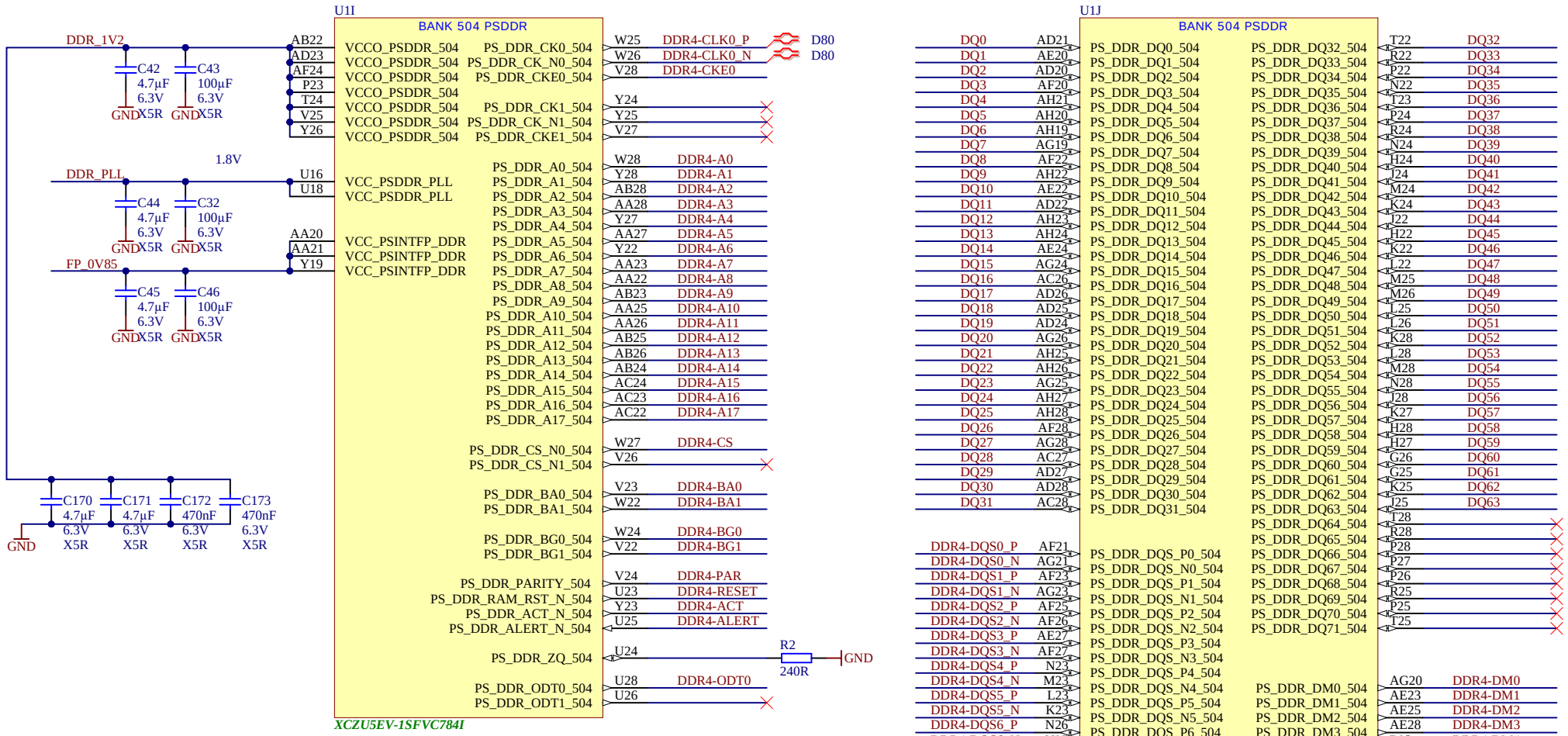
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page14 of 30
Filename: B_MIO.SchDoc			



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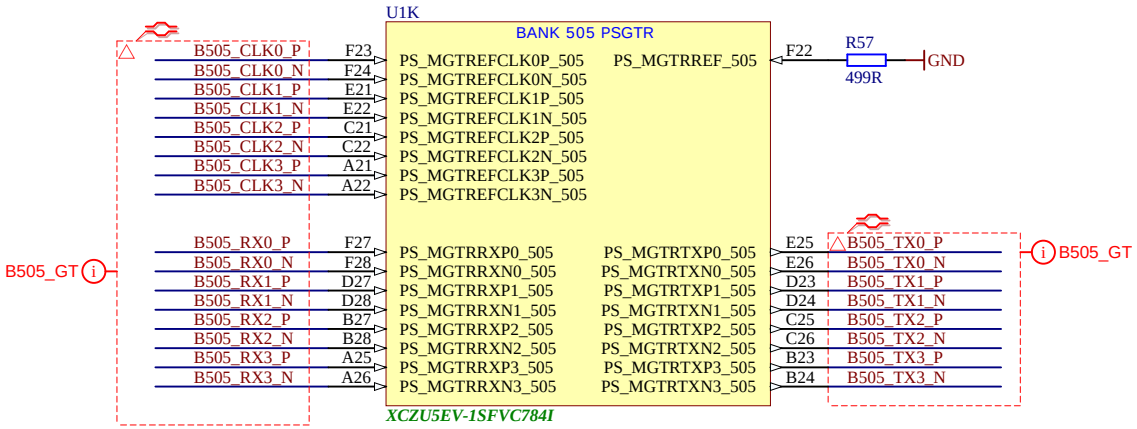
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page15 of 30
Filename: PS_DDR.SchDoc			



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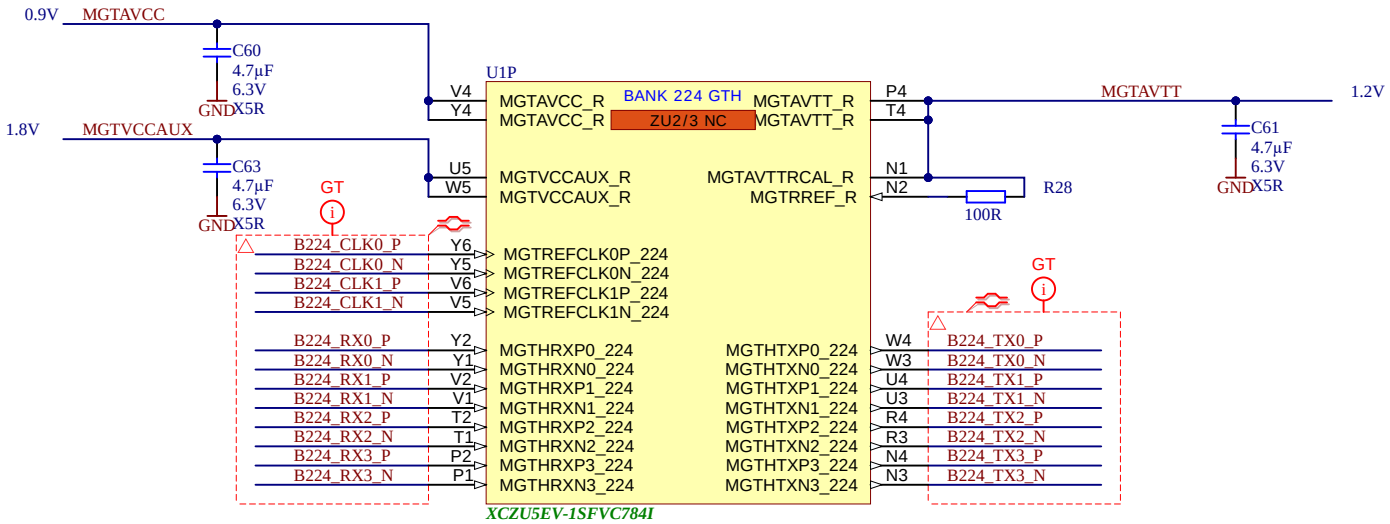

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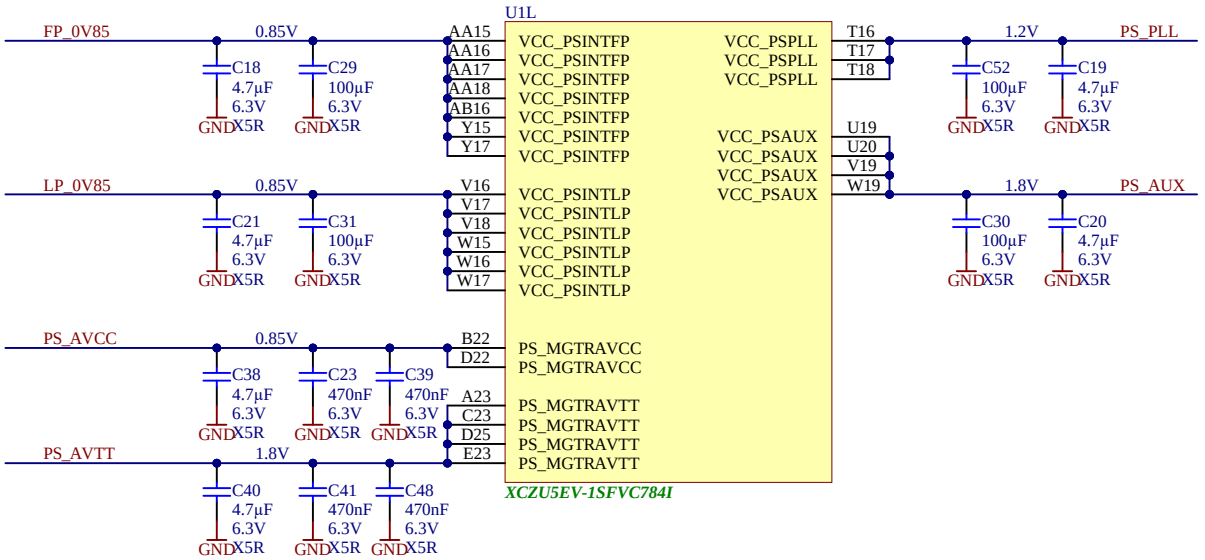

trenz electronic	Title: TE0803 - ZU_PS_POWER		
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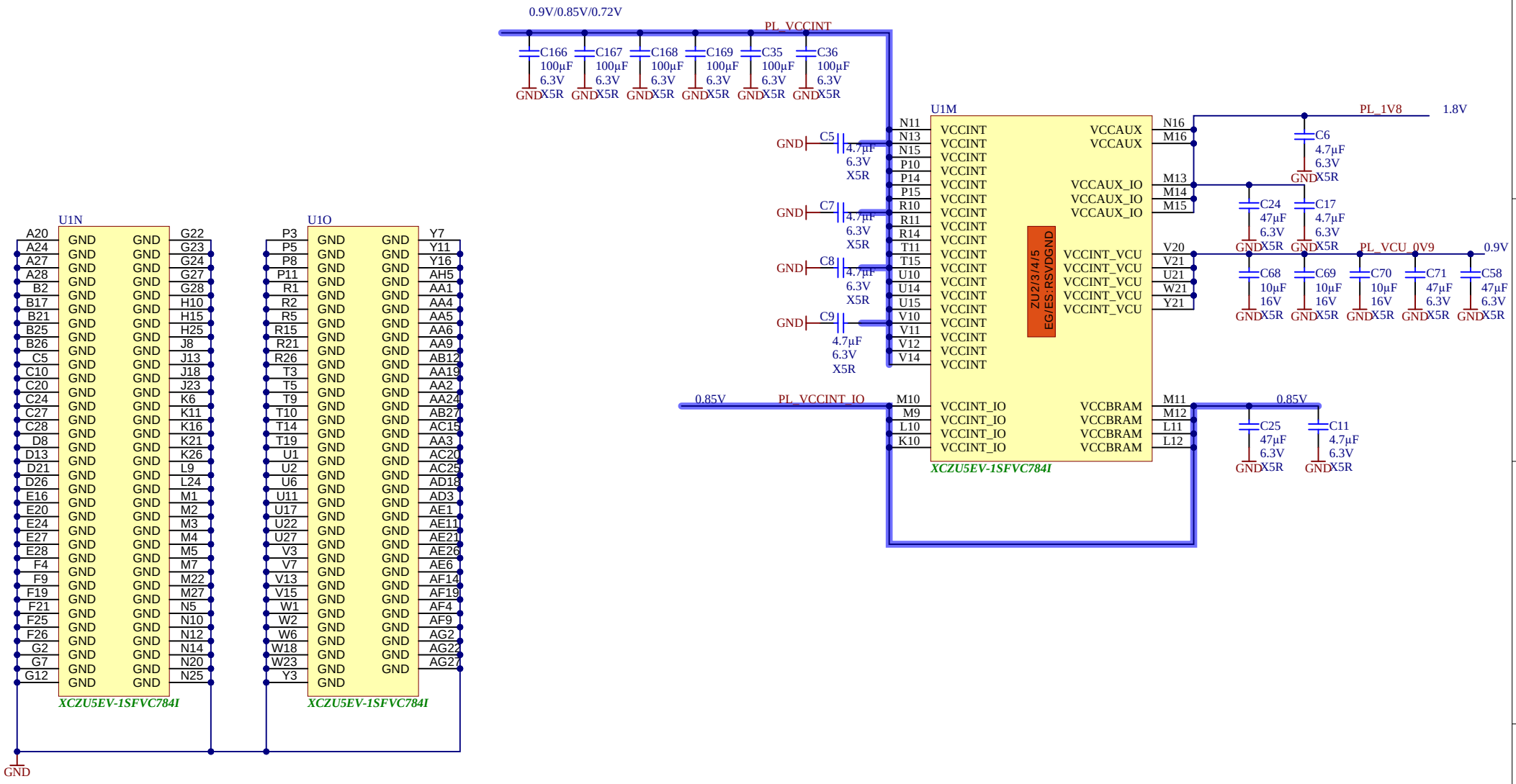
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page18 of 30
Filename: ZU_PS_POWER.SchDoc			



trenz electronic	Title: TE0803 - ZU_POWER		
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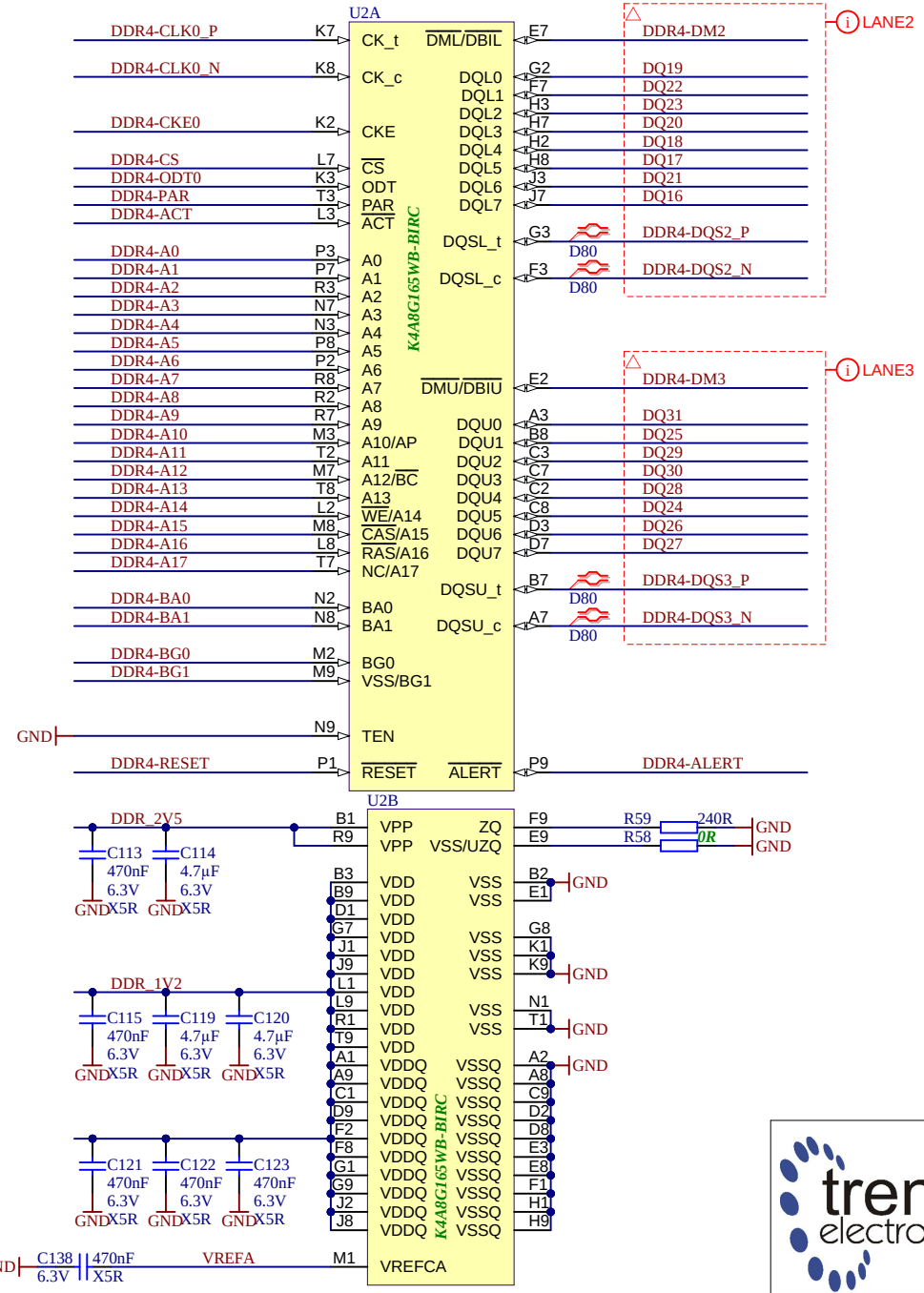
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page19 of 30
Filename: ZU_POWER.SchDoc			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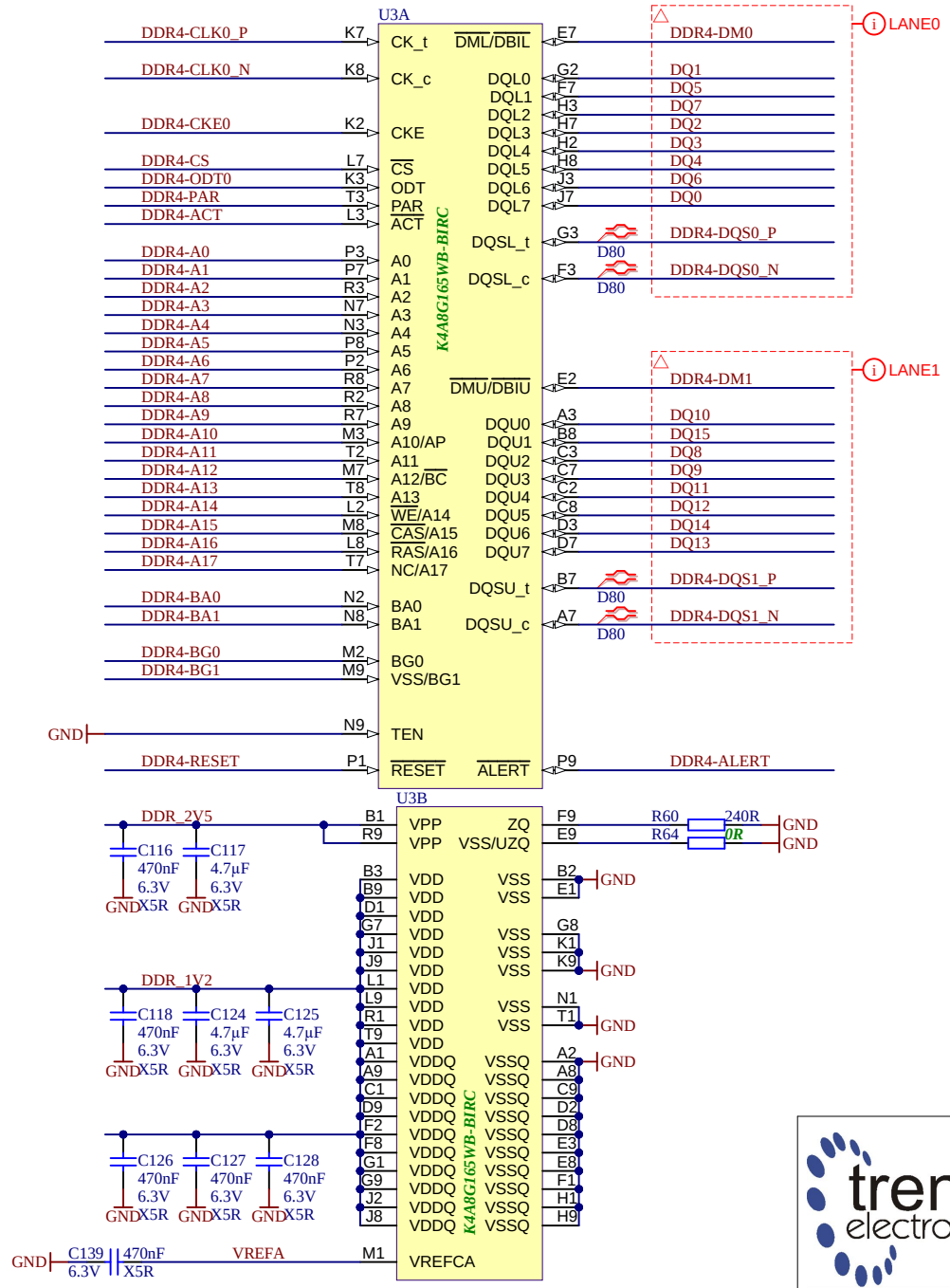
K4A8G165WB-BIRC
DDR4-CLK0_P
DDR4-CLK0_N
DDR4-CKE0
DDR4-CS
DDR4-ODT0
DDR4-PAR
DDR4-ACT
DDR4-A0
DDR4-A1
DDR4-A2
DDR4-A3
DDR4-A4
DDR4-A5
DDR4-A6
DDR4-A7
DDR4-A8
DDR4-A9
DDR4-A10
DDR4-A11
DDR4-A12
DDR4-A13
DDR4-A14
DDR4-A15
DDR4-A16
DDR4-A17
DDR4-BA0
DDR4-BA1
DDR4-BG0
DDR4-BG1
GND
DDR4-RESET
DDR4-DM2
DDR4-DQS2_P
DDR4-DQS2_N
LANE2
DDR4-DM3
DDR4-DQS3_P
DDR4-DQS3_N
LANE3
DDR4-ALERT
D80
U2B
DDR_2V5
DDR_1V2
C113
C114
C115
C119
C120
C121
C122
C123
C138
470nF
4.7µF
6.3V
X5R
R59
R58
240R
0R
VREFA
trenz electronic
Title: TE0803 - DDR4_1_RAM
A4
Number: TE0803 5DI21-A
Rev. 04
Date: 2021-01-19
Copyright: Trenz Electronic GmbH / TT
Page20 of 30
Filename: DDR4-RAM.SchDoc



Title: TE0803 - DDR4_2_RAM			
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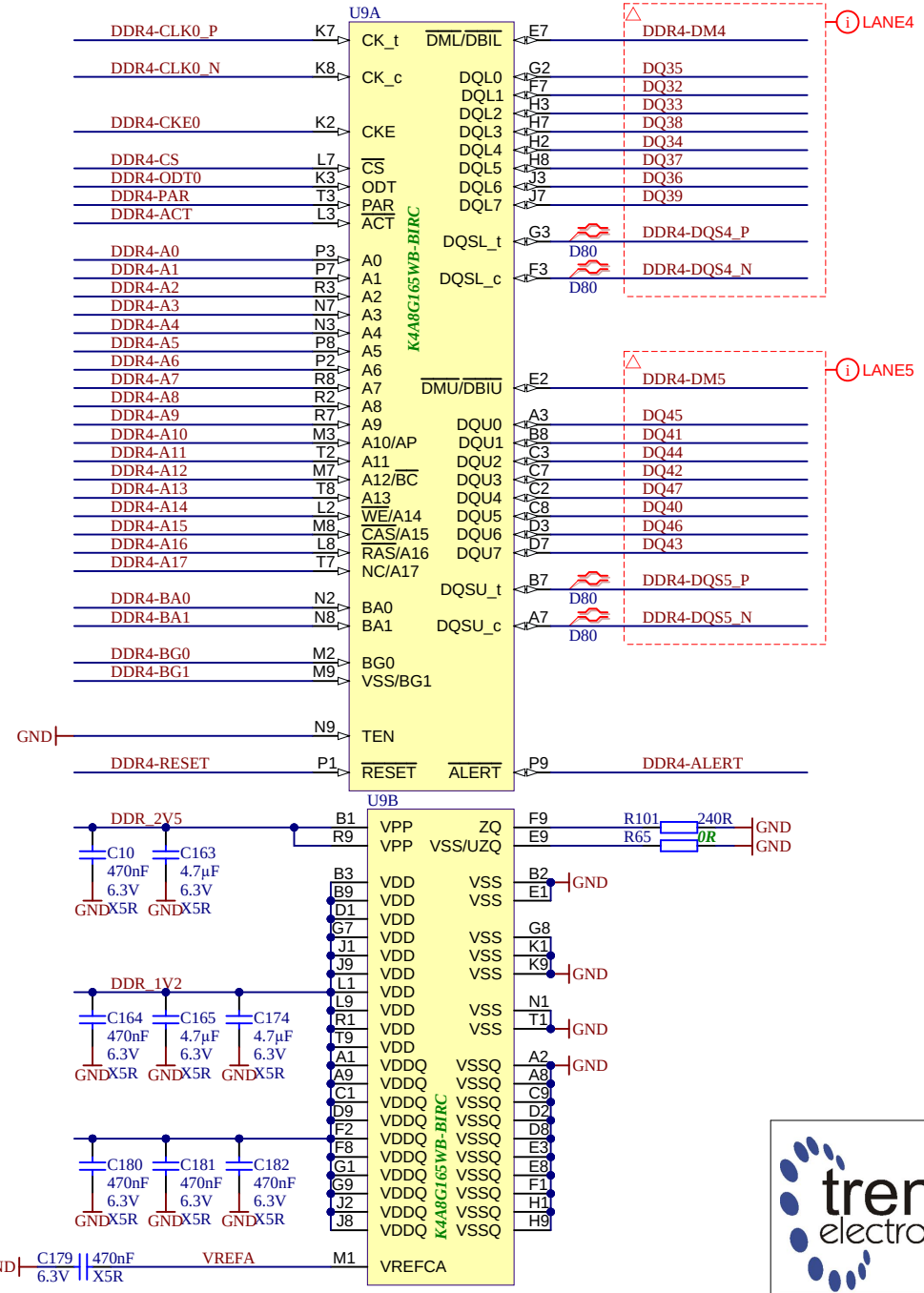
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page21 of 30
Filename: DDR4-RAM_2.SchDoc			



Title: TE0803 - DDR4_3_RAM			
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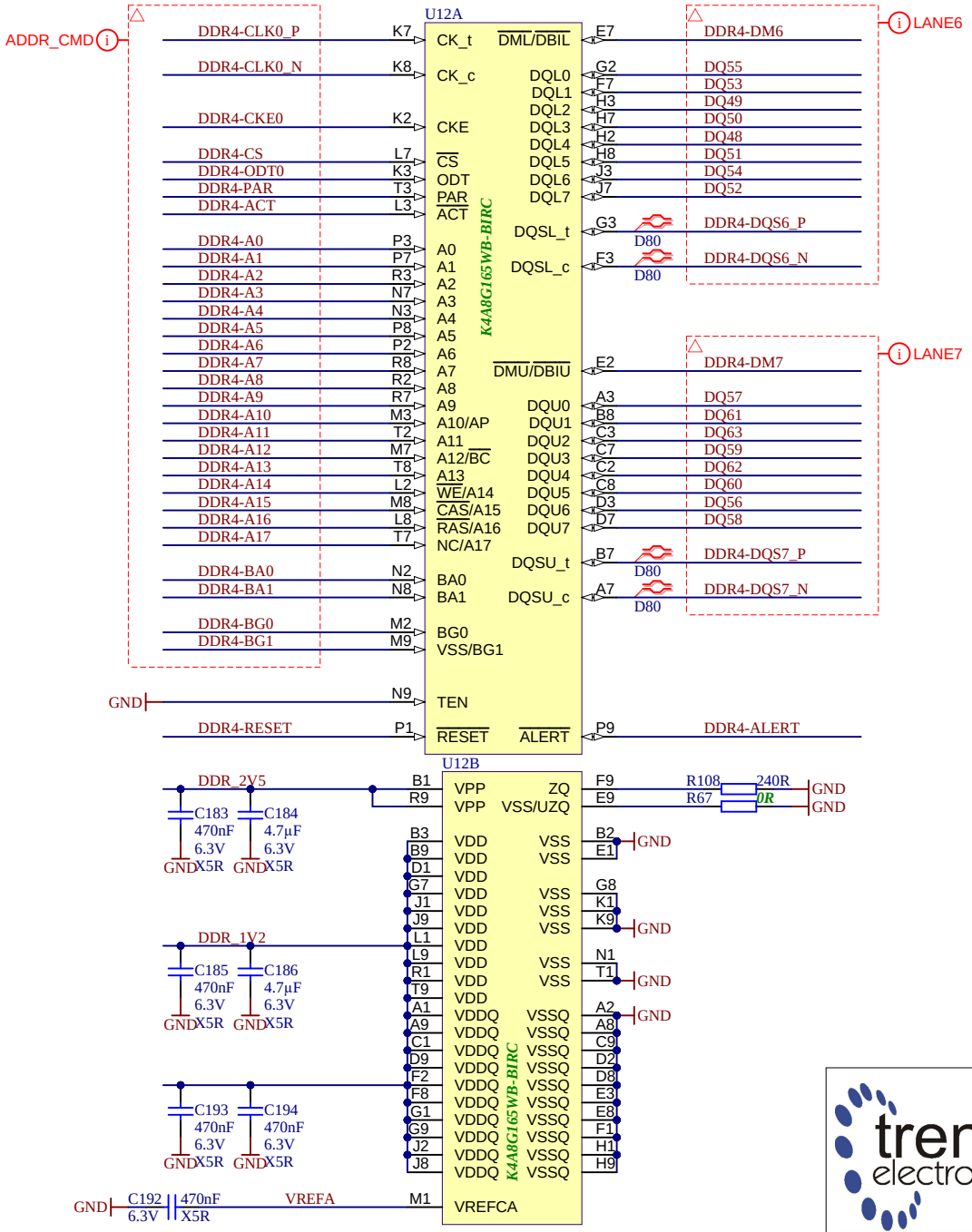
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page 22 of 30
Filename: DDR4-RAM_3.SchDoc			



Title: TE0803 - DDR4_4_RAM			
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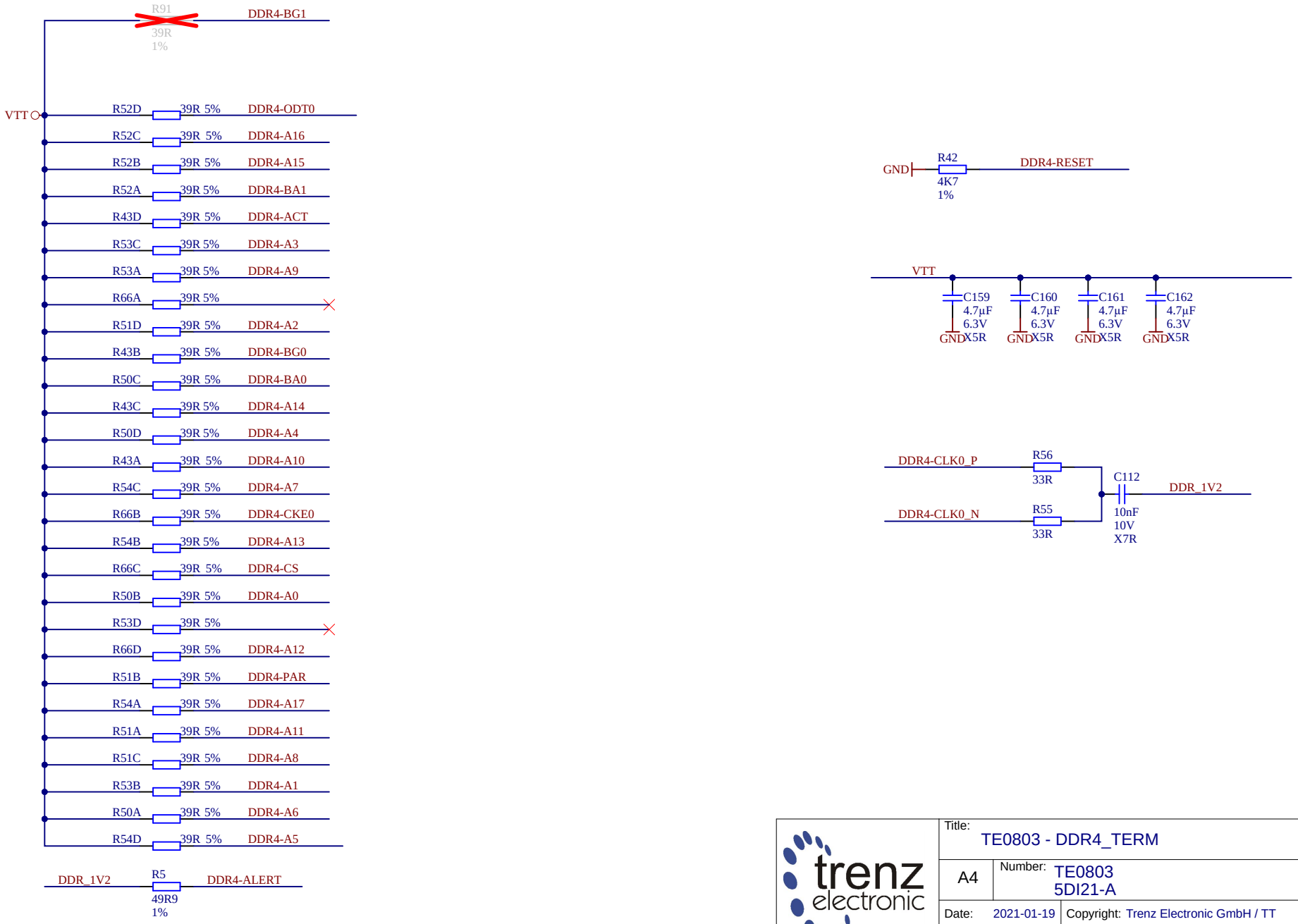
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT		Page 23 of 30
Filename: DDR4-RAM_4.SchDoc			



Title: TE0803 - DDR4_TERM			
A4	Number: TE0803 5DI21-A		Rev. 04
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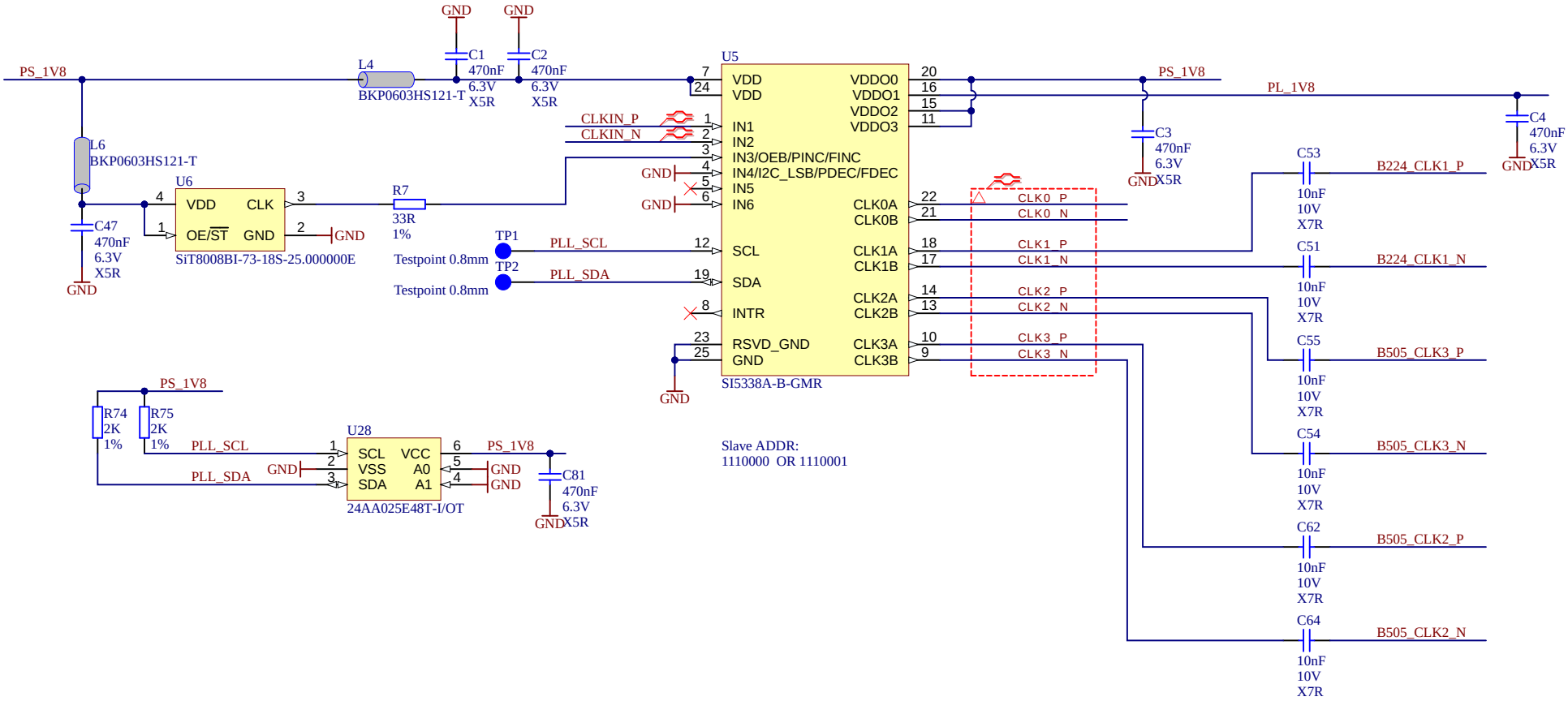
Filename: DDR4-TERM.SchDoc			



trenz electronic	Title: TE0803 - CLOCK		
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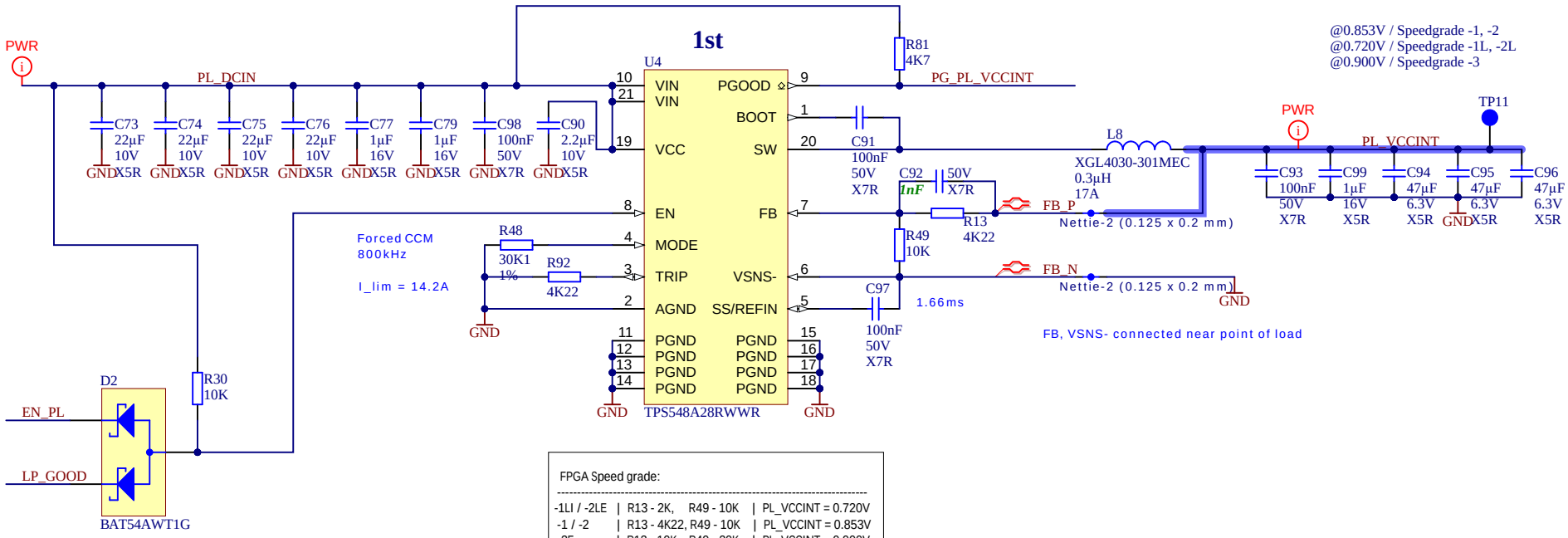
PL VCCINT



FPGA Speed grade:		
-1LI / -2LE	R13 - 2K, R49 - 10K	PL_VCCINT = 0.720V
-1 / -2	R13 - 4K22, R49 - 10K	PL_VCCINT = 0.853V
-3E	R13 - 10K, R49 - 20K	PL_VCCINT = 0.900V

U4 pin compatible with
-- TPS548B28 (20A)
-- TPS54JA20 (12A)

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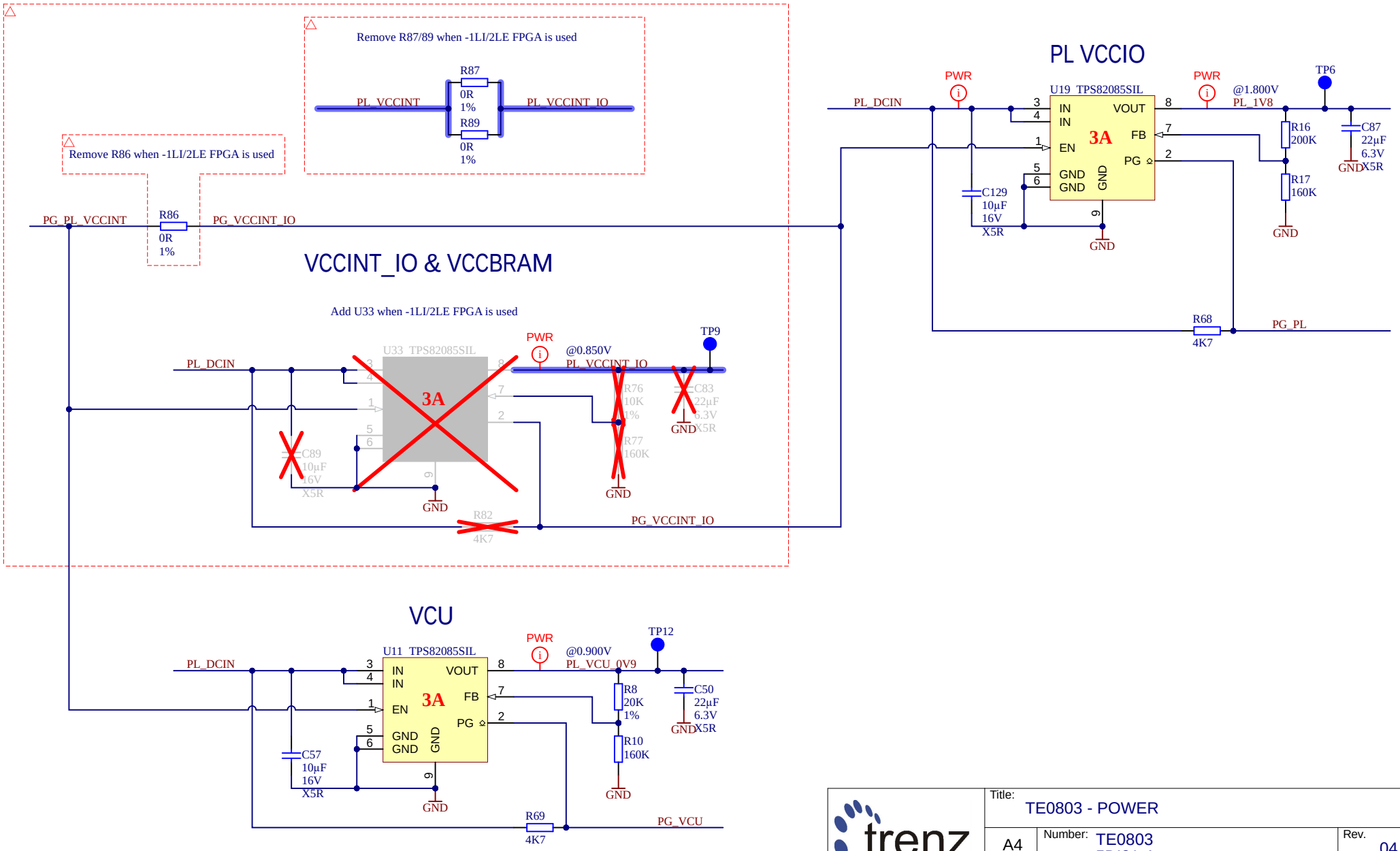

trenz electronic	Title: TE0803 - POWER		
	A4	Number: TE0803 5DI21-A	Rev. 04
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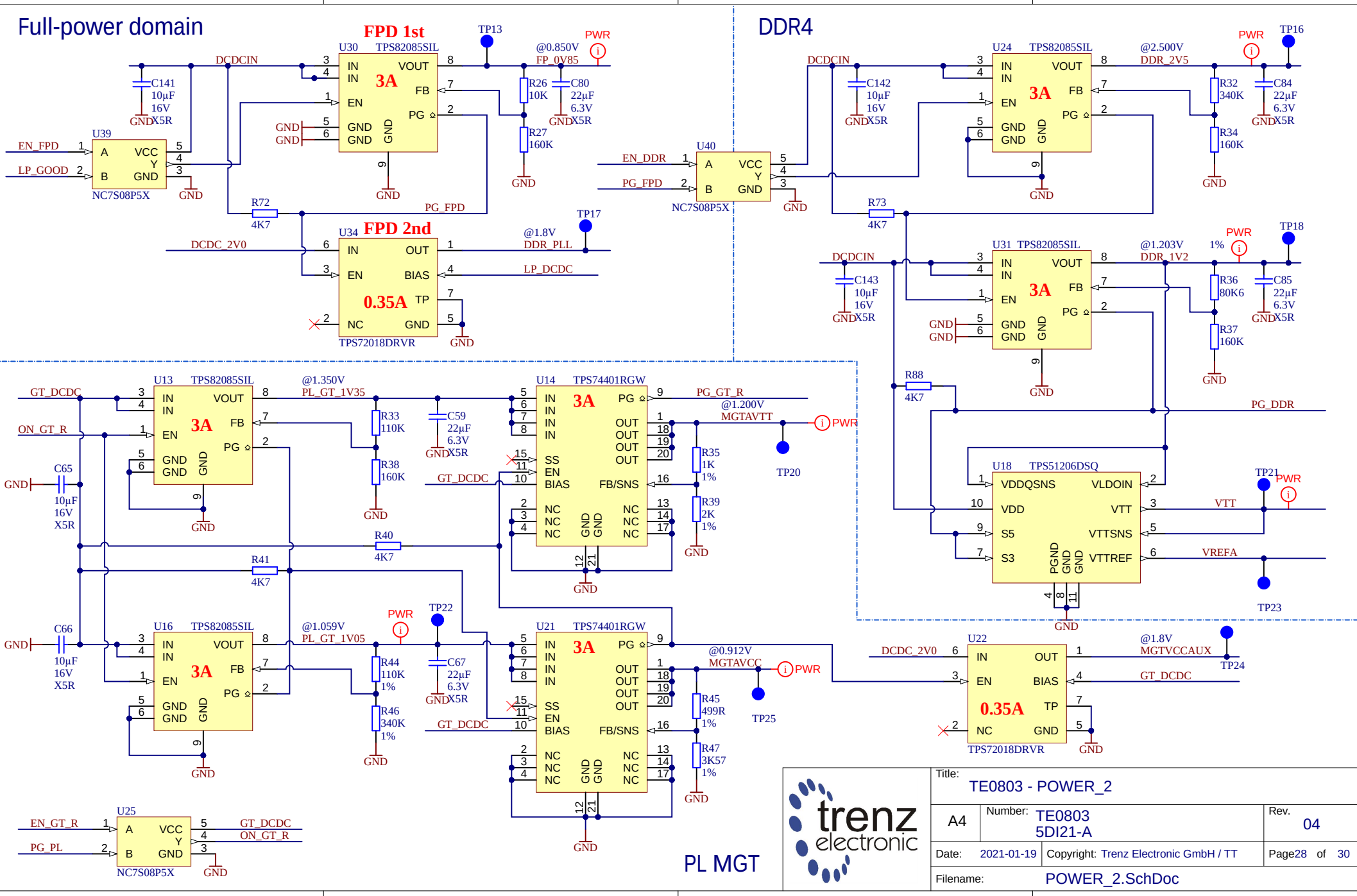
	Filename: POWER_1.SchDoc		


Full-power domain
FPD 1st
U30 TPS82085SIL
3A
@0.850V
FP_0V85
PWR
TP13
DCDCIN
C141 10µF 16V X5R
R26 10K
C80 22µF 6.3V X5R
R27 160K
U39
NC7S08P5X
EN_FPD
LP_GOOD
R72 4K7
PG_FPD
FPD 2nd
U34
TPS72018DRVR
0.35A
DCDC_2V0
@1.8V
DDR_PLL
TP17
LP_DCDC
DDR4
U24 TPS82085SIL
@2.500V
DDR_2V5
TP16
R32 340K
C84 22µF 6.3V X5R
R34 160K
U40
EN_DDR
PG_FPD
C142 10µF 16V X5R
R73 4K7
U31 TPS82085SIL
@1.203V
DDR_1V2
1%
TP18
R36 80K6
C85 22µF 6.3V X5R
R37 160K
C143 10µF 16V X5R
R88 4K7
PG_DDR
U18 TPS51206DSQ
VDDQSNS
VLDOIN
VDD
VTT
S5
VTTSNS
S3
VTTREF
PGND
VTT
VREFA
TP21
TP23
U13 TPS82085SIL
@1.350V
PL_GT_1V35
GT_DCDC
ON_GT_R
C65 10µF 16V X5R
R33 110K
R38 160K
C59 22µF 6.3V X5R
R40 4K7
R41 4K7
U14 TPS74401RGW
PG_GT_R
@1.200V
MGTAVTT
TP20
R35 1K 1%
R39 2K 1%
U16 TPS82085SIL
@1.059V
PL_GT_1V05
C66 10µF 16V X5R
R44 110K 1%
R46 340K 1%
C67 22µF 6.3V X5R
TP22
U21 TPS74401RGW
@0.912V
MGTAVCC
TP25
R45 499R 1%
R47 3K57 1%
U22
DCDC_2V0
@1.8V
MGTVCCAUX
TP24
GT_DCDC
U25
NC7S08P5X
EN_GT_R
PG_PL
ON_GT_R
PL MGT
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Title: TE0803 - POWER_2
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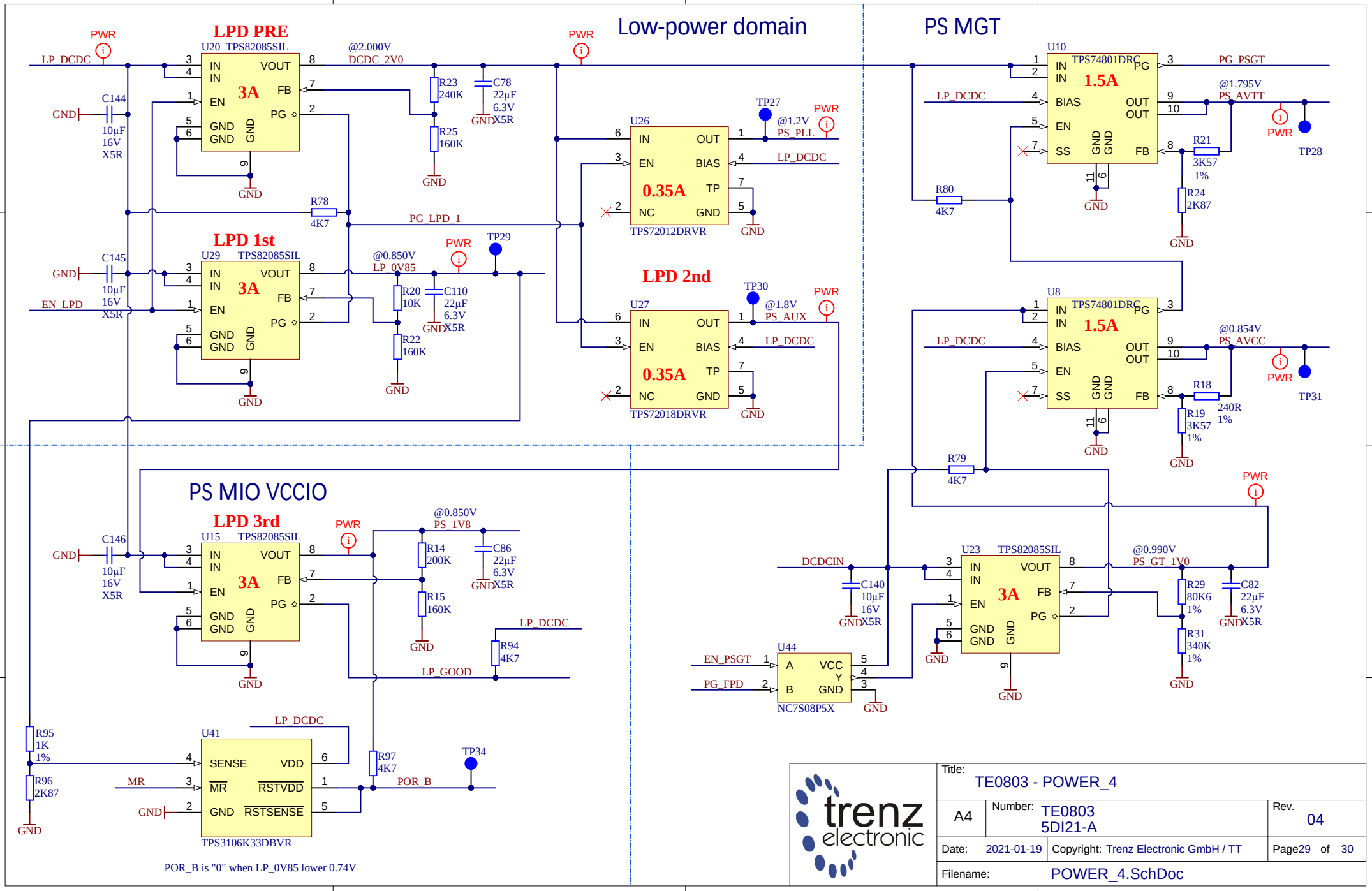

Title: TE0803 - POWER_4			
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REV	DATE	Description	
-01		Initial revision	VT
-01a	20.11.2017	1. VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9.	VT
-02	20.06.2018	1. Added LDO to DDR_PLL 2. All differential pairs wath length matched with tollerance 0.1mm (excluding package delays) 3. Added MAC EEPROM U28 4. VPS_MGTRAVCC set to 0.85V 5. Added pull-up resistors R68,R69	VT
-03	21.02.2019	1. Added support of DDP DDR4 2. Added support of Low power FPGA (-L1/L2). 3. Revised testpoints 4. Revised J1-J4 connectors net label style	VY
-04	15.12.2020	1. Revised PL_VCCINT power supply. EN63A0QI replaced by TPS548A28RWWR. PCB: revised routing and components placement; 2. Added support of wide SDRAM DDR4 packages. PCB: revised routing and components placement; 3. Added option to select POR_OVERRIDE level (R12 and R93) 4. VCCO pins if unused Bank 44 connected together. Same for unused Bank 24 (UG583 recomendation) 5. PCB: updated signal trace lengths. 6. PCB: updated silckscreen. Added company address, CE and WEEE symbols; 7. PCB: added module orientation rectangle poiner 8. Changed resistors value of R29, R31, R35, R39, R44-R47 (BOM optimization) 9. Removed traceability part (Obsolete component)	VY
-04	23.02.2022	10. Changed capacitor C92 for all variants from 100 nF to 1 nF.	ED

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Title: TE0803 - Revision History			
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Drawn by: VY	Filename: Revision Changes.SchDoc		