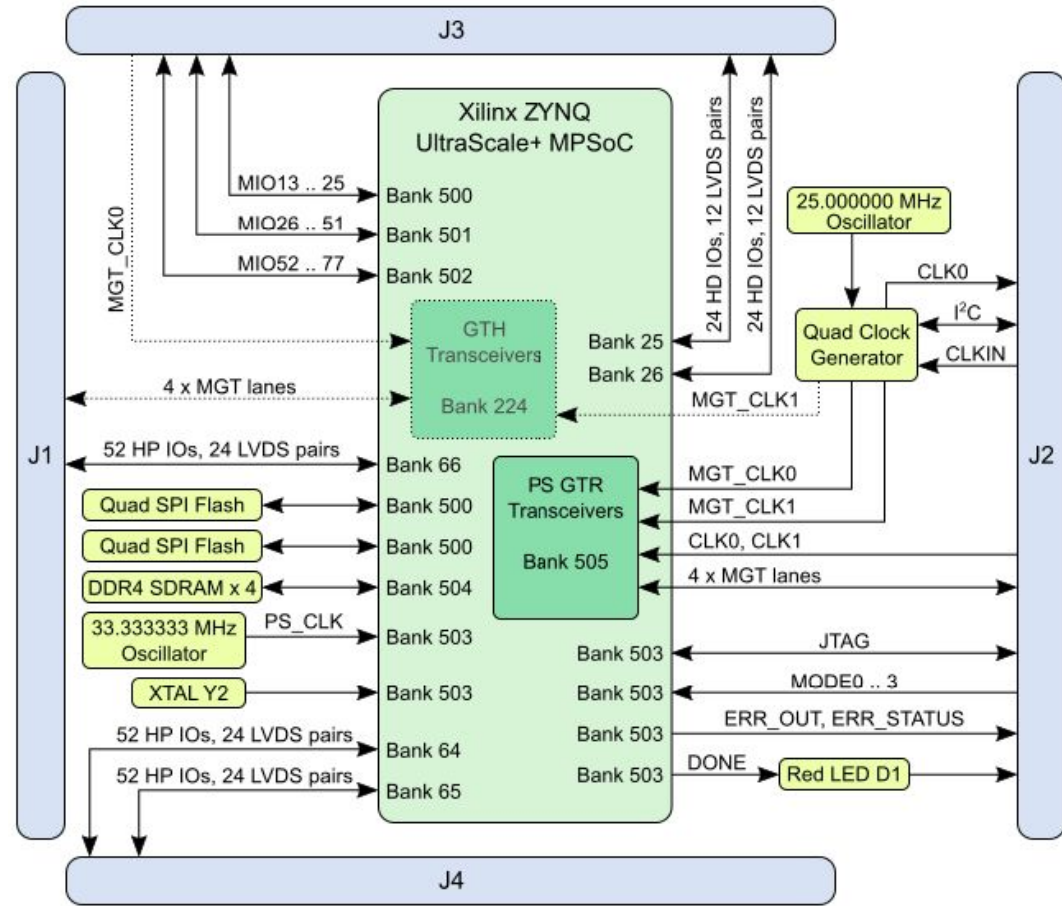



Regarding the usage of our schematics and alike documentation for Trenz module TE0803.

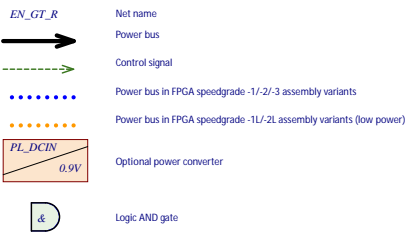
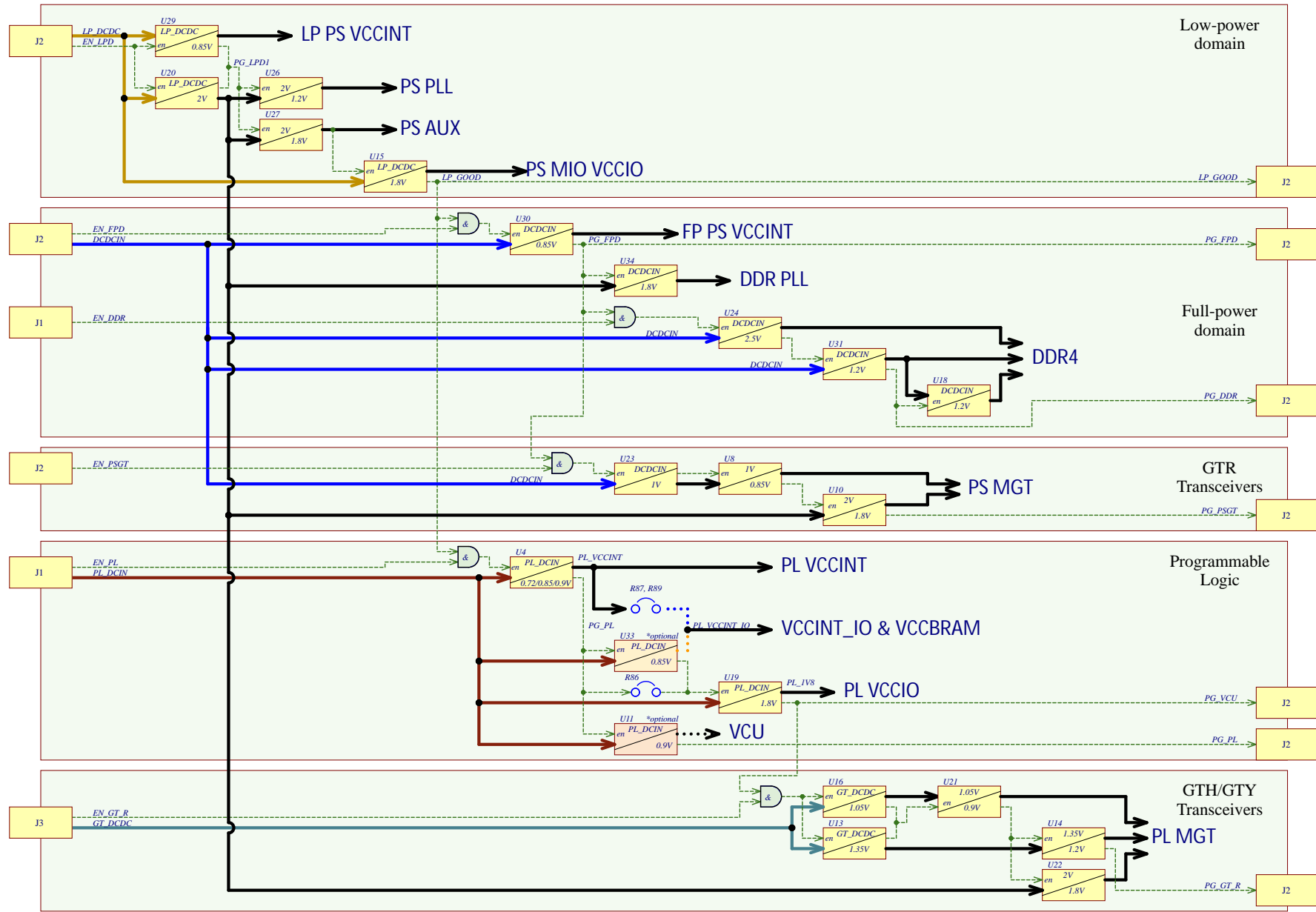
Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0803 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

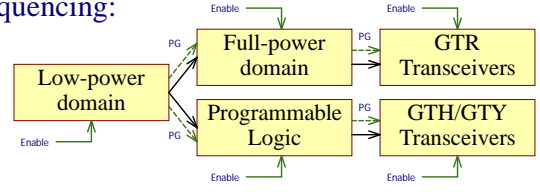
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	A4	Number: TE0803 5DI21-AZ	Rev. 04
	Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 1 of 30
	Filename: Legal Notices Modules.SchDoc		



	Title: TE0803 - System Overview		
	A4	Number: TE0803 5DI21-AZ	Rev. 04
	Date: 2021-01-19	Copyright: 2015 Trenz Electronic GmbH	Page 2 of 30
	Filename: TE0803-Overview.SchDoc		



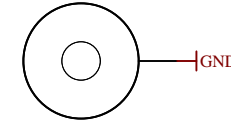
Power-on sequencing:



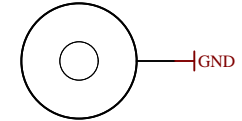
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A3	Number: TE0803 5DI21-AZ	Rev. 04
Datum: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 3 of 30
Filename: Power_Diagram.SchDoc		

U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_LN Legal Notices Modules.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_1 POWER_1.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_REV_CH Revision Changes.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	U_OVERVIEW TE0803-Overview.SchDoc
U_PD Power_Diagram.SchDoc	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

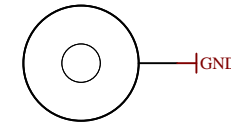
Special notes:



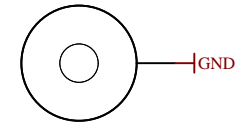
Mount.Hole 3.2mm für Unterlegscheibe



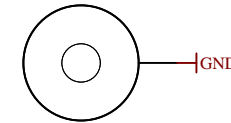
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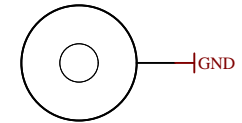
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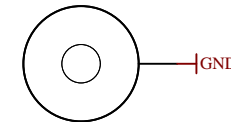
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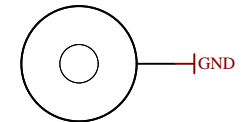
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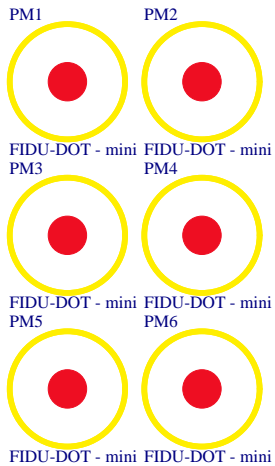
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



MECH1

TE Address Overlay

LOGO ADDRESS

LOGO1

TE Logo PRINT Layer

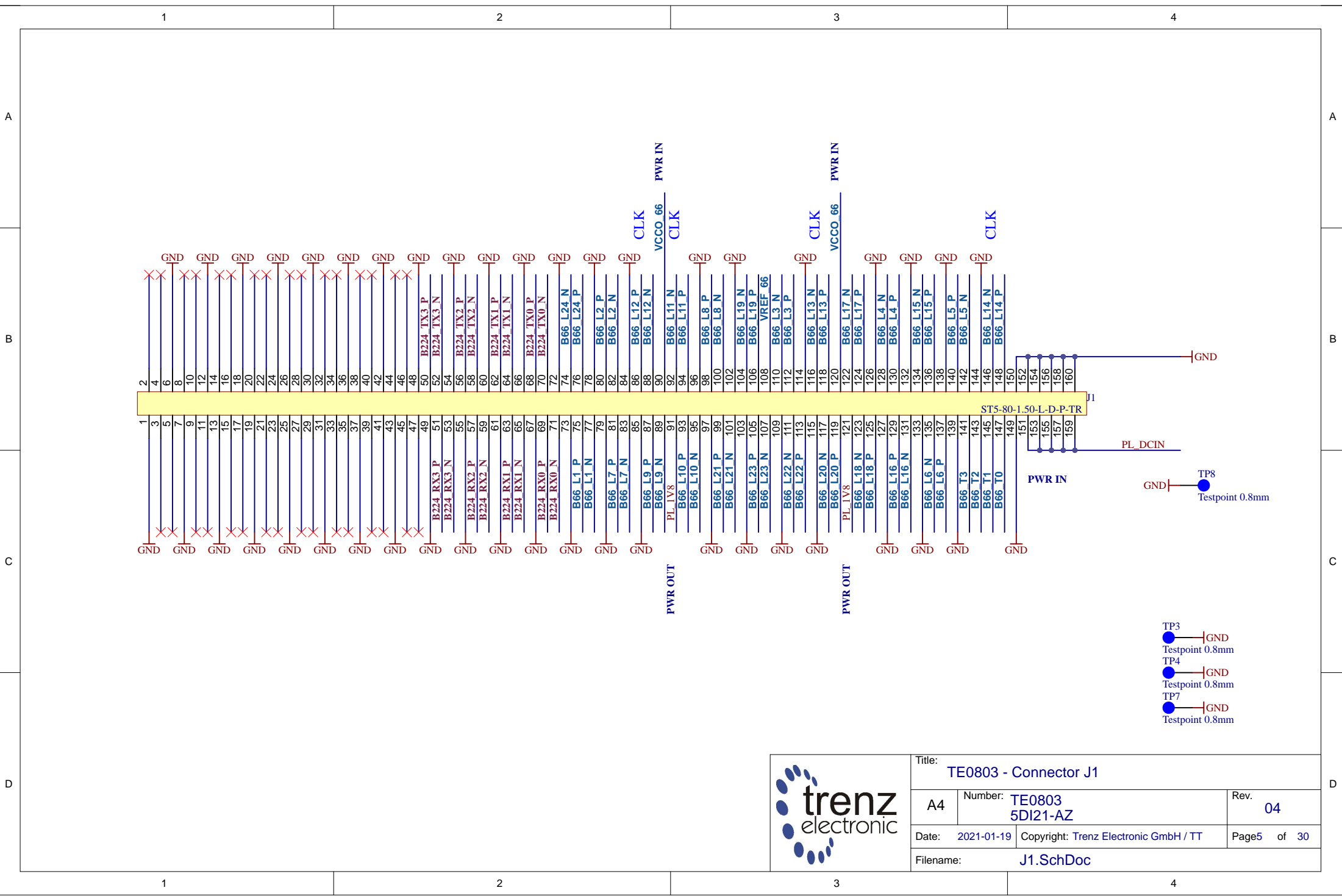
LOGO PRINT

Serial
Serial
Serialnumber 6,3 x 6.3mm

Assembly variant	5DI21-AZ
Created by	VT
Modified by	VT
Modified at	2022-12-14
SVN Revision	11196



Title: TE0803		
A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 4 of 30
Filename: TE0803.SchDoc		



TP8
Testpoint 0.8mm

TP3
Testpoint 0.8mm
TP4
Testpoint 0.8mm
TP7
Testpoint 0.8mm



Title: TE0803 - Connector J1		
A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page5 of 30
Filename: J1.SchDoc		

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A

A

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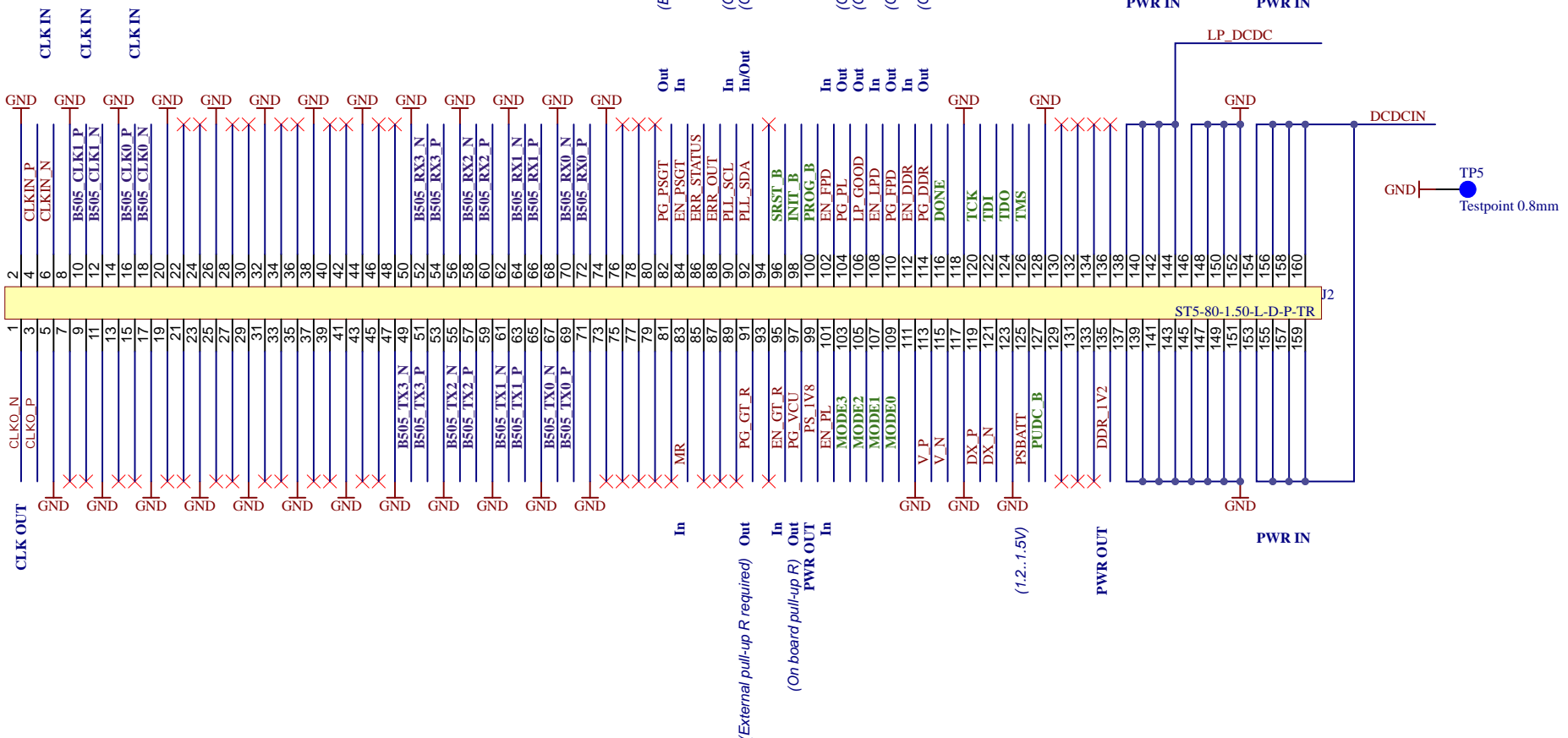
B

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D

D



(External pull-up R required)

(On board pull-up R)
(On board pull-up R)

(On board pull-up R)
(On board pull-up R)

(On board pull-up R)

(On board pull-up R)

PWR IN

PWR IN

LP_DCDC

DCDCIN

PS_IV8

GND

TP14

TP15

Testpoint 0.8mm
Testpoint 0.8mm


GND

TP5

Testpoint 0.8mm

ST5-80-1.50-L-D-P-TR

J2



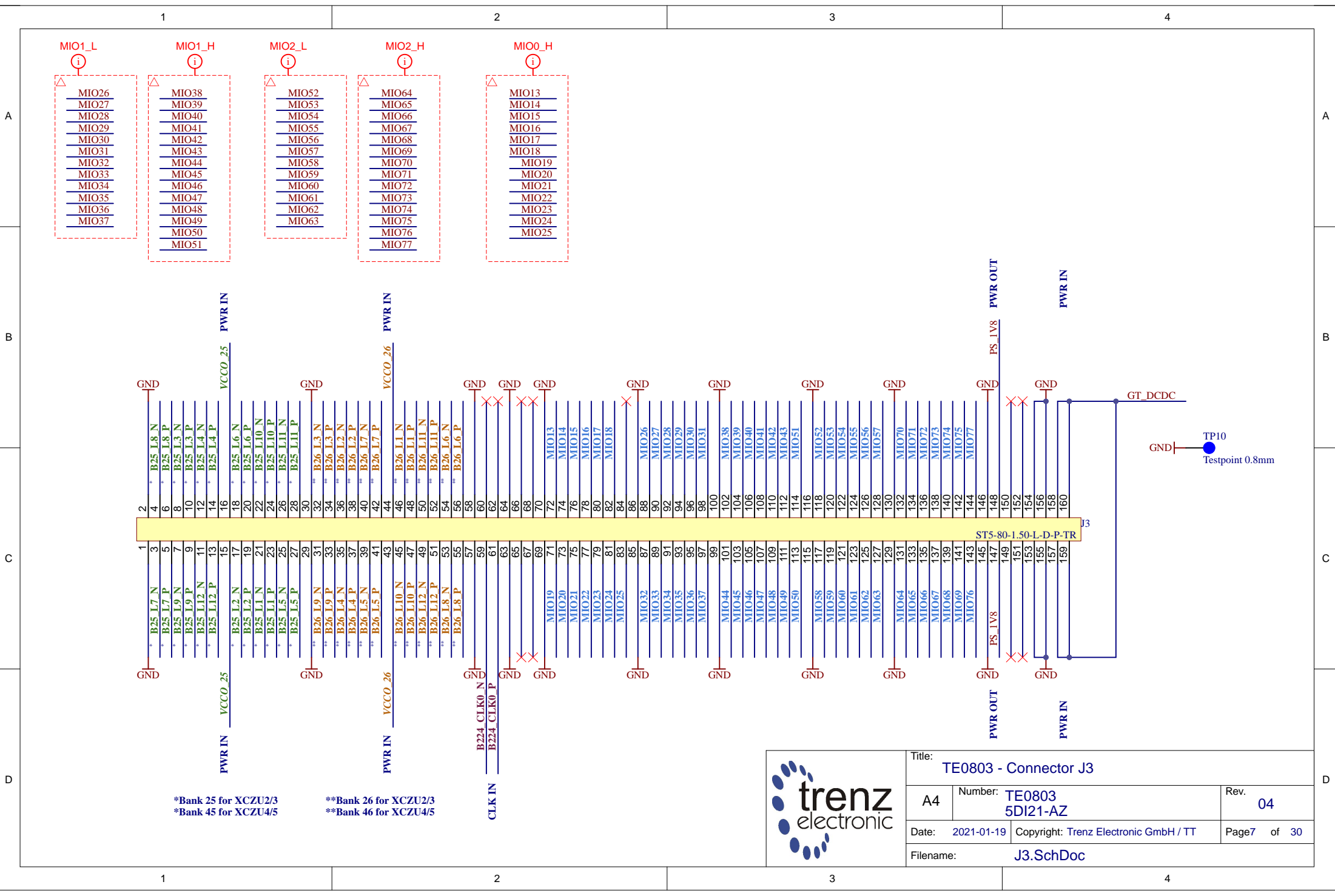
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A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 6 of 30
Filename: J2.SchDoc		

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Title: TE0803 - Connector J3		
A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 7 of 30
Filename: J3.SchDoc		

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B

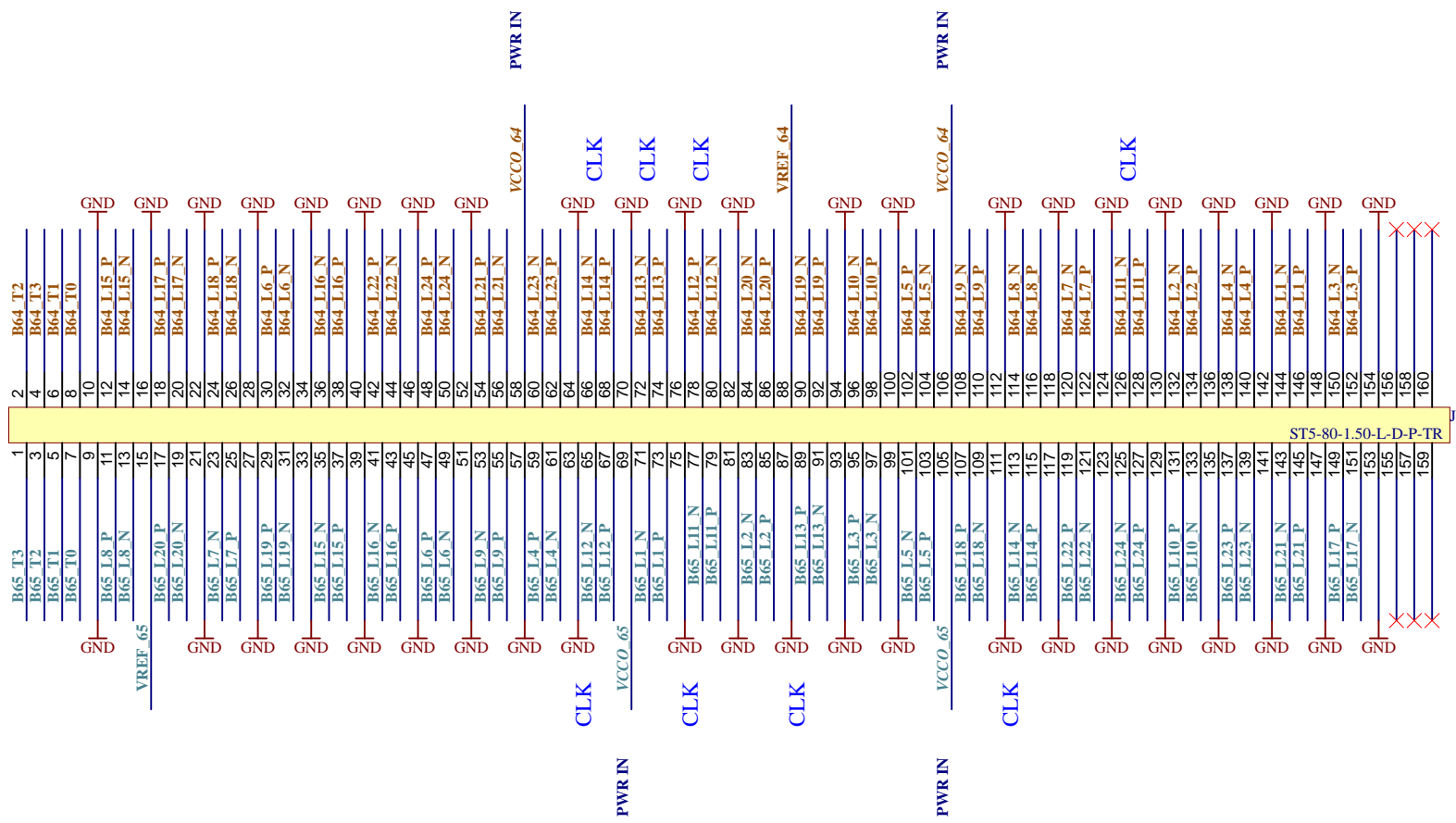
B

C

C

D

D



J4 ST5.80-1.50-L-D-P-TR



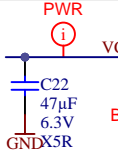
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A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page8 of 30
Filename: J4.SchDoc		

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U1C **XCZU5EV-1SFVC784I**
BANK 46 HD (ZU2/3 BANK 26 HD)

B26 L1 P	B15	IO_L1P_AD11P_46	IO_L7P_HDGC_AD5P_46	G13	B26 L7 P
B26 L1 N	A15	IO_L1N_AD11N_46	IO_L7N_HDGC_AD5N_46	F13	B26 L7 N
B26 L2 P	B14	IO_L2P_AD10P_46	IO_L8P_HDGC_AD4P_46	F15	B26 L8 P
B26 L2 N	A14	IO_L2N_AD10N_46	IO_L8N_HDGC_AD4N_46	E15	B26 L8 N
B26 L3 P	B13	IO_L3P_AD9P_46	IO_L9P_AD3P_46	G15	B26 L9 P
B26 L3 N	A13	IO_L3N_AD9N_46	IO_L9N_AD3N_46	G14	B26 L9 N
B26 L4 P	C13	IO_L4P_AD8P_46	IO_L10P_AD2P_46	H14	B26 L10 P
B26 L4 N	C12	IO_L4N_AD8N_46	IO_L10N_AD2N_46	H13	B26 L10 N
B26 L5 P	D13	IO_L5P_HDGC_AD7P_46	IO_L11P_AD1P_46	K14	B26 L11 P
B26 L5 N	D12	IO_L5N_HDGC_AD7N_46	IO_L11N_AD1N_46	L14	B26 L11 N
B26 L6 P	E13	IO_L6P_HDGC_AD6P_46	IO_L12P_AD0P_46	L14	B26 L12 P
B26 L6 N	E12	IO_L6N_HDGC_AD6N_46	IO_L12N_AD0N_46	K13	B26 L12 N

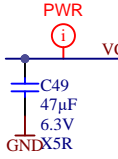
BANK 43 HD (ZU2/3 BANK 44 HD)

AC10	VCCO_43			AD11	
AG12	VCCO_43			AD10	
AG10	IO_L1P_AD11P_43	IO_L7P_HDGC_AD5P_43		AB11	
AH10	IO_L1N_AD11N_43	IO_L7N_HDGC_AD5N_43		AC11	
AF11	IO_L2P_AD10P_43	IO_L8P_HDGC_AD4P_43		AA11	
AG11	IO_L2N_AD10N_43	IO_L8N_HDGC_AD4N_43		AA10	
AH11	IO_L3P_AD9P_43	IO_L9P_AD3P_43		W10	
AH10	IO_L3N_AD9N_43	IO_L9N_AD3N_43		Y10	
AE10	IO_L4P_AD8P_43	IO_L10P_AD2P_43		Y9	
AF10	IO_L4N_AD8N_43	IO_L10N_AD2N_43		AA8	
AE11	IO_L5P_HDGC_AD7P_43	IO_L11P_AD1P_43		AB10	
AF11	IO_L5N_HDGC_AD7N_43	IO_L11N_AD1N_43		AB9	
AC11	IO_L6P_HDGC_AD6P_43	IO_L12P_AD0P_43			
AD11	IO_L6N_HDGC_AD6N_43	IO_L12N_AD0N_43			

U1B
BANK 44 HD (ZU2/3 BANK 24 HD)

AA14	VCCO_44			AA13	
AD13	VCCO_44			AB13	
AE15	IO_L1P_AD15P_44	IO_L7P_HDGC_44		AB15	
AE14	IO_L1N_AD15N_44	IO_L7N_HDGC_44		AB14	
AG14	IO_L2P_AD14P_44	IO_L8P_HDGC_44		W14	
AH14	IO_L2N_AD14N_44	IO_L8N_HDGC_44		W13	
AG13	IO_L3P_AD13P_44	IO_L9P_AD1P_44		Y14	
AH13	IO_L3N_AD13N_44	IO_L9N_AD1N_44		Y13	
AE13	IO_L4P_AD12P_44	IO_L10P_AD10P_44		Y12	
AF13	IO_L4N_AD12N_44	IO_L10N_AD10N_44		Y11	
AD13	IO_L5P_HDGC_44	IO_L11P_AD9P_44		Y12	
AD12	IO_L5N_HDGC_44	IO_L11N_AD9N_44		Y11	
AC14	IO_L6P_HDGC_44	IO_L12P_AD8P_44		Y12	
AC13	IO_L6N_HDGC_44	IO_L12N_AD8N_44		AA12	

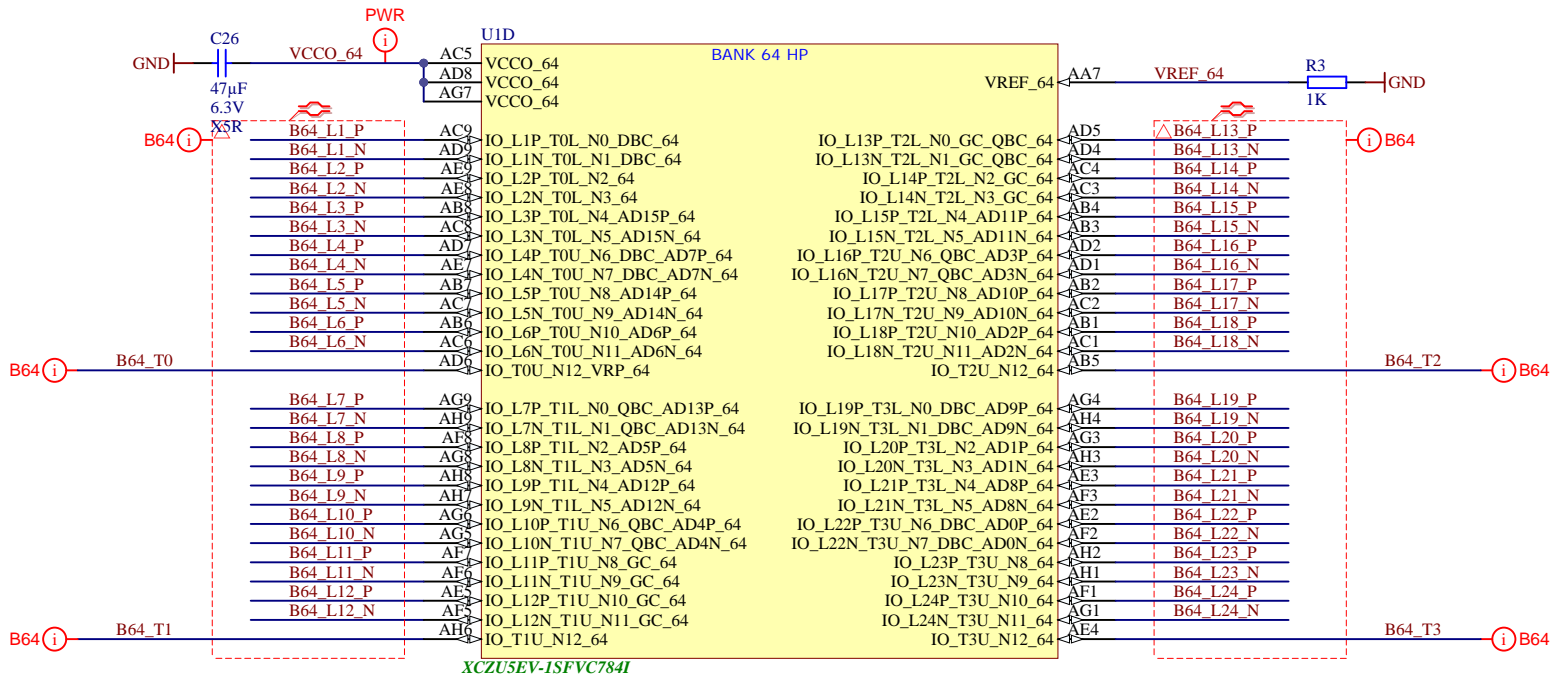
XCZU5EV-1SFVC784I
BANK 45 HD (ZU2/3 BANK 25 HD)




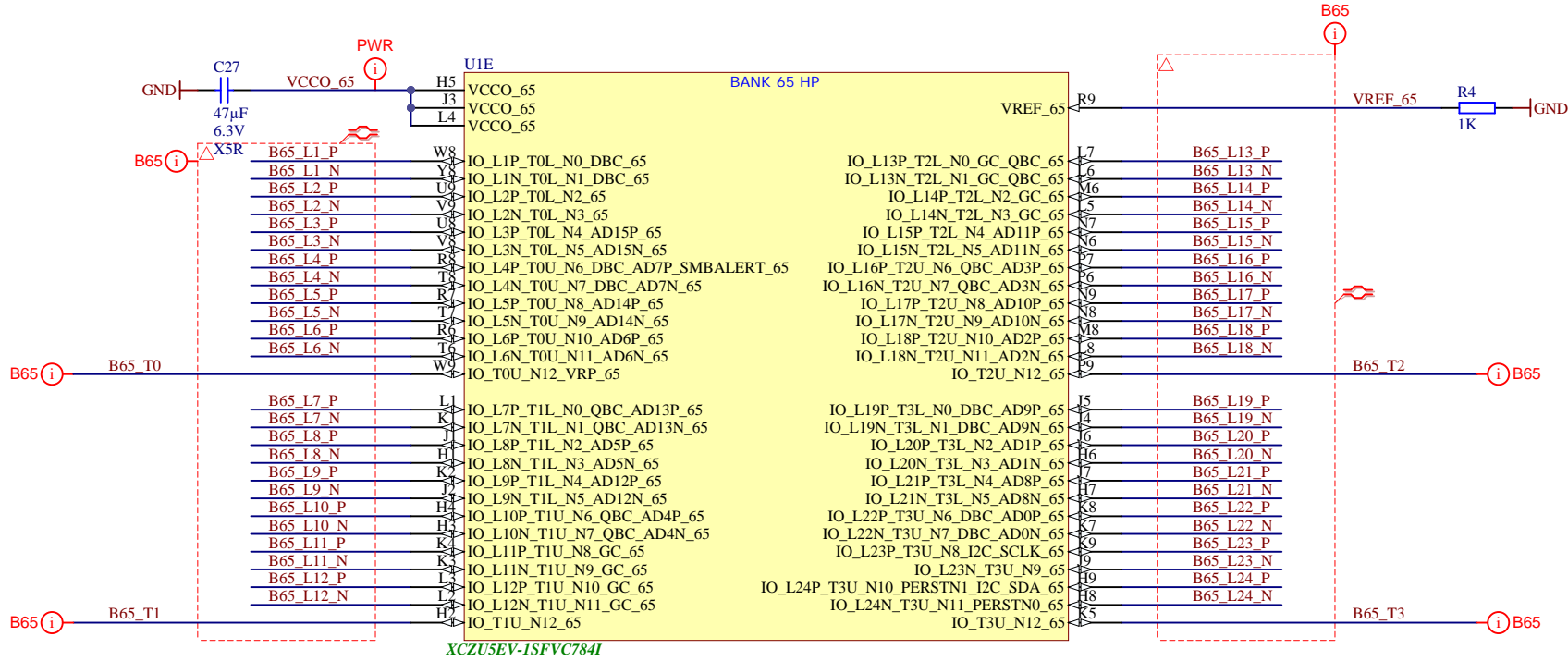
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B25 L1 N	J10	IO_L1N_AD15N_45	IO_L7N_HDGC_45	D10	B25 L7 N
B25 L2 P	K11	IO_L2P_AD14P_45	IO_L8P_HDGC_45	E12	B25 L8 P
B25 L2 N	K10	IO_L2N_AD14N_45	IO_L8N_HDGC_45	D11	B25 L8 N
B25 L3 P	H11	IO_L3P_AD13P_45	IO_L9P_AD1P_45	F11	B25 L9 P
B25 L3 N	G10	IO_L3N_AD13N_45	IO_L9N_AD1N_45	B10	B25 L9 N
B25 L4 P	J11	IO_L4P_AD12P_45	IO_L10P_AD10P_45	B11	B25 L10 P
B25 L4 N	H10	IO_L4N_AD12N_45	IO_L10N_AD10N_45	A10	B25 L10 N
B25 L5 P	G11	IO_L5P_HDGC_45	IO_L11P_AD9P_45	A12	B25 L11 P
B25 L5 N	F10	IO_L5N_HDGC_45	IO_L11N_AD9N_45	A11	B25 L11 N
B25 L6 P	F11	IO_L6P_HDGC_45	IO_L12P_AD8P_45	D12	B25 L12 P
B25 L6 N	F10	IO_L6N_HDGC_45	IO_L12N_AD8N_45	C12	B25 L12 N



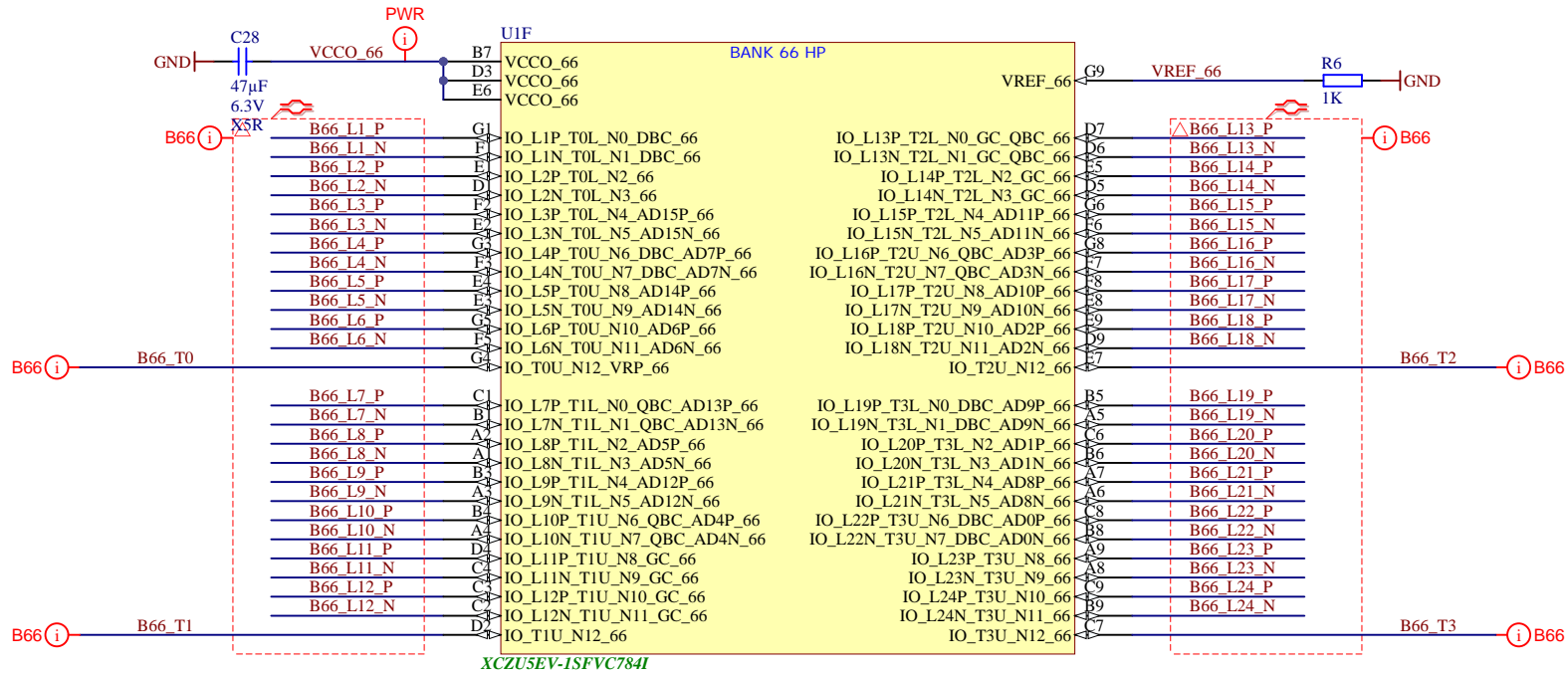
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Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page9 of 30
Filename: B_HD.SchDoc		



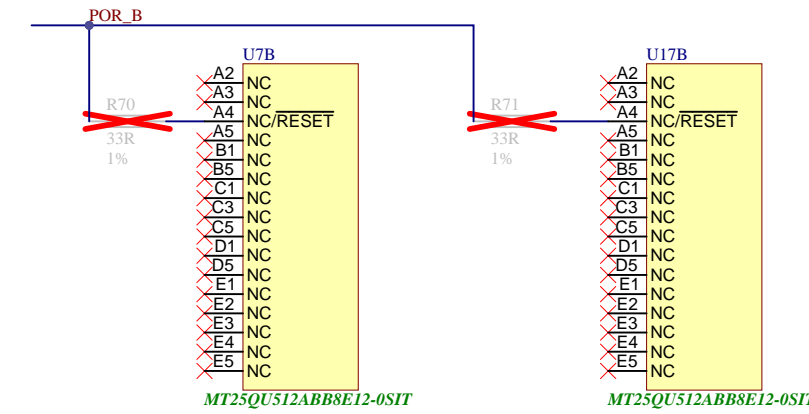
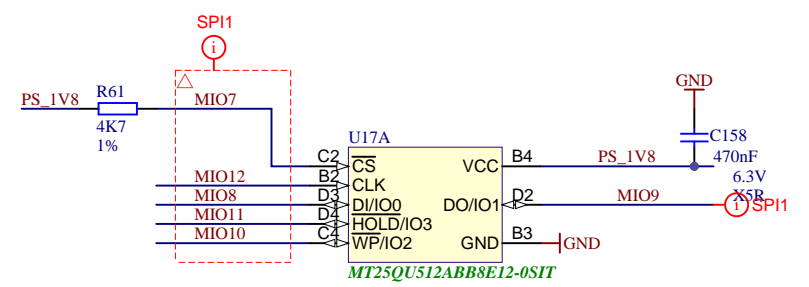
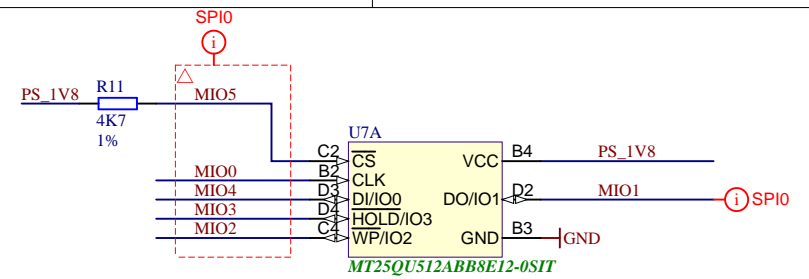
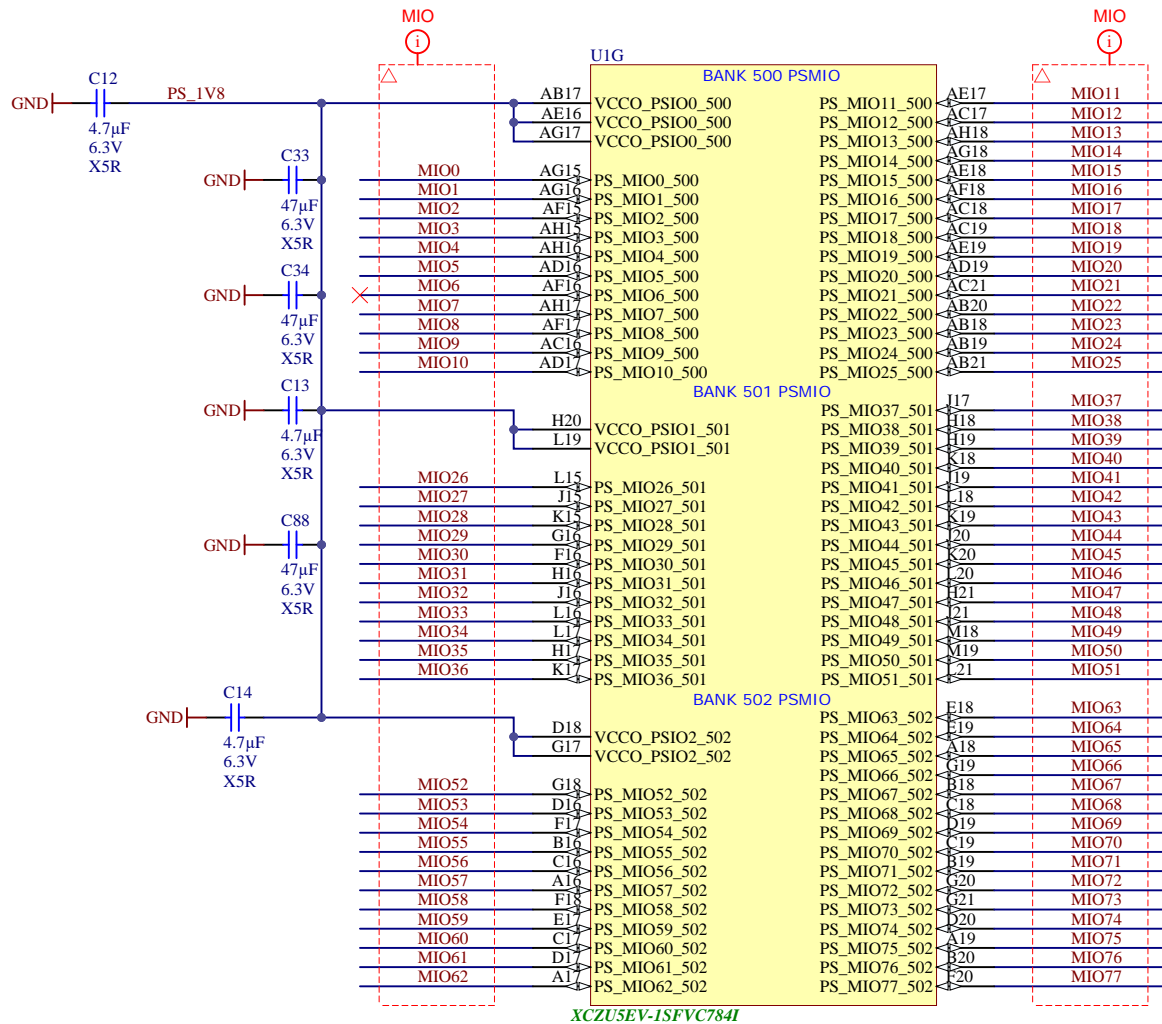
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			A4	Number: TE0803 5DI21-AZ
Date: 2021-01-19		Copyright: Trenz Electronic GmbH / TT		Page 11 of 30
Filename: B64.SchDoc				



Title: TE0803 - B65		
A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 12 of 30
Filename: B65.SchDoc		



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	A4	Number: TE0803 5DI21-AZ	Rev. 04
	Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 13 of 30
	Filename: B66.SchDoc		



	Title: TE0803 - MIO Banks		
	A4	Number: TE0803 5DI21-AZ	Rev. 04
	Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 14 of 30
	Filename: B_MIO.SchDoc		

A

A

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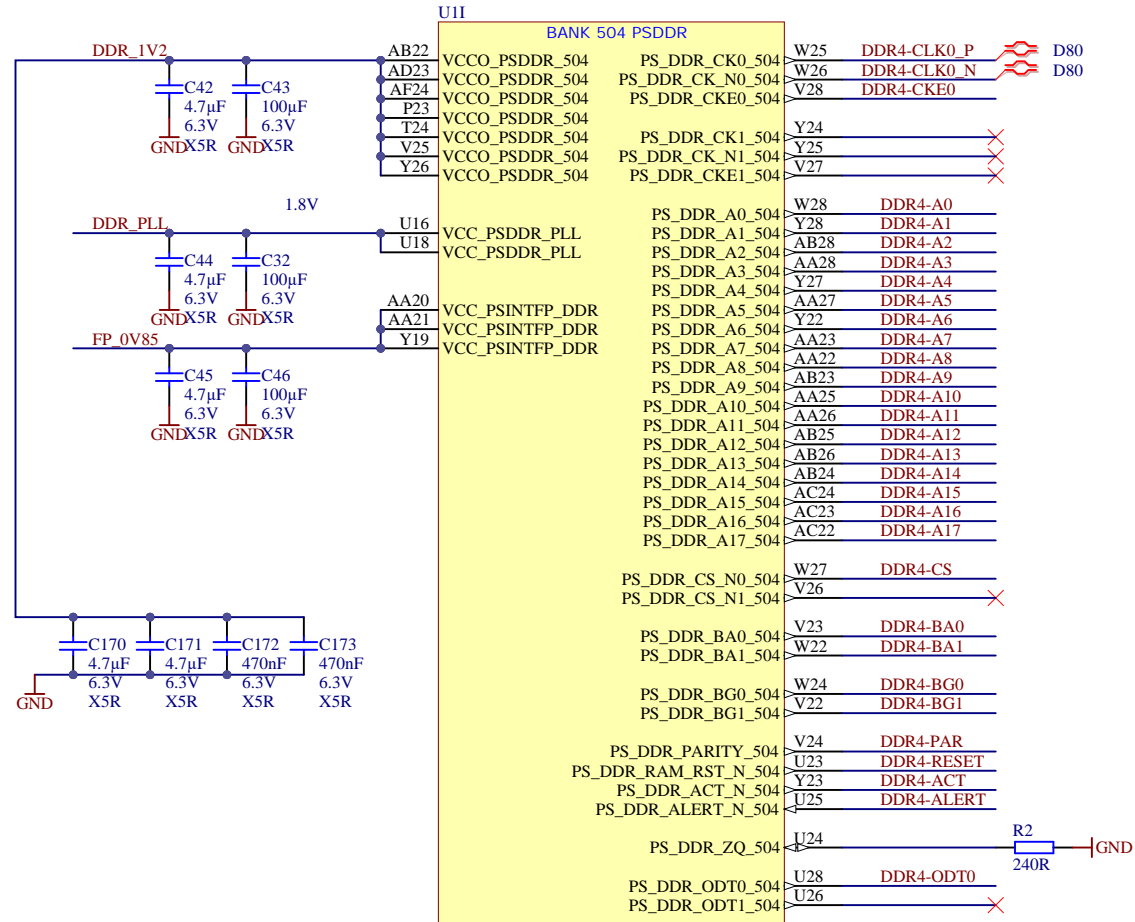
B

C

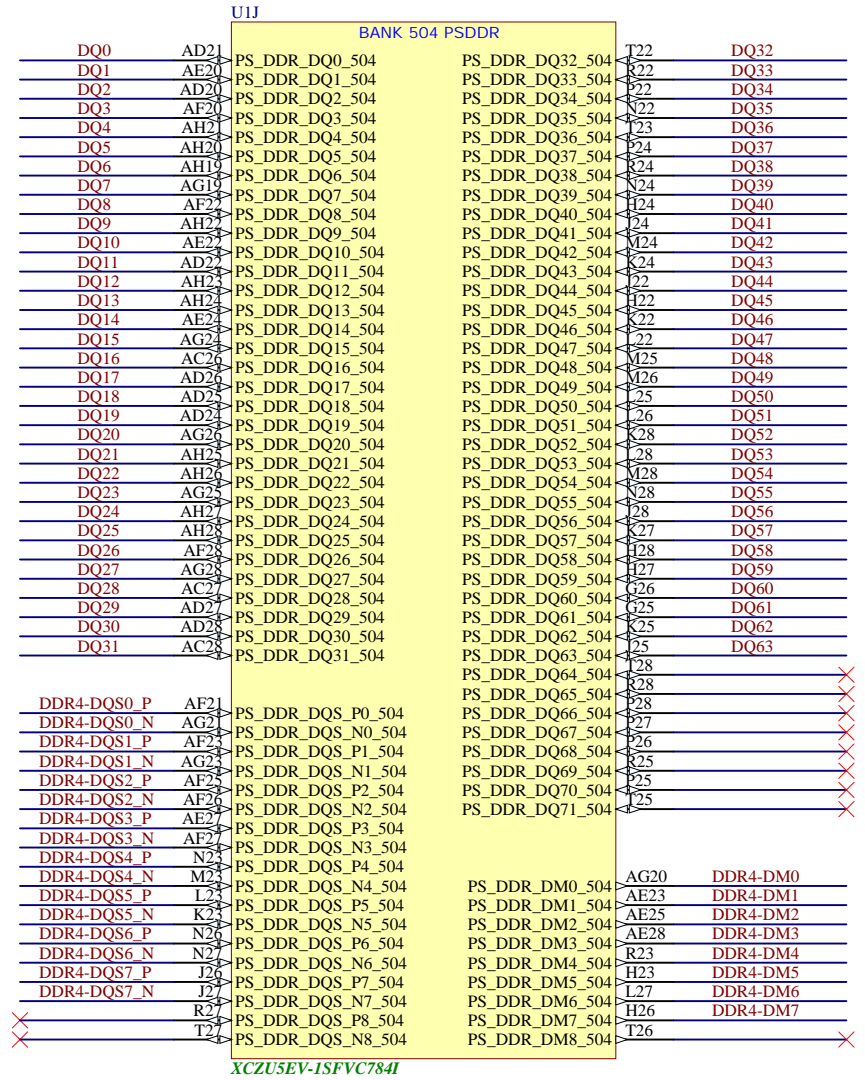
C

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D



XCZU5EV-1SFVC784I



XCZU5EV-1SFVC784I



Title: TE0803 - PS_DDR		
A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 15 of 30
Filename: PS_DDR.SchDoc		

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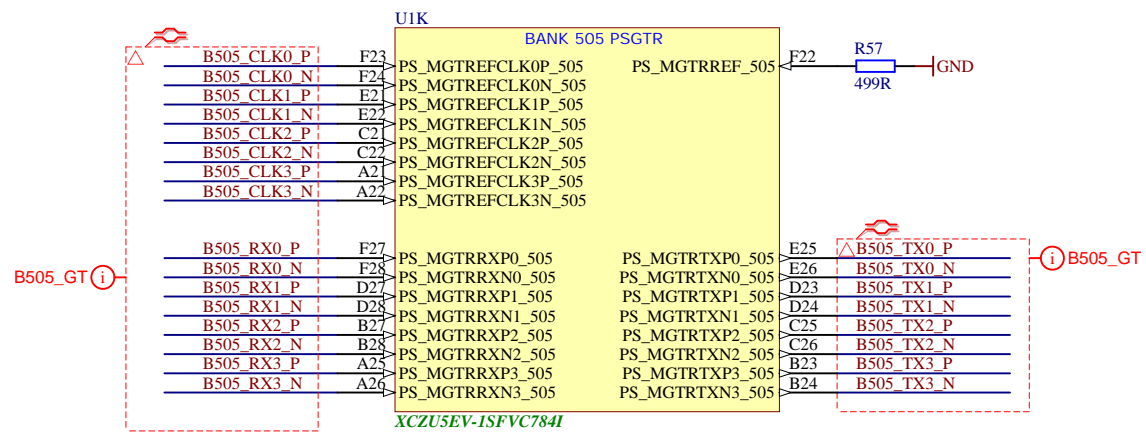
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C

C

D

D



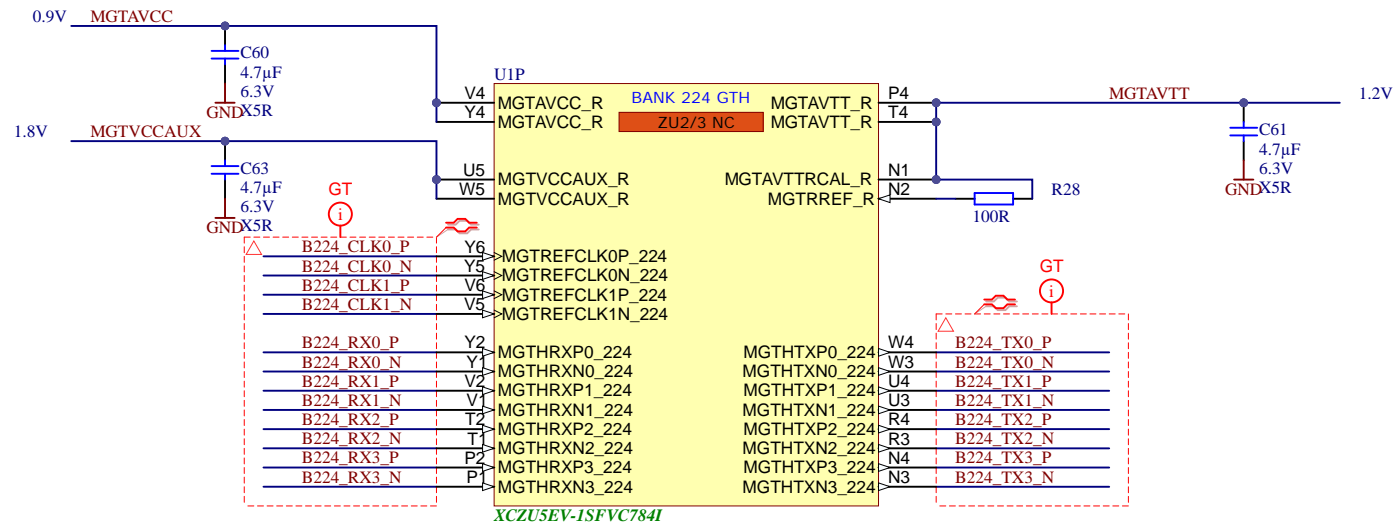
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Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 16 of 30
Filename: B_PS_GT.SchDoc		


1

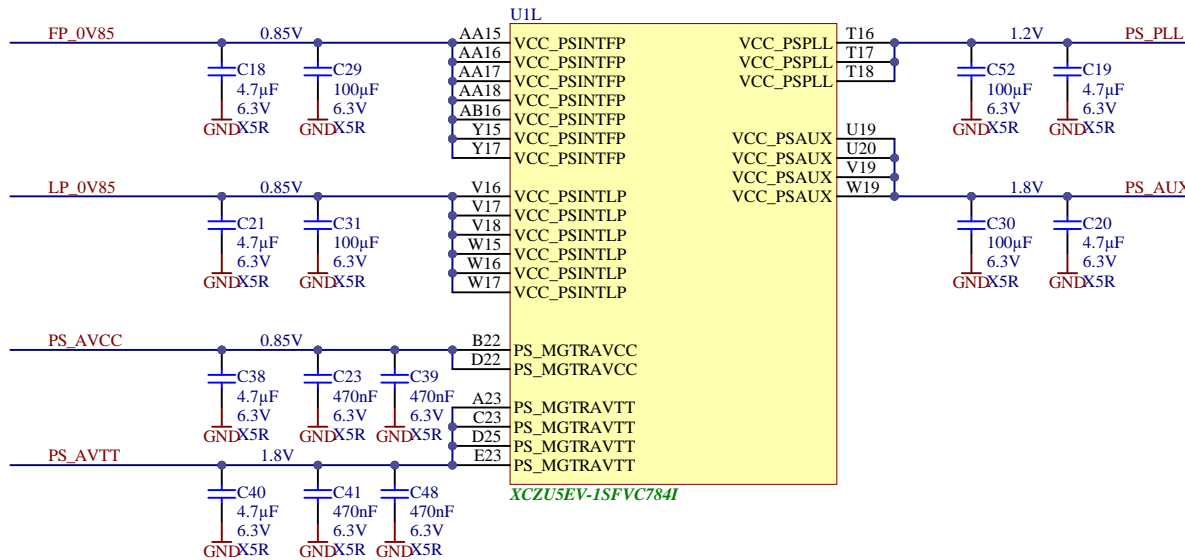
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	Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 17 of 30
	Filename: B_GT.SchDoc		



Title: TE0803 - ZU_PS_POWER		
A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 18 of 30
Filename: ZU_PS_POWER.SchDoc		

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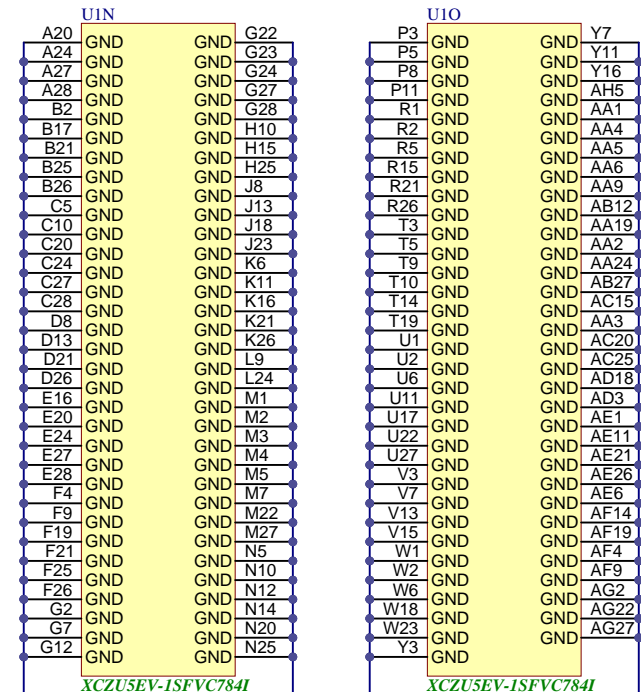
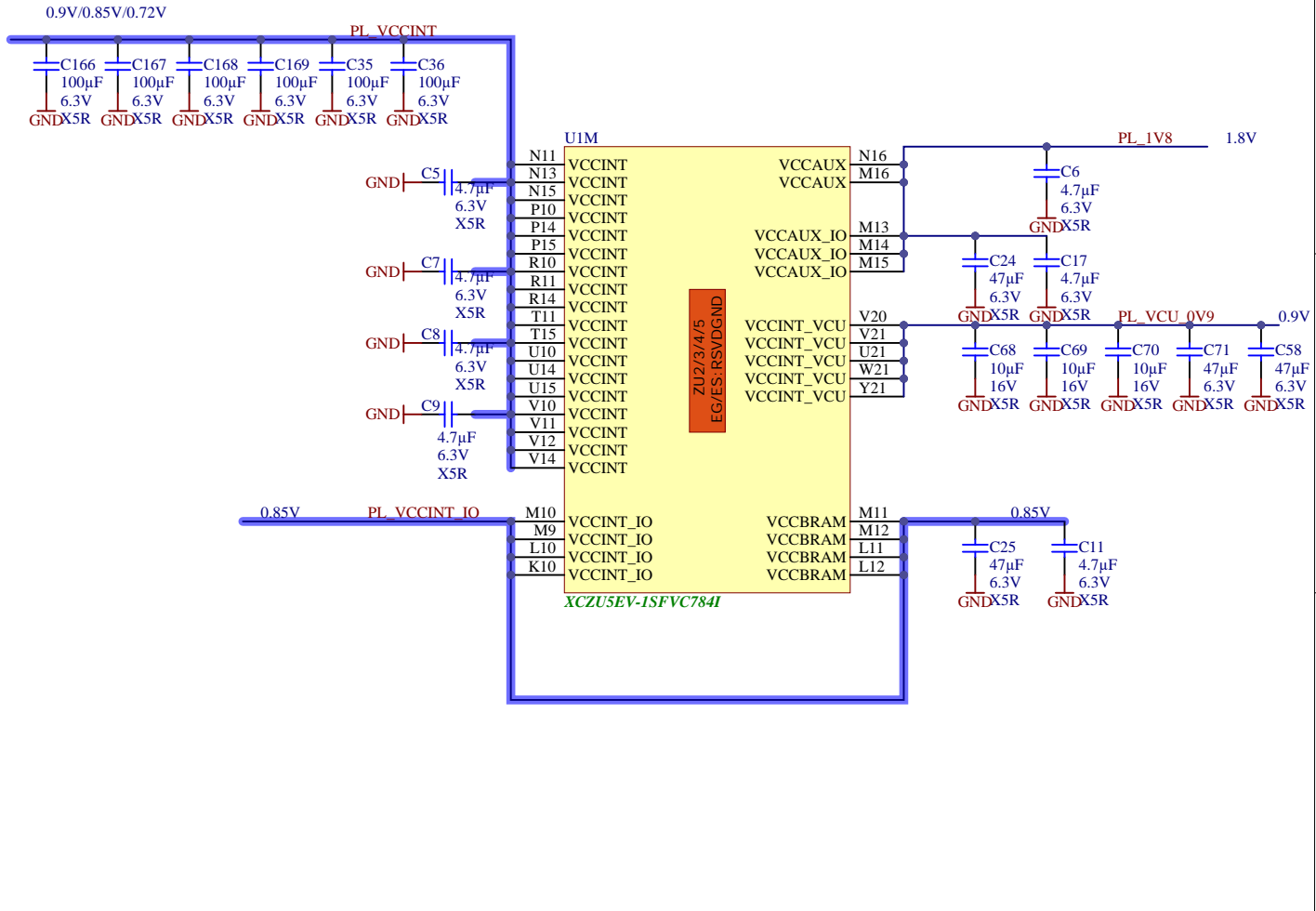
B

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C

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D



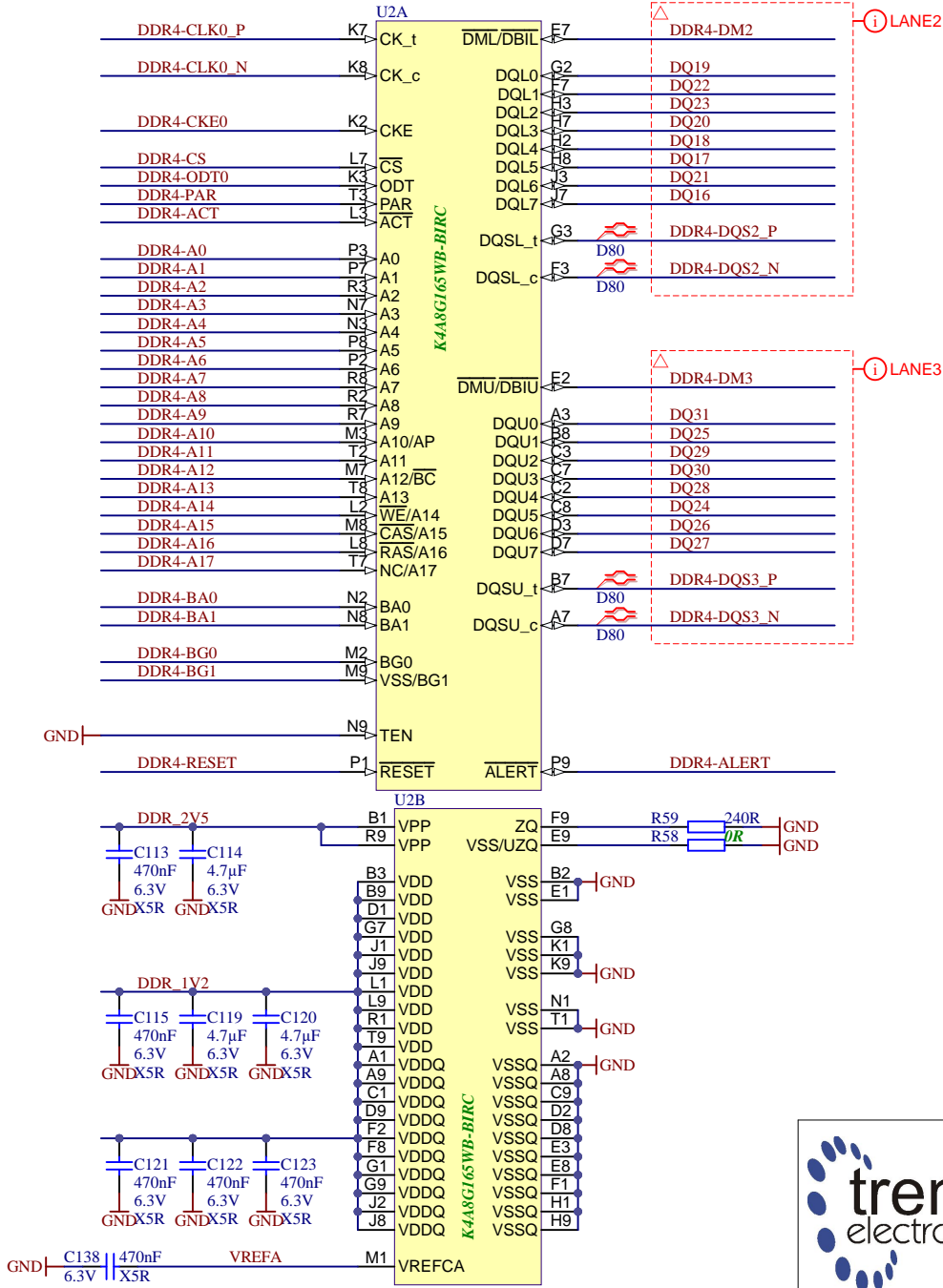
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	Page 19 of 30		
Filename: ZU_POWER.SchDoc			

1

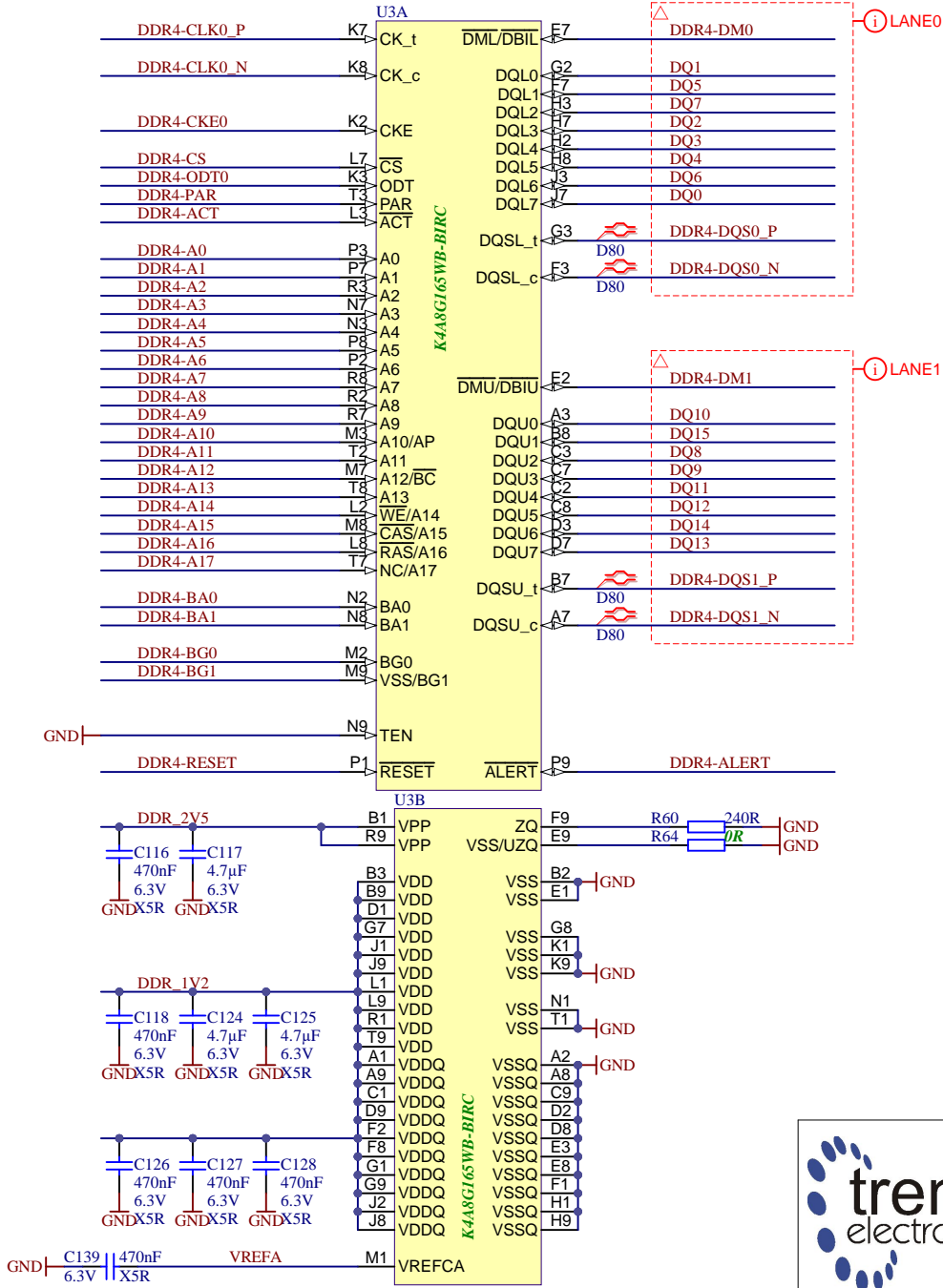
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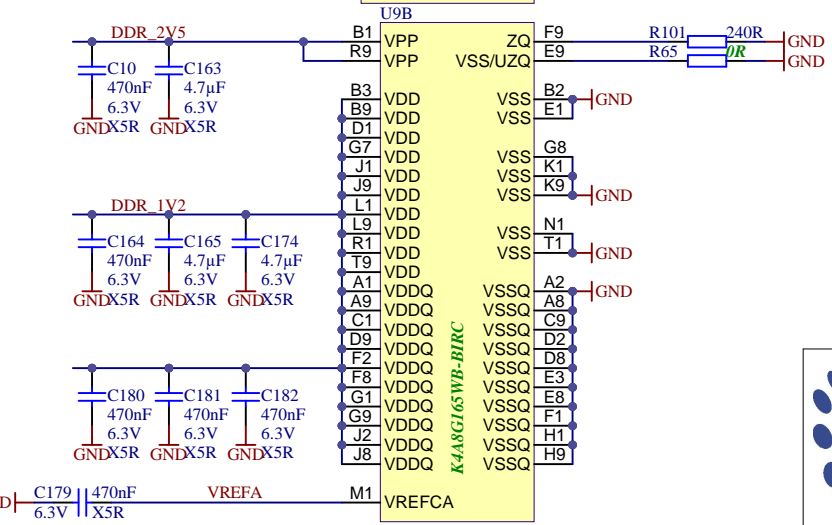
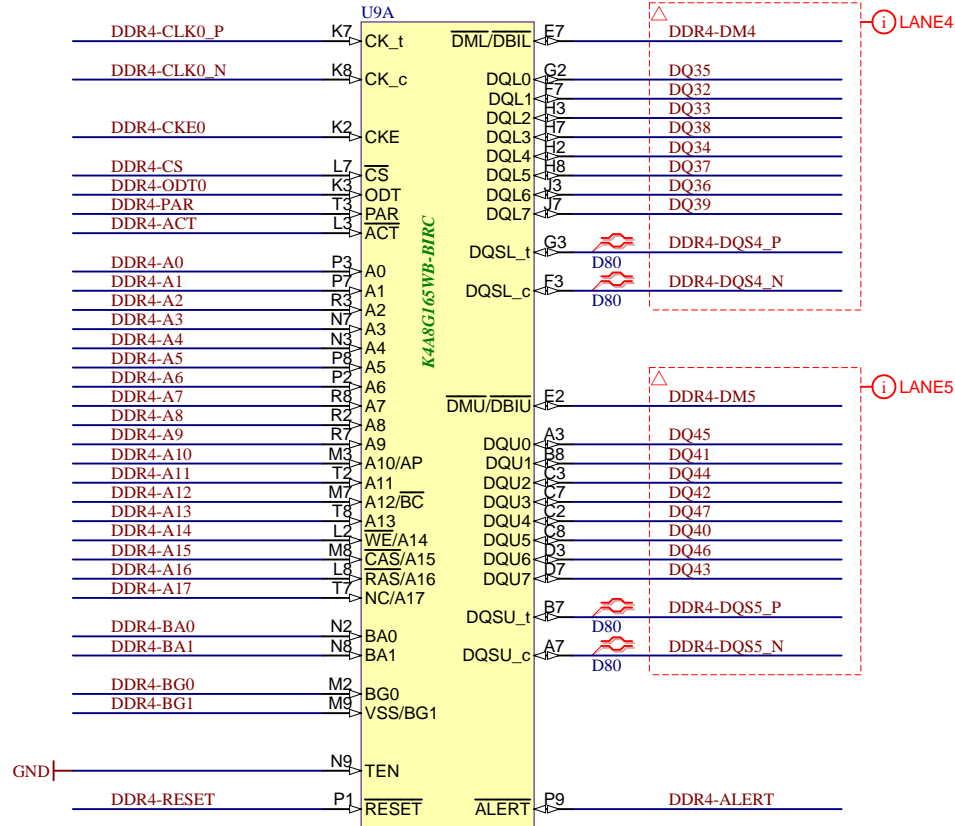
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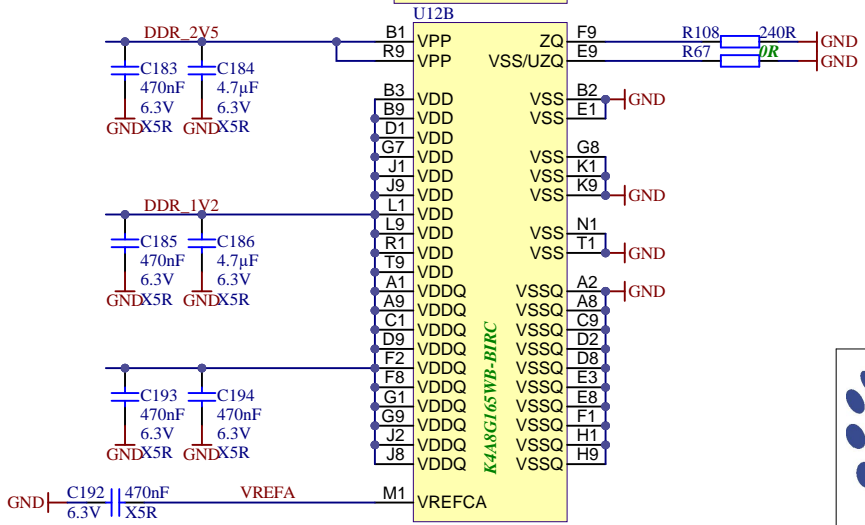
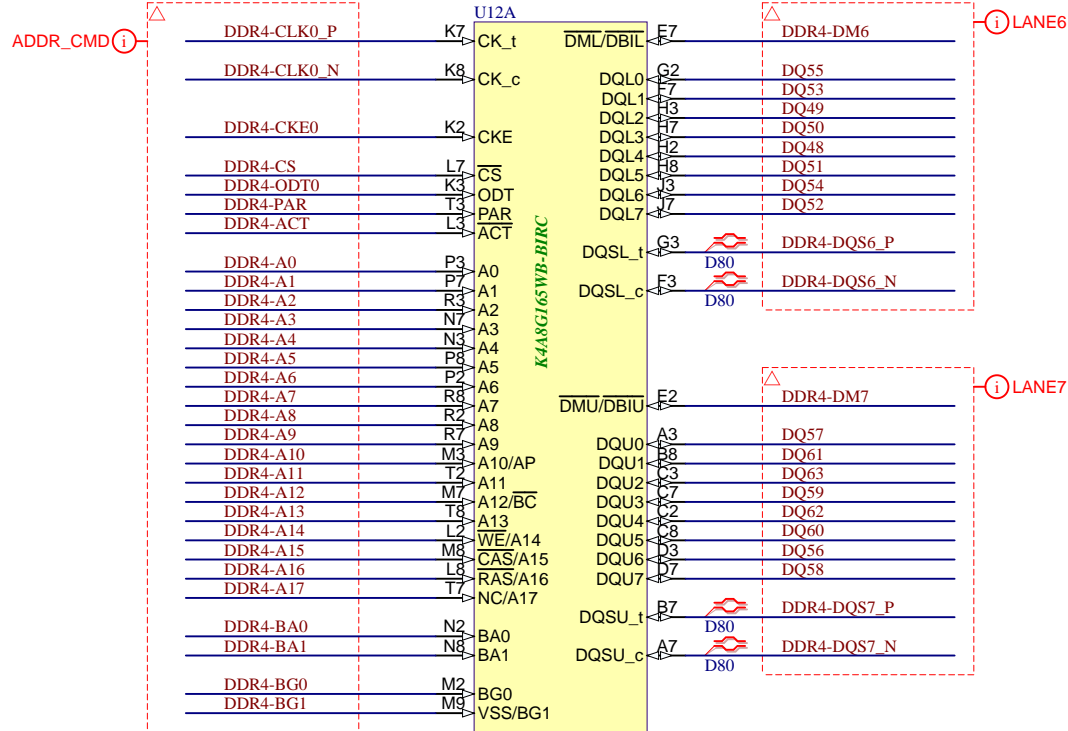
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Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page20 of 30
Filename: DDR4-RAM.SchDoc		



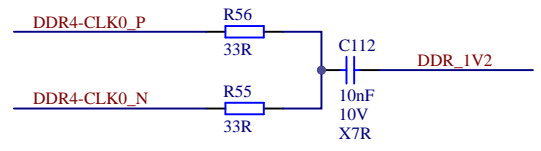
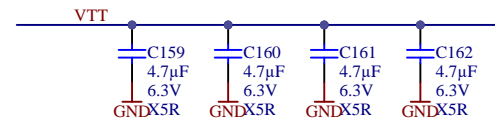
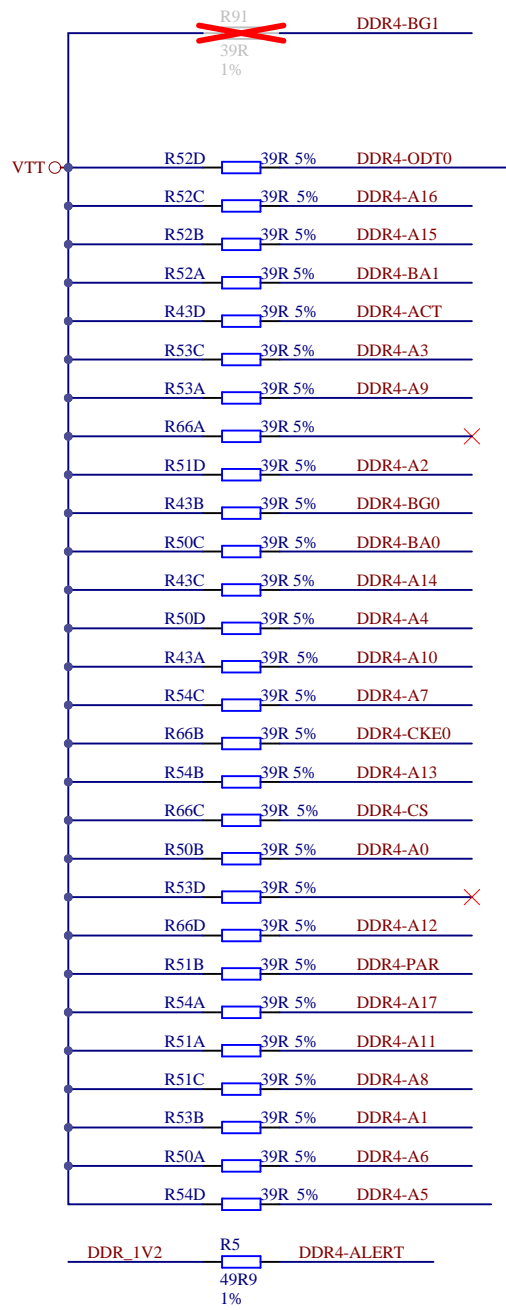
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A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page21 of 30
Filename: DDR4-RAM_2.SchDoc		



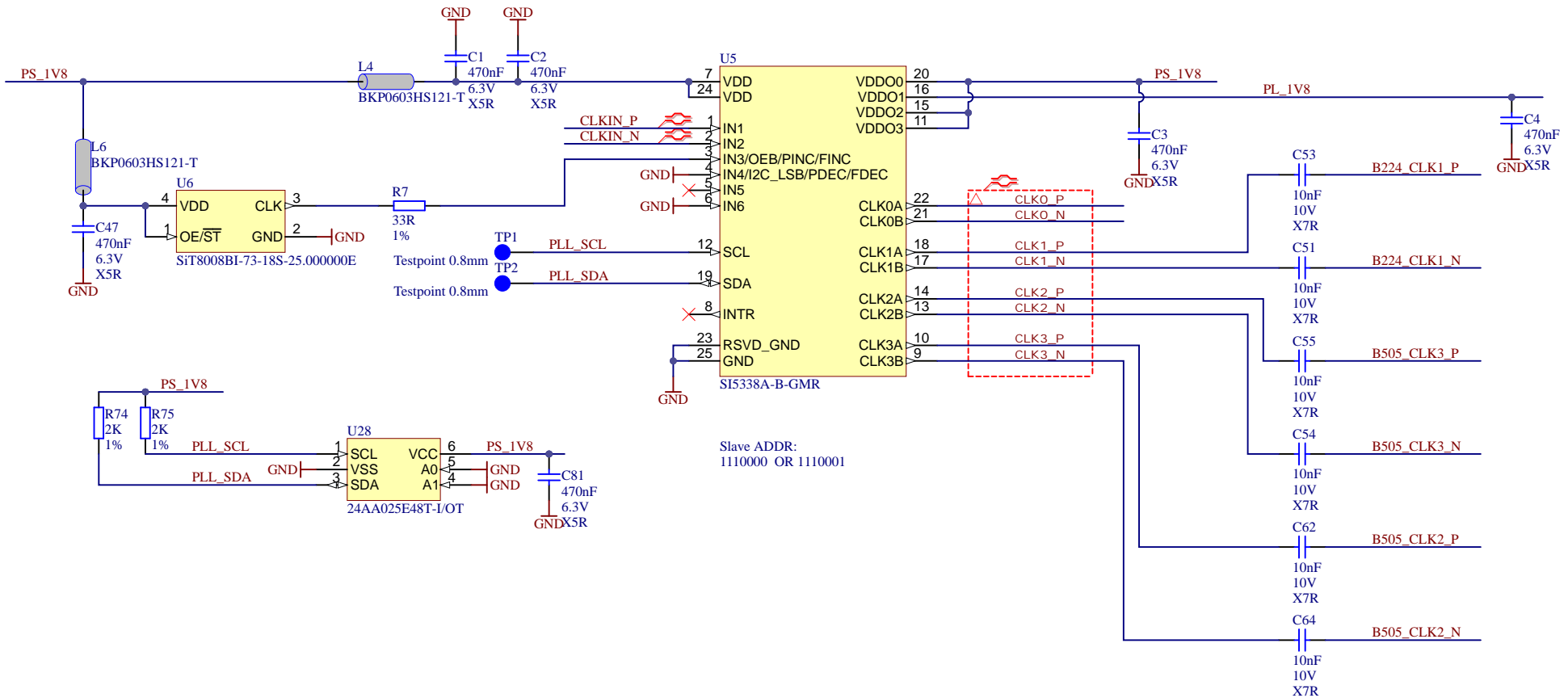
Title: TE0803 - DDR4_3_RAM		
A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page22 of 30
Filename: DDR4-RAM_3.SchDoc		



Title: TE0803 - DDR4_4_RAM		
A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page23 of 30
Filename: DDR4-RAM_4.SchDoc		



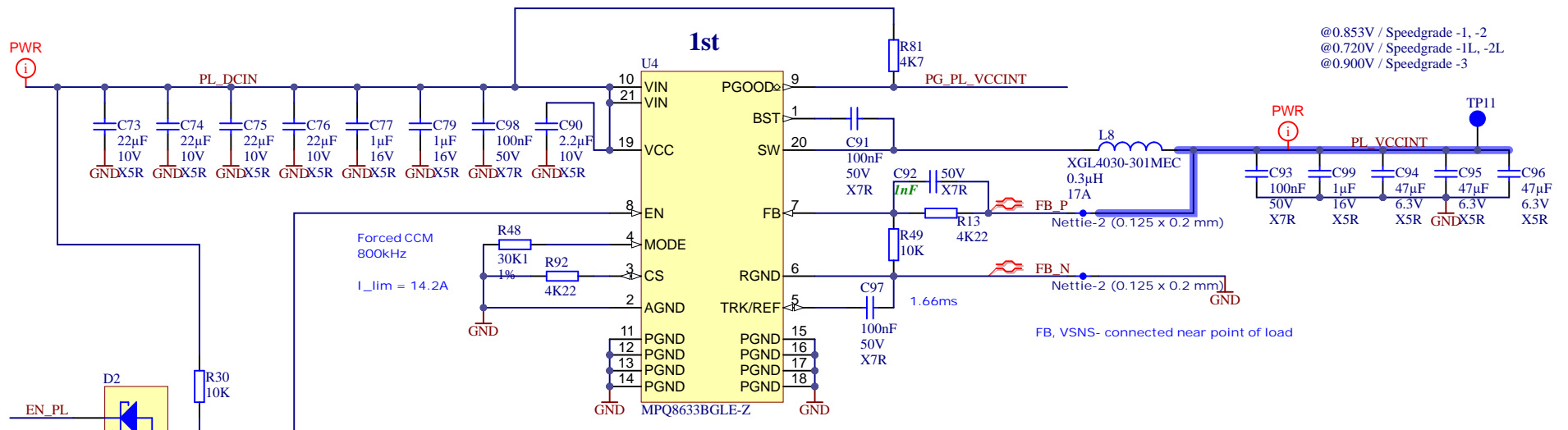
Title: TE0803 - DDR4_TERM		
A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page24 of 30
Filename: DDR4-TERM.SchDoc		



Slave ADDR:
1110000 OR 1110001

Title: TE0803 - CLOCK		
A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 25 of 30
Filename: Clock.SchDoc		

PL VCCINT



@0.853V / Speedgrade -1, -2
 @0.720V / Speedgrade -1L, -2L
 @0.900V / Speedgrade -3

Forced CCM
 800kHz
 I_lim = 14.2A

FB, VSNS- connected near point of load

FPGA Speed grade:		
-1L1 / -2LE	R13 - 2K, R49 - 10K	PL_VCCINT = 0.720V
-1 / -2	R13 - 4K22, R49 - 10K	PL_VCCINT = 0.853V
-3E	R13 - 10K, R49 - 20K	PL_VCCINT = 0.900V

U4 pin compatible with
 -- TPS548A28 (15A)
 -- TPS548B28 (20A)
 -- TPS54JA20 (12A)
 -- MPQ8633B (20A)

U4 can be either TPS548A28RWW or MPQ8633BGL-E-Z which is up to Trenz Electronic GmbH.

	Title: TE0803 - POWER	
	A4	Number: TE0803 5DI21-AZ
	Date: 2021-01-19	Rev. 04
	Page 26 of 30	Copyright: Trenz Electronic GmbH / TT
Filename: POWER.SchDoc		

1

2

3

4

A

A

B

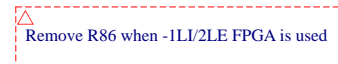
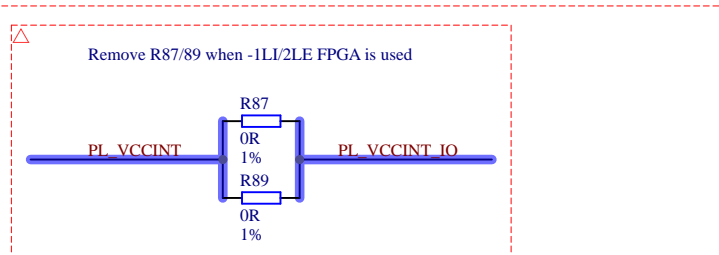
B

C

C

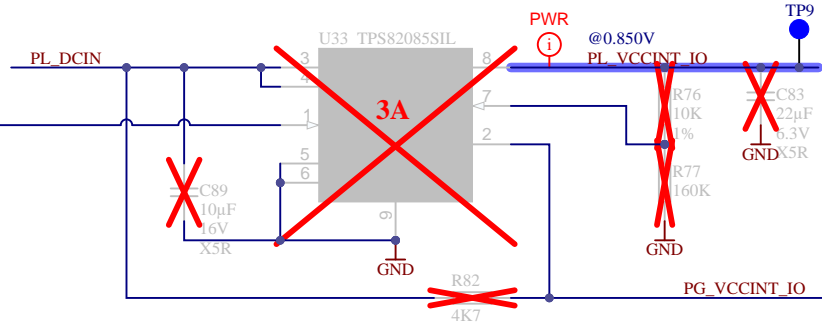
D

D

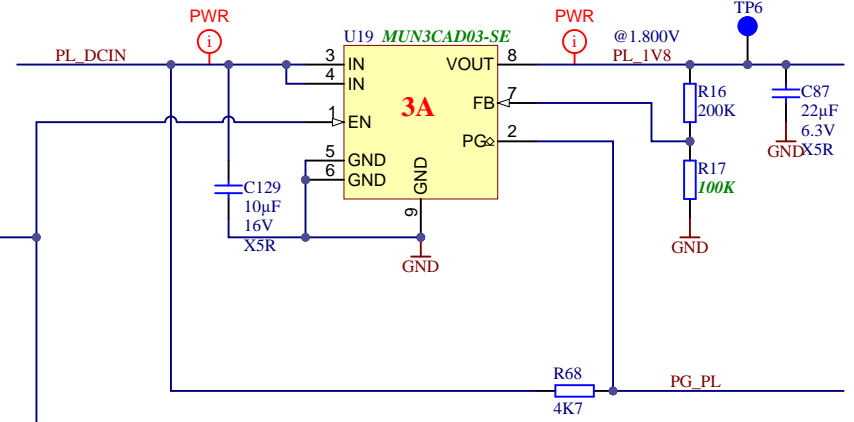


VCCINT_IO & VCCBRAM

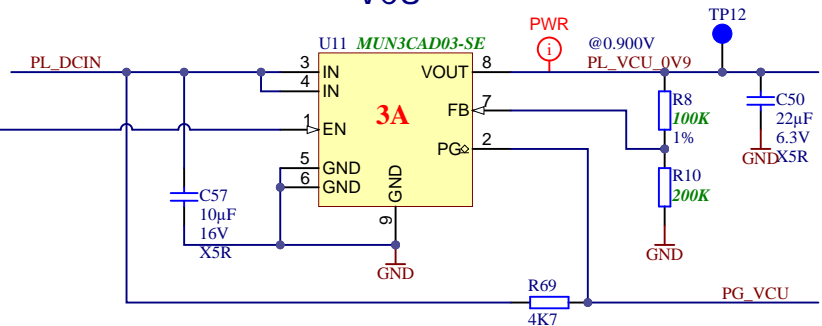
Add U33 when -1L1/2LE FPGA is used



PL VCCIO



VCU



Title: TE0803 - POWER		
A4	Number: TE0803 5DI21-AZ	Rev. 04
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Filename: POWER_1.SchDoc		

1

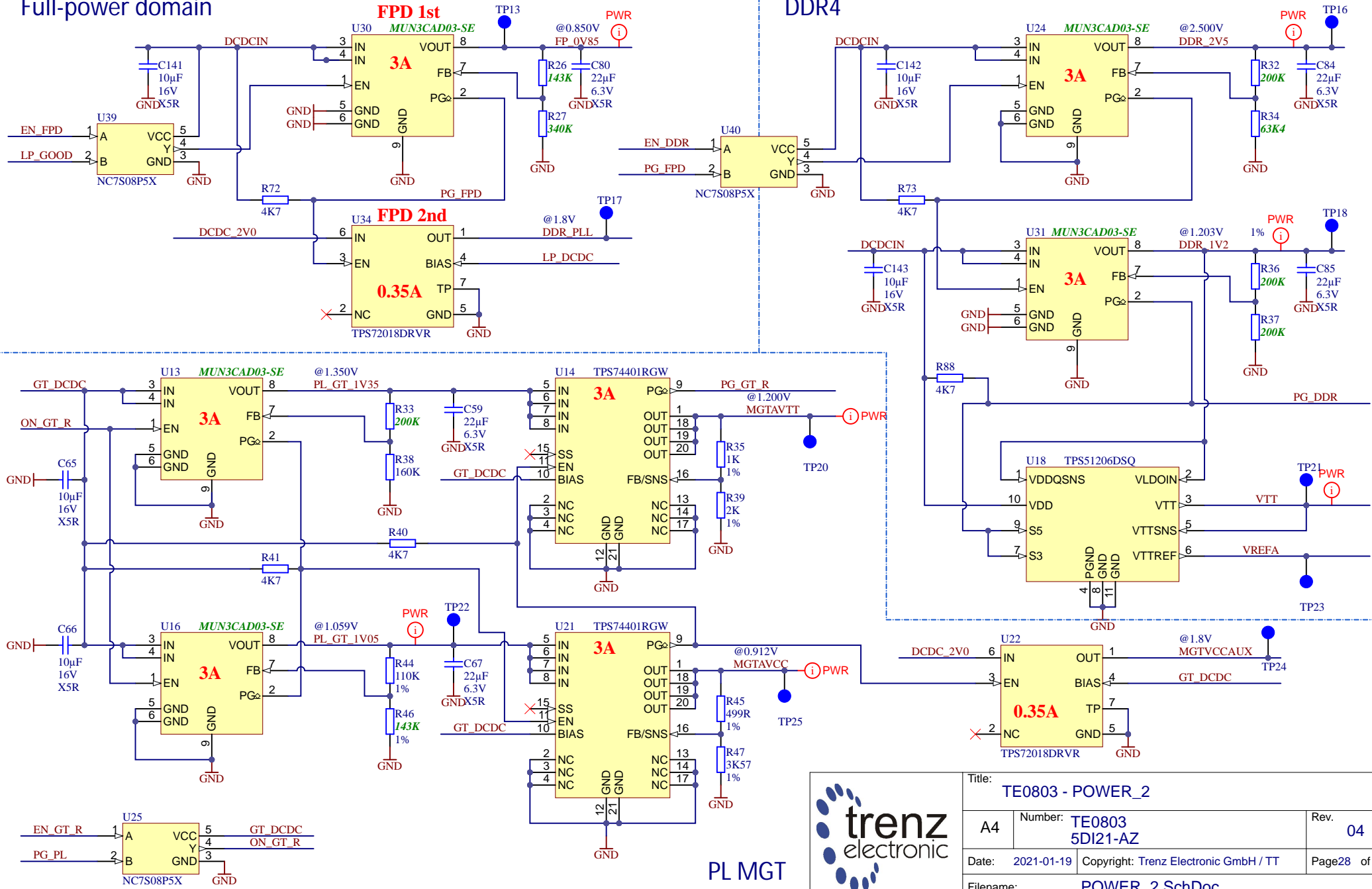
2

3

4

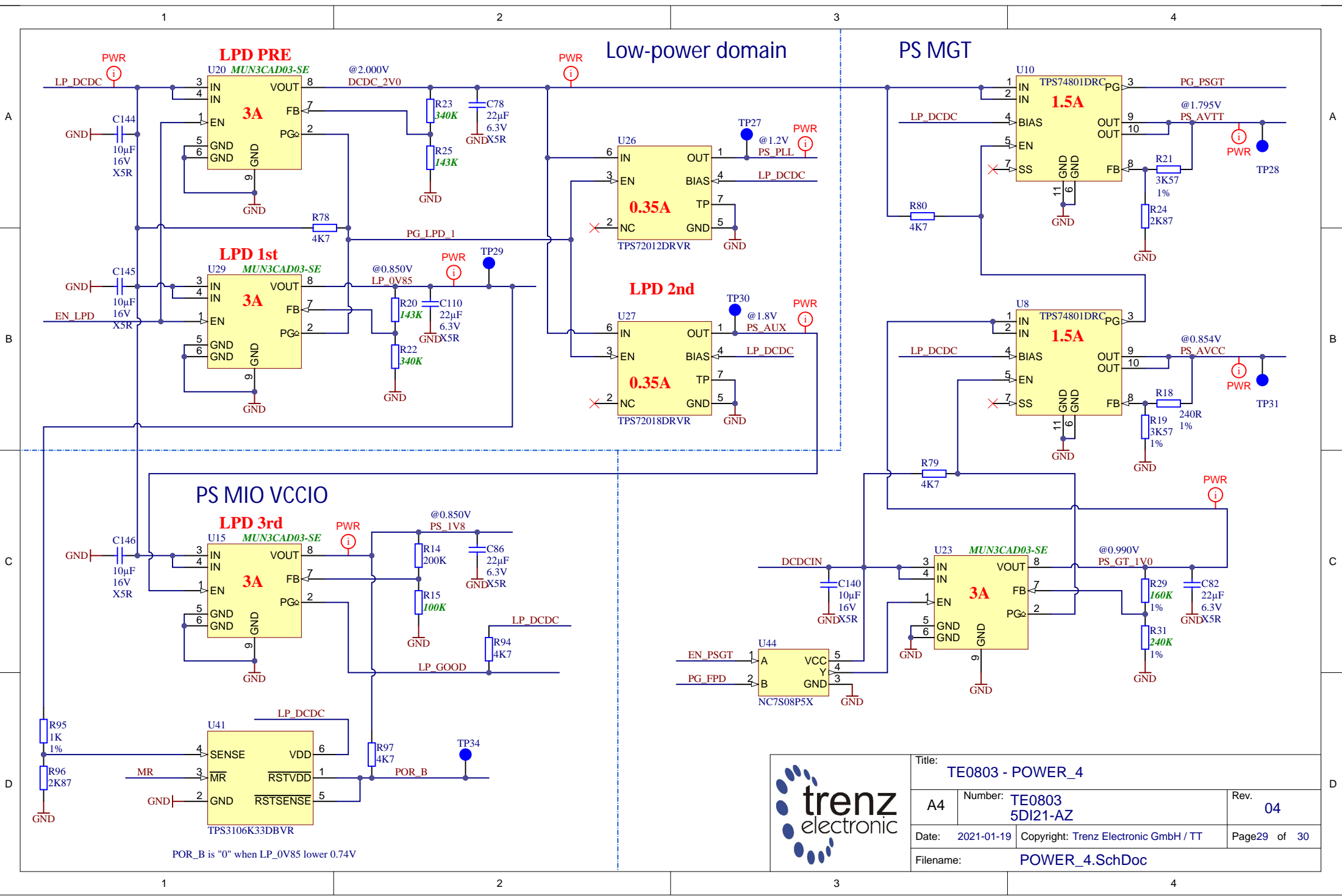
Full-power domain

DDR4



Title: TE0803 - POWER_2		
A4	Number: TE0803 5DI21-AZ	Rev. 04
Date: 2021-01-19	Copyright: Trenz Electronic GmbH / TT	Page 28 of 30
Filename: POWER_2.SchDoc		

PL MGT



Low-power domain

PS MGT


PS MIO VCCIO



Title: TE0803 - POWER_4		
A4	Number: TE0803 5DI21-AZ	Rev. 04
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Filename: POWER_4.SchDoc		

POR_B is "0" when LP_OV85 lower 0.74V

REV	DATE	Description	
-01		Initial revision	VT
-01a	20.11.2017	1. VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9;	VT
-02	20.06.2018	1. Added LDO to DDR_PLL 2. All differential pairs with length matched with tolerance 0.1mm (excluding package delays) 3. Added MAC EEPROM U28 4. VPS_MGTRAVCC set to 0.85V 5. Added pull-up resistors R68,R69	VT
-03	21.02.2019	1. Added support of DDP DDR4 2. Added support of Low power FPGA (-L1/L2). 3. Revised testpoints 4. Revised J1-J4 connectors net label style	VY
-04	15.12.2020	1. Revised PL_VCCINT power supply. EN63A0QI replaced by TPS548A28RWWR. PCB: revised routing and components placement; 2. Added support of wide SDRAM DDR4 packages. PCB: revised routing and components placement; 3. Added option to select POR_OVERRIDE level (R12 and R93) 4. VCCO pins if unused Bank 44 connected together. Same for unused Bank 24 (UG583 recommendation) 5. PCB: updated signal trace lengths. 6. PCB: updated silkscreen. Added company address, CE and WEEE symbols; 7. PCB: added module orientation rectangle pointer 8. Changed resistors value of R29, R31, R35, R39, R44-R47 (BOM optimization) 9. Removed traceability part (Obsolete component)	VY
-04	23.02.2022	10. Changed capacitor C92 for all variants from 100 nF to 1 nF.	ED
-04	08.06.2023	11. U4 can be either TPS548A28RWWR or MPQ8633BGLE-Z which is up to Trenz Electronic GmbH.	VY

				Title: TE0803 - Revision History	
				A4	Number: TE0803 5DI21-AZ
Date: 2021-01-19		Copyright: Trenz Electronic GmbH		Page 30 of 30	
Drawn by: VY			Filename: Revision Changes.SchDoc		