TE0803 StarterKit

Revision: v.21
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Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation

Overview

Linux with basic periphery of TE0808 Starterkit (TEBF0808 Carrier).

Key Features

- TEBF0808
- Linux
- USB
- ETH
- PCIe
- SATA
- SD
- I2C
- RGPIO
- user LED access
- Modified FSBL for Si5345 programming
- Special FSBL for QSPI Programming

Revision History

Date	Vivado	Project Built	Authors	Description
2018-05-17	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_09_20180517141540.zip TE0803-Starterkit-vivado_2017.4-build_09_20180517141523.zip	John Hartfiel	• new assembly variant • solved Linux flash issue
2018-04-11	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_07_20180411082139.zip TE0803-Starterkit-vivado_2017.4-build_07_20180411082116.zip	John Hartfiel	• bugfix TE0803-01-04EG board part file
2018-02-13	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_06_20180213120642.zip TE0803-Starterkit-vivado_2017.4-build_06_20180213120615.zip	John Hartfiel	• new assembly variant
2018-02-06	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_05_20180206082527.zip TE0803-Starterkit-vivado_2017.4-build_05_20180206082513.zip	John Hartfiel	• same CLK for both VIO
2018-02-05	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_05_20180205154248.zip TE0803-Starterkit-vivado_2017.4-build_05_20180205154230.zip	John Hartfiel	• new assembly variant • solved JTAG/Linux issue
2018-01-31	2017.4	TE0803-Starterkit-vivado_2017.4-build_05_20180131124042.zip TE0803-Starterkit_noprebuilt-vivado_2017.4-build_05_20180131124057.zip	John Hartfiel	• new assembly variant

Date	Vivado	Project Built	Authors	Description
2018-01-18	2017.4	TE0803-Starterkit-vivado_2017.4-build_05_20180118164553.zip TE0803-Starterkit_noprebuilt-vivado_2017.4-build_05_20180118164613.zip	John Hartfiel	• initial release

Release Notes and Know Issues

Issues	Description	Workaround/Solution	To be fixed version
Flash access on Linux	Device tree is not correct on Linux	add compatibility to "compatible “jedec, spi-nor”"	**Solved** with 20180517 update
USB UART Terminal is blocked / SDK Debugging is blocked	This happens only with 2017.4 Linux , when JTAG connection is established on Vivado HW Manager.	Do not use HW Manager connection, or if debugging is nessecary: 1. Boot linux with usb terminal 2. From the terminal: root root mount ifconfig eth0 3. Open two new SSH terminals via ethernet: root root , run user application ... 4. Exit and close the usb terminal	**Solved** with 20180205 update

Requirements

Software

Software	Version	Note
Vivado	2017.4	needed
SDK	2017.4	needed
PetaLinux	2017.4	needed

Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TE0803-ES1	es1_sk	REV01	2GB	64MB		
TE0803-01-02EG-1E	2eg_sk	REV01	2GB	64MB		
TE0803-01-02CG-1E	2cg_sk	REV01	2GB	64MB		
TE0803-01-03EG-1E	3eg_sk	REV01	2GB	64MB		

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TE0803-01-03CG-1E	3cg_sk	REV01	2GB	64MB		
TE0803-01-02EG-1EA	2eg_sk	REV01	2GB	128MB		
TE0803-01-02CG-1EA	2cg_sk	REV01	2GB	128MB		
TE0803-01-03EG-1EA	3eg_sk	REV01	2GB	128MB		
TE0803-01-03EG-1EB	3egb_sk	REV01	4GB	128MB		
TE0803-01-03CG-1EA	3cg_sk	REV01	2GB	128MB		
TE0803-01-04CG-1EA	4cg_sk	REV01	2GB	128MB		
TE0803-01-04EV-1EA	4ev_sk	REV01	2GB	128MB		
TE0803-01-04EV-1E3	4ev_sk	REV01	2GB	128MB	1 mm connectors	
TE0803-01-04EG-1EA	4eg_sk	REV01	2GB	128MB		
TE0803-01-04CG-1EB	4cg_sk	REV01	2GB	256MB		
TE0803-01-05EV-1EA	5ev_sk	REV01	2GB	128MB		
TE0803-01-05EV-1IA	5ev_i_sk	REV01	2GB	128MB		

Note: Design contains also Board Part Files for TE0808 only configuration, this boart part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
TEBF0808	Used as reference carrier.

Additional HW Requirements:

Additional Hardware	Notes

Content

For general structure and of the reference design, see Project Delivery

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

Additional Sources

Type	Location	Notes
SI5338	<design name>/misc/Si5338	SI5338 Project with current PLL Configuration

Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0803 "StarterKit" Reference Design

Design Flow

⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

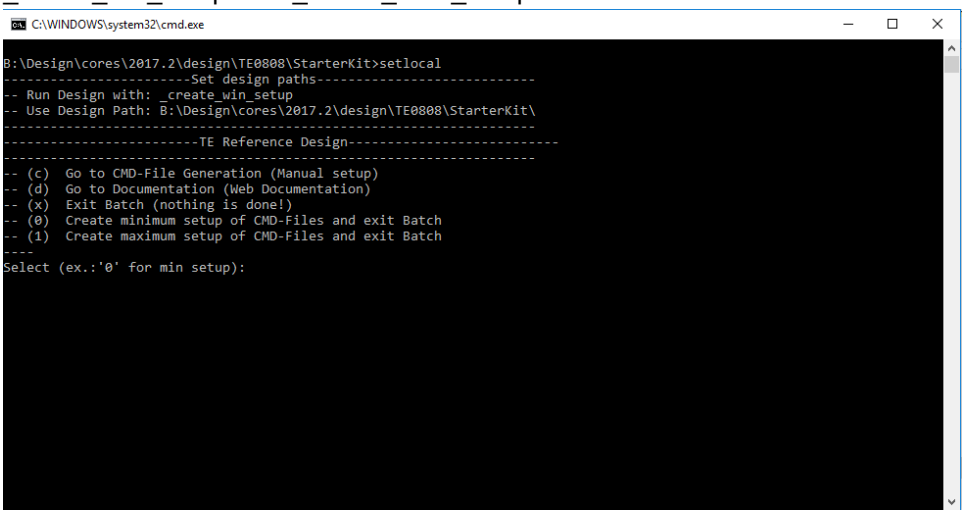
See also:

- Vivado/SDK/SDSoC#XilinxSoftware-BasicUserGuides
- Vivado Projects
- Project Delivery.

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
    a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
    Note: Select correct one, see TE Board Part Files
    Important: Use Board Part Files, which ends with *_tebf0808

5. Create HDF and export to prebuilt folder
    a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
    Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (bl31.elf, uboot.elf and image.ub) with exported HDF
    a. HDF is exported to "prebuilt\hardware\<short name>"
    Note: HW Export from Vivado GUI create another path as default workspace.
    b. Create Linux images on VM, see PetaLinux KICKstart
        i. Use TE Template from /os/petalinux
        Note: run init_config.sh before you start petalinux config. This will set correct temporary path variable.
7. Add Linux files (bl31.elf, uboot.elf and image.ub) to prebuilt folder
    a. "prebuilt\os\petalinux\default" or "prebuilt\os\petalinux\<short name>"
    Notes: Scripts select "prebuilt\os\petalinux\<short name>", if exist, otherwise "prebuilt\os\petalinux\default"
8. Generate Programming Files with HSI/SDK
    a. Run on Vivado TCL: TE::sw_run_hsi
    Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
    b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
    Note: See SDK Projects

Launch

Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging

QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
4. Copy image.ub on SD-Card
5. Insert SD-Card

SD

1. Copy image.ub and Boot.bin on SD-Card.
   - For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Set Boot Mode to SD-Boot.
3. Insert SD-Card in SD-Slot.

JTAG

Not used on this Example.

Usage

1. Prepare HW like described on section Programming
2. Connect UART USB (JTAG XMOD)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)
   Note: See TRM of the Carrier, which is used.
4. (Optional) Insert PCIe Card (detection depends on Linux driver. Only some basic drivers are installed)
5. (Optional) Connect Sata Disc

6. (Optional) Connect DisplayPort Monitor (List of usable Monitors: https://www.xilinx.com/support/answers/68671.html)
7. (Optional) Connect Network Cable
8. Power On PCB
   Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD into OCM, 2. FSBL loads ATF (bl31.elf) and U-boot from SD/QSPI into DDR, 3. U-boot load Linux from SD into DDR.

Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root
3. You can use Linux shell now.
   a. I2C 0 Bus type: i2cdetect -y -r 0
   b. ETH0 works with udhcpc
   c. USB type "lsusb" or connect USB device
   d. PCIe type "lspci"

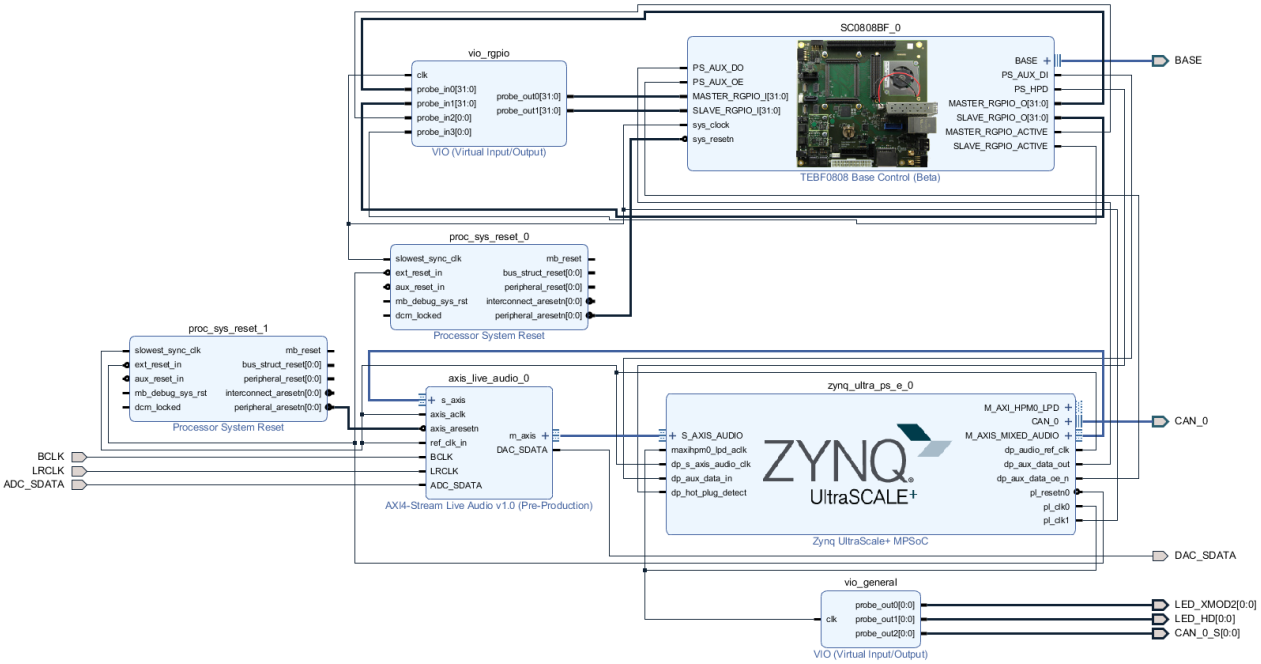
Vivado Hardware Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).

- RGPIO Interface:
  - Set Bit 31-28 to "1010" to activat RGPIO Interface of Master or Slave CPLD.
    - Description: TEBF0808 Master CPLD#RGPIO, TEBF0808 Slave CPLD#RGPIO
- LED Control:
  - XMOD 2(without green dot) and HD LED are accessible.

System Design - Vivado

Block Design



PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
CAN0	EMIO
I2C0	MIO
PJTAG0	MIO
UART0	MIO
GPIO0	MIO
SWDT0..1	
TTC0..3	
GEM3	MIO

Type	Note
USB0	MIO/GTP
PCIe	MIO/GTP
SATA	GTP

Constrains

Basic module constrains

_i_bitgen.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

Design specific constrain

_i_io.xdc

```
# system controller ip
set_property PACKAGE_PIN A13 [get_ports BASE_sc10_io]
set_property PACKAGE_PIN B13 [get_ports BASE_sc11]
set_property PACKAGE_PIN A14 [get_ports BASE_sc12]
set_property PACKAGE_PIN B14 [get_ports BASE_sc13]
set_property PACKAGE_PIN F13 [get_ports BASE_sc14]
set_property PACKAGE_PIN G13 [get_ports BASE_sc15]
set_property PACKAGE_PIN D15 [get_ports BASE_sc5]
set_property PACKAGE_PIN H13 [get_ports BASE_sc6]
set_property PACKAGE_PIN H14 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc5]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc6]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc10_io]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc11]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc12]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc13]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc14]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc15]

# Audio Codec
#LRCLK          J3:49
#BCLK            J3:51
#DAC_SDATA    J3:53
#ADC_SDATA    J3:55
set_property PACKAGE_PIN L13 [get_ports LRCLK ]
set_property PACKAGE_PIN L14 [get_ports BCLK ]
set_property PACKAGE_PIN E15 [get_ports DAC_SDATA ]
set_property PACKAGE_PIN F15 [get_ports ADC_SDATA ]
set_property IOSTANDARD LVCMOS18 [get_ports LRCLK ]
set_property IOSTANDARD LVCMOS18 [get_ports BCLK ]
set_property IOSTANDARD LVCMOS18 [get_ports DAC_SDATA ]
set_property IOSTANDARD LVCMOS18 [get_ports ADC_SDATA ]
#LED
#LED_HD SC0 J3:31
set_property PACKAGE_PIN G14 [get_ports {LED_HD[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {LED_HD[0]}]
#LED_XMOD SC17 J3:48
set_property PACKAGE_PIN B15 [get_ports {LED_XMOD2[0]}]
set_property IOSTANDARD LVCMOS18 [get_ports {LED_XMOD2[0]}]

# CAN
#CAN RX SC19 J3:52 B26_L11_P
#CAN TX SC18 J3:50 B26_L11_N
#CAN S  SC16 J3:46 B26_L1_N

set_property PACKAGE_PIN A15 [get_ports CAN_0_S ]
set_property IOSTANDARD LVCMOS18 [get_ports CAN_0_S ]
set_property PACKAGE_PIN K14 [get_ports CAN_0_rx ]
set_property IOSTANDARD LVCMOS18 [get_ports CAN_0_rx ]
set_property PACKAGE_PIN J14 [get_ports CAN_0_tx ]
set_property IOSTANDARD LVCMOS18 [get_ports CAN_0_tx ]
```

Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects

Application

zynqmp_fsbl

TE modified 2017.4 FSBL

Changes:

- Si5338Configuration, PCIe Reset over GPIO see xfsbl_board.c and xfsbl_board.h
- Add register_map.h, si5338.c, si5338.h

zynqmp_fsbl_flash

TE modified 2017.4 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

PMU

Xilinx default PMU firmware.

Hello TE0803

Hello TE0803 is a Xilinx Hello World example as endless loop instead of one console output.

U-Boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart

Config

No changes.

U-Boot

- Change platform-top.h

```
#include <configs/platform-auto.h>
#define CONFIG_SYS_BOOTM_LEN 0xF000000

#define DFU_ALT_INFO_RAM \
                "dfu_ram_info=" \
        "setenv dfu_alt_info " \
        "image.ub ram $netstart 0x1e00000\0" \
        "dfu_ram=run dfu_ram_info && dfu 0 ram 0\0" \
        "thor_ram=run dfu_ram_info && thordown 0 ram 0\0"

#define DFU_ALT_INFO  \
                DFU_ALT_INFO_RAM

/*Required for uartless designs */
#ifndef CONFIG_BAUDRATE
#define CONFIG_BAUDRATE 115200
#ifdef CONFIG_DEBUG_UART
#undef CONFIG_DEBUG_UART
#endif
#endif

/*select sd instead of mmc for autoboot */

#define CONFIG_BOOTCOMMAND    "run uenvboot;  mmcinfo && fatload mmc 1 ${netstart}
${kernel_img};bootm ${netstart}"
```

Device Tree

```
/include/ "system-conf.dtsi"
/ {
};

/* default */

/* SD */
```

```
&sdhci1 {
    // disable-wp;
    no-1-8-v;

};

/* USB  */

&dwc3_0 {
    status = "okay";
    dr_mode = "host";
};

/* ETH PHY */

&gem3 {
    phy-handle = <&phy0>;
    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};

/* QSPI */

&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

/* I2C */

&i2c0 {
    i2cswitch@73 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x73>;
        i2c-mux-idle-disconnect;

        i2c@2 { // PCIe
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <2>;
        };
        i2c@3 { // i2c SFP
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <3>;
        };
```

```
        i2c@4 { // i2c SFP
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <4>;
        };
        i2c@5 { // i2c EEPROM
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <5>;
        };
        i2c@6 { // i2c FMC
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <6>;

            si570_2: clock-generator3@5d {
                #clock-cells = <0>;
                compatible = "silabs,si570";
                reg = <0x5d>;
                temperature-stability = <50>;
                factory-fout = <156250000>;
                clock-frequency = <78800000>;
            };
        };
        i2c@7 { // i2c USB HUB
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <7>;
        };
    };
    i2cswitch@77 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x77>;
        i2c-mux-idle-disconnect;
        i2c@0 { // i2c PMOD
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0>;
        };
        i2c@1 { // i2c Audio Codec
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <1>;
            /*
            adau1761: adau1761@38 {
                compatible = "adi,adau1761";
                reg = <0x38>;
            };
            */
        };
        i2c@2 { // i2c FireFly A
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <2>;
        };
        i2c@3 { // i2c FireFly B
```

```
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <3>;
        };
        i2c@4 { // i2c PLL
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <4>;
        };
        i2c@5 { // i2c SC
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <5>;
        };
        i2c@6 { // i2c
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <6>;
        };
        i2c@7 { // i2c
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <7>;
        };
    };
};

/* UNUSED DMA disable */

&lpd_dma_chan1 {
    status = "disabled";
};
&lpd_dma_chan2 {
    status = "disabled";
};
&lpd_dma_chan3 {
    status = "disabled";
};
&lpd_dma_chan4 {
    status = "disabled";
};
&lpd_dma_chan5 {
    status = "disabled";
};
&lpd_dma_chan6 {
    status = "disabled";
};
&lpd_dma_chan7 {
    status = "disabled";
};
&lpd_dma_chan8 {
    status = "disabled";
};
```

Kernel

Deactivate:

- CONFIG_CPU_IDLE (only needed to fix JTAG Debug issue)
- CONFIG_CPU_FREQ (only needed to fix JTAG Debug issue)

Rootfs

Activate:

- i2c-tools

Applications

startup

Script App to load init.sh from SD Card if available.

See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files

adau1761init

Audio initialisation.

Additional Software

SI5338

Download ClockBuilder Desktop for SI5338

1. Install and start ClockBuilder
2. Select SI5338
3. Options Open register map file
   Note: File location <design name>/misc/Si5338/RegisterMap.txt
4. Modify settings
5. Options save C code header files
6. Replace Header files from FSBL template with generated file

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2018-10-26	v.21 Unbekanntes Makro: 'metadata'	John Hartfiel	• new assembly variant • solved known issues
30.04.2018	v.13	John Hartfiel	• Update known Issues
11.04.2018	v.12	John Hartfiel	• bugfix board part files
13.02.2018	v.11	John Hartfiel	• new assembly variant • solved known issues
2018-01-29	v.4	John Hartfiel	• Update known Issues
2018-01-18	v.3	John Hartfiel	• Release 2017.4
	All	John Hartfiel	

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REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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