



TE0803 StarterKit

Revision v.21

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Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0803+StarterKit>

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Online version of this manual and other related documents can be found at <https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation>

4 Overview

Linux with basic periphery of TE0808 Starterkit (TEBF0808 Carrier).

4.1 Key Features

- TEBF0808
- Linux
- USB
- ETH
- PCIe
- SATA
- SD
- I2C
- RGPIO
- DP
- user LED access
- Modified FSBL for Si5338 programming
- Special FSBL for QSPI Programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2018-10-25	2018.2	TE0803-Starterkit-vivado_2018.2-build_03_20181026141553.zip TE0803-Starterkit_noprebuilt-vivado_2018.2-build_03_20181026141611.zip	John Hartfiel	<ul style="list-style-type: none"> • new assembly variant
2018-08-14	2018.2	TE0803-Starterkit-vivado_2018.2-build_02_20180814103204.zip TE0803-Starterkit_noprebuilt-vivado_2018.2-build_02_20180814103221.zip	John Hartfiel	<ul style="list-style-type: none"> • new assembly variant

Date	Vivado	Project Built	Authors	Description
2018-07-23	2018.2	TE0803-Starterkit-vivado_2018.2-build_02_20180723204618.zip TE0803-Starterkit_noprebuilt-vivado_2018.2-build_02_20180723204638.zip	John Hartfiel	<ul style="list-style-type: none"> correction on FSBL
2018-07-12	2018.2	TE0803-Starterkit_noprebuilt-vivado_2018.2-build_02_20180713085800.zip TE0803-Starterkit-vivado_2018.2-build_02_20180713085740.zip	John Hartfiel	<ul style="list-style-type: none"> small petalinux changes IO renaming PL Design changes additional notes for FSBL generated with Win SDK changed *.bif
2018-05-17	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_09_20180517141540.zip TE0803-Starterkit-vivado_2017.4-build_09_20180517141523.zip	John Hartfiel	<ul style="list-style-type: none"> new assembly variant solved Linux flash issue
2018-04-11	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_07_20180411082139.zip TE0803-Starterkit-vivado_2017.4-build_07_20180411082116.zip	John Hartfiel	<ul style="list-style-type: none"> bugfix TE0803-01-04EG board part file

Date	Vivado	Project Built	Authors	Description
2018-02-13	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_06_20180213120642.zip TE0803-Starterkit-vivado_2017.4-build_06_20180213120615.zip	John Hartfiel	<ul style="list-style-type: none"> new assembly variant
2018-02-06	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_05_20180206082527.zip TE0803-Starterkit-vivado_2017.4-build_05_20180206082513.zip	John Hartfiel	<ul style="list-style-type: none"> same CLK for both VIO
2018-02-05	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_05_20180205154248.zip TE0803-Starterkit-vivado_2017.4-build_05_20180205154230.zip	John Hartfiel	<ul style="list-style-type: none"> new assembly variant solved JTAG/Linux issue
2018-01-31	2017.4	TE0803-Starterkit-vivado_2017.4-build_05_20180131124042.zip TE0803-Starterkit_noprebuilt-vivado_2017.4-build_05_20180131124057.zip	John Hartfiel	<ul style="list-style-type: none"> new assembly variant

Date	Vivado	Project Built	Authors	Description
2018-01-18	2017.4	TE0803-Starterkit-vivado_2017.4-build_05_20180118164553.zip TE0803-Starterkit_noprebuilt-vivado_2017.4-build_05_20180118164613.zip	John Hartfiel	<ul style="list-style-type: none"> initial release

4.3 Release Notes and Know Issues

Issues	Description	Workaround/Solution	To be fixed version
Flash access on Linux	Device tree is not correct on Linux	add compatibility to "compatible "jedec,spi-nor""	Solved with 20180517 update
USB UART Terminal is blocked / SDK Debugging is blocked	This happens only with 2017.4 Linux , when JTAG connection is established on Vivado HW Manager.	Do not use HW Manager connection, or if debugging is nessecary: <ol style="list-style-type: none"> 1. Boot linux with usb terminal 2. From the terminal: root root mount ifconfig eth0 3. Open two new SSH terminals via ethernet: root root , run user application ... 4. Exit and close the usb terminal 	Solved with 20180205 update

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vivado	2018.2	needed
SDK	2018.2	needed
PetaLinux	2018.2	needed

4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).¹

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TE0803-ES1	es1_sk	REV01	2GB	64MB		Xilinx has stopped ES1 support with 2018.2, please use 2017.4 reference design
TE0803-01-02EG-1E	2eg_sk	REV01	2GB	64MB		
TE0803-01-02CG-1E	2cg_sk	REV01	2GB	64MB		
TE0803-01-03EG-1E	3eg_sk	REV01	2GB	64MB		
TE0803-01-03CG-1E	3cg_sk	REV01	2GB	64MB		

¹ <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TE0803-01-02EG-1EA	2eg_sk	REV01	2GB	128MB		
TE0803-01-02CG-1EA	2cg_sk	REV01	2GB	128MB		
TE0803-01-03EG-1EA	3eg_sk	REV01	2GB	128MB		
TE0803-02-03EG-1EB	3egb_sk	REV02, REV01	4GB	128MB		
TE0803-01-03CG-1EA	3cg_sk	REV01	2GB	128MB		
TE0803-01-04CG-1EA	4cg_sk	REV01	2GB	128MB		
TE0803-01-04EV-1EA	4ev_sk	REV01	2GB	128MB		
TE0803-01-04EV-1E3	4ev_sk	REV01	2GB	128MB	1 mm connectors	
TE0803-02-04EV-1EB	4evb_sk	REV02	4GB	128MB		
TE0803-02-04EV-1E3	4evb_sk	REV02	4GB	128MB	1 mm connectors	
TE0803-01-04EG-1EA	4eg_sk	REV01	2GB	128MB		
TE0803-02-04EG-1IC	4eg_i_sk	REV02	8GB	128MB		
TE0803-01-04CG-1EB	4cg_sk	REV01	2GB	256MB		
TE0803-01-05EV-1EA	5ev_sk	REV01	2GB	128MB		
TE0803-01-05EV-1IA	5ev_i_sk	REV01	2GB	128MB		

Note: Design contains also Board Part Files for TE0808 only configuration, this board part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
TEBF0808	Used as reference carrier.

Additional HW Requirements:

Additional Hardware	Notes
---------------------	-------

4.5 Content

For general structure and of the reference design, see [Project Delivery](#)²

4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for SDK/ HSI and apps_list.csv with settings for HSI
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

4.5.2 Additional Sources

Type	Location	Notes
SI5338	<design name>/misc/SI5338	SI5338 Project with current PLL Configuration

² <https://wiki.trenz-electronic.de/display/PD/Project+Delivery>

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0803 "StarterKit" Reference Design³](#)

³ https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0803/Reference_Design/2018.2/StarterKit

5 Design Flow

⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

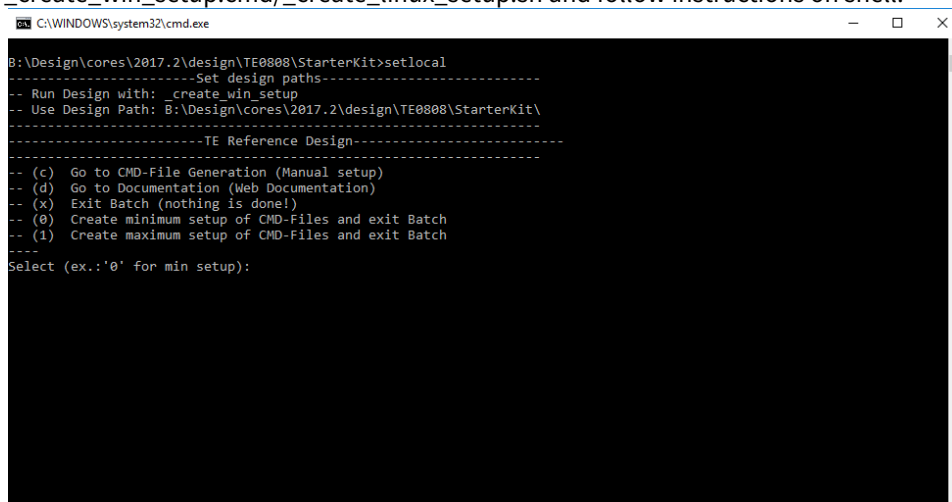
See also:

- [Vivado/SDK/SDSoC](#)⁴
- [Vivado Projects](#)⁵
- [Project Delivery](#).⁶

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)⁷

1. `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell:



```

C:\WINDOWS\system32\cmd.exe
B:\Design\cores\2017.2\design\TE0808\StarterKit>setlocal
-----Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: B:\Design\cores\2017.2\design\TE0808\StarterKit\
-----TE Reference Design-----
-- (c) Go to CMD-File Generation (Manual setup)
-- (d) Go to Documentation (Web Documentation)
-- (x) Exit Batch (nothing is done!)
-- (0) Create minimum setup of CMD-Files and exit Batch
-- (1) Create maximum setup of CMD-Files and exit Batch
-----
Select (ex.: '0' for min setup):
  
```

2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project
 - a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guiemode.cmd"

Note: Select correct one, see [TE Board Part Files](#)⁸

Important: Use Board Part Files, which ends with *_tebf0808
5. Create HDF and export to prebuilt folder
 - a. Run on Vivado TCL: `TE::hw_build_design -export_prebuilt`

Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (bl31.elf, uboot.elf and image.ub) with exported HDF

⁴ <https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=14746264#Vivado/SDK/SDSoC-XilinxSoftware-BasicUserGuides>

⁵ <https://wiki.trenz-electronic.de/display/PD/Vivado+Projects>

⁶ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery>

⁷ <https://wiki.trenz-electronic.de/display/PD/Project+Delivery#ProjectDelivery-Currentlylimitationsoffunctionality>

⁸ <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>


- a. HDF is exported to "prebuilt\hardware\"
Note: HW Export from Vivado GUI create another path as default workspace.
Create Linux images on VM, see [PetaLinux KICKstart](#)⁹
 - i. Use TE Template from /os/petalinux
Note: run init_config.sh before you start petalinux config. This will set correct temporary path variable.
7. Add Linux files (bl31.elf, uboot.elf and image.ub) to prebuilt folder
 - a. "prebuilt\os\petalinux\default" or "prebuilt\os\petalinux\"
Notes: Scripts select "prebuilt\os\petalinux\", if exist, otherwise "prebuilt\os\petalinux\default"
8. Generate Programming Files with HSI/SDK
 - a. Run on Vivado TCL: TE::sw_run_hsi
Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
 - b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
Note: See [SDK Projects](#)¹⁰

⁹ <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

¹⁰ <https://wiki.trenz-electronic.de/display/PD/SDK+Projects>

6 Launch

6.1 Programming

 Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](#)¹¹

6.1.1 QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guiemode.cmd" or if not created, create with "vivado_create_project_guiemode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp u-boot
Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
optional "TE::pr_program_flash_binfile -swapp hello_te0803" possible
4. Copy image.ub on SD-Card
5. Insert SD-Card

6.1.2 SD

1. Copy image.ub and Boot.bin on SD-Card.
 - For correct prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Set Boot Mode to SD-Boot.
3. Insert SD-Card in SD-Slot.

6.1.3 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section [Programming](#)(see page 17)
2. Connect UART USB (JTAG XMOD)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)
Note: See TRM of the Carrier, which is used.
4. (Optional) Insert PCIe Card (detection depends on Linux driver. Only some basic drivers are installed)
5. (Optional) Connect Sata Disc
6. (Optional) Connect DisplayPort Monitor (List of usable Monitors: <https://www.xilinx.com/support/answers/68671.html>)
7. (Optional) Connect Network Cable

¹¹ <https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=14746264#Vivado/SDK/SDSoC-XilinxSoftwareProgrammingandDebugging>

8. Power On PCB

Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD into OCM, 2. FSBL loads ATF(bl31.elf) and U-boot from SD/QSPI into DDR, 3. U-boot load Linux from SD into DDR.

6.2.1 Linux

1. Open Serial Console (e.g. putty)

- a. Speed: 115200
- b. COM Port: Win OS, see device manager, Linux OS see `dmesg |grep tty` (UART is *USB1)

2. Linux Console:

Note: Wait until Linux boot finished For Linux Login use:

- a. User Name: root
- b. Password: root

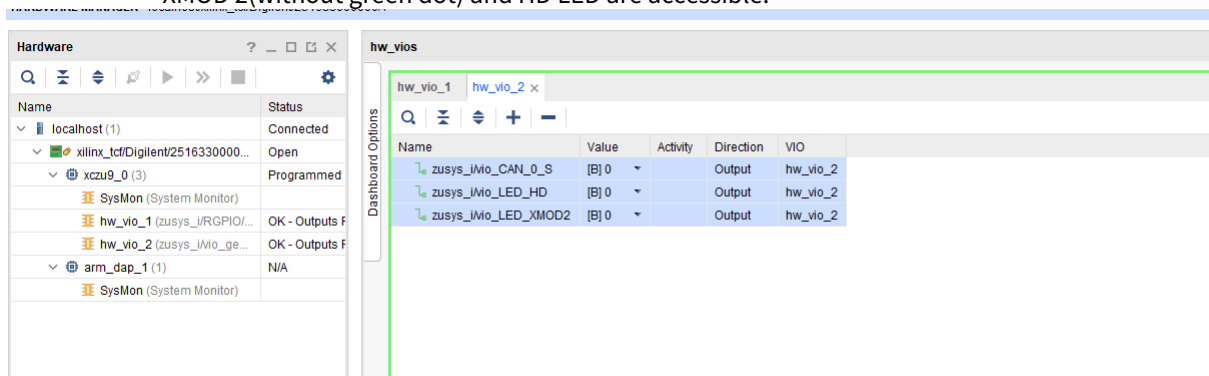
3. You can use Linux shell now.

- a. I2C 0 Bus type: `i2cdetect -y -r 0`
- b. ETH0 works with `udhpcp`
- c. USB type "lsusb" or connect USB device
- d. PCIe type "lspci"

6.2.2 Vivado Hardware Manager

Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).

- RGPIO Interface:
 - Set Enable to send Write data over RGPIO interface.
 - Important, see description to set correct values: [TEBF0808 Master CPLD¹²](#), [TEBF0808 Slave CPLD¹³](#)
- LED Control +CAN_S:
 - XMOD 2(without green dot) and HD LED are accessible.



12 <https://wiki.trenz-electronic.de/display/PD/TEBF0808+Master+CPLD#TEBF0808MasterCPLD-RGPIO>

13 <https://wiki.trenz-electronic.de/display/PD/TEBF0808+Slave+CPLD#TEBF0808SlaveCPLD-RGPIO>

Hardware

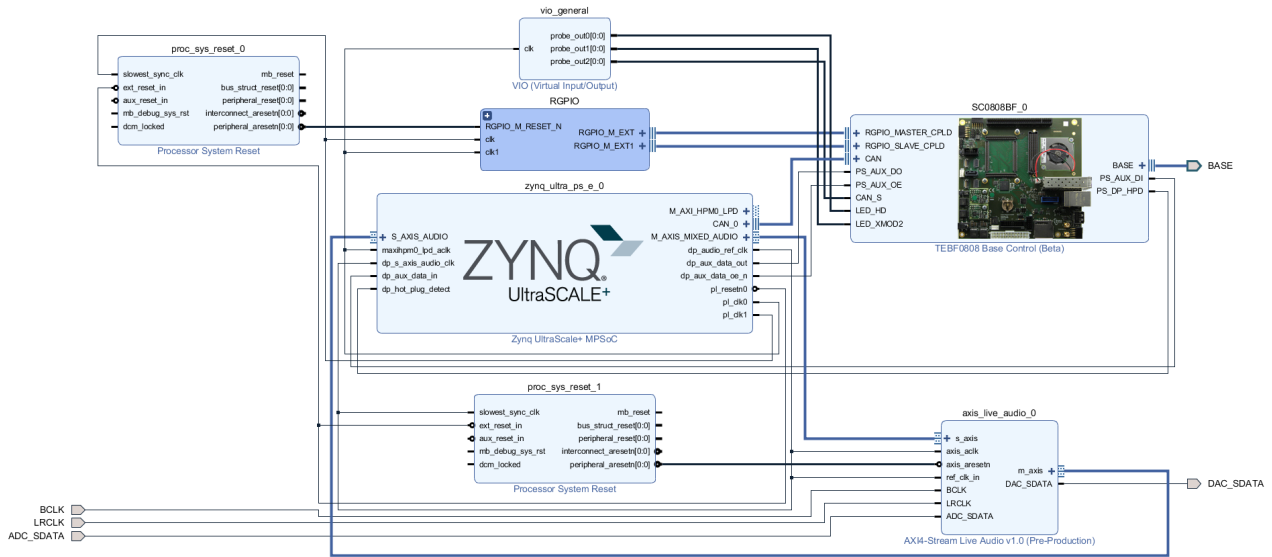
Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/2516330000...	Open
xczu9_0 (3)	Programmed
SystemMon (System Monitor)	
hw_vio_1 (zusys_i/RGPIO/...	OK - Outputs F
hw_vio_2 (zusys_i/Vio_ge...	OK - Outputs F
arm_dap_1 (1)	N/A
SystemMon (System Monitor)	

hw_vios

Name	Value	Activity	Direction	VIO
zusys_i/RGPIO/RGPIO_MASTER_CPLD_ENABLE	[B] 0		Output	hw_vio_1
zusys_i/RGPIO/RGPIO_MASTER_CPLD_RX[23:0]	[H] 30_DE08		Input	hw_vio_1
zusys_i/RGPIO/RGPIO_MASTER_CPLD_TX[23:0]	[H] 00_0000		Output	hw_vio_1
zusys_i/RGPIO/RGPIO_SLAVE_CPLD_ENABLE	[B] 0		Output	hw_vio_1
zusys_i/RGPIO/RGPIO_SLAVE_CPLD_RX[23:0]	[H] FF_F51C		Input	hw_vio_1
zusys_i/RGPIO/RGPIO_SLAVE_CPLD_TX[23:0]	[H] 00_0000		Output	hw_vio_1

7 System Design - Vivado

7.1 Block Design



7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
CAN0	EMIO
I2C0	MIO
PJTAG0	MIO
UART0	MIO
GPIO0	MIO
SWDT0..1	

Type	Note
TTC0..3	
GEM3	MIO
USB0	MIO/GTP
PCIe	MIO/GTP
SATA	GTP
DisplayPort	EMIO/GTP

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

7.2.2 Design specific constrain

_i_io.xdc

```

# system controller ip
#LED_HD SC0 J3:31
#LED_XMOD SC17 J3:48
#CAN RX SC19 J3:52 B26_L11_P
#CAN TX SC18 J3:50 B26_L11_N
#CAN S SC16 J3:46 B26_L1_N

set_property PACKAGE_PIN G14 [get_ports BASE_sc0]
set_property PACKAGE_PIN D15 [get_ports BASE_sc5]
set_property PACKAGE_PIN H13 [get_ports BASE_sc6]
set_property PACKAGE_PIN H14 [get_ports BASE_sc7]
set_property PACKAGE_PIN A13 [get_ports BASE_sc10_io]
set_property PACKAGE_PIN B13 [get_ports BASE_sc11]
set_property PACKAGE_PIN A14 [get_ports BASE_sc12]
set_property PACKAGE_PIN B14 [get_ports BASE_sc13]
set_property PACKAGE_PIN F13 [get_ports BASE_sc14]
set_property PACKAGE_PIN G13 [get_ports BASE_sc15]
set_property PACKAGE_PIN A15 [get_ports BASE_sc16]
set_property PACKAGE_PIN B15 [get_ports BASE_sc17]
set_property PACKAGE_PIN J14 [get_ports BASE_sc18]
set_property PACKAGE_PIN K14 [get_ports BASE_sc19 ]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc0]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc5]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc6]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc10_io]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc11]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc12]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc13]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc14]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc15]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc16]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc17]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc18]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc19]

# Audio Codec
#LRCLK J3:49
#BCLK J3:51
#DAC_SDATA J3:53
#ADC_SDATA J3:55
set_property PACKAGE_PIN L13 [get_ports LRCLK ]
set_property PACKAGE_PIN L14 [get_ports BCLK ]
set_property PACKAGE_PIN E15 [get_ports DAC_SDATA ]
set_property PACKAGE_PIN F15 [get_ports ADC_SDATA ]
set_property IOSTANDARD LVCMOS18 [get_ports LRCLK ]
set_property IOSTANDARD LVCMOS18 [get_ports BCLK ]
set_property IOSTANDARD LVCMOS18 [get_ports DAC_SDATA ]
    
```

```
set_property IOSTANDARD LVCMOS18 [get_ports ADC_SDATA ]
```

8 Software Design - SDK/HSI

For SDK project creation, follow instructions from:

[SDK Projects](#)¹⁴

8.1 Application

SDK template in ./sw_lib/sw_apps/ available.

8.1.1 zynqmp_fsbl

TE modified 2018.2 FSBL

Changes:

- Si5338 Configuration, PCIe Reset over GPIO
 - see xfsbl_board.c and xfsbl_board.h, xfsbl_main.c
 - Add register_map.h, si5338.c, si5338.h

Note: Remove compiler flags "-Os -flto -ffat-lto-objects" on 2018.2 SDK to generate FSBL

8.1.2 zynqmp_fsbl_flash

TE modified 2018.2 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

Note: Remove compiler flags "-Os -flto -ffat-lto-objects" on 2018.2 SDK to generate FSBL

8.1.3 zynqmp_pmufw

Xilinx default PMU firmware.

8.1.4 hello_te0803

Hello TE0803 is a Xilinx Hello World example as endless loop instead of one console output.

8.1.5 u-boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

¹⁴ <https://wiki.trenz-electronic.de/display/PD/SDK+Projects>

9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- [PetaLinux KICKstart](#)¹⁵

9.1 Config

Activate:

- SUBSYSTEM_PRIMARY_SD_PSU_SD_1_SELECT

9.2 U-Boot

- Change platform-top.h

```
#include <configs/platform-auto.h>
#define CONFIG_SYS_BOOTM_LEN 0xF000000

#define DFU_ALT_INFO_RAM \
    "dfu_ram_info=" \
    "setenv dfu_alt_info " \
    "image.ub ram $netstart 0x1e00000\0" \
    "dfu_ram=run dfu_ram_info && dfu 0 ram 0\0" \
    "thor_ram=run dfu_ram_info && thordown 0 ram 0\0"

#define DFU_ALT_INFO_MMC \
    "dfu_mmc_info=" \
    "set dfu_alt_info " \
    "${kernel_image} fat 0 1\\\\"; \
    "dfu_mmc=run dfu_mmc_info && dfu 0 mmc 0\0" \
    "thor_mmc=run dfu_mmc_info && thordown 0 mmc 0\0"

/*Required for uartless designs */
#ifndef CONFIG_BAUDRATE
#define CONFIG_BAUDRATE 115200
#endif
#define CONFIG_DEBUG_UART
#undef CONFIG_DEBUG_UART
#endif

/*Define CONFIG_ZYNQMP_EEPROM here and its necessities in u-boot menuconfig if you
had EEPROM memory. */
#ifdef CONFIG_ZYNQMP_EEPROM
#define CONFIG_SYS_I2C_EEPROM_ADDR_LEN 1
#define CONFIG_CMD_EEPROM
#define CONFIG_ZYNQ_EEPROM_BUS 5
#define CONFIG_ZYNQ_GEM_EEPROM_ADDR 0x54
#define CONFIG_ZYNQ_GEM_I2C_MAC_OFFSET 0x20
#endif
```

¹⁵ <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

9.3 Device Tree

```
/include/ "system-conf.dtsi"
/ {
};

/* default */

/* SD */

&sdhci1 {
    // disable-wp;
    no-1-8-v;
};

/* USB */

&dwc3_0 {
    status = "okay";
    dr_mode = "host";
};

/* ETH PHY */

&gem3 {
    phy-handle = <&phy0>;
    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};

/* QSPI */

&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

/* I2C */

&i2c0 {
    i2cswitch@73 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
```

```

#size-cells = <0>;
reg = <0x73>;
i2c-mux-idle-disconnect;

i2c@2 { // PCIe
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <2>;
};
i2c@3 { // i2c SFP
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <3>;
};
i2c@4 { // i2c SFP
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <4>;
};
i2c@5 { // i2c EEPROM
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <5>;
};
i2c@6 { // i2c FMC
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <6>;

    si570_2: clock-generator3@5d {
        #clock-cells = <0>;
        compatible = "silabs,si570";
        reg = <0x5d>;
        temperature-stability = <50>;
        factory-fout = <156250000>;
        clock-frequency = <78800000>;
    };
};
i2c@7 { // i2c USB HUB
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <7>;
};
i2cswitch@77 { // u
    compatible = "nxp,pca9548";
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <0x77>;
    i2c-mux-idle-disconnect;
    i2c@0 { // i2c PMOD
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0>;
    };
};
i2c@1 { // i2c Audio Codec

```

```

        #address-cells = <1>;
        #size-cells = <0>;
        reg = <1>;
        /*
        adau1761: adau1761@38 {
            compatible = "adi,adau1761";
            reg = <0x38>;
        };
        */
};
i2c@2 { // i2c FireFly A
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <2>;
};
i2c@3 { // i2c FireFly B
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <3>;
};
i2c@4 { // i2c PLL
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <4>;
};
i2c@5 { // i2c SC
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <5>;
};
i2c@6 { // i2c
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <6>;
};
i2c@7 { // i2c
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <7>;
};
};
};

/* UNUSED DMA disable */

&lpd_dma_chan1 {
    status = "disabled";
};
&lpd_dma_chan2 {
    status = "disabled";
};
&lpd_dma_chan3 {
    status = "disabled";
};
&lpd_dma_chan4 {
    status = "disabled";
};

```

```
};
&lpad_dma_chan5 {
    status = "disabled";
};
&lpad_dma_chan6 {
    status = "disabled";
};
&lpad_dma_chan7 {
    status = "disabled";
};
&lpad_dma_chan8 {
    status = "disabled";
};
```

9.4 Kernel

Deactivate:

- CONFIG_CPU_IDLE (only needed to fix JTAG Debug issue)
- CONFIG_CPU_FREQ (only needed to fix JTAG Debug issue)

9.5 Rootfs

Activate:

- i2c-tools

9.6 Applications

9.6.1 startup

Script App to load init.sh from SD Card if available.

See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files

10 Additional Software

10.1 SI5338

Download [ClockBuilder Desktop for SI5338](#)¹⁶










1. Install and start ClockBuilder
2. Select SI5338
3. Options → Open register map file
Note: File location <design name>/misc/SI5338/RegisterMap.txt
4. Modify settings
5. Options → save C code header files
6. Replace Header files from FSBL template with generated file

¹⁶ <https://www.silabs.com/products/development-tools/software/clock>

11 Appx. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
 2018-10-26	v.21(see page 6)  Unbekanntes Makro: 'metadata'	John Hartfiel ¹⁷	<ul style="list-style-type: none"> new assembly variant
 14.08.2018	v.19	John Hartfiel	<ul style="list-style-type: none"> design update
 23.07.2018	v.18	John Hartfiel	<ul style="list-style-type: none"> new assembly variant
 20.07.2018	v.16	John Hartfiel	<ul style="list-style-type: none"> Release 2018.2
 17.05.2018	v.14	John Hartfiel	<ul style="list-style-type: none"> new assembly variant solved known issues
 30.04.2018	v.13	John Hartfiel	<ul style="list-style-type: none"> Update known Issues
 11.04.2018	v.12	John Hartfiel	<ul style="list-style-type: none"> bugfix board part files
 13.02.2018	v.11	John Hartfiel	<ul style="list-style-type: none"> new assembly variant solved known issues
2018-01-29	v.4	John Hartfiel	<ul style="list-style-type: none"> Update known Issues
2018-01-18	v.3	John Hartfiel	<ul style="list-style-type: none"> Release 2017.4
	All	John Hartfiel ¹⁸	

¹⁷ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

¹⁸ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

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 2018-09-18

¹⁹ <http://guidance.echa.europa.eu/>

²⁰ <https://echa.europa.eu/candidate-list-table>

²¹ <http://www.echa.europa.eu/>