



## TE0803 StarterKit

Revision v.24

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Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0803+StarterKit>

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## 4 Overview

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Linux with basic periphery of TE0808 Starterkit (TEBF0808 Carrier).

Refer to <http://trenz.org/te0803-info> for the current online version of this manual and other available documentation.

### 4.1 Key Features

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- Vivado 2018.3
- TEBF0808
- Linux
- USB
- ETH
- MAC from EEPROM
- PCIe
- SATA
- SD
- I2C
- RGPIIO
- DP
- user LED access
- Modified FSBL for Si5338 programming
- Special FSBL for QSPI Programming

### 4.2 Revision History

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Date	Vivado	Project Built	Authors	Description
2019-05-07	2018.3	TE0803-StarterKit-vivado_2018.3-build_05_20190507093424.zip TE0803-StarterKit_noprebuilt-vivado_2018.3-build_05_20190507093443.zip	John Hartfie	<ul style="list-style-type: none"> <li>• new assembly variant</li> <li>• TE Script update</li> <li>• rework of the FSBLs</li> <li>• SI5338 CLKBuilder Pro Project</li> <li>• some additional Linux features</li> <li>• MAC from EEPROM</li> <li>• new assembly variants</li> <li>• remove special compiler flags, which was needed in 2018.2</li> </ul>
2018-10-25	2018.2	TE0803-Starterkit-vivado_2018.2-build_03_20181026141553.zip TE0803-Starterkit_noprebuilt-vivado_2018.2-build_03_20181026141611.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>

Date	Vivado	Project Built	Authors	Description
2018-08-14	2018.2	TE0803-Starterkit-vivado_2018.2-build_02_20180814103204.zip TE0803-Starterkit_noprebuilt-vivado_2018.2-build_02_20180814103221.zip	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> </ul>
2018-07-23	2018.2	TE0803-Starterkit-vivado_2018.2-build_02_20180723204618.zip TE0803-Starterkit_noprebuilt-vivado_2018.2-build_02_20180723204638.zip	John Hartfiel	<ul style="list-style-type: none"> <li>correction on FSBL</li> </ul>
2018-07-12	2018.2	TE0803-Starterkit_noprebuilt-vivado_2018.2-build_02_20180713085800.zip TE0803-Starterkit-vivado_2018.2-build_02_20180713085740.zip	John Hartfiel	<ul style="list-style-type: none"> <li>small petalinux changes</li> <li>IO renaming</li> <li>PL Design changes</li> <li>additional notes for FSBL generated with Win SDK</li> <li>changed *.bif</li> </ul>
2018-05-17	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_09_20180517141540.zip TE0803-Starterkit-vivado_2017.4-build_09_20180517141523.zip	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> <li>solved Linux flash issue</li> </ul>
2018-04-11	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_07_20180411082139.zip TE0803-Starterkit-vivado_2017.4-build_07_20180411082116.zip	John Hartfiel	<ul style="list-style-type: none"> <li>bugfix TE0803-01-04EG board part file</li> </ul>
2018-02-13	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_06_20180213120642.zip TE0803-Starterkit-vivado_2017.4-build_06_20180213120615.zip	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> </ul>
2018-02-06	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_05_20180206082527.zip TE0803-Starterkit-vivado_2017.4-build_05_20180206082513.zip	John Hartfiel	<ul style="list-style-type: none"> <li>same CLK for both VIO</li> </ul>

Date	Vivado	Project Built	Authors	Description
2018-02-05	2017.4	TE0803-Starterkit_noprebuilt-vivado_2017.4-build_05_20180205154248.zip TE0803-Starterkit-vivado_2017.4-build_05_20180205154230.zip	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> <li>solved JTAG/Linux issue</li> </ul>
2018-01-31	2017.4	TE0803-Starterkit-vivado_2017.4-build_05_20180131124042.zip TE0803-Starterkit_noprebuilt-vivado_2017.4-build_05_20180131124057.zip	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> </ul>
2018-01-18	2017.4	TE0803-Starterkit-vivado_2017.4-build_05_20180118164553.zip TE0803-Starterkit_noprebuilt-vivado_2017.4-build_05_20180118164613.zip	John Hartfiel	<ul style="list-style-type: none"> <li>initial release</li> </ul>

**Table 1: Design Revision History**

### 4.3 Release Notes and Know Issues

Issues	Description	Workaround/Solution	To be fixed version
Flash access on Linux	Device tree is not correct on Linux	add compatibility to "compatible "jedec,spi-nor""	<b>Solved</b> with 20180517 update
USB UART Terminal is blocked / SDK Debugging is blocked	This happens only with 2017.4 Linux , when JTAG connection is established on Vivado HW Manager.	Do not use HW Manager connection, or if debugging is nessecary: <ol style="list-style-type: none"> <li>1. Boot linux with usb terminal</li> <li>2. From the terminal: root root mount ifconfig eth0</li> <li>3. Open two new SSH terminals via ethernet: root root , run user application ...</li> <li>4. Exit and close the usb terminal</li> </ol>	<b>Solved</b> with 20180205 update

**Table 2: Known Issues**



## 4.4 Requirements

### 4.4.1 Software

Software	Version	Note
Vivado	2018.3	needed
SDK	2018.3	needed
PetaLinux	2018.3	needed
SI ClockBuilder Pro	---	optional

**Table 3: Software**

### 4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).<sup>1</sup>

Complete List is available on <design name>/board\_files/\*\_board\_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EM MC	Others	Notes
<del>TE0803-ES1</del>	es1_2gb	REV01	2GB	64MB	NA	NA	Not longer supported by vivado
TE0803-01-02EG-1E	2eg_2gb	REV01	2GB	64MB	NA	NA	NA
TE0803-01-02CG-1E	2cg_2gb	REV01	2GB	64MB	NA	NA	NA
TE0803-01-03EG-1E	3eg_2gb	REV01	2GB	64MB	NA	NA	NA
TE0803-01-03CG-1E	3cg_2gb	REV01	2GB	64MB	NA	NA	NA

<sup>1</sup> <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EM MC	Others	Notes
TE0803-01-02EG-1EA	2eg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-02CG-1EA	2cg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-03EG-1EA	3eg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-03CG-1EA	3cg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-02-03EG-1EB	3eg_4gb	REV02  REV01	4GB	128MB	NA	NA	NA
TE0803-01-04CG-1EA	4cg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-04EV-1EA	4ev_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-04EV-1E3	4ev_2gb	REV01	2GB	128MB	NA	1 mm connectors	NA
TE0803-01-04EG-1EA	4eg_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-04CG-1EB	4cg_2gb	REV01	2GB	256MB	NA	NA	NA
TE0803-01-05EV-1EA	5ev_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-01-05EV-1IA	5ev_i_2gb	REV01	2GB	128MB	NA	NA	NA
TE0803-02-04EV-1EB	4ev_4gb	REV02	4GB	128MB	NA	NA	NA
TE0803-02-04EV-1E3	4ev_4gb	REV02	4GB	128MB	NA	1 mm connectors	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EM MC	Others	Notes
TE0803-02-04EG-1E3	4eg_4gb	REV02	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-2AE11-A	2cg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-2BE11-A	2eg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-3AE11-A	3cg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-3BE11-A	3eg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4AE11-A	4cg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4BE11-A	4eg_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4BE21-L	4eg_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-4BI21-A	4eg_i_4gb	REV03	4GB	128MB	NA	NA	NA
TE0803-03-4DE11-A	4ev_2gb	REV03	2GB	128MB	NA	NA	NA
TE0803-03-4DE21-L	4ev_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-4GE21-L	4eg_2_4gb	REV03	4GB	128MB	NA	1 mm connectors	NA
TE0803-03-5DE11-A	5ev_2gb	REV03	2GB	128MB	NA	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EM MC	Others	Notes
TE0803-03-5DI21-A	5ev_i_4gb	REV03	4GB	128MB	NA	NA	NA

**Table 4: Hardware Modules**

Note: Design contains also Board Part Files for TE0808 only configuration, this board part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
TEBF0808	Used as reference carrier. <b>Important:</b> CPLD Firmware REV07 or newer is recommended

**Table 5: Hardware Carrier**

## 4.5 Content

For general structure and of the reference design, see [Project Delivery - Xilinx devices](#)<sup>2</sup>

### 4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/ block_design <design name>/ constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
SDK/ HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI
PetaLinux ux	<design name>/os/ petalinux	PetaLinux template with current configuration

**Table 6: Design sources**

<sup>2</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

## 4.5.2 Additional Sources

Type	Location	Notes
SI5338	<design name>/misc/SI5338	SI5338 Project with current PLL Configuration
init.sh	<design name>/sd/	Additional Initialization Script for Linux

**Table 7: Additional design sources**

## 4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

**Table 8: Prebuilt files (only on ZIP with prebuilt content)**

## 4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0803 "StarterKit" Reference Design](#)<sup>3</sup>

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<sup>3</sup> [https://shop.trenz-electronic.de/Download/?path=Trenz\\_Electronic/Modules\\_and\\_Module\\_Carriers/5.2x7.6/TE0803/Reference\\_Design/2018.3/StarterKit](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0803/Reference_Design/2018.3/StarterKit)

## 5 Design Flow

**⚠** Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

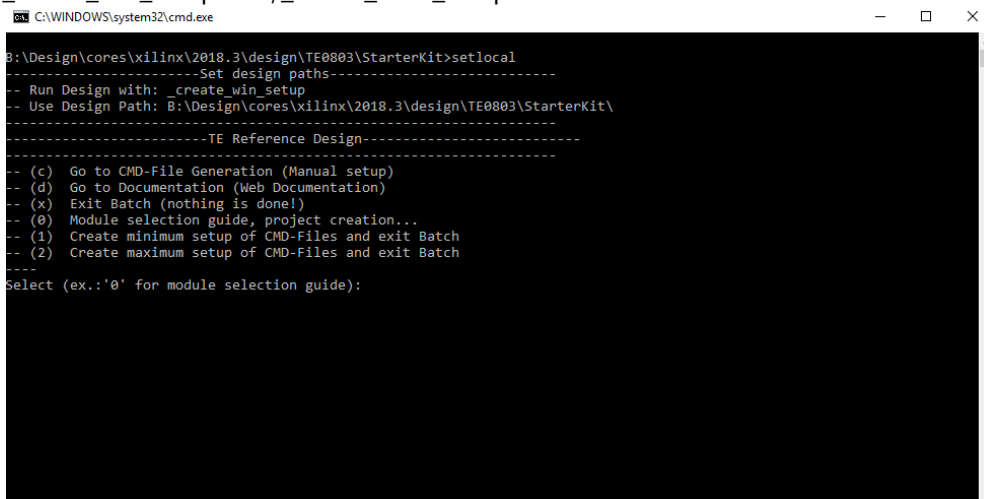
See also:

- [Xilinx Development Tools](#)<sup>4</sup>
- [Vivado Projects - TE Reference Design](#)<sup>5</sup>
- [Project Delivery](#).<sup>6</sup>

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "\_create\_win\_setup.cmd" on Windows OS and "\_create\_linux\_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)<sup>7</sup>

1. \_create\_win\_setup.cmd/\_create\_linux\_setup.sh and follow instructions on shell:



```

C:\WINDOWS\system32\cmd.exe
B:\Design\cores\xilinx\2018.3\design\TE0803\StarterKit>setlocal
-----Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: B:\Design\cores\xilinx\2018.3\design\TE0803\StarterKit\
-----
----- TE Reference Design -----
-----
-- (c) Go to CMD-File Generation (Manual setup)
-- (d) Go to Documentation (Web Documentation)
-- (x) Exit Batch (nothing is done!)
-- (0) Module selection guide, project creation...
-- (1) Create minimum setup of CMD-Files and exit Batch
-- (2) Create maximum setup of CMD-Files and exit Batch
-----
Select (ex.: '0' for module selection guide):
  
```

2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process
5. Create Project
  - a. (optional for manual changes) Select correct device and Xilinx install path on "design\_basic\_settings.cmd" and create Vivado project with "vivado\_create\_project\_guiemode.cmd"
 Note: Select correct one, see [TE Board Part Files](#)
- 8 **Important:** Use Board Part Files, which ends with \*\_tebf0808
6. Create HDF and export to prebuilt folder

<sup>4</sup> <https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides>

<sup>5</sup> <https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design>

<sup>6</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices>

<sup>7</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDelivery-Xilinxdevices-Currentlylimitationsoffunctionality>

<sup>8</sup> <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

- a. Run on Vivado TCL: `TE::hw_build_design -export_prebuilt`  
Note: Script generate design and export files into `\prebuilt\hardware\<short dir>`. Use GUI is the same, except file export to prebuilt folder
7. Create Linux (bl31.elf, uboot.elf and image.ub) with exported HDF
  - a. HDF is exported to `"prebuilt\hardware\<short name>"`  
Note: HW Export from Vivado GUI create another path as default workspace.  
Create Linux images on VM, see [PetaLinux KICKstart](#)<sup>9</sup>
    - i. Use TE Template from `/os/petalinux`  
Note: run `init_config.sh` before you start petalinux config. This will set correct temporary path variable.
8. Add Linux files (bl31.elf, uboot.elf and image.ub) to prebuilt folder
  - a. `prebuilt\os\petalinux\<ddr size>"` or `"prebuilt\os\petalinux\<short name>"`
9. Generate Programming Files with HSI/SDK
  - a. Run on Vivado TCL: `TE::sw_run_hsi`  
Note: Scripts generate applications and bootable files, which are defined in `"sw_lib\apps_list.csv"`
  - b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: `TE::sw_run_sdk`  
Note: See [SDK Projects](#)<sup>10</sup>

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<sup>9</sup> <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

<sup>10</sup> <https://wiki.trenz-electronic.de/display/PD/SDK+Projects>




## 6 Launch

---

### 6.1 Programming

---

 Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](#)<sup>11</sup>

#### 6.1.1 QSPI

---

Optional for Boot.bin on QSPI Flash and image.ub on SD.

- Connect JTAG and power on carrier with module
- Open Vivado Project with "vivado\_open\_existing\_project\_guiemode.cmd" or if not created, create with "vivado\_create\_project\_guiemode.cmd"
- Type on Vivado TCL Console: TE::pr\_program\_flash\_binfile -swapp u-boot  
Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp\_fsb\_flash) on setup  
optional "TE::pr\_program\_flash\_binfile -swapp hello\_te0803" possible
- Copy image.ub on SD-Card
  - For correct prebuilt file location, see <design\_name>/prebuilt/readme\_file\_location.txt
- Set Boot Mode to QSPI-Boot and inserted SD.
  - Depends on Carrier, see carrier TRM.
  - TEBF0808 change automatically the Boot Mode to SD, if SD is inserted, optional CPLD Firmware without Boot Mode changing for microSD Slot is available on the download area

#### 6.1.2 SD

---

1. Copy image.ub and Boot.bin on SD-Card.
  - For correct prebuilt file location, see <design\_name>/prebuilt/readme\_file\_location.txt
2. Set Boot Mode to SD-Boot.
  - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

#### 6.1.3 JTAG

---

Not used on this Example.

### 6.2 Usage

---

1. Prepare HW like described on section [Programming](#)(see page 17)
2. Connect UART USB (JTAG XMOD)
3. Select SD Card as Boot Mode (or QSPI - depending on step 1)  
Note: See TRM of the Carrier, which is used.
4. (Optional) Insert PCIe Card (detection depends on Linux driver. Only some basic drivers are installed)
5. (Optional) Connect Sata Disc

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<sup>11</sup><https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging>

6. (Optional) Connect DisplayPort Monitor (List of usable Monitors: <https://www.xilinx.com/support/answers/68671.html>)
7. (Optional) Connect Network Cable
8. Power On PCB  
Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from SD into OCM, 2. FSBL loads ATF(bl31.elf) and U-boot from SD/QSPI into DDR, 3. U-boot load Linux from SD into DDR.

## 6.2.1 Linux

---

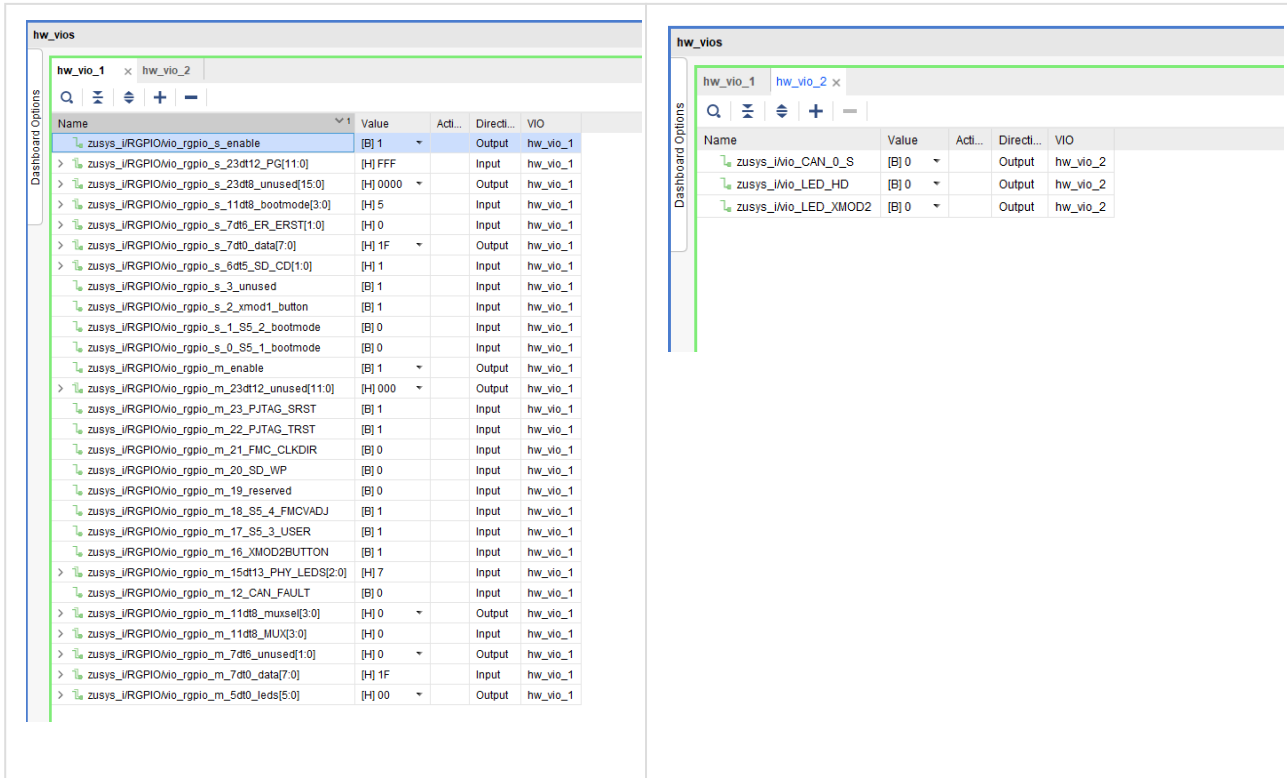
1. Open Serial Console (e.g. putty)
  - a. Speed: 115200
  - b. COM Port: Win OS, see device manager, Linux OS see `dmesg |grep tty` (UART is \*USB1)
2. Linux Console:  
Note: Wait until Linux boot finished For Linux Login use:
  - a. User Name: root
  - b. Password: root
3. You can use Linux shell now.
  - a. I2C 0 Bus type: `i2cdetect -y -r 0`
  - b. ETH0 works with `udhcpc`
  - c. USB type "lsusb" or connect USB device
  - d. PCIe type "lspci"
4. Option Features
  - a. Webserver to get access to Zynq
    - i. insert IP on web browser to start web interface
  - b. `init.sh` scripts
    - i. add `init.sh` script on SD, content will be load automatically on startup (template included in `./misc/SD`)

## 6.2.2 Vivado Hardware Manager

---

Open Vivado HW-Manager and add VIO signal to dashboard (\*.ltx located on prebuilt folder).

- RGPIO Interface (**Important:** CPLD Firmware REV07 or newer is needed) for Control and Monitoring:
  - Set Enable to send Write date over RGPIO interface.
    - **Important use CPLD Firmware REV07 or newer:** <https://wiki.trenz-electronic.de/display/PD/TEBF0808+CPLD>
      - Buttons, LEDs, Status...
- Control:
  - LEDs: XMOD 2(without green dot) and HD LED are accessible.
  - CAN\_S



The image shows two screenshots of the Vivado Hardware Manager interface. The left screenshot displays the configuration for 'hw\_vio\_1', listing various GPIO pins with their names, values, directions, and associated VIOs. The right screenshot displays the configuration for 'hw\_vio\_2', showing a subset of pins.

Name	Value	Acti...	Directi...	VIO
zsys_IRGPIOIo_rgpio_s_enable	[B] 1		Output	hw_vio_1
zsys_IRGPIOIo_rgpio_s_23dt12_PG[11:0]	[H] FFF		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_s_23dt8_unused[15:0]	[H] 0000		Output	hw_vio_1
zsys_IRGPIOIo_rgpio_s_11dt8_bootmode[3:0]	[H] 5		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_s_7dt6_ER_ERST[1:0]	[H] 0		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_s_7dt0_data[7:0]	[H] 1F		Output	hw_vio_1
zsys_IRGPIOIo_rgpio_s_6dt5_SD_CD[1:0]	[H] 1		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_s_3_unused	[B] 1		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_s_2_xmod1_button	[B] 1		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_s_1_S5_2_bootmode	[B] 0		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_s_0_S5_1_bootmode	[B] 0		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_m_enable	[B] 1		Output	hw_vio_1
zsys_IRGPIOIo_rgpio_m_23dt12_unused[11:0]	[H] 000		Output	hw_vio_1
zsys_IRGPIOIo_rgpio_m_23_PJTAG_SRST	[B] 1		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_m_22_PJTAG_TRST	[B] 1		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_m_21_FMC_CLKDIR	[B] 0		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_m_20_SD_WP	[B] 0		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_m_19_reserved	[B] 0		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_m_18_S5_4_FMCVADJ	[B] 1		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_m_17_S5_3_USER	[B] 1		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_m_16_XMOD2BUTTON	[B] 1		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_m_15dt13_PHY_LEDS[2:0]	[H] 7		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_m_12_CAN_FAULT	[B] 0		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_m_11dt8_muxse[3:0]	[H] 0		Output	hw_vio_1
zsys_IRGPIOIo_rgpio_m_11dt8_MUX[3:0]	[H] 0		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_m_7dt6_unused[1:0]	[H] 0		Output	hw_vio_1
zsys_IRGPIOIo_rgpio_m_7dt0_data[7:0]	[H] 1F		Input	hw_vio_1
zsys_IRGPIOIo_rgpio_m_5dt0_leds[5:0]	[H] 00		Output	hw_vio_1

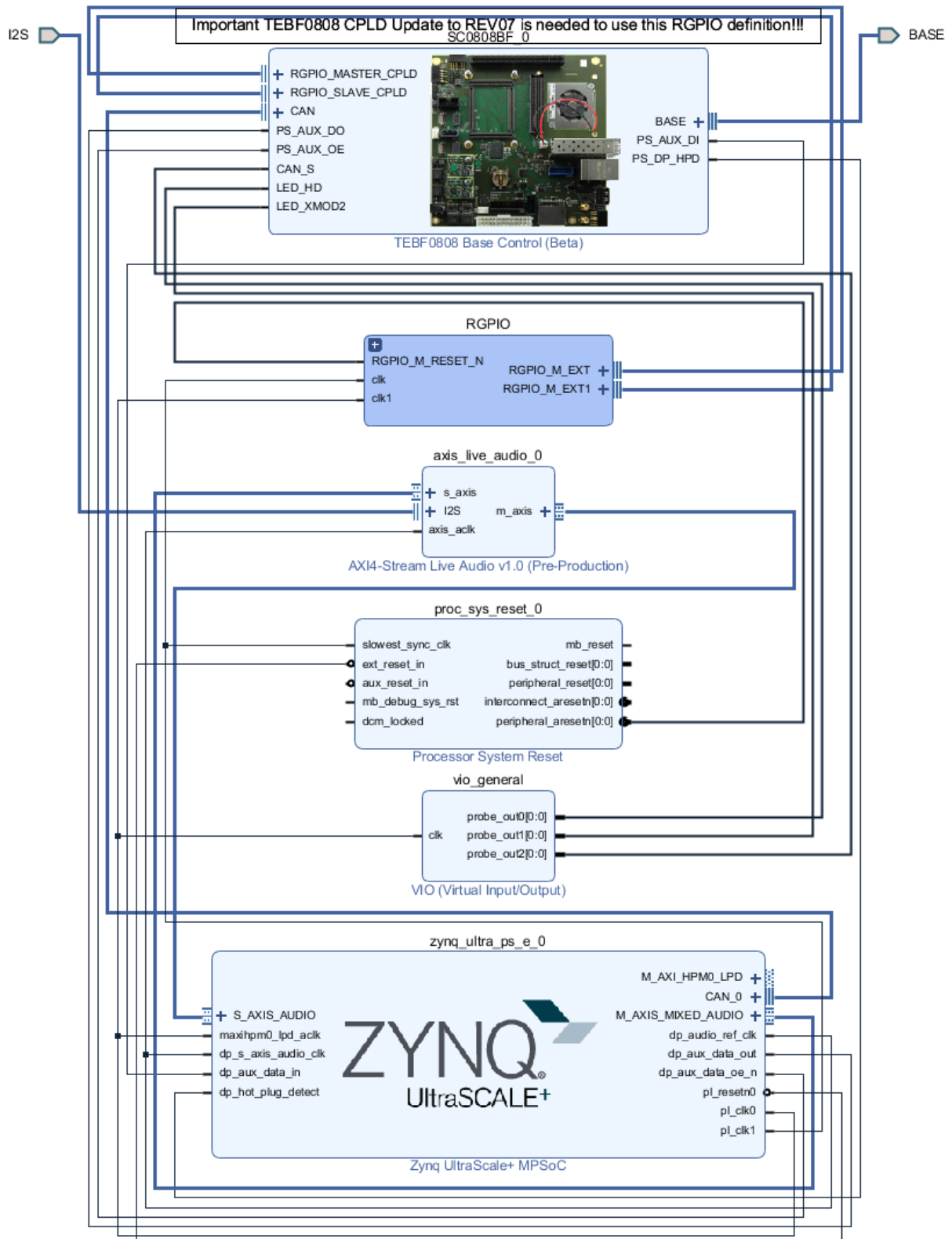
  

Name	Value	Acti...	Directi...	VIO
zsys_iVio_CAN_0_S	[B] 0		Output	hw_vio_2
zsys_iVio_LED_HD	[B] 0		Output	hw_vio_2
zsys_iVio_LED_XMOD2	[B] 0		Output	hw_vio_2

**Table 9: Vivado Hardware Manager**

## 7 System Design - Vivado

### 7.1 Block Design



**Figure 1: Block Design**

### 7.1.1 PS Interfaces

---

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
SD0	MIO
SD1	MIO
CAN0	EMIO
I2C0	MIO
PJTAG0	MIO
UART0	MIO
GPIO0	MIO
SWDT0..1	
TTC0..3	
GEM3	MIO
USB0	MIO/GTP
PCIe	MIO/GTP
SATA	GTP
DisplayPort	EMIO/GTP

## 7.2 Constrains

---

### 7.2.1 Basic module constrains

---

#### **\_i\_bitgen.xdc**

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]  
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

## 7.2.2 Design specific constrain

### **\_i\_io.xdc**

```

# system controller ip
#LED_HD SC0 J3:31
#LED_XMOD SC17 J3:48
#CAN RX SC19 J3:52 B26_L11_P
#CAN TX SC18 J3:50 B26_L11_N
#CAN S SC16 J3:46 B26_L1_N

set_property PACKAGE_PIN G14 [get_ports BASE_sc0]
set_property PACKAGE_PIN D15 [get_ports BASE_sc5]
set_property PACKAGE_PIN H13 [get_ports BASE_sc6]
set_property PACKAGE_PIN H14 [get_ports BASE_sc7]
set_property PACKAGE_PIN A13 [get_ports BASE_sc10_io]
set_property PACKAGE_PIN B13 [get_ports BASE_sc11]
set_property PACKAGE_PIN A14 [get_ports BASE_sc12]
set_property PACKAGE_PIN B14 [get_ports BASE_sc13]
set_property PACKAGE_PIN F13 [get_ports BASE_sc14]
set_property PACKAGE_PIN G13 [get_ports BASE_sc15]
set_property PACKAGE_PIN A15 [get_ports BASE_sc16]
set_property PACKAGE_PIN B15 [get_ports BASE_sc17]
set_property PACKAGE_PIN J14 [get_ports BASE_sc18]
set_property PACKAGE_PIN K14 [get_ports BASE_sc19 ]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc0]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc5]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc6]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc7]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc10_io]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc11]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc12]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc13]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc14]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc15]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc16]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc17]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc18]
set_property IOSTANDARD LVCMOS18 [get_ports BASE_sc19]

# Audio Codec
#LRCLK J3:49
#BCLK J3:51
#DAC_SDATA J3:53
#ADC_SDATA J3:55
set_property PACKAGE_PIN L13 [get_ports LRCLK ]
set_property PACKAGE_PIN L14 [get_ports BCLK ]
set_property PACKAGE_PIN E15 [get_ports DAC_SDATA ]
set_property PACKAGE_PIN F15 [get_ports ADC_SDATA ]
set_property IOSTANDARD LVCMOS18 [get_ports LRCLK ]
set_property IOSTANDARD LVCMOS18 [get_ports BCLK ]
set_property IOSTANDARD LVCMOS18 [get_ports DAC_SDATA ]
    
```

```
set_property IOSTANDARD LVCMOS18 [get_ports ADC_SDATA ]
```



## 8 Software Design - SDK/HSI

---

For SDK project creation, follow instructions from:

[SDK Projects](#)<sup>12</sup>

### 8.1 Application

---

SDK template in ./sw\_lib/sw\_apps/ available.

#### 8.1.1 zynqmp\_fsbl

---

TE modified 2018.3 FSBL

General:

- Modified Files: xfsbl\_main.c, xfsbl\_hooks.h/.c, xfsbl\_board.h/.c(search for 'TE Mod' on source code)
- Add Files: te\_xfsbl\_hooks.h/.c (for hooks and board)\n\
- General Changes:
  - Display FSBL Banner and Device Name

Module Specific:

- Add Files: all TE Files start with te\_\*
  - Si5338 Configuration
  - OTG+PCIe Reset over MIO
  - I2C MUX for EEPROM MAC

#### 8.1.2 zynqmp\_fsbl\_flash

---

TE modified 2018.3 FSBL

General:

- Modified Files: xfsbl\_initialisation.c, xfsbl\_hw.h, xfsbl\_handoff.c, xfsbl\_main.c
- General Changes:
  - Display FSBL Banner
  - Set FSBL Boot Mode to JTAG
  - Disable Memory initialisation

#### 8.1.3 hello\_te0803

---

Hello TE0803 is a Xilinx Hello World example as endless loop instead of one console output.

#### 8.1.4 u-boot

---

U-Boot.elf is generated with Petalinux. SDK/HSI is used to generate Boot.bin.

---

<sup>12</sup> <https://wiki.trenz-electronic.de/display/PD/SDK+Projects>

## 9 Software Design - PetaLinux

---

For PetaLinux installation and project creation, follow instructions from:

- [PetaLinux KICKstart](#)<sup>13</sup>

### 9.1 Config

---

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Activate:

- CONFIG\_SUBSYSTEM\_PRIMARY\_SD\_PSU\_SD\_1\_SELECT=y
- CONFIG\_SUBSYSTEM\_ETHERNET\_PSU\_ETHERNET\_3\_MAC=""

### 9.2 U-Boot

---

Start with **petalinux-config -c u-boot**

Changes:

- CONFIG\_ENV\_IS\_NOWHERE=y
- CONFIG\_ENV\_IS\_IN\_SPI\_FLASH is not set

Change platform-top.h:

---

<sup>13</sup> <https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart>

```
#include <configs/platform-auto.h>
#define CONFIG_SYS_BOOTM_LEN 0xF000000

#define DFU_ALT_INFO_RAM \
    "dfu_ram_info=" \
    "setenv dfu_alt_info " \
    "image.ub ram $netstart 0x1e00000\0" \
    "dfu_ram=run dfu_ram_info && dfu 0 ram 0\0" \
    "thor_ram=run dfu_ram_info && thordown 0 ram 0\0"

#define DFU_ALT_INFO_MMC \
    "dfu_mmc_info=" \
    "set dfu_alt_info " \
    "${kernel_image} fat 0 1\\\\\\\\;" \
    "dfu_mmc=run dfu_mmc_info && dfu 0 mmc 0\0" \
    "thor_mmc=run dfu_mmc_info && thordown 0 mmc 0\0"

/*Required for uartless designs */
#ifndef CONFIG_BAUDRATE
#define CONFIG_BAUDRATE 115200
#endif
#define CONFIG_DEBUG_UART
#undef CONFIG_DEBUG_UART
#endif

/*Define CONFIG_ZYNQMP_EEPROM here and its necessities in u-boot menuconfig if you
had EEPROM memory. */
#define CONFIG_ZYNQMP_EEPROM
#ifdef CONFIG_ZYNQMP_EEPROM
#define CONFIG_SYS_I2C_EEPROM_ADDR_LEN 1
#define CONFIG_CMD_EEPROM
#define CONFIG_ZYNQ_EEPROM_BUS 0
#define CONFIG_ZYNQ_GEM_EEPROM_ADDR 0x50
#define CONFIG_ZYNQ_GEM_I2C_MAC_OFFSET 0xFA
#endif
```

## 9.3 Device Tree

```
/include/ "system-conf.dtsi"
/ {
};
/* notes:
serdes: // PHY TYP see: dt-bindings/phy/phy.h
*/

/* default */

/* SD */

&sdhci1 {
    // disable-wp;
    no-1-8-v;
};

/*PCIE*/
&pcie {
    phys = <&lane0 2 0 2 100000000>; //not recognized at the moment on linux
};

/* DP */
&zynqmp_dpsub {
    phys = <&lane3 5 0 3 270000000>; //Xilinx default is 5 (UFS), 6 (DP) does not work
};

/* SATA */

&sata {
    //phys = <&lane2 1 0 1 150000000>; //TE0808,TE0807
    phys = <&lane2 1 0 0 150000000>; //TE0803
};

/* USB */

&dwc3_0 {
    status = "okay";
    dr_mode = "host";
    snps,usb3_lpm_capable;
    snps,dis_u3_susphy_quirk;
    snps,dis_u2_susphy_quirk;
    phy-names = "usb2-phy","usb3-phy";
    phys = <&lane1 4 0 2 1000000000>;
    maximum-speed = "super-speed";
};

/* ETH PHY */
```

```
&gem3 {
    phy-handle = <&phy0>;
    phy0: phy0@1 {
        device_type = "ethernet-phy";
        reg = <1>;
    };
};

/* QSPI */

&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};

/* I2C */

&i2c0 {
    i2cswitch@73 { // u
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x73>;
        i2c-mux-idle-disconnect;

        i2c@2 { // PCIe
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <2>;
        };
        i2c@3 { // i2c SFP
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <3>;
        };
        i2c@4 { // i2c SFP
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <4>;
        };
        i2c@5 { // i2c EEPROM
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <5>;
        };
        i2c@6 { // i2c FMC
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <6>;
        };
    };
};
```

```

    si570_2: clock-generator3@5d {
        #clock-cells = <0>;
        compatible = "silabs,si570";
        reg = <0x5d>;
        temperature-stability = <50>;
        factory-fout = <156250000>;
        clock-frequency = <78800000>;
    };
};
i2c@7 { // i2c USB HUB
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <7>;
};
};
i2cswitch@77 { // u
    compatible = "nxp,pca9548";
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <0x77>;
    i2c-mux-idle-disconnect;
    i2c@0 { // i2c PMOD
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0>;
    };
};
i2c@1 { // i2c Audio Codec
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <1>;
    /*
    adau1761: adau1761@38 {
        compatible = "adi,adau1761";
        reg = <0x38>;
    };
    */
};
i2c@2 { // i2c FireFly A
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <2>;
};
i2c@3 { // i2c FireFly B
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <3>;
};
};
i2c@4 { // i2c PLL
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <4>;
};
};
i2c@5 { // i2c SC
    #address-cells = <1>;
    #size-cells = <0>;
};

```

```
        reg = <5>;
    };
    i2c@6 { // i2c
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <6>;
    };
    i2c@7 { // i2c
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <7>;
    };
};
```

## 9.4 Kernel

---

Start with **petalinux-config -c kernel**

Changes:

- CONFIG\_CPU\_IDLE is not set (only needed to fix JTAG Debug issue)
- CONFIG\_CPU\_FREQ is not set (only needed to fix JTAG Debug issue)
- CONFIG\_CPU\_FREQ\_DEFAULT\_GOV\_USERSPACE is not set (only needed to fix JTAG Debug issue)
- CONFIG\_EDAC\_CORTEX\_ARM64=y

## 9.5 Rootfs

---

Start with **petalinux-config -c rootfs**

Changes:

- CONFIG\_busybox-httpd=y (for web server app)
- CONFIG\_packagegroup-petalinux-utils(util-linux,cpufrequtils,bridge-utils,mtd-utils,usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)

## 9.6 Applications

---

### 9.6.1 startup

---

Script App to load init.sh from SD Card if available.

See: \os\petalinux\project-spec\meta-user\recipes-apps\startup\files

### 9.6.2 webfwu

---

Webserver application acembale for Zynq access. Need busybox-httpd

## 10 Additional Software

---

### 10.1 SI5338

---

File location <design name>/misc/SI5338/SI5338-\*.slabtimeproj

General documentation how you work with these project will be available on [SI5338](#)<sup>14</sup>

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<sup>14</sup> <https://wiki.trenz-electronic.de/display/PD/SI5338>



## 11 Appx. A: Change History and Legal Notices

### 11.1 Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
 2019-05-07	v.24( <a href="#">see page 6</a> )	<a href="#">John Hartfiel</a> <sup>15</sup>	<ul style="list-style-type: none"> <li>• Release 2018.3</li> </ul>
2018-10-26	v.21	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>
2018-08-14	v.19	John Hartfiel	<ul style="list-style-type: none"> <li>• design update</li> </ul>
2018-07-23	v.18	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>
2018-07-20	v.16	John Hartfiel	<ul style="list-style-type: none"> <li>• Release 2018.2</li> </ul>
2018-05-17	v.14	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> <li>• solved known issues</li> </ul>
2018-04-30	v.13	John Hartfiel	<ul style="list-style-type: none"> <li>• Update known Issues</li> </ul>
2018-04-11	v.12	John Hartfiel	<ul style="list-style-type: none"> <li>• bugfix board part files</li> </ul>
2018-02-13	v.11	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> <li>• solved known issues</li> </ul>
2018-01-29	v.4	John Hartfiel	<ul style="list-style-type: none"> <li>• Update known Issues</li> </ul>
2018-01-18	v.3	John Hartfiel	<ul style="list-style-type: none"> <li>• Release 2017.4</li> </ul>

<sup>15</sup> <https://wiki.trenz-electronic.de/display/~j.hartfiel>

Date	Document Revision	Authors	Description
	All	<a href="#">John Hartfiel</a> <sup>16</sup>	

**Table 10: Document change history.**

## 11.2 Legal Notices

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### 11.3 Data Privacy

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Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

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<sup>16</sup> <https://wiki.trenz-electronic.de/display/~j.hartfiel>

## 11.8 Environmental Protection

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To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

## 11.9 REACH, RoHS and WEEE

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Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

 2019-06-07

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<sup>17</sup> <http://guidance.echa.europa.eu/>

<sup>18</sup> <https://echa.europa.eu/candidate-list-table>

<sup>19</sup> <http://www.echa.europa.eu/>