



## TE0803 Test Board

Revision v.33

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Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TE0803+Test+Board>

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## 4 Overview

Design Example with minimum PS Setup (DDR, QSPI, UART0) only for custom boards or easier debug via Vitis. Refer to <http://trenz.org/te0803-info> for the current online version of this manual and other available documentation.

### 4.1 Key Features

- Vitis/Vivado 2021.2.1
- QSPI
- Custom Carrier (minimum PS Design with available module components only)
- Modified FSBL (some additional outputs only)

### 4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2022-10-17	2021.2.1	TE0803-test_board-vivado_2021.2-build_18_20221017093148.zip TE0803-test_board_noprebuilt-vivado_2021.2-build_18_20221017093148.zip	Manuela Strücker	<ul style="list-style-type: none"> <li>• script update</li> </ul>
2022-08-30	2021.2.1	TE0803-test_board-vivado_2021.2-build_15_20220830131430.zip TE0803-test_board_noprebuilt-vivado_2021.2-build_15_20220830131430.zip	Manuela Strücker	<ul style="list-style-type: none"> <li>• new assembly variants</li> </ul>
2022-04-05	2021.2	TE0803-test_board-vivado_2021.2-build_11_20220405100116.zip TE0803-test_board_noprebuilt-vivado_2021.2-	Manuela Strücker	<ul style="list-style-type: none"> <li>• 2021.2 update</li> </ul>

Date	Vivado	Project Built	Authors	Description
		build_11_20220405100116.zip		
2021-09-06	2020.2	TE0803-test_board-vivado_2020.2-build_7_20210906104518.zip TE0803-test_board_noprebuilt-vivado_2020.2-build_7_20210906104536.zip	Manuela Strücker	<ul style="list-style-type: none"> <li>• 2020.2 update</li> <li>• update document style</li> </ul>
2020-04-06	2019.2	TE0803-test_board-vivado_2019.2-build_9_20200406081019.zip TE0803-test_board_noprebuilt-vivado_2019.2-build_9_20200406081036.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variants</li> </ul>
2020-03-25	2019.2	TE0803-test_board-vivado_2019.2-build_8_20200325082253.zip TE0803-test_board_noprebuilt-vivado_2019.2-build_8_20200325082311.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• script update</li> </ul>
2020-01-23	2019.2	TE0803-test_board-vivado_2019.2-build_3_20200123070036.zip TE0803-test_board_noprebuilt-vivado_2019.2-	John Hartfiel	<ul style="list-style-type: none"> <li>• 2019.2 update</li> <li>• Vitis support</li> <li>• FSBL SI programming procedure update</li> </ul>



Date	Vivado	Project Built	Authors	Description
		build_3_20200123070049.zip		
2019-5-06	2018.3	TE0803-test_board_noprebuilt-vivado_2018.3-build_05_20190506161948.zip  TE0803-test_board-vivado_2018.3-build_05_20190506161936.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• custom FSBL</li> <li>• new assembly variants</li> </ul>
2018-10-26	2018.2	TE0803-test_board_noprebuilt-vivado_2018.2-build_03_20181026141705.zip  TE0803-test_board-vivado_2018.2-build_03_20181026141651.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>
2018-08-14	2018.2	TE0803-test_board_noprebuilt-vivado_2018.2-build_02_20180814103119.zip  TE0803-test_board-vivado_2018.2-build_02_20180814103105.zip	John Hartfiel	<ul style="list-style-type: none"> <li>• new assembly variant</li> </ul>
2018-07-13	2018.2	TE0803-test_board_noprebuilt-vivado_2018.2-build_02_20180713085721.zip  TE0803-test_board-vivado_2018.2-	John Hartfiel	<ul style="list-style-type: none"> <li>• additional notes for FSBL generated with Win SDK</li> <li>• changed *.bif</li> </ul>

Date	Vivado	Project Built	Authors	Description
		build_02_20180713085704.zip		
2018-05-17	2017.4	TE0803-test_board_noprebuilt-vivado_2017.4-build_09_20180517152118.zip  TE0803-test_board-vivado_2017.4-build_09_20180517152103.zip	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> </ul>
2018-04-11	2017.4	TE0803-test_board_noprebuilt-vivado_2017.4-build_07_20180411081821.zip  TE0803-test_board-vivado_2017.4-build_07_20180411081757.zip	John Hartfiel	<ul style="list-style-type: none"> <li>bugfix TE0803-01-04EG board part file</li> </ul>
2018-02-13	2017.4	TE0803-test_board_noprebuilt-vivado_2017.4-build_06_20180213120257.zip  TE0803-test_board-vivado_2017.4-build_06_20180213120229.zip	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> </ul>
2018-02-05	2017.4	TE0803-test_board-vivado_2017.4-build_05_20180205101915.zip  TE0803-test_board_noprebuilt-vivado_2017.4-	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> </ul>

Date	Vivado	Project Built	Authors	Description
		build_05_20180205101943.zip		
2018-01-31	2017.4	TE0803-test_board-vivado_2017.4-build_05_20180131124202.zip  TE0803-test_board_noprebuilt-vivado_2017.4-build_05_20180131124215.zip	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> </ul>
2018-01-18	2017.4	TE0803-test_board-vivado_2017.4-build_05_20180118160549.zip  TE0803-test_board_noprebuilt-vivado_2017.4-build_05_20180118160604.zip	John Hartfiel	<ul style="list-style-type: none"> <li>rework Board Part Files</li> </ul>
2017-11-16	2017.2	TE0803-test_board-vivado_2017.2-build_05_20171116152716.zip  TE0803-test_board_noprebuilt-vivado_2017.2-build_05_20171116154619.zip	John Hartfiel	<ul style="list-style-type: none"> <li>Update Board Part CSV File with new Flash assembly variants</li> </ul>
2017-11-14	2017.2	TE0803-test_board-vivado_2017.2-build_05_20171114090712.zip  TE0803-test_board_noprebuilt-vivado_2017.2-	John Hartfiel	<ul style="list-style-type: none"> <li>Initial release</li> </ul>

Date	Vivado	Project Built	Authors	Description
		build_05_20171114090725.zip		

**Table 1: Design Revision History**

## 4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
Xilinx Software	Incompatibility of board files for ZynqMP with eMMC activated between 2021.2 and 2021.2.1 patch, see <a href="#">Xilinx Forum Request<sup>1</sup></a>	use corresponding board files for the Vivado versions	--
QSPI Flash	Flash programming is not supported with boot mode QSPI or SD.	If flash programming fails, configure device for JTAG boot mode and try again or use older Vivado Versions for programming. (Vivado 2020.2 or 2019.2)	--

**Table 2: Known Issues**

## 4.4 Requirements

### 4.4.1 Software

Software	Version	Note
Vitis	2021.2.1	needed, Vivado is included into Vitis installation

**Table 3: Software**

<sup>1</sup> [https://support.xilinx.com/s/feed/0D54U00005Wbon6SAB?language=en\\_US](https://support.xilinx.com/s/feed/0D54U00005Wbon6SAB?language=en_US)

## 4.4.2 Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).<sup>2</sup>  
Complete List is available on "<project folder>\board\_files\\*\_board\_files.csv"

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	D D R	QSPI Flash	EM MC	Others	Notes
TE0803-01-02EG-1E	2eg_2gb	REV01	2G B	64MB	NA	NA	NA
TE0803-01-02CG-1E	2cg_2gb	REV01	2G B	64MB	NA	NA	NA
TE0803-01-03EG-1E	3eg_2gb	REV01	2G B	64MB	NA	NA	NA
TE0803-01-03CG-1E	3cg_2gb	REV01	2G B	64MB	NA	NA	NA
TE0803-01-02EG-1EA	2eg_2gb	REV01	2G B	128MB	NA	NA	NA
TE0803-01-02CG-1EA	2cg_2gb	REV01	2G B	128MB	NA	NA	NA
TE0803-01-03EG-1EA	3eg_2gb	REV01	2G B	128MB	NA	NA	NA
TE0803-01-03CG-1EA	3cg_2gb	REV01	2G B	128MB	NA	NA	NA
TE0803-02-03EG-1EB	3eg_4gb	REV02  REV01	4G B	128MB	NA	NA	NA
TE0803-01-04CG-1EA	4cg_2gb	REV01	2G B	128MB	NA	NA	NA

<sup>2</sup> <https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files>

Module Model	Board Part Short Name	PCB Revision Support	D D R	QSPI Flash	EM MC	Others	Notes
TE0803-02-04EV-1EA	4ev_2gb	REV02 REV01	2G B	128MB	NA	NA	NA
TE0803-01-04EV-1E3	4ev_2gb	REV01	2G B	128MB	NA	1 mm connectors	NA
TE0803-01-04EG-1EA	4eg_2gb	REV01	2G B	128MB	NA	NA	NA
TE0803-01-04CG-1EB	4cg_2gb	REV01	2G B	256MB	NA	NA	NA
TE0803-01-05EV-1EA	5ev_2gb	REV01	2G B	128MB	NA	NA	NA
TE0803-01-05EV-1IA	5ev_i_2gb	REV01	2G B	128MB	NA	NA	NA
TE0803-02-04EV-1E3	4ev_4gb	REV02	4G B	128MB	NA	1 mm connectors	NA
TE0803-02-04EG-1E3	4eg_4gb	REV02	4G B	128MB	NA	1 mm connectors	NA
TE0803-03-2AE11-A	2cg_2gb	REV03	2G B	128MB	NA	NA	NA
TE0803-03-2BE11-A	2eg_2gb	REV03	2G B	128MB	NA	NA	NA
TE0803-03-3AE11-A	3cg_2gb	REV03	2G B	128MB	NA	NA	NA
TE0803-03-3BE11-A	3eg_2gb	REV03	2G B	128MB	NA	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	D D R	QSPI Flash	EM MC	Others	Notes
TE0803-03-4AE11-A	4cg_2gb	REV03	2G B	128MB	NA	NA	NA
TE0803-03-4BE11-A	4eg_2gb	REV03	2G B	128MB	NA	NA	NA
TE0803-03-4BE21-L	4eg_4gb	REV03	4G B	128MB	NA	1 mm connectors	NA
TE0803-03-4BI21-A	4eg_i_4gb	REV03	4G B	128MB	NA	NA	NA
TE0803-03-4DE11-A	4ev_2gb	REV03	2G B	128MB	NA	NA	NA
TE0803-03-4DE21-L	4ev_4gb	REV03	4G B	128MB	NA	1 mm connectors	NA
TE0803-03-4GE21-L	4eg_2_4gb	REV03	4G B	128MB	NA	1 mm connectors	NA
TE0803-03-5DE11-A	5ev_2gb	REV03	2G B	128MB	NA	NA	NA
TE0803-03-5DI21-A	5ev_i_4gb	REV03	4G B	128MB	NA	NA	NA
TE0803-03-3RI21-A	3eg_li_4gb	REV03	4G B	128MB	NA	NA	NA
TE0803-03-3BI21-A	3eg_i_4gb	REV03	4G B	128MB	NA	NA	NA

Module Model	Board Part Short Name	PCB Revision Support	D D R	QSPI Flash	EM MC	Others	Notes
TE0803-03-4DI21-L	4ev_i_4gb	REV03	4G B	128MB	NA	1 mm connectors	NA
TE0803-03-4GI11-A	4eg_2i_2gb	REV03	2G B	128MB	NA	NA	NA
TE0803-03-4GE11-A	4eg_2_2gb	REV03	2G B	128MB	NA	NA	NA
TE0803-03-4GI21-A	4eg_2i_4gb	REV03	4G B	128MB	NA	NA	NA
TE0803-03-5BE11-A	5eg_2gb	REV03	2G B	128MB	NA	NA	NA
TE0803-03-5DI24-A	5ev_i_4gb	REV03	4G B	512MB	NA	NA	NA
TE0803-03-4BI21-X	4eg_i_4gb	REV03	4G B	128MB	NA	NA	U41 replaced with diode
TE0803-03-3BE21-A	3eg_4gb	REV03	4G B	128MB	NA	NA	NA
TE0803-03-3BE31-A <sup>*</sup>	3eg_8gb	REV03	8G B	128MB	NA	NA	dual die ddr
TE0803-04-2AE11-A	2cg_2gb	REV04	2G B	128MB	NA	NA	NA
TE0803-04-2BE11-A	2eg_2gb	REV04	2G B	128MB	NA	NA	NA
TE0803-04-3AE11-A	3cg_2gb	REV04	2G B	128MB	NA	NA	NA



Module Model	Board Part Short Name	PCB Revision Support	D D R	QSPI Flash	EM MC	Others	Notes
TE0803-04-3BE11-A	3eg_2gb	REV04	2G B	128MB	NA	NA	NA
TE0803-04-4BE21-L	4eg_4gb	REV04	4G B	128MB	NA	1 mm connectors	NA
TE0803-04-4BI21-A	4eg_i_4gb	REV04	4G B	128MB	NA	NA	NA
TE0803-04-4BI21-X	4eg_i_4gb	REV04	4G B	128MB	NA	NA	U41 replaced with diode
TE0803-03-4BI61-A	4eg_8gb	REV03	8G B	128MB	NA	NA	dual die ddr
TE0803-03-4BI61-X	4eg_8gb	REV03	8G B	128MB	NA	NA	dual die ddr
TE0803-04-4BI61-A	4eg_8gb	REV04	8G B	128MB	NA	NA	dual die ddr
TE0803-04-4BI61-X	4eg_8gb	REV04	8G B	128MB	NA	NA	dual die ddr
TE0803-04-4DE11-A	4ev_2gb	REV04	2G B	128MB	NA	NA	NA
TE0803-04-4DE21-L	4ev_4gb	REV04	4G B	128MB	NA	1 mm connectors	NA
TE0803-04-4DI21-L	4ev_i_4gb	REV04	4G B	128MB	NA	1 mm connectors	NA

Module Model	Board Part Short Name	PCB Revision Support	D D R	QSPI Flash	EM MC	Others	Notes
TE0803-03-4DI21-D	4ev_i_4gb	REV03	4G B	128MB	NA		NA
TE0803-04-4DI21-D	4ev_i_4gb	REV04	4G B	128MB	NA		NA
TE0803-04-4GE21-L	4eg_2_4gb	REV04	4G B	128MB	NA	1 mm connectors	NA
TE0803-04-4GI21-A	4eg_2i_4gb	REV04	4G B	128MB	NA	NA	NA
TE0803-04-5BE11-A	5eg_2gb	REV04	2G B	128MB	NA	NA	NA
TE0803-04-5DE11-A	5ev_2gb	REV04	2G B	128MB	NA	NA	NA
TE0803-04-5DI21-A	5ev_i_4gb	REV04	4G B	128MB	NA	NA	NA
TE0803-03-S003	4ev_2gb	REV04	2G B	128MB	NA	NA	CAO
TE0803-03-S006	4ev_4gb	REV04	4G B	128MB	NA	1 mm connectors	CAO
TE0803-04-4BE11-A	4eg_2gb	REV04	2G B	128MB	NA	NA	CAO
TE0803-03-S005	4eg_2gb	REV03	2G B	128MB	NA	NA	CAO: TE0803-03-4BI1?-A

Module Model	Board Part Short Name	PCB Revision Support	D D R	QSPI Flash	EM MC	Others	Notes
TE0803-04-S009	4eg_2_4gb	REV04	4G B	128MB	NA	1 mm connectors	CAO: TE0803-04-4 GE21-L
TE0803-04-S011	4eg_2_4gb	REV04	4G B	64MB	NA	1 mm connectors	CAO: TE0803-04-4 GE25-L
TE0803-04-4AE11-A	4cg_2gb	REV04	2G B	128MB	NA	NA	NA
TE0803-04-S012	2cg_2gb	REV04	2G B	128MB	NA	NA	CAO

**Table 4: Hardware Modules**

\*used as reference

Note: Design contains also Board Part Files for TE0803+TEBF0808 configuration, this board part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
Custom PCB	use simple Board Part files, if MIO connected is different to TEBF0808
TEBF0808 <sup>*</sup>	Used as reference carrier. <b>Important:</b> CPLD Firmware REV07 or newer is recommended
TEBT0808-01	Change UART0 to UART1 (MIO68...69) and regenerate design

**Table 5: Hardware Carrier**

\*used as reference

Additional HW Requirements:

Additional Hardware	Notes
---	---

**Table 6: Additional Hardware**

\* used as reference

## 4.5 Content

For general structure and usage of the reference design, see [Project Delivery - AMD devices](#)<sup>3</sup>

### 4.5.1 Design Sources

Type	Location	Notes
Vivado	<project folder>\block_design <project folder>\constraints <project folder>\ip_lib <project folder>\board_files	Vivado Project will be generated by TE Scripts
Vitis	<project folder>\sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation

**Table 7: Design sources**

### 4.5.2 Additional Sources

Type	Location	Notes
---	---	---

**Table 8: Additional design sources**

### 4.5.3 Prebuilt

<sup>3</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+AMD+devices>

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Diverse Reports	---	Report files in different formats
Hardware-Platform-Description-File	*.xsa	Exported Vivado <a href="#">hardware description file</a> for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

**Table 9: Prebuilt files (only on ZIP with prebuilt content)**

#### 4.5.4 Download

Reference Design is only usable with the specified Vivado/Vitis/PetaLinux version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0803 "Test Board" Reference Design](#)<sup>4</sup>

<sup>4</sup> [https://shop.trenz-electronic.de/Download/?path=Trenz\\_Electronic/Modules\\_and\\_Module\\_Carriers/5.2x7.6/TE0803/Reference\\_Design/2021.2/test\\_board](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0803/Reference_Design/2021.2/test_board)

## 5 Design Flow

**!** Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first launch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

See also:

- [AMD Development Tools](#)<sup>5</sup>
- [Vivado Projects - TE Reference Design](#)<sup>6</sup>
- [Project Delivery](#).<sup>7</sup>

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "\_create\_win\_setup.cmd" on Windows OS and "\_create\_linux\_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also be executed by Xilinx Vivado/Vitis GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)<sup>8</sup>

**!** **Caution!** Win OS has a 260 character limit for path lengths which can affect the Vivado tools. To avoid this issue, use Virtual Drive or the shortest possible names and directory locations for the reference design (for example "x:\<project folder>")

1. Run \_create\_win\_setup.cmd/\_create\_linux\_setup.sh and follow instructions on shell:

### **\_create\_win\_setup.cmd/\_create\_linux\_setup.sh**

```
-----Set design paths-----
-- Run Design with: _create_win_setup
-- Use Design Path: <absolute project path>
-----
-----TE Reference Design-----
-----
-- (0)  Module selection guide, project creation...prebuilt export...
-- (1)  Create minimum setup of CMD-Files and exit Batch
-- (2)  Create maximum setup of CMD-Files and exit Batch
-- (3)  (internal only) Dev
-- (4)  (internal only) Prod
-- (c)  Go to CMD-File Generation (Manual setup)
-- (d)  Go to Documentation (Web Documentation)
-- (g)  Install Board Files from Xilinx Board Store (beta)
-- (a)  Start design with unsupported Vivado Version (beta)
-- (x)  Exit Batch (nothing is done!)
-----
Select (ex.: '0' for module selection guide):
```

2. Press 0 and enter to start "Module Selection Guide"
3. Create project and follow instructions of the product selection guide, settings file will be configured automatically during this process.


<sup>5</sup> <https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDDevelopmentTools-XilinxSoftware-BasicUserGuides>

<sup>6</sup> <https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design>

<sup>7</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+AMD+devices>

<sup>8</sup> <https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+AMD+devices#ProjectDeliveryAMDdevices-Currentlylimitationsoffunctionality>


- optional for manual changes: Select correct device and Xilinx install path on "design\_basic\_settings.cmd" and create Vivado project with "vivado\_create\_project\_gui mode.cmd"

 Note: Select correct one, see also [Vivado Board Part Flow](#)<sup>9</sup>  
**Important:** Use Board Part Files, which **did not** ends with \*\_tebf0808

4. Create hardware description file (.xsa file) for PetaLinux project and export to prebuilt folder

**run on Vivado TCL (Script generates design and export files into "\prebuilt\hardware\")**


```
\prebuilt\hardware\")">  
TE::hw_build_design -export_prebuilt
```

 Using Vivado GUI is the same, except file export to prebuilt folder.

5. Generate Programming Files with Vitis

**run on Vivado TCL (Script generates applications and bootable files, which are defined in "test\_board\sw\_lib\apps\_list.csv")**

```
TE::sw_run_vitis -all  
TE::sw_run_vitis (optional; Start Vitis from Vivado GUI or start with TE  
Scripts on Vivado TCL)
```

 TCL scripts generate also platform project, this must be done manually in case GUI is used. See [Vitis](#)<sup>10</sup>

<sup>9</sup> <https://wiki.trenz-electronic.de/display/PD/Vivado+Board+Part+Flow>


<sup>10</sup> <https://wiki.trenz-electronic.de/display/PD/Vitis>

## 6 Launch

---

### 6.1 Programming

---


 Check Module and Carrier TRMs for proper HW configuration before you try any design. Reference Design is also available with prebuilt files. It's recommended to use TE prebuilt files for first launch.

Xilinx documentation for programming and debugging: [Vivado/Vitis/SDSoC-Xilinx Software Programming and Debugging](#)<sup>11</sup>

#### 6.1.1 Get prebuilt boot binaries

---

1. Run `_create_win_setup.cmd/_create_linux_setup.sh` and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
  - a. Select assembly version
  - b. Validate selection
  - c. Select create and open delivery binary folder

 Note: Folder "<project folder>\\_binaries\_<Article Name>" with subfolder "boot\_<app name>" for different applications will be generated

#### 6.1.2 QSPI-Boot mode

---

1. Connect **JTAG** and power on carrier with module
2. Open Vivado Project with "vivado\_open\_existing\_project\_guimode.cmd" or if not created, create with "vivado\_create\_project\_guimode.cmd"

**run on Vivado TCL (Script programs BOOT.bin on QSPI flash)**

```
TE::pr_program_flash -swapp hello_te0803
```

#### 6.1.3 SD-Boot mode

---

This does not work, because SD controller is not selected on PS.

#### 6.1.4 JTAG

---

Load configuration and Application with Vitis Debugger into device

---

<sup>11</sup> <https://wiki.trenz-electronic.de/display/PD/AMD+Development+Tools#AMDDDevelopmentTools-XilinxSoftwareProgrammingandDebugging>



## 6.2 Usage

---

### QSPI Boot:

1. Prepare HW like described on section [Programming](#)(see page 24)
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI as Boot Mode



Note: See TRM of the Carrier, which is used.

4. Power On PCB

#### **boot process**

1. ZynqMP Boot ROM loads FSBL from QSPI into OCM,
2. FSBL init the PS, programs the PL using the bitstream and loads PMU, ATF and U-boot from QSPI into DDR,

## 7 System Design - Vivado

### 7.1 Block Design



Figure 1: Block Design

#### 7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
UART0	MIO, please select other one, if you have connected UART to second controller or other MIO
SWDT0..1	
TTC0..3	

Table 10: PS Interfaces

## 7.2 Constrains

---

### 7.2.1 Basic module constrains

---

#### **\_i\_bitgen.xdc**

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]  
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

### 7.2.2 Design specific constrain

---

Not needed.

## 8 Software Design - Vitis

---

For Vitis project creation, follow instructions from:

[Vitis](#)<sup>12</sup>

### 8.1 Application

---

Template location: "<project folder>\sw\_lib\sw\_apps\"

#### 8.1.1 zynqmp\_fsbl

---

TE modified 2021.2 FSBL

General:

- Modified Files: xfsbl\_main.c, xfsbl\_hooks.h/.c, xfsbl\_board.h/.c (search for 'TE Mod' on source code)
- Add Files: te\_xfsbl\_hooks.h/.c (for hooks and board)
- General Changes:
  - Display FSBL Banner and Device Name

#### 8.1.2 zynqmp\_fsbl\_flash

---

TE modified 2021.2 FSBL

General:

- Modified Files: xfsbl\_initialisation.c, xfsbl\_hw.h, xfsbl\_handoff.c, xfsbl\_main.c
- General Changes:
  - Display FSBL Banner
  - Set FSBL Boot Mode to JTAG
  - Disable Memory initialisation

#### 8.1.3 hello\_te0803

---

Hello TE0803 is a Xilinx Hello World example as endless loop instead of one console output.

---

<sup>12</sup> <https://wiki.trenz-electronic.de/display/PD/Vitis>

## 9 Additional Software


---

No additional software is needed.

## 10 Appx. A: Change History and Legal Notices

### 10.1 Document Change History

To get content of older revision go to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
 2022-10-17	v.33 (see page 6)	Manuela Strücker <sup>13</sup>	<ul style="list-style-type: none"> <li>script update</li> </ul>
2022-09-06	v.32	Manuela Strücker	<ul style="list-style-type: none"> <li>new assembly variants</li> </ul>
2022-07-15	v.30	Manuela Strücker	<ul style="list-style-type: none"> <li>Release 2021.2</li> </ul>
2021-09-09	v.25	Manuela Strücker	<ul style="list-style-type: none"> <li>Release 2020.2</li> </ul>
2020-04-06	v.24	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variants</li> </ul>
2020-03-25	v.23	John Hartfiel	<ul style="list-style-type: none"> <li>Script update</li> </ul>
2020-01-23	v.22	John Hartfiel	<ul style="list-style-type: none"> <li>Release 2019.2</li> </ul>
2019-05-07	v.21	John Hartfiel	<ul style="list-style-type: none"> <li>Release 2018.3</li> </ul>
2018-10-26	v.18	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> </ul>
2018-08-14	v.16	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> </ul>
2018-07-13	v.15	John Hartfiel	<ul style="list-style-type: none"> <li>Release 2018.2</li> </ul>
2018-05-18	v.14	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> </ul>
2018-04-11	v.13	John Hartfiel	<ul style="list-style-type: none"> <li>bugfix board part file</li> </ul>

<sup>13</sup> <https://wiki.trenz-electronic.de/display/~m.struecker>

Date	Document Revision	Authors	Description
2018-04-03	v.11	John Hartfiel	<ul style="list-style-type: none"> <li>new assembly variant</li> </ul>
2018-01-18	v.6	John Hartfiel	<ul style="list-style-type: none"> <li>Release 2017.4</li> </ul>
2017-11-16	v.4	John Hartfiel	<ul style="list-style-type: none"> <li>Update assembly versions with new Flash size</li> </ul>
2017-11-14	v.3	John Hartfiel	<ul style="list-style-type: none"> <li>Release 2017.2</li> </ul>
	All		

**Table 11: Document change history.**

Legal Notices

## 10.2 Data Privacy

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<sup>14</sup> <https://wiki.trenz-electronic.de/display/~j.hartfiel>

<sup>15</sup> <https://wiki.trenz-electronic.de/display/~m.struecker>

<sup>16</sup> <https://wiki.trenz-electronic.de/display/~tht>

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<sup>17</sup> <http://guidance.echa.europa.eu/>


<sup>18</sup> <https://echa.europa.eu/candidate-list-table>

<sup>19</sup> <http://www.echa.europa.eu/>



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