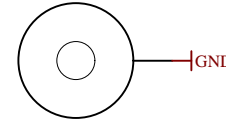


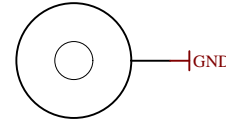
U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_DDR4-TERM DDR4-TERM.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	U_POWER_3 POWER_3.SchDoc
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	
U_B_GT_2 B_GT_2.SchDoc	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

Special notes:

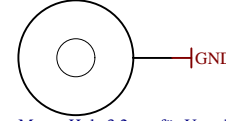
*U41 Power supervisor TPS3106K33DBVR replaced by Schottky diodes SBAS70-04LT1G*



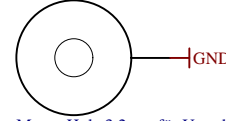
Mount.Hole 3.2mm für Unterlegscheibe



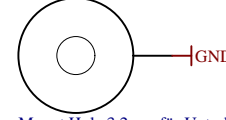
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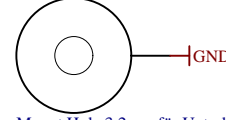
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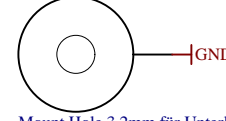
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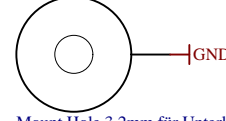
Mount.Hole 3.2mm für Unterlegscheibe



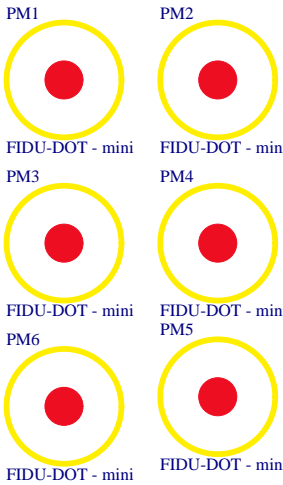
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



LOGO1  
TE Logo PRINT Layer  
LOGO PRINT

Serial  
Serialnumber 6,3 x 6.3mm

Assembly variant	4AI21-X
Created by	VY
Modified by	VY
Modified at	2020-03-02
SVN Revision	9080 [Locally Modified]



Title: TE0807		
A4	Number: TE0807 4AI21-X	Rev. 02
Date: 2018-07-09	Copyright: Trenz Electronic GmbH / TT	Page1 of 28
Filename: TE0807.SchDoc		

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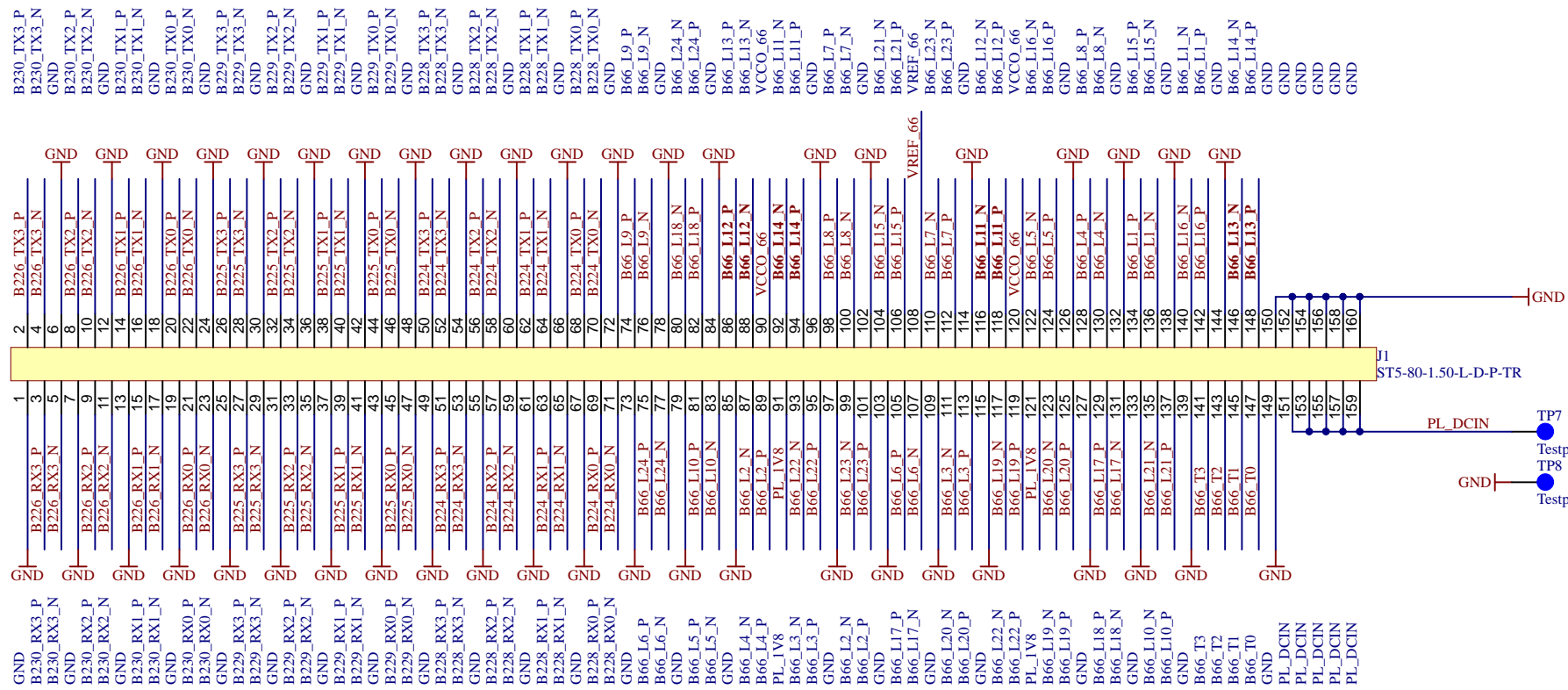
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		Title: TE0807 - Connector J1	
		A4	Number: TE0807 4AI21-X
Date: 2018-07-09		Copyright: Trenz Electronic GmbH / TT	
Filename: J1.SchDoc		Page2 of 28	

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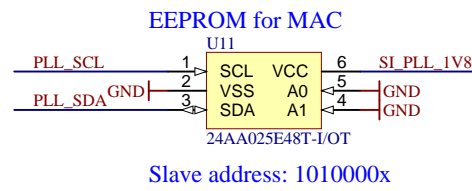
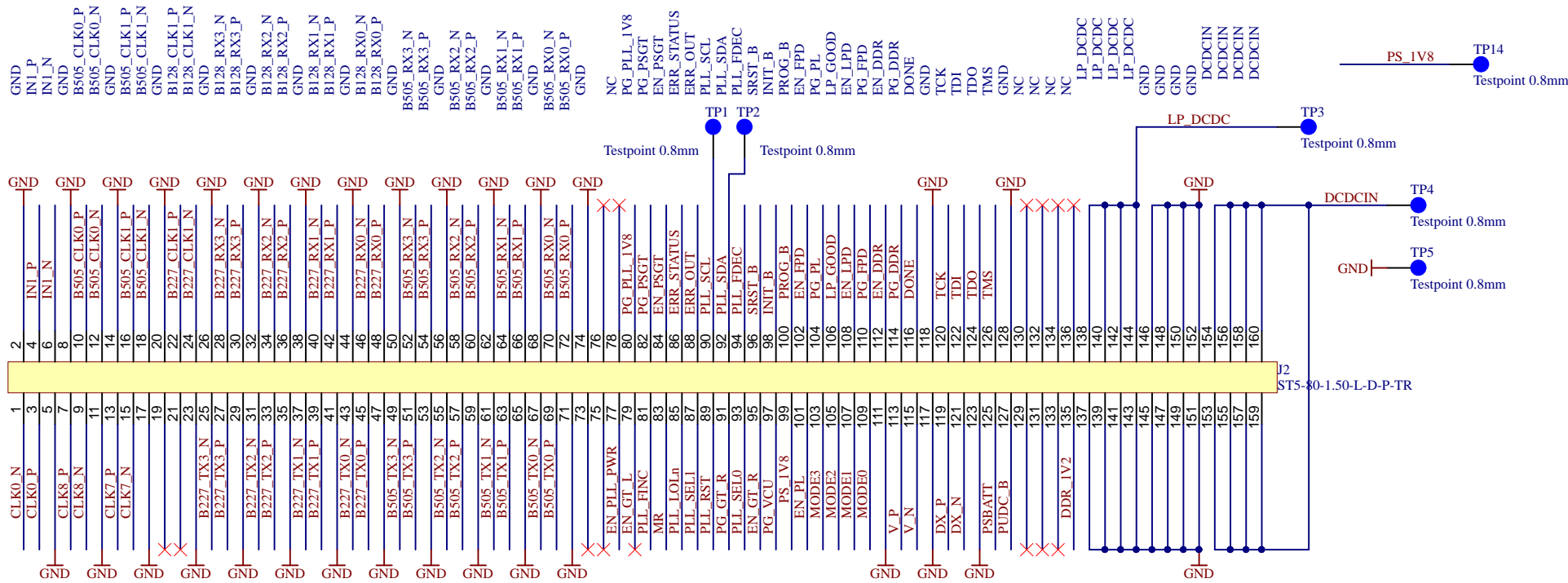
4

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Title: TE0807 - Connector J2		
A4	Number: TE0807 4AI21-X	Rev. 02
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Filename: J2.SchDoc		

A

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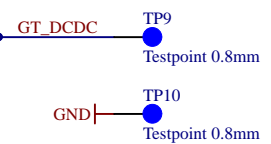
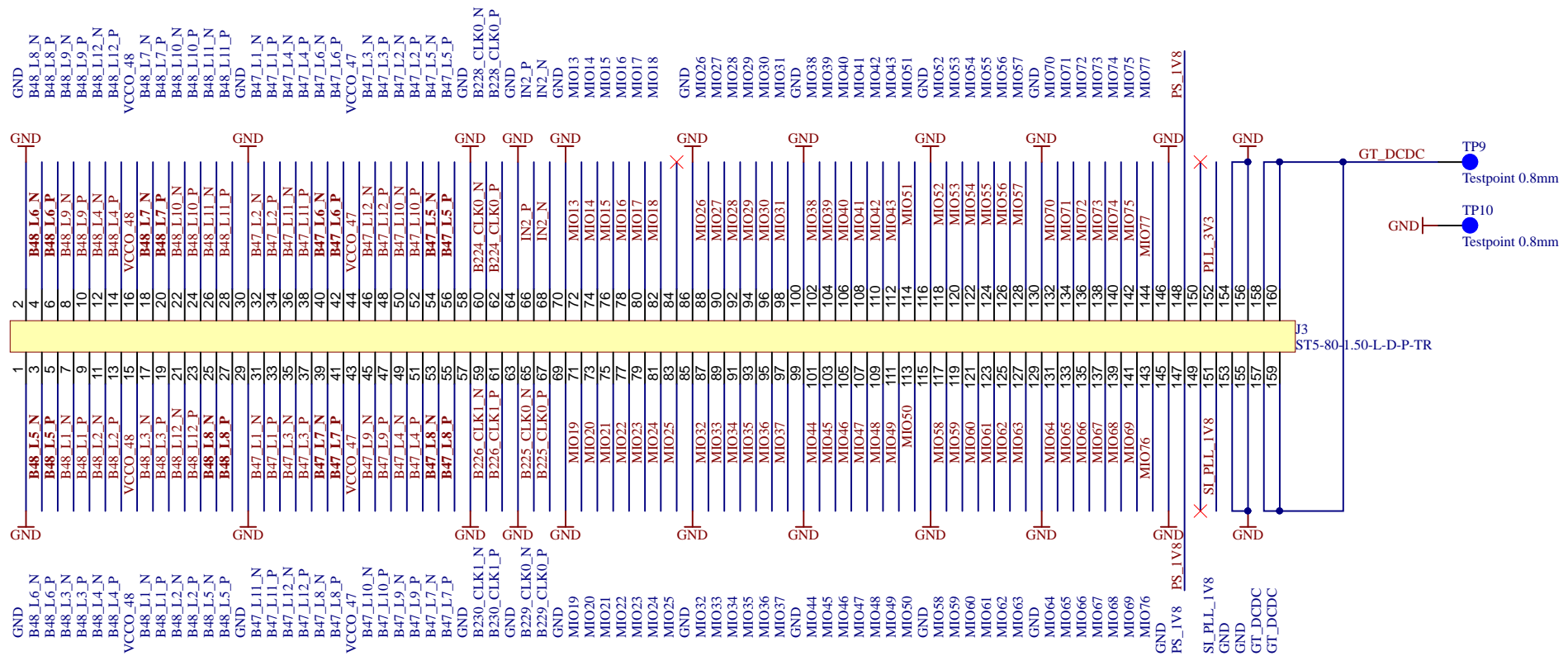
D


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			Title: TE0807 - Connector J3	
			A4	Number: TE0807 4A121-X
Date: 2018-07-09		Copyright: Trenz Electronic GmbH / TT		Page4 of 28
Filename: J3.SchDoc				

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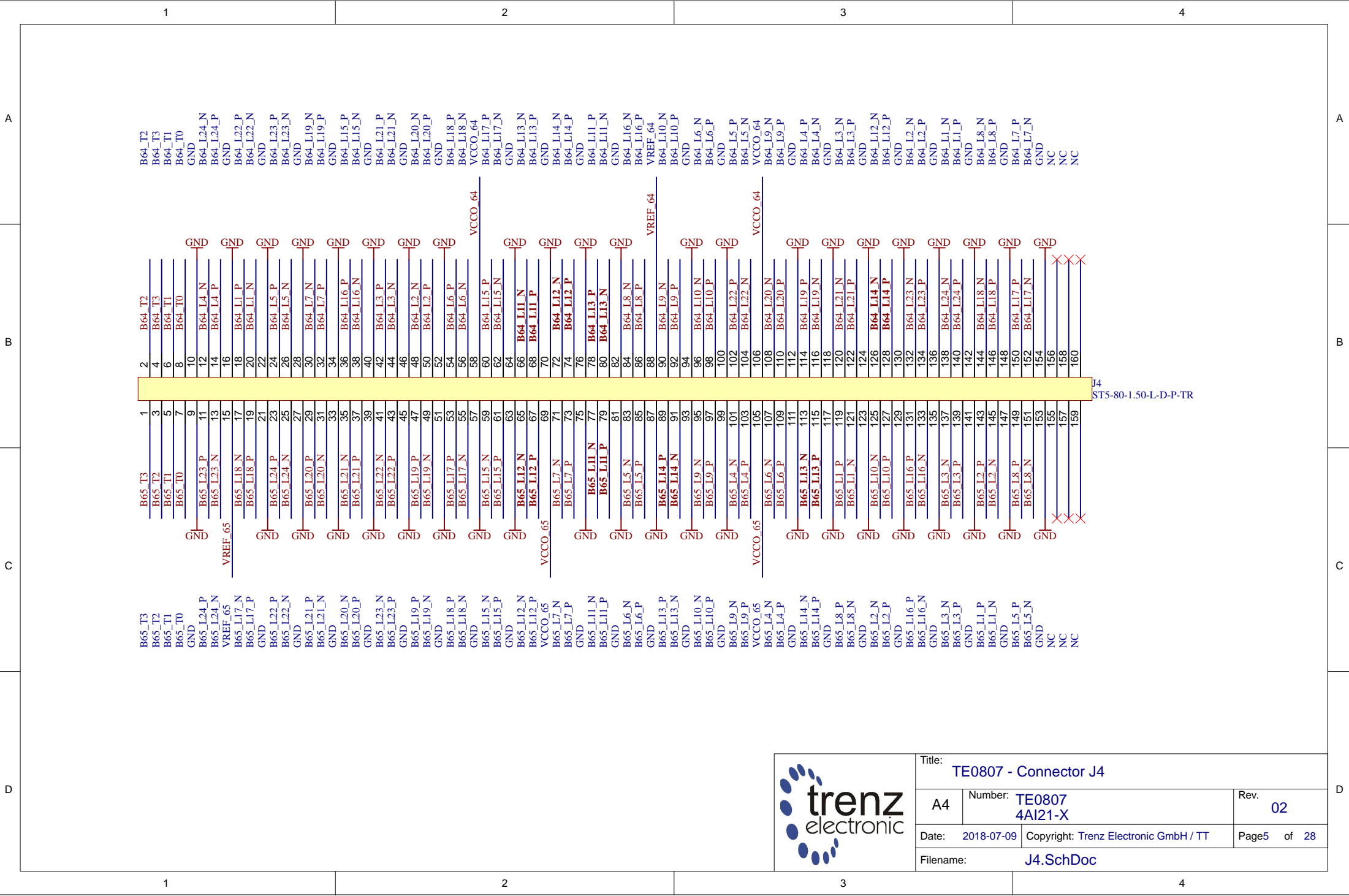
4

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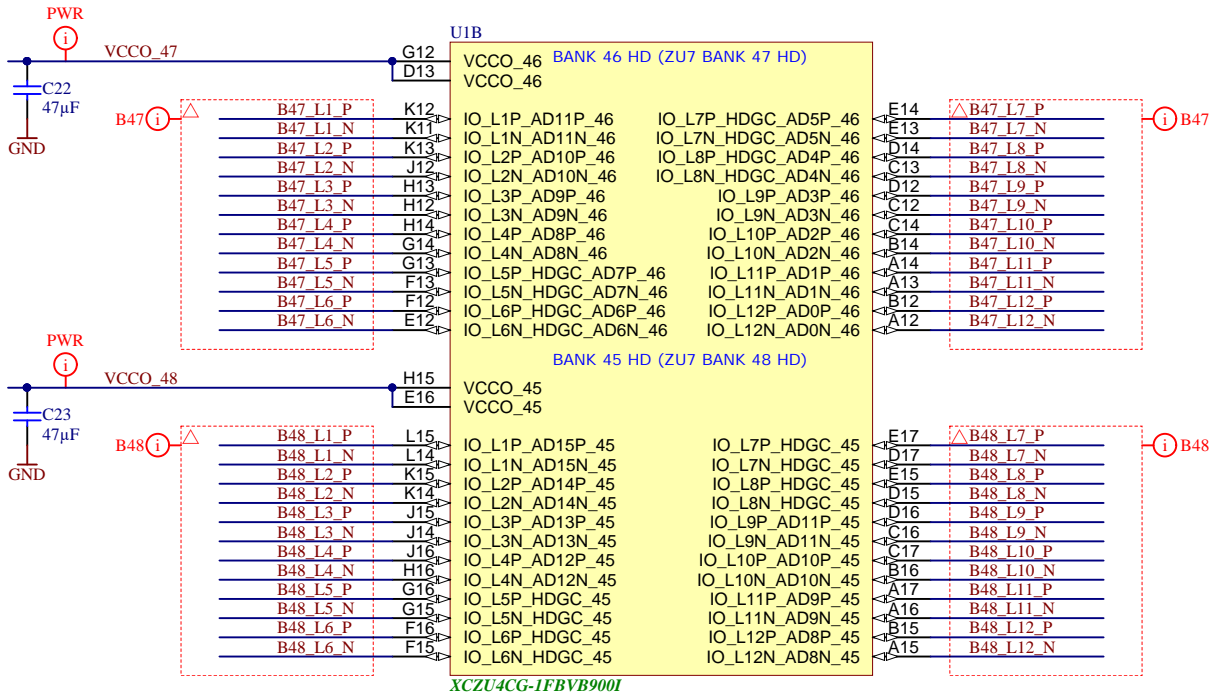
D



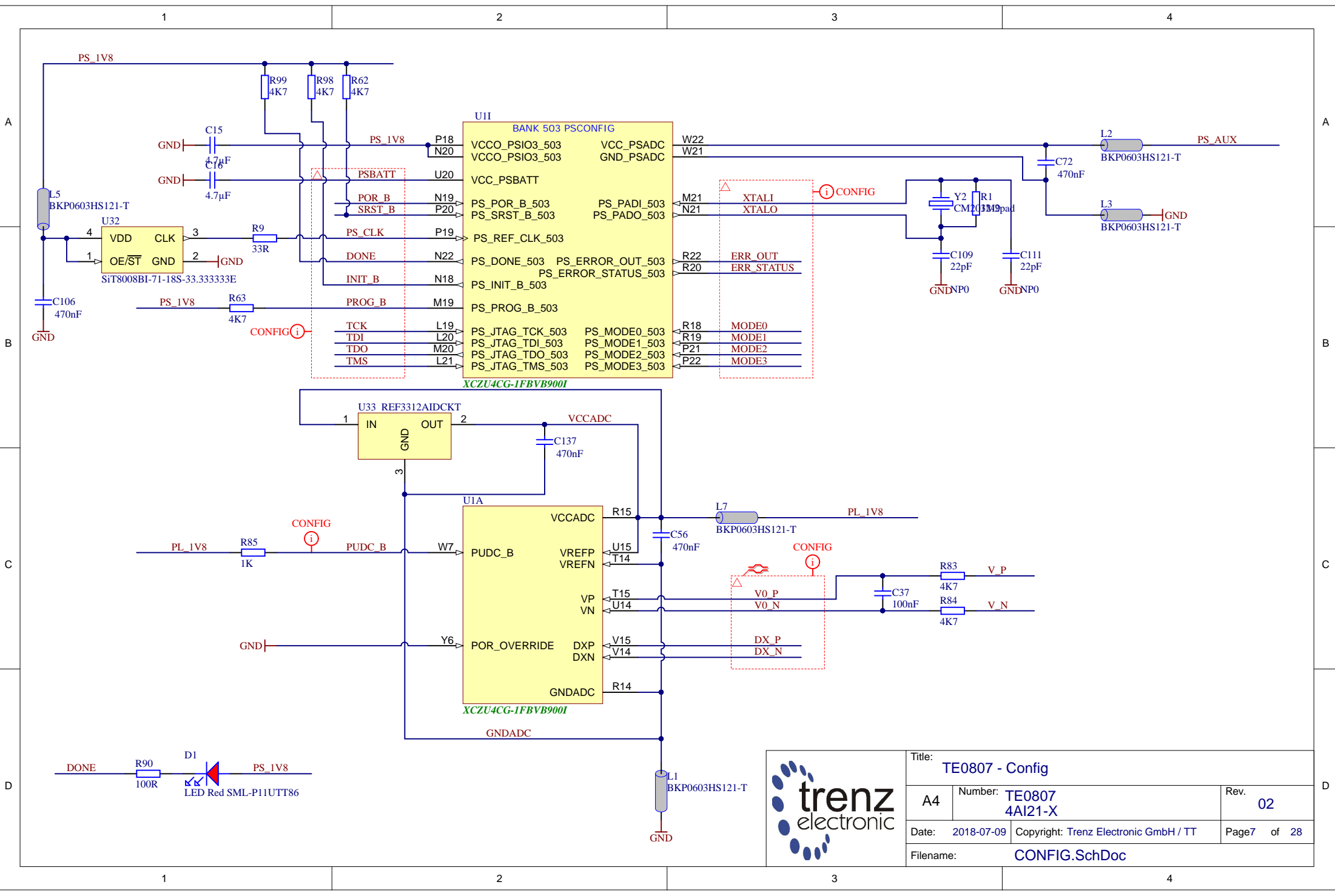
J4  
ST5-80-1.50-L-D-P-TR



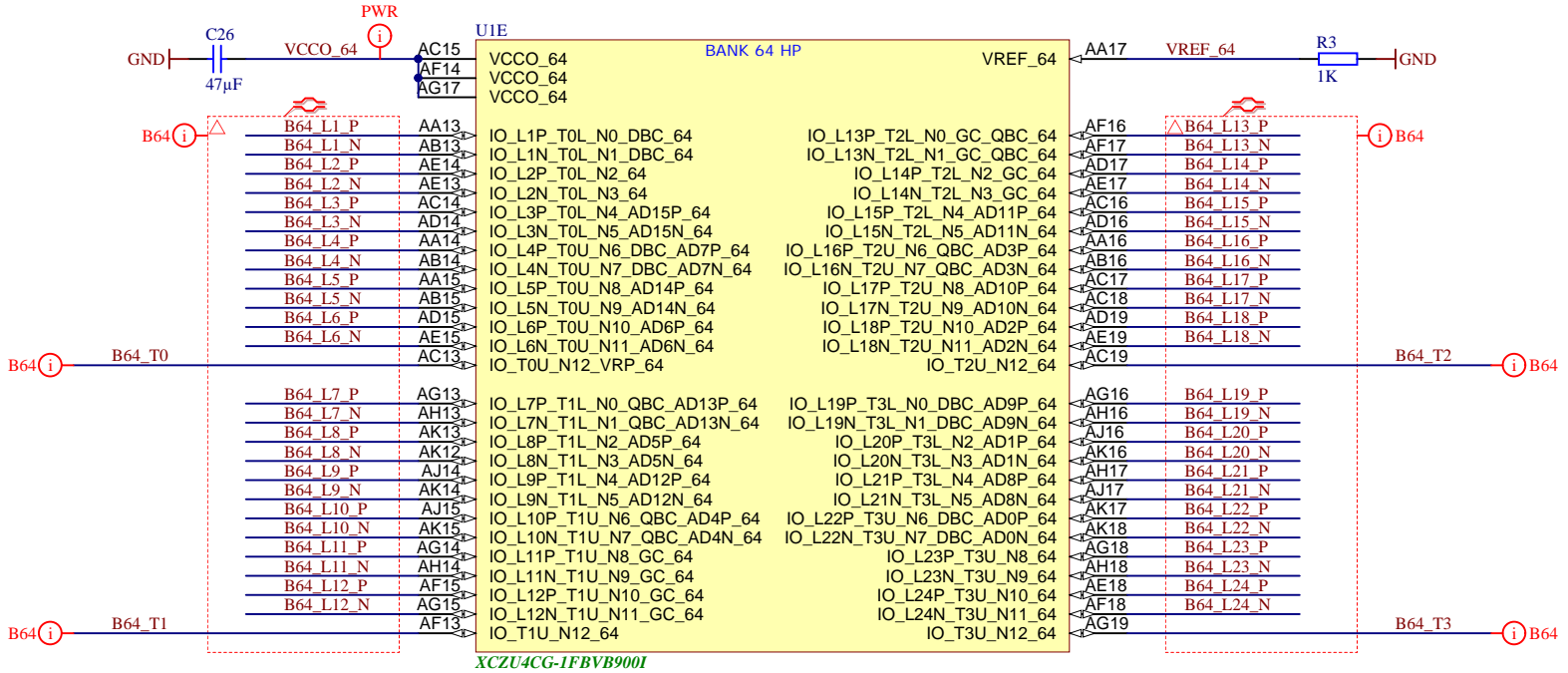
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A4	Number: TE0807 4AI21-X	Rev. 02
Date: 2018-07-09	Copyright: Trenz Electronic GmbH / TT	Page5 of 28
Filename: J4.SchDoc		



Title: TE0807 - B47HD and B48HD		
A4	Number: TE0807 4AI21-X	Rev. 02
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Filename: B_HD.SchDoc		

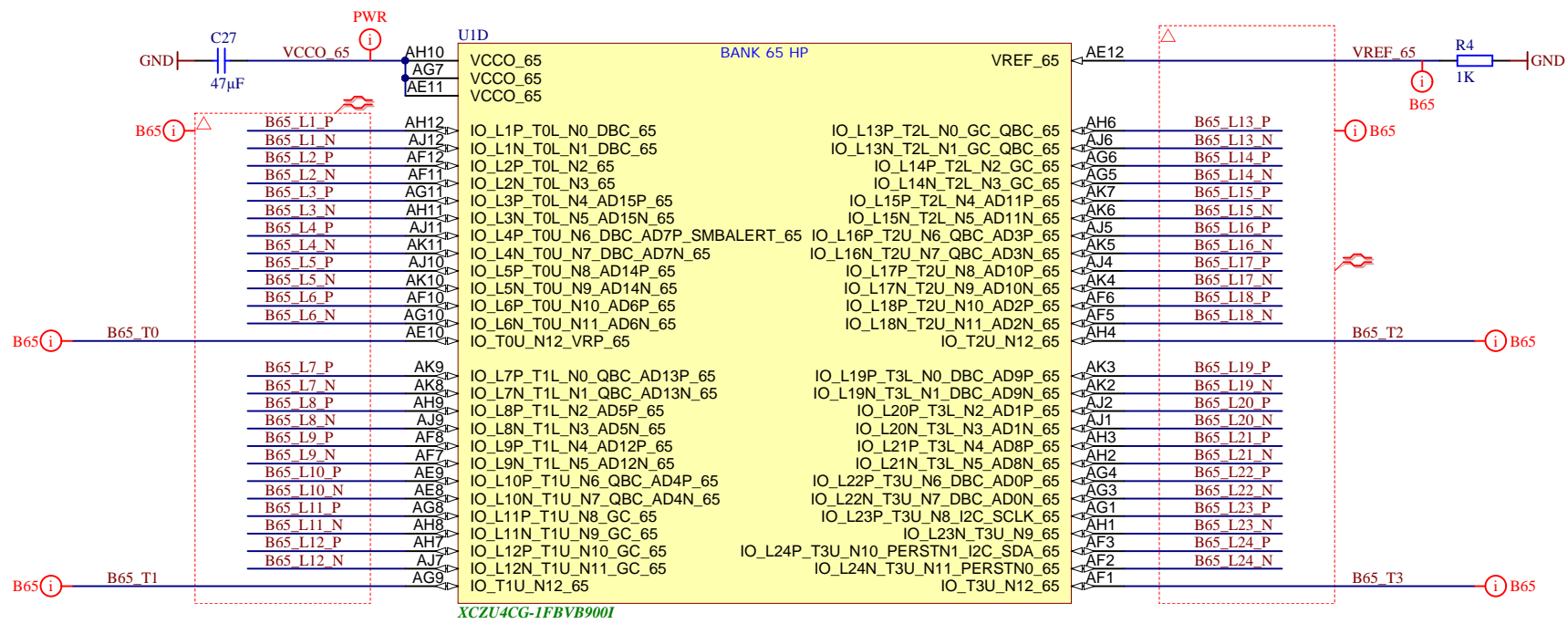


Title: TE0807 - Config		
A4	Number: TE0807 4AI21-X	Rev. 02
Date: 2018-07-09	Copyright: Trenz Electronic GmbH / TT	Page 7 of 28
Filename: CONFIG.SchDoc		



Title: <b>TE0807 - B64</b>		
A4	Number: <b>TE0807 4AI21-X</b>	Rev. <b>02</b>
Date: <b>2018-07-09</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>8</b> of <b>28</b>
Filename: <b>B64.SchDoc</b>		

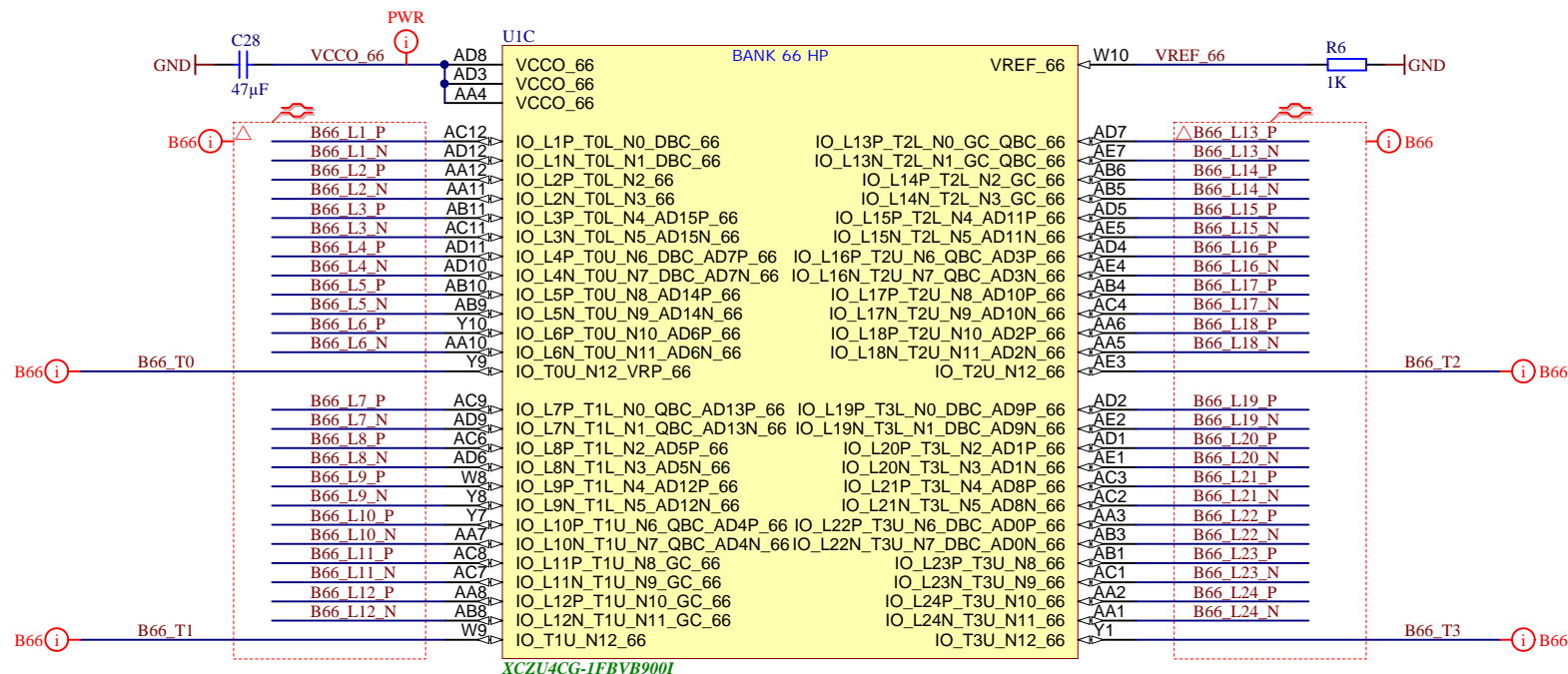




XCZU4CG-1FBVB900I



Title: <b>TE0807 - B65</b>		
A4	Number: <b>TE0807 4AI21-X</b>	Rev. <b>02</b>
Date: <b>2018-07-09</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>9</b> of <b>28</b>
Filename: <b>B65.SchDoc</b>		



Title: TE0807 - B66		
A4	Number: TE0807 4AI21-X	Rev. 02
Date: 2018-07-09	Copyright: Trenz Electronic GmbH / TT	Page 10 of 28
Filename: B66.SchDoc		

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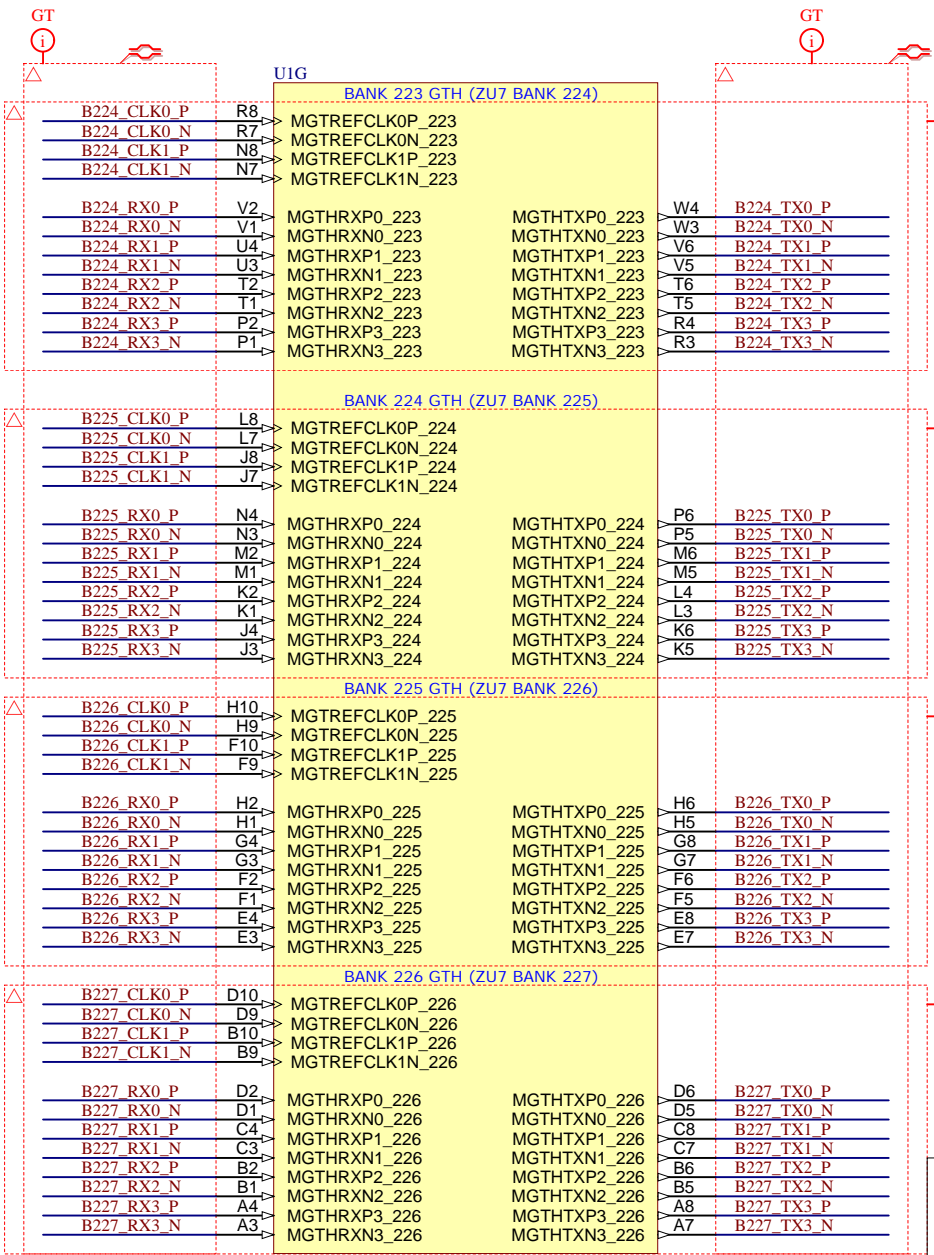
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228

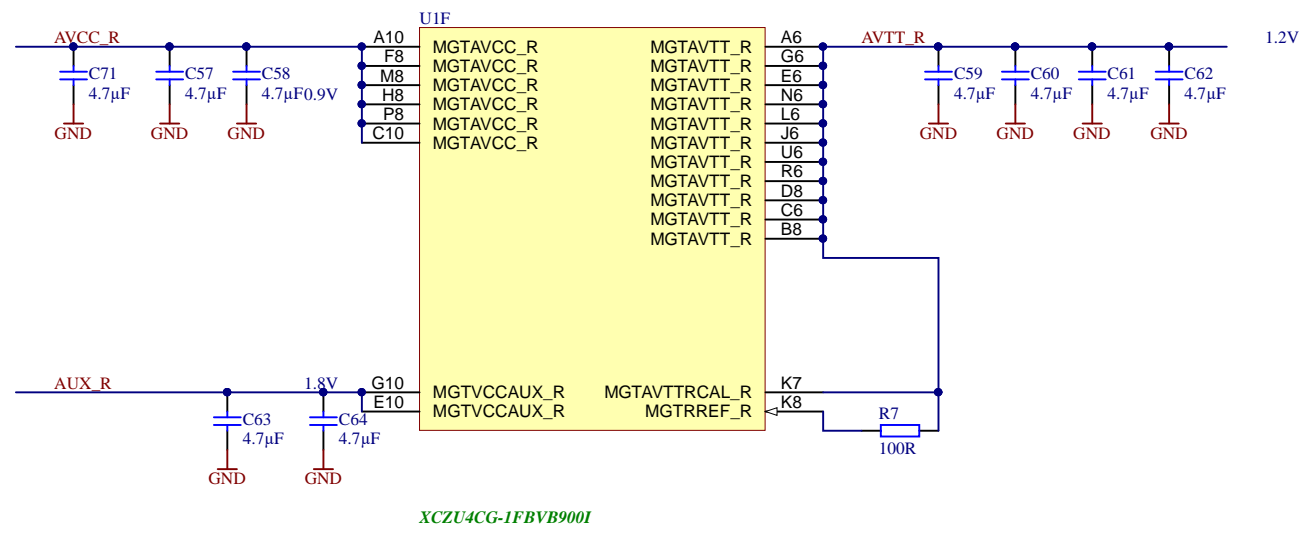
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230


*XCZU4CG-1FBVB9001*

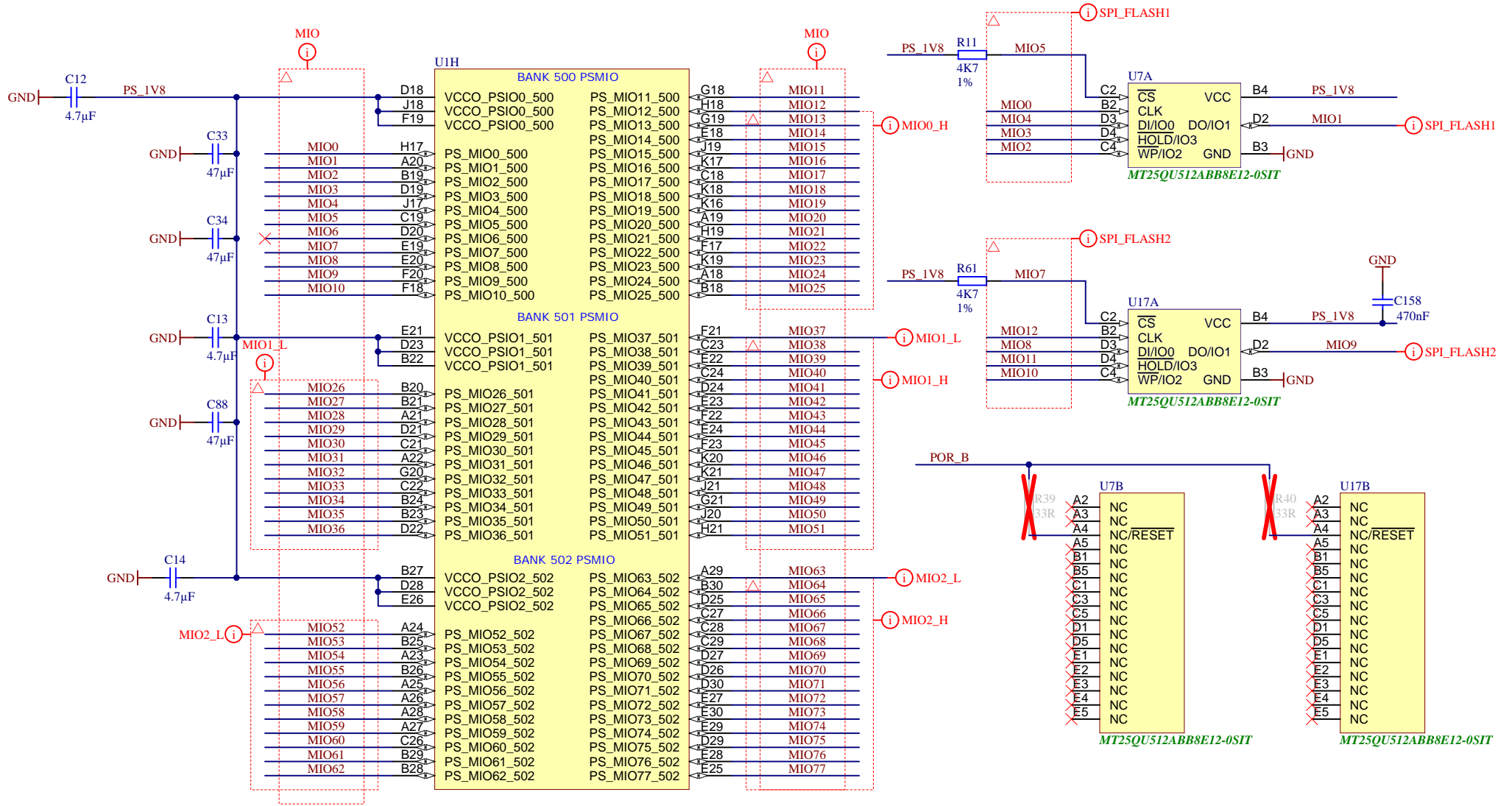


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A4	Number: <b>TE0807 4AI21-X</b>	Rev. <b>02</b>
Date: <b>2018-07-09</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>11</b> of <b>28</b>
Filename: <b>B_GT.SchDoc</b>		




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			Title: TE0807 - GTH_PWR	
			A4	Number: TE0807 4AI21-X
Date: 2018-07-09		Copyright: Trenz Electronic GmbH / TT		Page 12 of 28
Filename: B_GT_2.SchDoc				



XCZU4CG-1FBVB9001

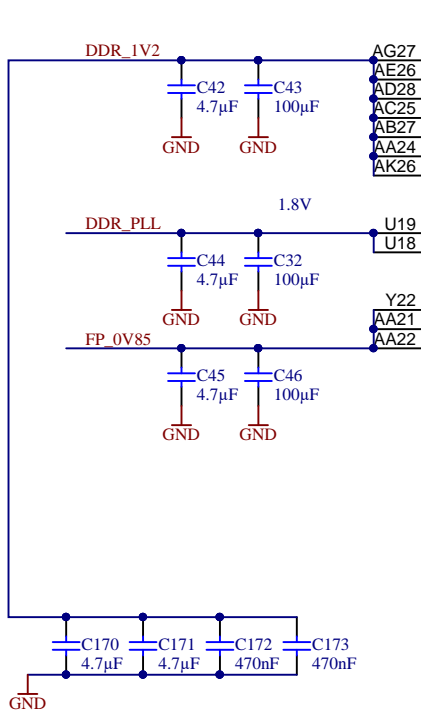
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		A4	Number: TE0807 4AI21-X
Date: 2018-07-09		Copyright: Trenz Electronic GmbH / TT	
Filename: B_MIO.SchDoc		Page 13 of 28	

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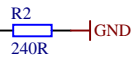
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UIJ BANK 504 PSDDR		
AG27	VCCO_PSDDR_504	PS_DDR_CK0_504
AE26	VCCO_PSDDR_504	PS_DDR_CK_N0_504
AD28	VCCO_PSDDR_504	PS_DDR_CKE0_504
AC25	VCCO_PSDDR_504	
AB27	VCCO_PSDDR_504	PS_DDR_CK1_504
AA24	VCCO_PSDDR_504	PS_DDR_CK_N1_504
AK26	VCCO_PSDDR_504	PS_DDR_CKE1_504
U19	VCC_PSDDR_PLL	PS_DDR_A0_504
U18	VCC_PSDDR_PLL	PS_DDR_A1_504
Y22	VCC_PSINTFP_DDR	PS_DDR_A2_504
AA21	VCC_PSINTFP_DDR	PS_DDR_A3_504
AA22	VCC_PSINTFP_DDR	PS_DDR_A4_504
		PS_DDR_A5_504
		PS_DDR_A6_504
		PS_DDR_A7_504
		PS_DDR_A8_504
		PS_DDR_A9_504
		PS_DDR_A10_504
		PS_DDR_A11_504
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		PS_DDR_A14_504
		PS_DDR_A15_504
		PS_DDR_A16_504
		PS_DDR_A17_504
		PS_DDR_CS_N0_504
		PS_DDR_CS_N1_504
		PS_DDR_BA0_504
		PS_DDR_BA1_504
		PS_DDR_BG0_504
		PS_DDR_BG1_504
		PS_DDR_PARITY_504
		PS_DDR_RAM_RST_N_504
		PS_DDR_ACT_N_504
		PS_DDR_ALERT_N_504
		PS_DDR_ZQ_504
		PS_DDR_ODT0_504
		PS_DDR_ODT1_504

XCZU4CG-1FBVB9001

AE30	DDR4-CLK0_P
AF30	DDR4-CLK0_N
AC30	DDR4-CKE0
AF28	
AG28	
AB28	
AH30	DDR4-A0
AG30	DDR4-A1
AK29	DDR4-A2
AJ30	DDR4-A3
AK28	DDR4-A4
AK27	DDR4-A5
AF27	DDR4-A6
AE27	DDR4-A7
AF26	DDR4-A8
AG26	DDR4-A9
AE29	DDR4-A10
AE28	DDR4-A11
AH29	DDR4-A12
AH28	DDR4-A13
AG29	DDR4-A14
AJ29	DDR4-A15
AH27	DDR4-A16
AJ27	DDR4-A17
AD30	DDR4-CS
AD29	
AD27	DDR4-BA0
AC26	DDR4-BA1
AC28	DDR4-BG0
AC27	
AB26	DDR4-PAR
AB25	DDR4-RESET
AD26	DDR4-ACT
AB24	DDR4-ALERT
AB23	
AB30	DDR4-ODT0
AC29	



DQ0	AH22
DQ1	AH21
DQ2	AJ22
DQ3	AK22
DQ4	AK20
DQ5	AJ19
DQ6	AK19
DQ7	AH19
DQ8	AH23
DQ9	AK23
DQ10	AG24
DQ11	AK24
DQ12	AJ26
DQ13	AK25
DQ14	AG25
DQ15	AH26
DQ16	AD22
DQ17	AE22
DQ18	AF22
DQ19	AG21
DQ20	AD20
DQ21	AF20
DQ22	AE20
DQ23	AG20
DQ24	AG23
DQ25	AF23
DQ26	AF25
DQ27	AE23
DQ28	AC22
DQ29	AC23
DQ30	AD25
DQ31	AC24
DDR4-DQS0_P	AJ21
DDR4-DQS0_N	AK21
DDR4-DQS1_P	AH24
DDR4-DQS1_N	AJ24
DDR4-DQS2_P	AC21
DDR4-DQS2_N	AD21
DDR4-DQS3_P	AD24
DDR4-DQS3_N	AE24
DDR4-DQS4_P	W24
DDR4-DQS4_N	W25
DDR4-DQS5_P	P25
DDR4-DQS5_N	R25
DDR4-DQS6_P	U29
DDR4-DQS6_N	V29
DDR4-DQS7_P	R28
DDR4-DQS7_N	R29
	Y28
	AA28

UIK BANK 504 PSDDR	
PS_DDR_DQ0_504	PS_DDR_DQ32_504
PS_DDR_DQ1_504	PS_DDR_DQ33_504
PS_DDR_DQ2_504	PS_DDR_DQ34_504
PS_DDR_DQ3_504	PS_DDR_DQ35_504
PS_DDR_DQ4_504	PS_DDR_DQ36_504
PS_DDR_DQ5_504	PS_DDR_DQ37_504
PS_DDR_DQ6_504	PS_DDR_DQ38_504
PS_DDR_DQ7_504	PS_DDR_DQ39_504
PS_DDR_DQ8_504	PS_DDR_DQ40_504
PS_DDR_DQ9_504	PS_DDR_DQ41_504
PS_DDR_DQ10_504	PS_DDR_DQ42_504
PS_DDR_DQ11_504	PS_DDR_DQ43_504
PS_DDR_DQ12_504	PS_DDR_DQ44_504
PS_DDR_DQ13_504	PS_DDR_DQ45_504
PS_DDR_DQ14_504	PS_DDR_DQ46_504
PS_DDR_DQ15_504	PS_DDR_DQ47_504
PS_DDR_DQ16_504	PS_DDR_DQ48_504
PS_DDR_DQ17_504	PS_DDR_DQ49_504
PS_DDR_DQ18_504	PS_DDR_DQ50_504
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PS_DDR_DQ20_504	PS_DDR_DQ52_504
PS_DDR_DQ21_504	PS_DDR_DQ53_504
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PS_DDR_DQ9_504	PS_DDR_DQ4_504
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PS_DDR_DQ69_504	PS_DDR_DQ64_504
PS_DDR_DQ70_504	PS_DDR_DQ65_504
PS_DDR_DQ71_504	PS_DDR_DQ66_504
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PS_DDR_DM1_504	PS_DDR_DM2_504
PS_DDR_DM2_504	PS_DDR_DM3_504
PS_DDR_DM3_504	PS_DDR_DM4_504
PS_DDR_DM4_504	PS_DDR_DM5_504
PS_DDR_DM5_504	PS_DDR_DM6_504
PS_DDR_DM6_504	PS_DDR_DM7_504
PS_DDR_DM7_504	PS_DDR_DM8_504
PS_DDR_DM8_504	

XCZU4CG-1FBVB9001



Title: TE0807 - PS_DDR		
A4	Number: TE0807 4AI21-X	Rev. 02
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Filename: PS_DDR.SchDoc		

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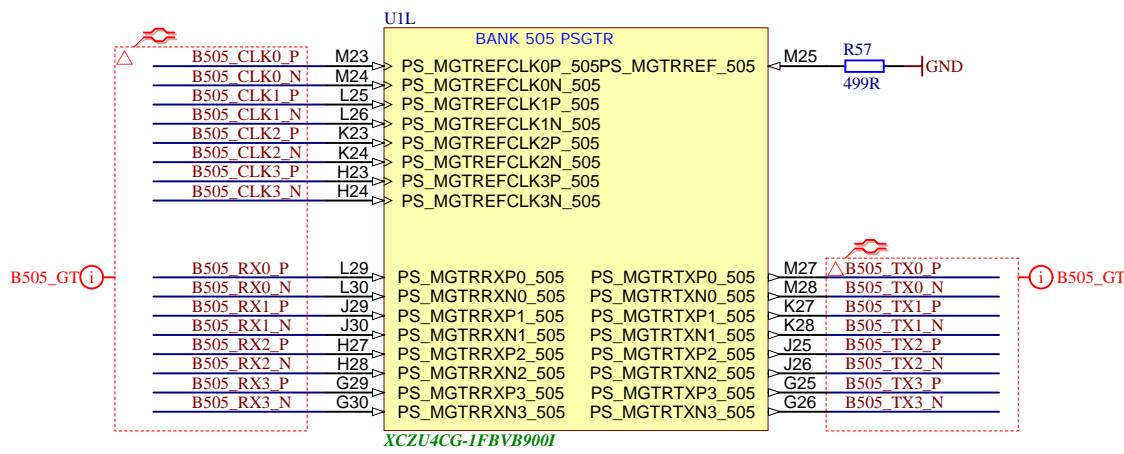
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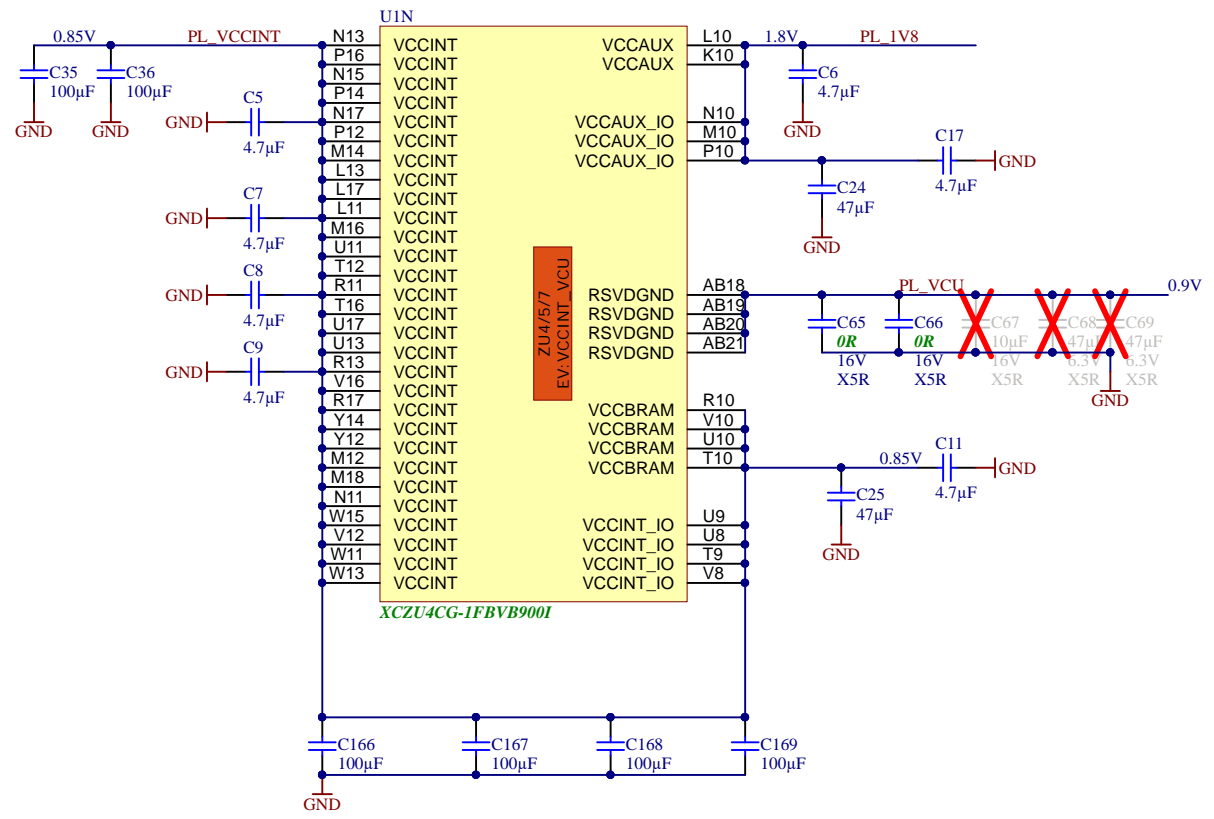
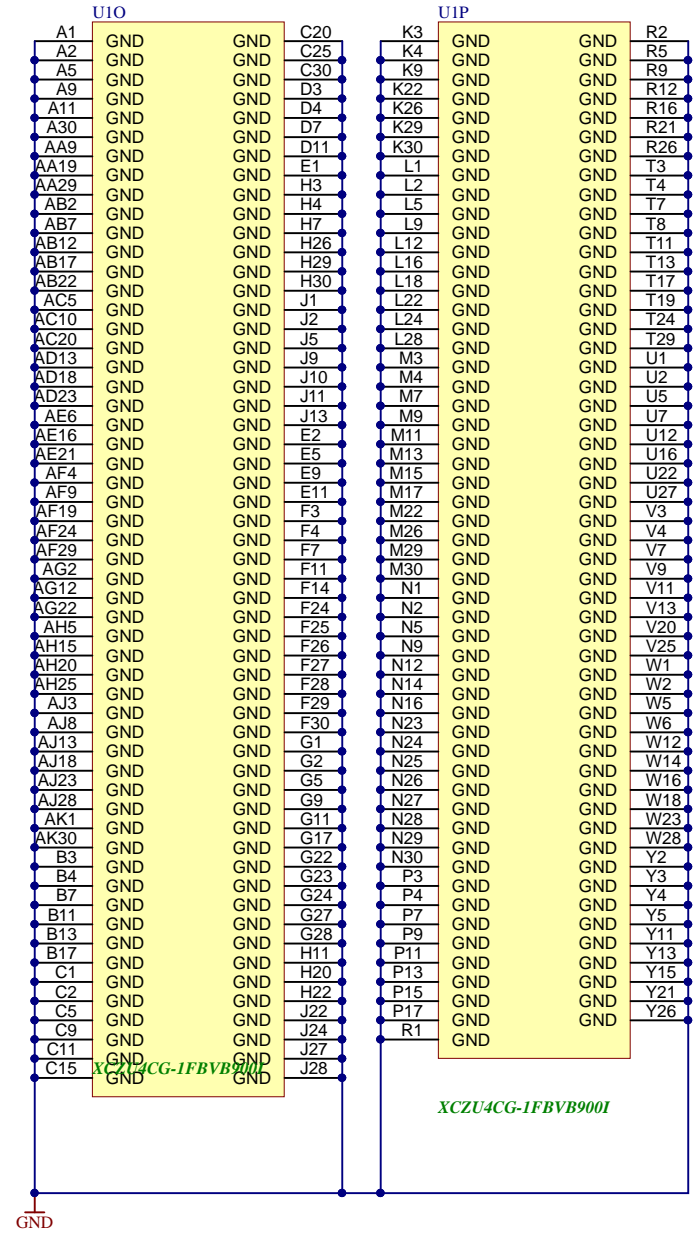
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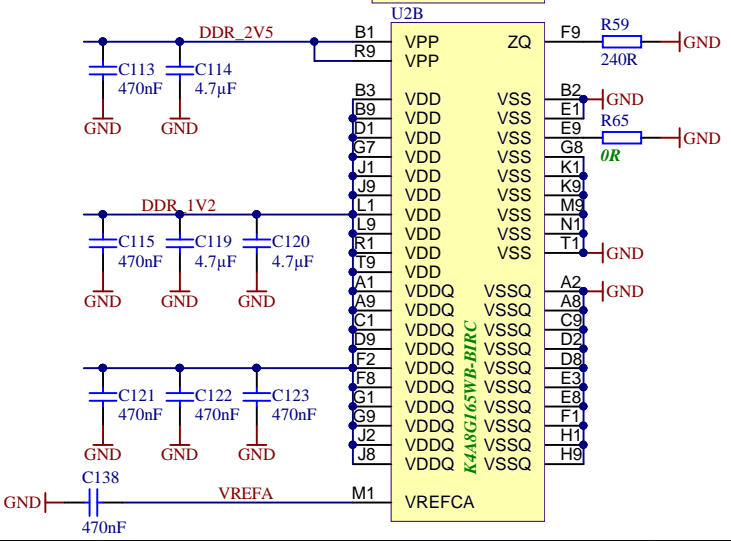
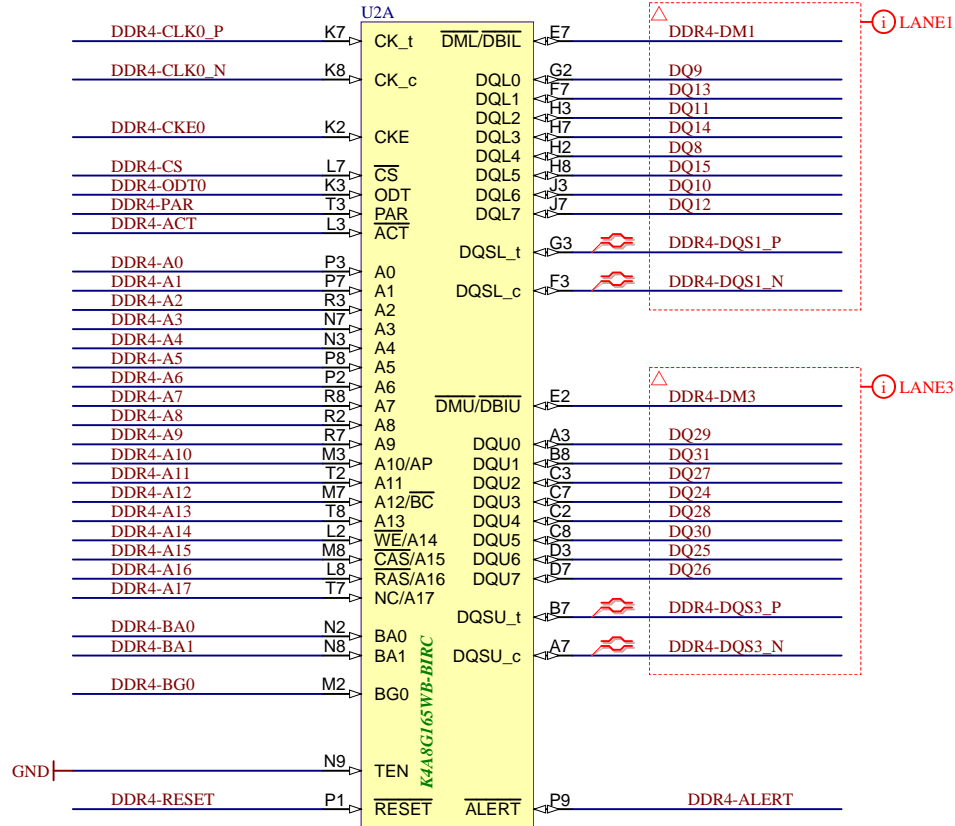
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	Date: 2018-07-09	Copyright: Trenz Electronic GmbH / TT	Page 15 of 28
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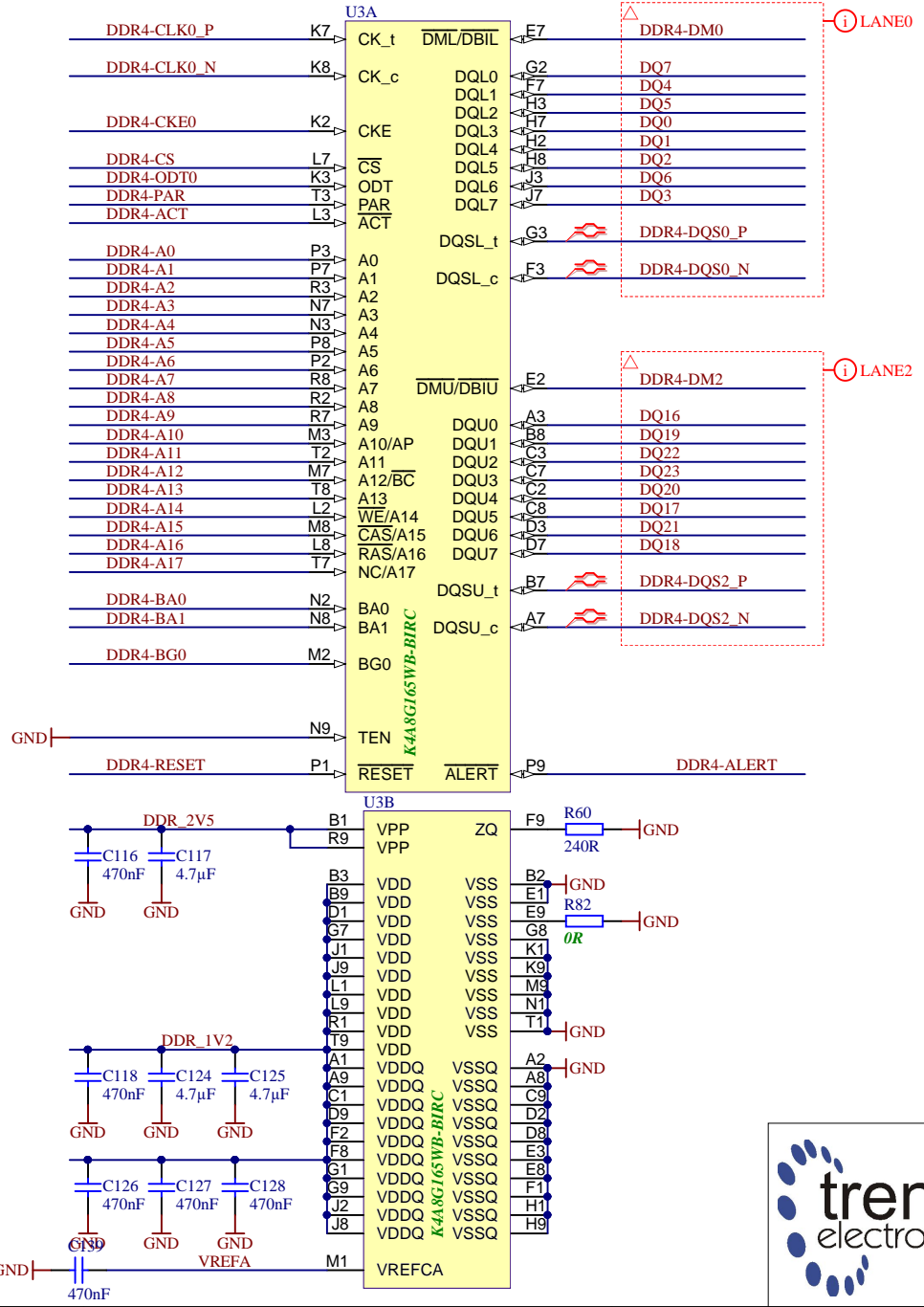




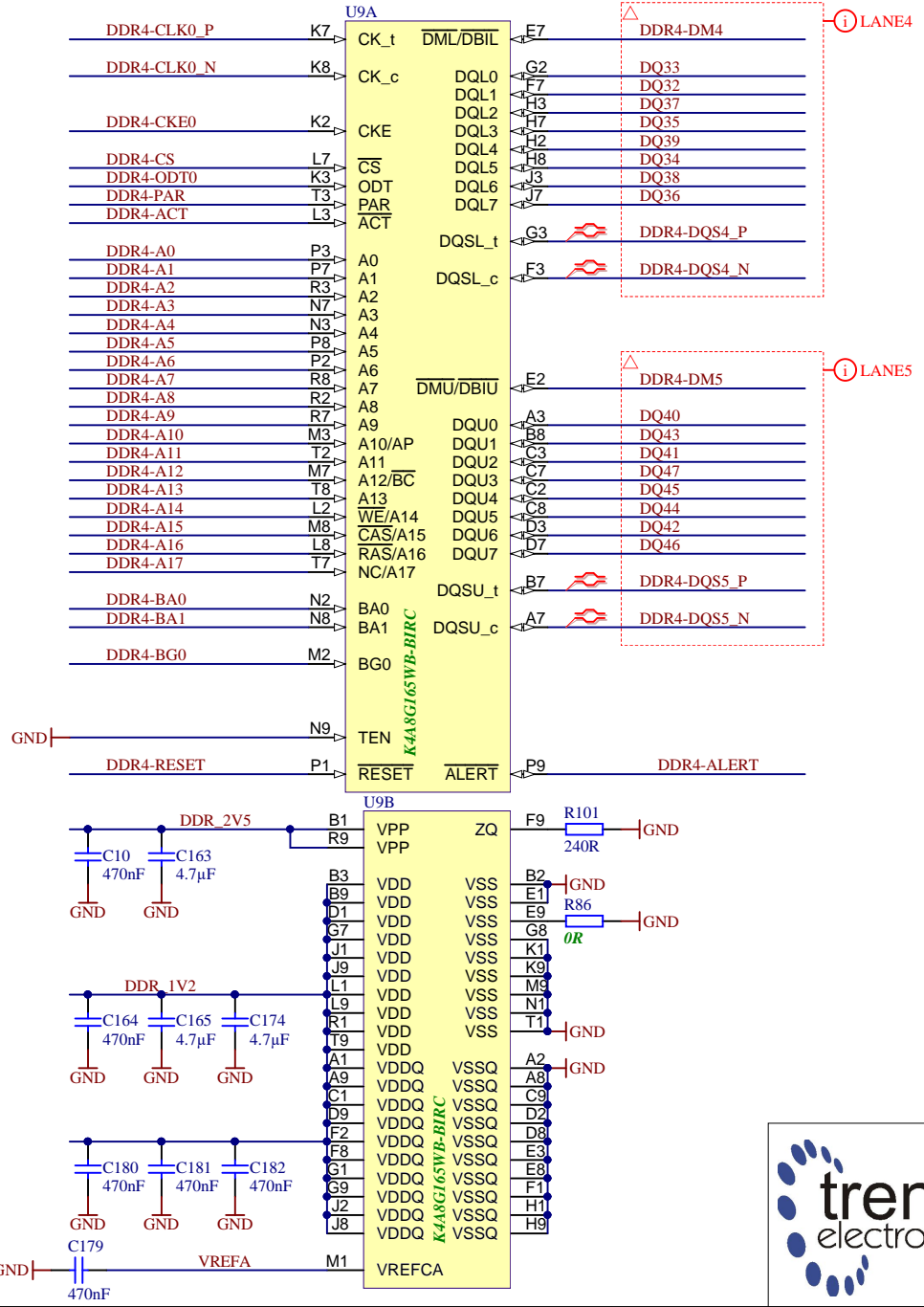
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Date: 2018-07-09	Copyright: Trenz Electronic GmbH / TT	Page 17 of 28
Filename: ZU_POWER.SchDoc		




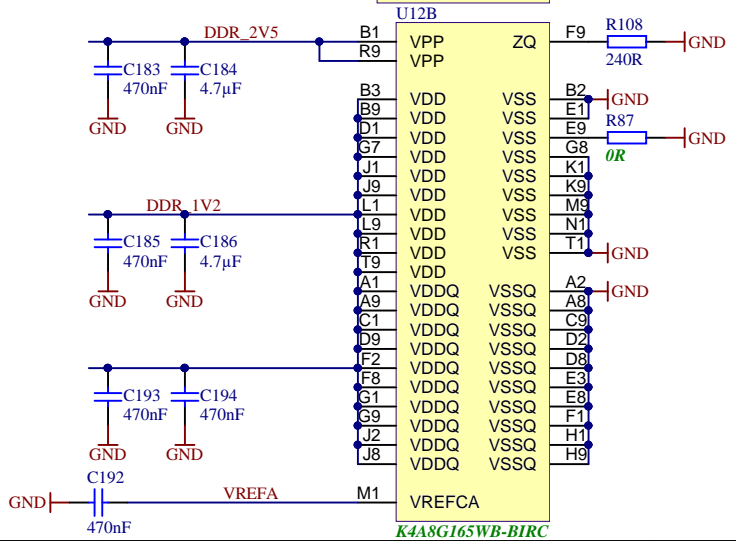
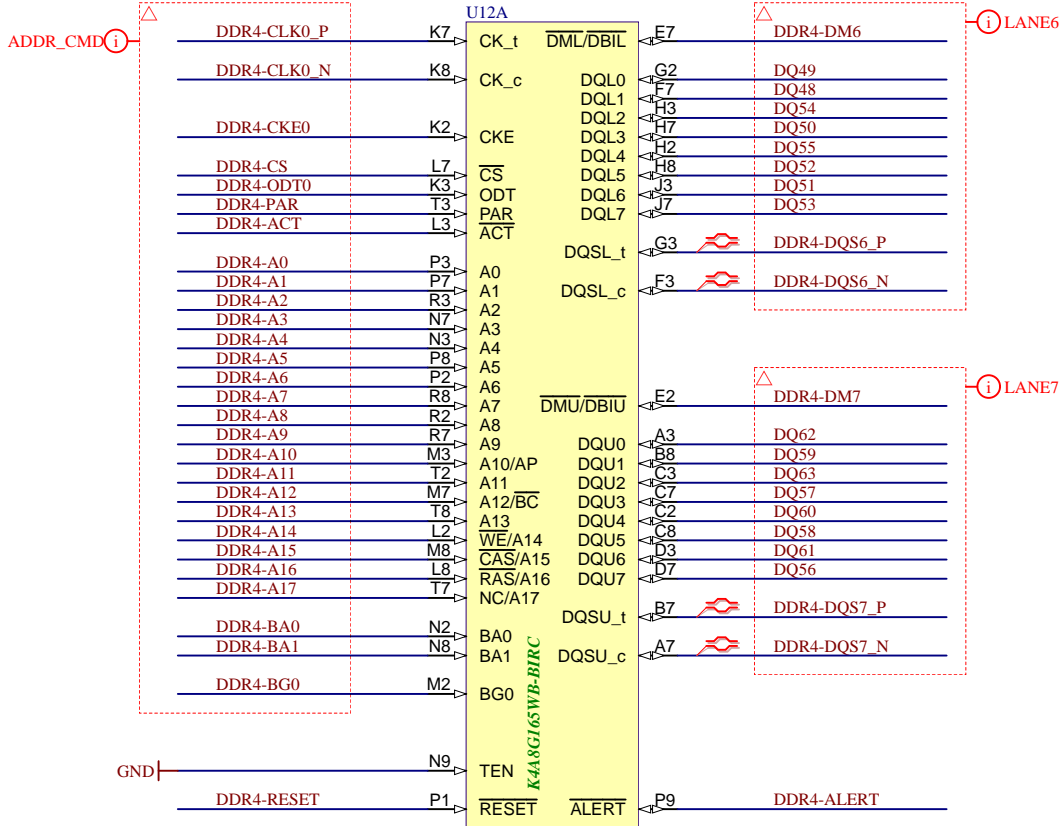
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Date: 2018-07-09	Copyright: Trenz Electronic GmbH / TT	Page 18 of 28
Filename: DDR4-RAM.SchDoc		



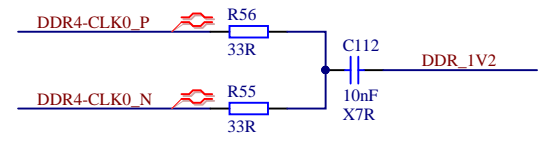
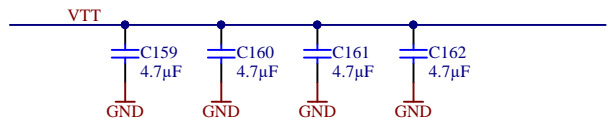
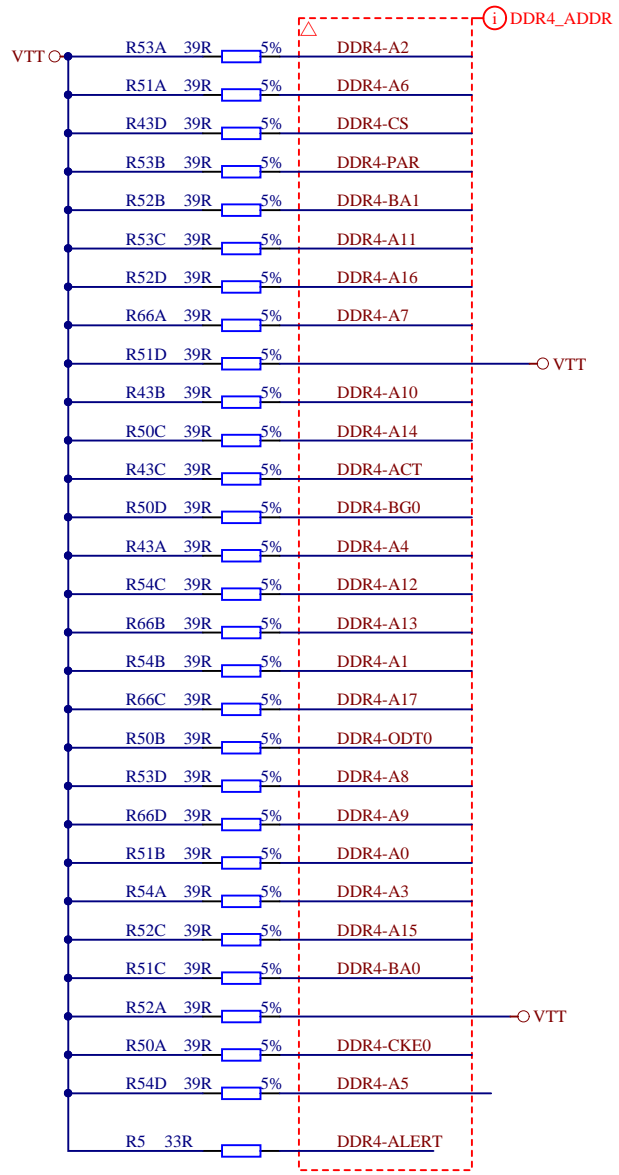
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Date: 2018-07-09	Copyright: Trenz Electronic GmbH / TT	Page 19 of 28
Filename: DDR4-RAM_2.SchDoc		



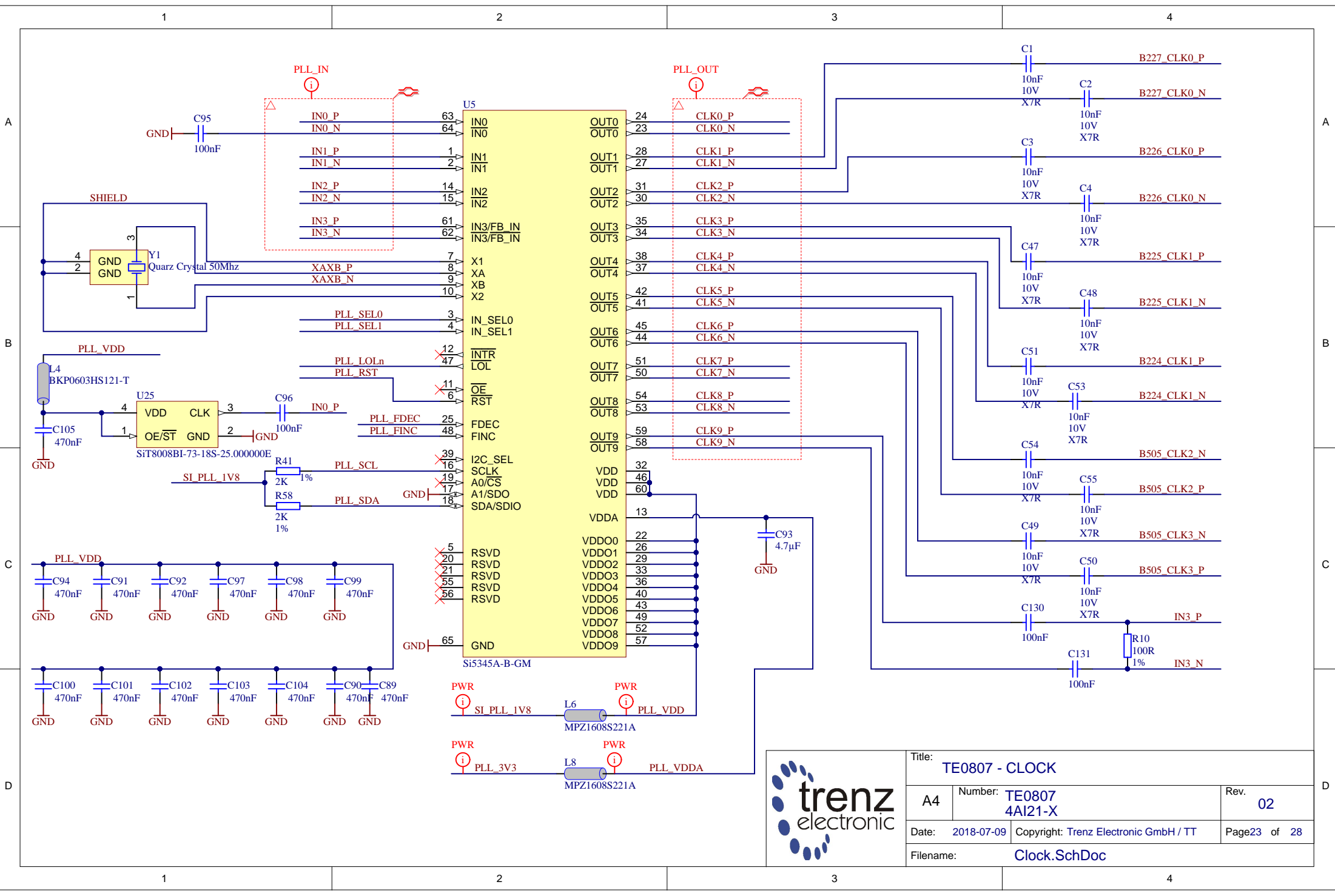
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Date: 2018-07-09		Copyright: Trenz Electronic GmbH / TT		Page20 of 28
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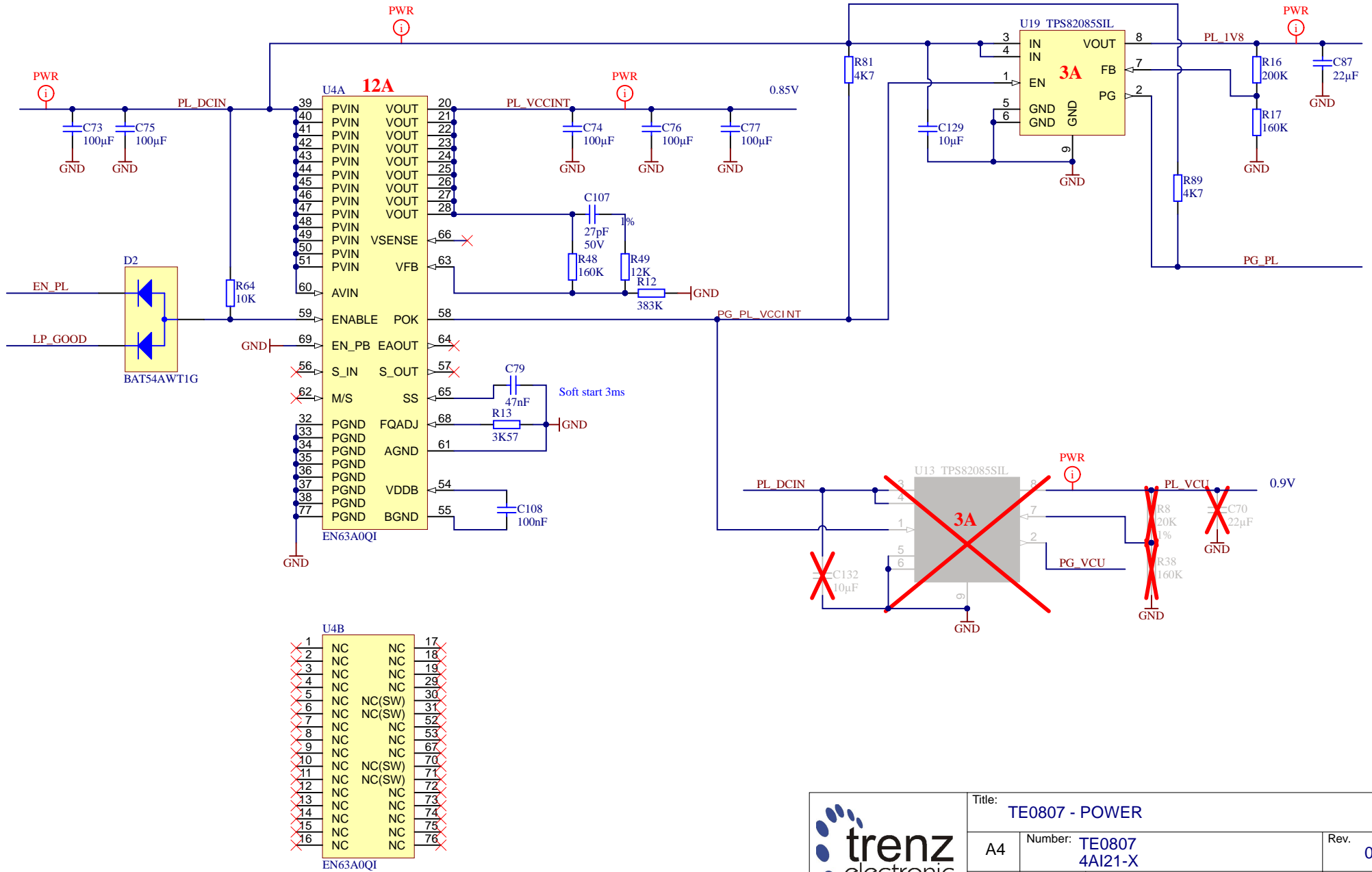
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Date: 2018-07-09	Copyright: Trenz Electronic GmbH / TT	Page 21 of 28
Filename: DDR4-RAM_4.SchDoc		




Title: TE0807 - DDR4_TERM		
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Date: 2018-07-09	Copyright: Trenz Electronic GmbH / TT	Page22 of 28
Filename: DDR4-TERM.SchDoc		

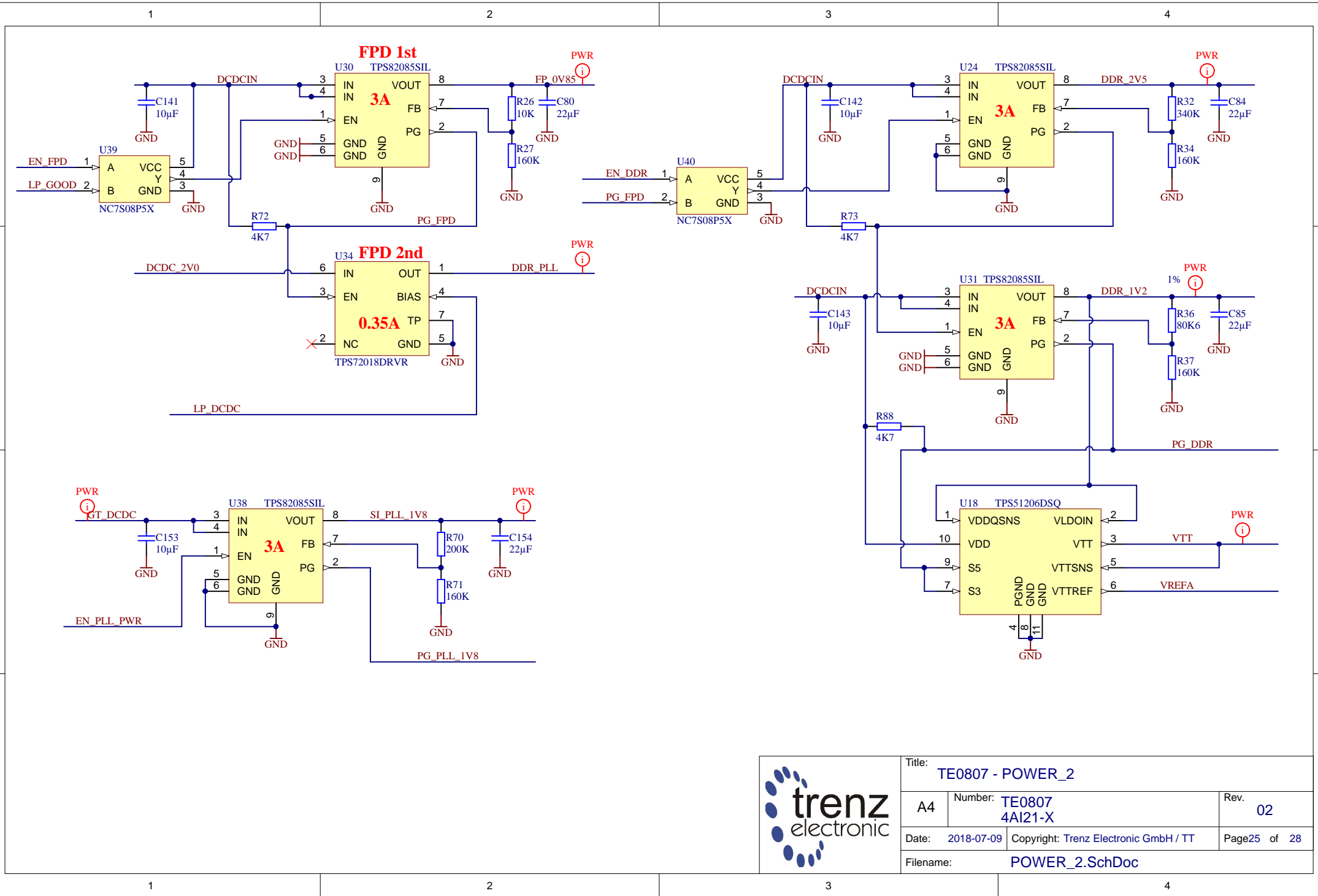



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Date: 2018-07-09	Copyright: Trenz Electronic GmbH / TT	Page 23 of 28
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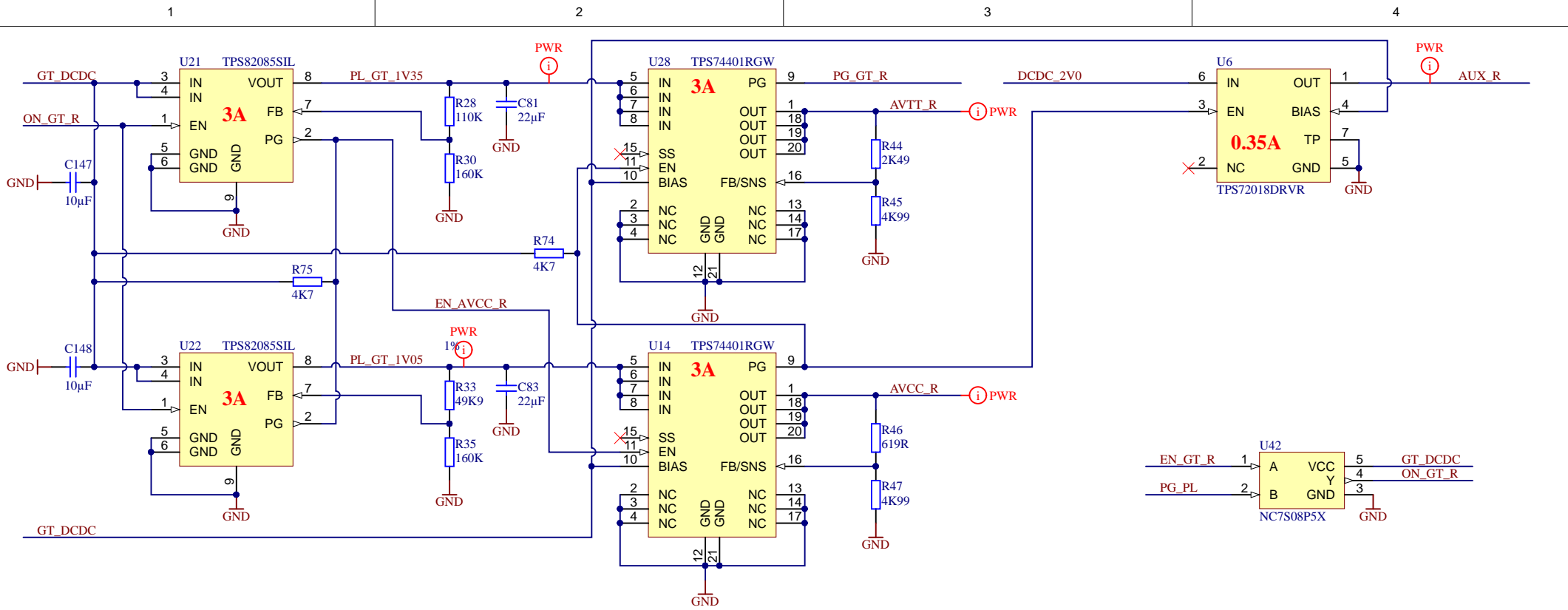


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	Date: <b>2018-07-09</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>24</b> of <b>28</b>
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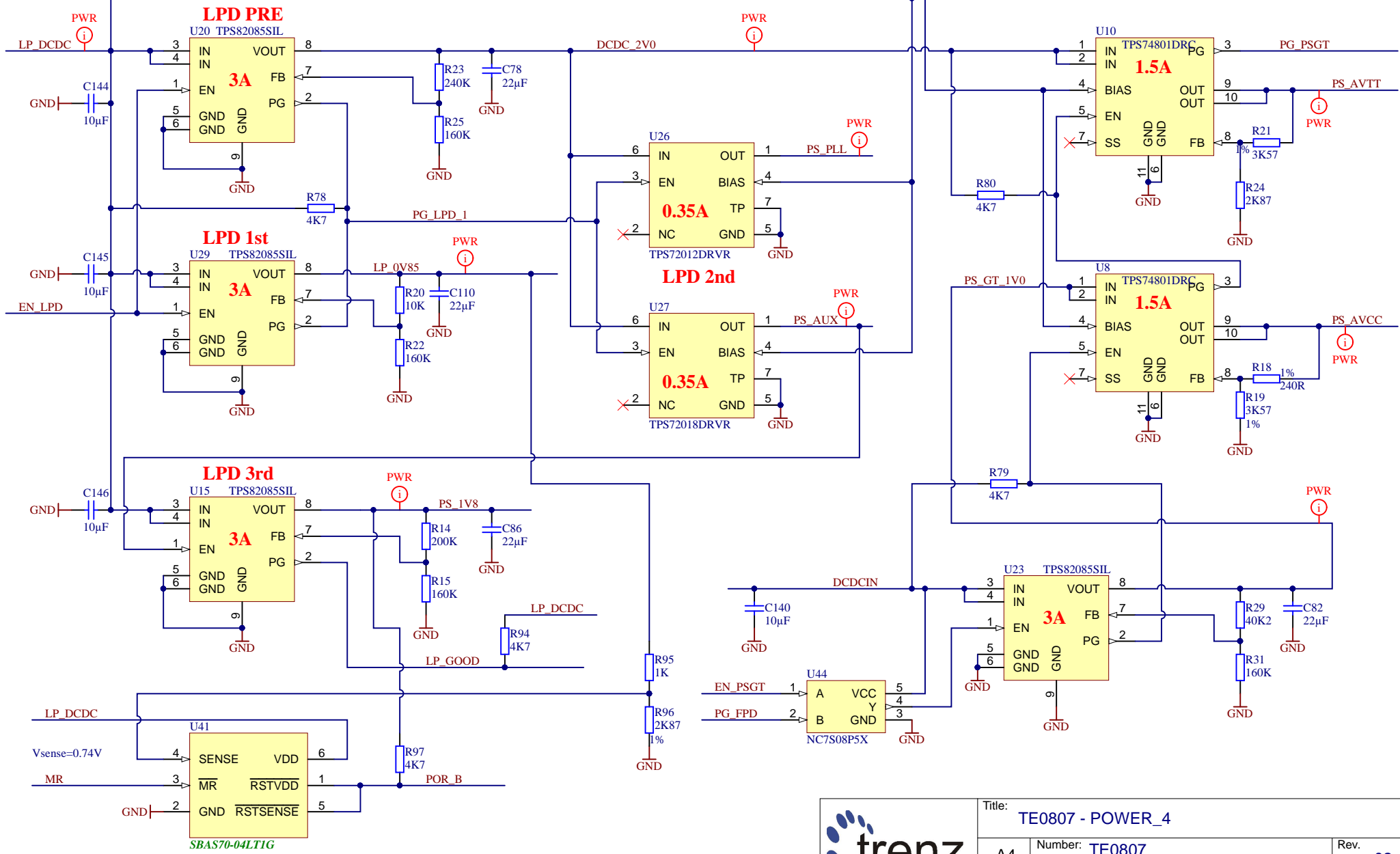




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Date: 2018-07-09		Copyright: Trenz Electronic GmbH / TT	
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Title: TE0807 - POWER_3		
A4	Number: TE0807 4AI21-X	Rev. 02
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Filename: POWER_3.SchDoc		



Title: TE0807 - POWER_4		
A4	Number: TE0807 4AI21-X	Rev. 02
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CHANGES REV01 to REV02

- 1) Added EEPROM (U11,24AA025E48T-I/OT)
- 2) Added optional resistors R39/R40 for QSPI flash (do not populated)
- 3) Fixed VCU connection (added additional DCDC and capacitors), recommendation from Xilinx
- 4) Changed obsolete DDR4 chips (NT5AD256M16B2-GN -> K4A8G165WB-BIRC)
- 5) Added net "PG\_VCU" to J2 (pin97)
- 6) full update lib

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Title: TE0807 - Changes list		
A4	Number: TE0807 4AI21-X	Rev. 02
Date: 2018-07-09	Copyright: Trenz Electronic GmbH	Page 28 of 28
Filename: Revision_Changes.SchDoc		

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