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Schematics and other handouts serve for informational purposes only!

	Title: <b>TE0807 - Legal Notices</b>		
	A4	Number: <b>TE0807 7AI21-A</b>	Rev. <b>03</b>
	Date: <b>2020-05-08</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>1</b> of <b>29</b>
	Filename: <b>Legal Notices Modules.SchDoc</b>		

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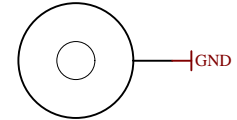
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U\_J1  
J1.SchDoc  
U\_J2  
J2.SchDoc  
U\_J3  
J3.SchDoc  
U\_J4  
J4.SchDoc  
U\_DDR4-TERM  
DDR4-TERM.SchDoc  
U\_B64  
B64.SchDoc  
U\_B65  
B65.SchDoc  
U\_B66  
B66.SchDoc  
U\_B\_GT  
B\_GT.SchDoc  
U\_B\_GT\_2  
B\_GT\_2.SchDoc

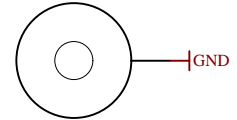
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U\_PS\_DDR  
PS\_DDR.SchDoc  
U\_B\_MIO  
B\_MIO.SchDoc  
U\_B\_HD  
B\_HD.SchDoc  
U\_Clock  
Clock.SchDoc  
U\_CONFIG  
CONFIG.SchDoc  
U\_DDR4-RAM  
DDR4-RAM.SchDoc  
U\_DDR4-RAM\_2  
DDR4-RAM\_2.SchDoc  
U\_DDR4-RAM\_3  
DDR4-RAM\_3.SchDoc  
U\_DDR4-RAM\_4  
DDR4-RAM\_4.SchDoc

U\_DDR4-TERM  
DDR4-TERM.SchDoc  
U\_ZU\_POWER  
ZU\_POWER.SchDoc  
U\_ZU\_PS\_POWER  
ZU\_PS\_POWER.SchDoc  
U\_POWER  
POWER.SchDoc  
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U\_POWER\_4  
POWER\_4.SchDoc

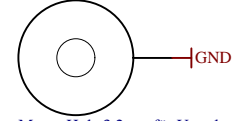
Special notes:



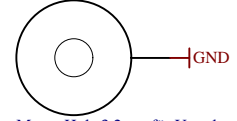
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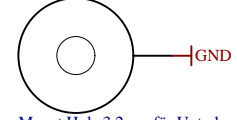
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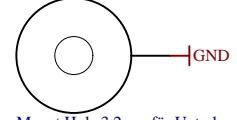
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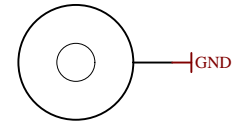
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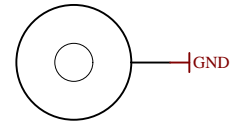
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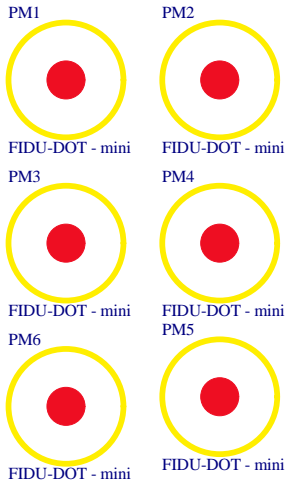
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



LOGO1  
TE Logo PRINT Layer  
LOGO PRINT

Serial  
Serialnummer 6,3 x 6,3mm

Assembly variant	7AI21-A
Created by	VT
Modified by	VT
Modified at	2020-03-23
SVN Revision	9271 [Locally Modified]



Title: TE0807		
A4	Number: TE0807 7AI21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 2 of 29
Filename: TE0807.SchDoc		

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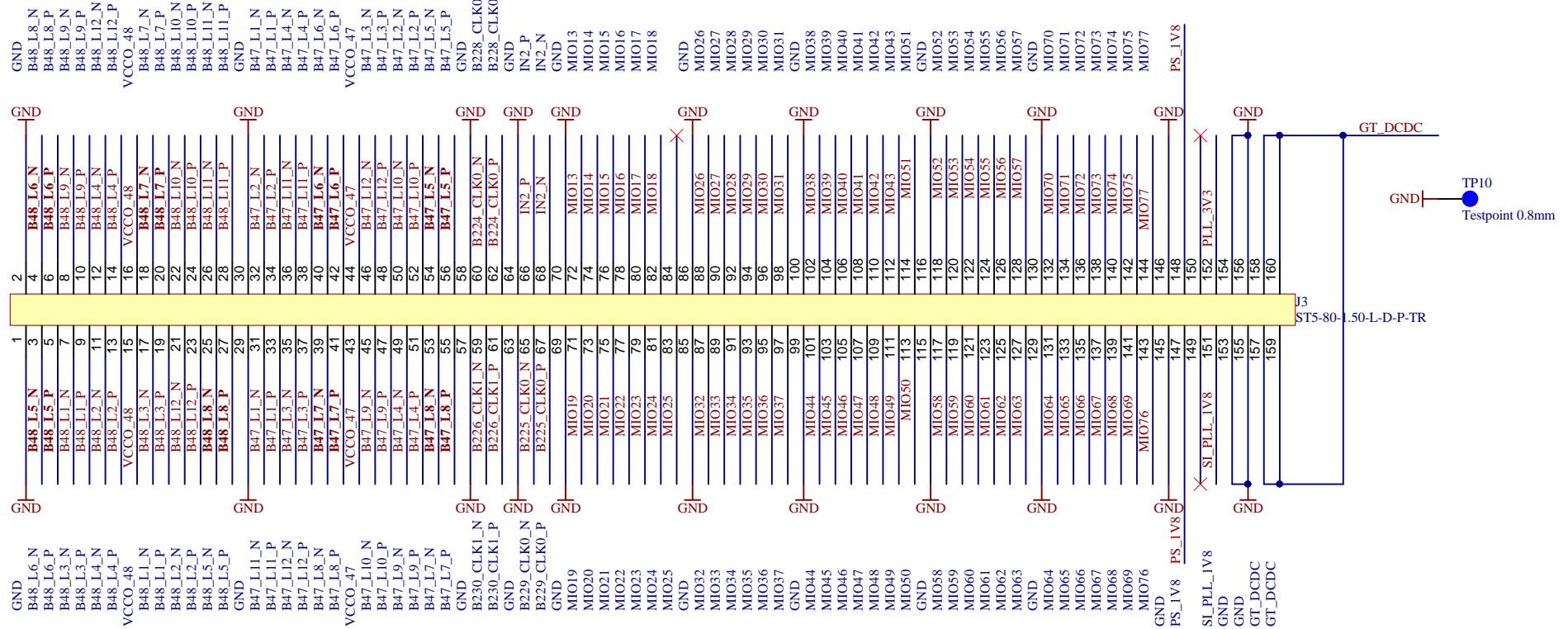
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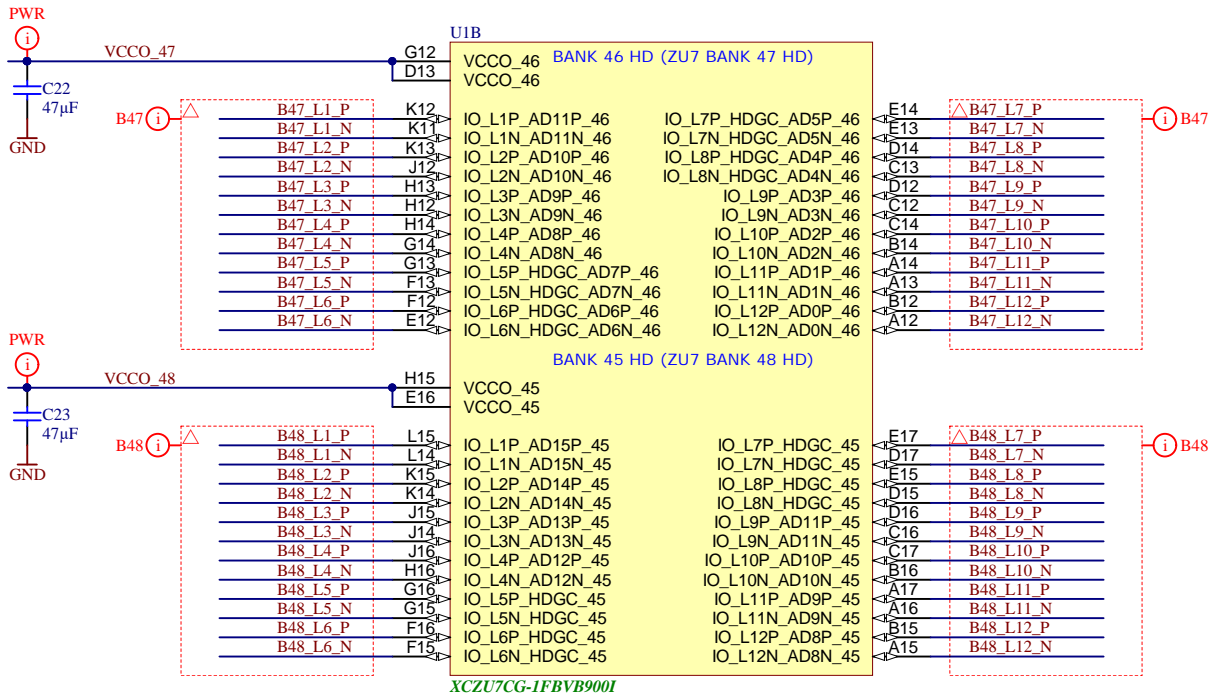
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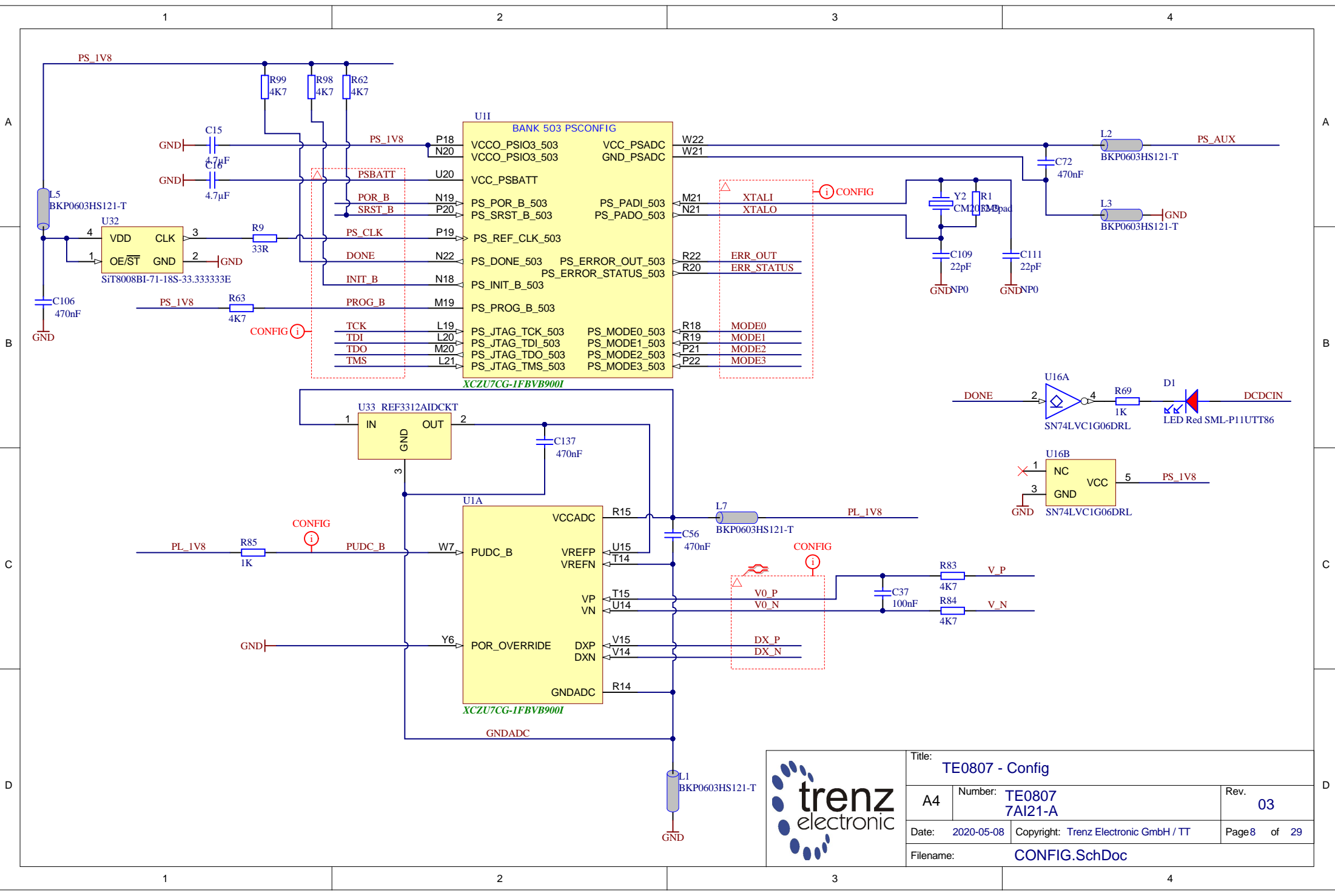



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Filename: J3.SchDoc		

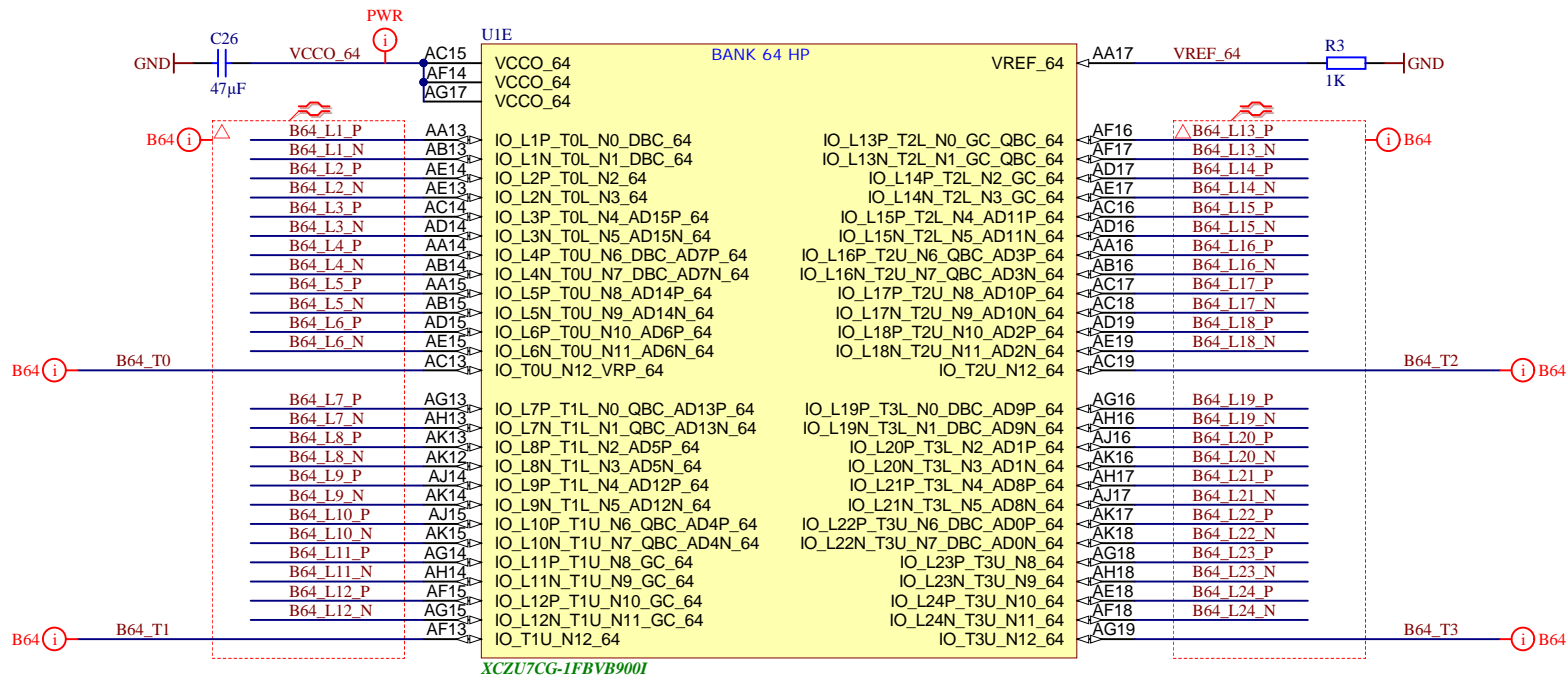




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Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 7 of 29
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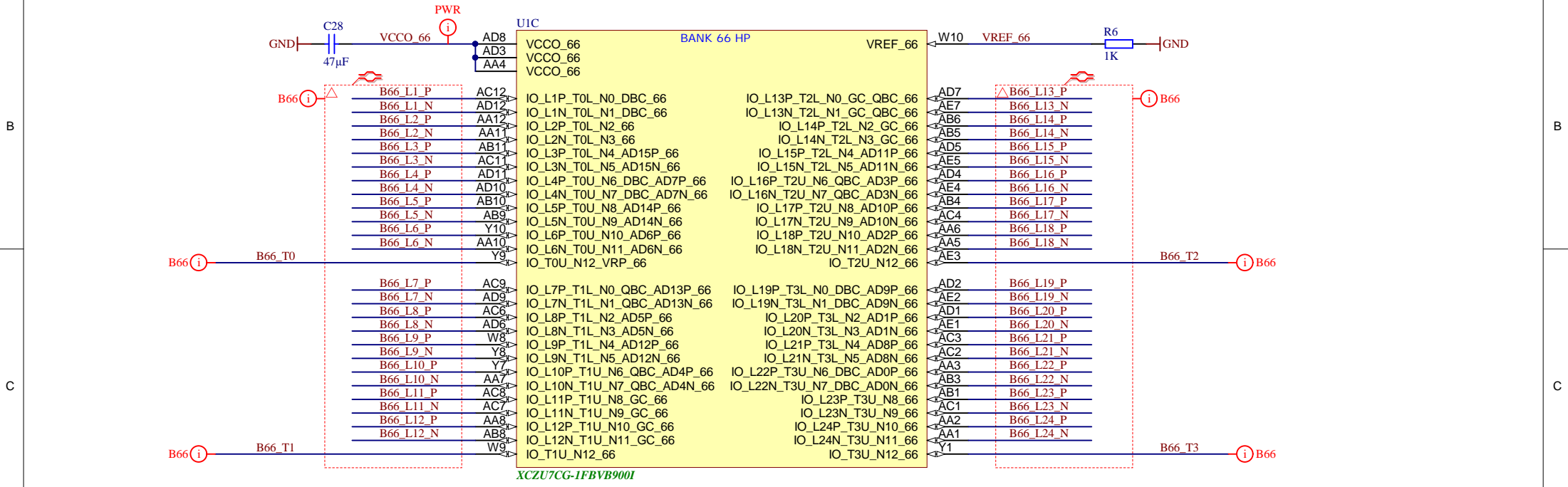


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			A4	Number: TE0807 7AI21-A
Date: 2020-05-08		Copyright: Trenz Electronic GmbH / TT		Page 8 of 29
Filename: CONFIG.SchDoc				



Title: <b>TE0807 - B64</b>		
A4	Number: <b>TE0807 7AI21-A</b>	Rev. <b>03</b>
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Filename: <b>B64.SchDoc</b>		





Title: <b>TE0807 - B66</b>		
A4	Number: <b>TE0807 7AI21-A</b>	Rev. <b>03</b>
Date: <b>2020-05-08</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>11</b> of <b>29</b>
Filename: <b>B66.SchDoc</b>		

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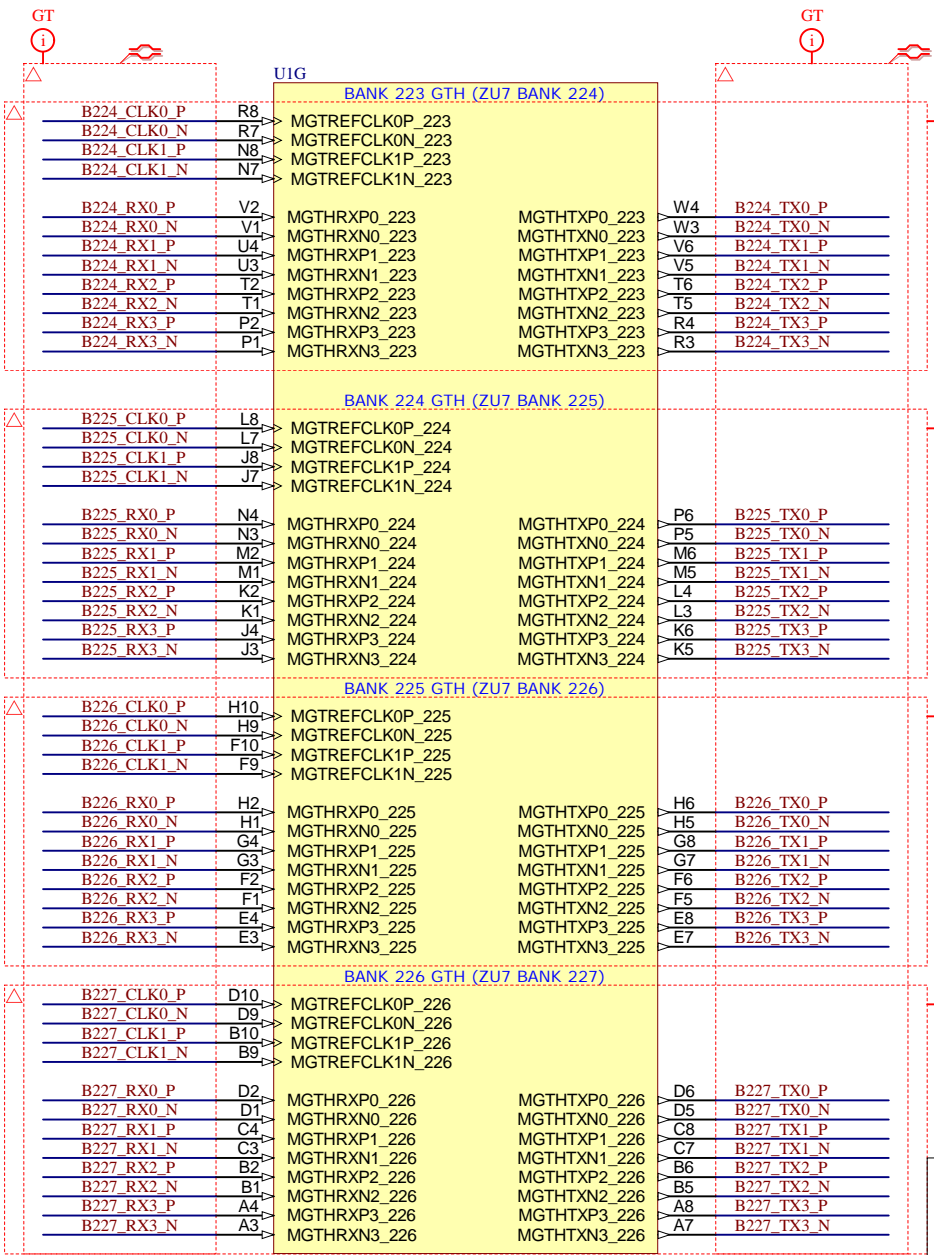
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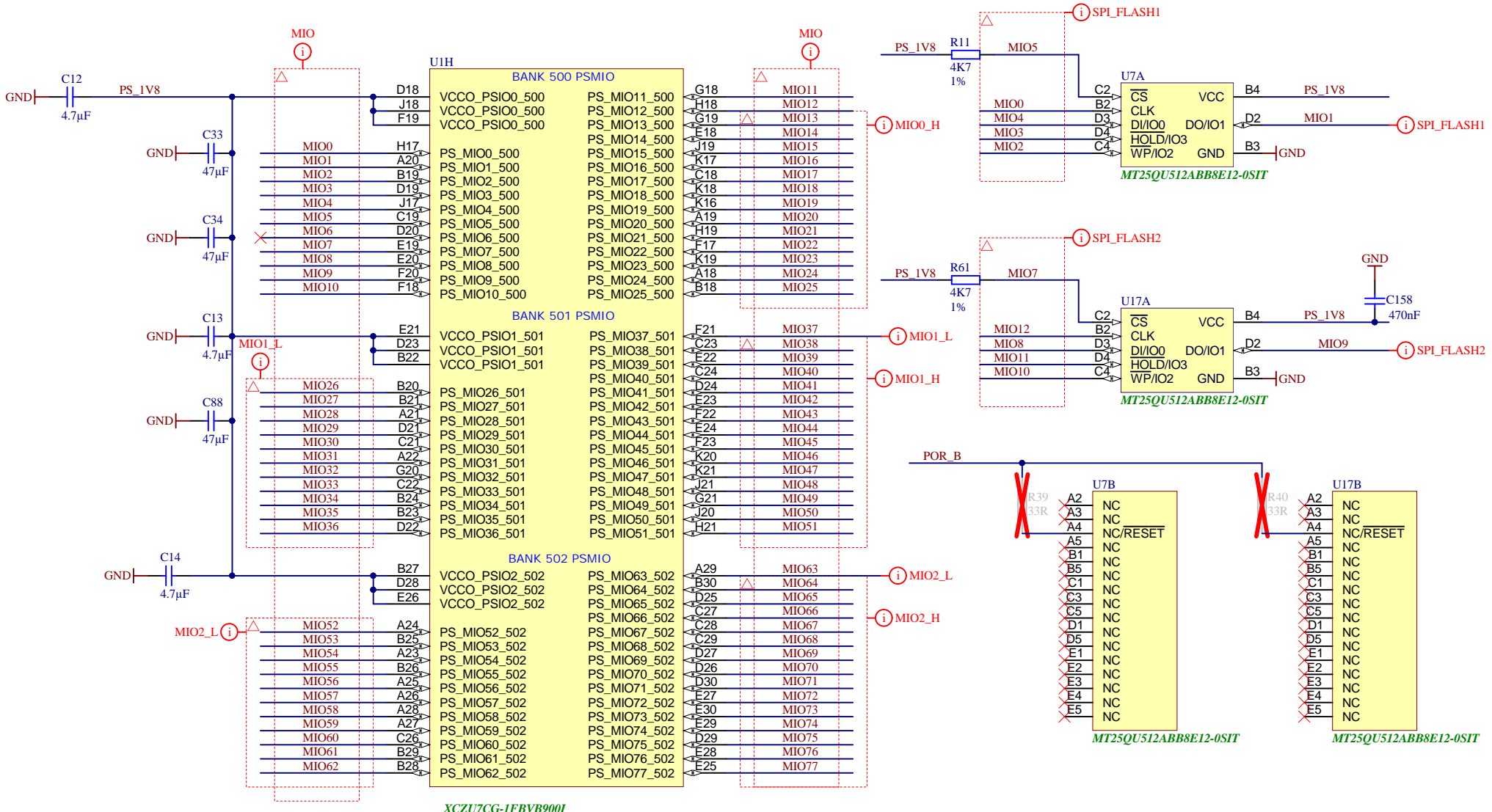
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Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 12 of 29
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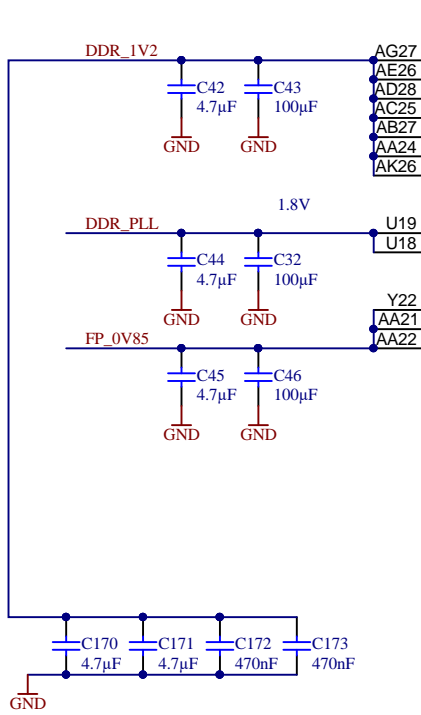






XCZU7CG-1FBVB900I

		Title: TE0807 - MIO Banks	
		A4	Number: TE0807 7AI21-A
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Filename: B_MIO.SchDoc			



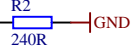
**UIJ**

**BANK 504 PSDDR**

VCCO_PSDDR_504	PS_DDR_CK0_504
VCCO_PSDDR_504	PS_DDR_CK_N0_504
VCCO_PSDDR_504	PS_DDR_CKE0_504
VCCO_PSDDR_504	PS_DDR_CK1_504
VCCO_PSDDR_504	PS_DDR_CK_N1_504
VCCO_PSDDR_504	PS_DDR_CKE1_504
VCC_PSDDR_PLL	PS_DDR_A0_504
VCC_PSDDR_PLL	PS_DDR_A1_504
VCC_PSDDR_PLL	PS_DDR_A2_504
VCC_PSDDR_PLL	PS_DDR_A3_504
VCC_PSDDR_PLL	PS_DDR_A4_504
VCC_PSDDR_PLL	PS_DDR_A5_504
VCC_PSDDR_PLL	PS_DDR_A6_504
VCC_PSDDR_PLL	PS_DDR_A7_504
VCC_PSDDR_PLL	PS_DDR_A8_504
VCC_PSDDR_PLL	PS_DDR_A9_504
VCC_PSDDR_PLL	PS_DDR_A10_504
VCC_PSDDR_PLL	PS_DDR_A11_504
VCC_PSDDR_PLL	PS_DDR_A12_504
VCC_PSDDR_PLL	PS_DDR_A13_504
VCC_PSDDR_PLL	PS_DDR_A14_504
VCC_PSDDR_PLL	PS_DDR_A15_504
VCC_PSDDR_PLL	PS_DDR_A16_504
VCC_PSDDR_PLL	PS_DDR_A17_504
PS_DDR_CS_N0_504	PS_DDR_CS_N1_504
PS_DDR_BA0_504	PS_DDR_BA1_504
PS_DDR_BG0_504	PS_DDR_BG1_504
PS_DDR_PARITY_504	PS_DDR_RAM_RST_N_504
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504
PS_DDR_ZQ_504	PS_DDR_ODT0_504
PS_DDR_ODT1_504	

*XCZU7CG-1FBVB900I*

AE30	DDR4-CLK0_P
AF30	DDR4-CLK0_N
AC30	DDR4-CKE0
AF28	
AG28	
AB28	
AH30	DDR4-A0
AG30	DDR4-A1
AK29	DDR4-A2
AJ30	DDR4-A3
AK28	DDR4-A4
AK27	DDR4-A5
AF27	DDR4-A6
AE27	DDR4-A7
AF26	DDR4-A8
AG26	DDR4-A9
AE29	DDR4-A10
AE28	DDR4-A11
AH29	DDR4-A12
AG29	DDR4-A14
AJ29	DDR4-A15
AH27	DDR4-A16
AJ27	DDR4-A17
AD30	DDR4-CS
AD29	
AD27	DDR4-BA0
AC26	DDR4-BA1
AC28	DDR4-BG0
AC27	DDR4-BG1
AB26	DDR4-PAR
AB25	DDR4-RESET
AD26	DDR4-ACT
AB24	DDR4-ALERT
AB23	
AB30	DDR4-ODT0
AC29	



**UIK**

**BANK 504 PSDDR**

DQ0	AH22	PS_DDR_DQ0_504	PS_DDR_DQ32_504
DQ1	AH21	PS_DDR_DQ1_504	PS_DDR_DQ33_504
DQ2	AJ22	PS_DDR_DQ2_504	PS_DDR_DQ34_504
DQ3	AK22	PS_DDR_DQ3_504	PS_DDR_DQ35_504
DQ4	AK20	PS_DDR_DQ4_504	PS_DDR_DQ36_504
DQ5	AJ19	PS_DDR_DQ5_504	PS_DDR_DQ37_504
DQ6	AK19	PS_DDR_DQ6_504	PS_DDR_DQ38_504
DQ7	AH19	PS_DDR_DQ7_504	PS_DDR_DQ39_504
DQ8	AH23	PS_DDR_DQ8_504	PS_DDR_DQ40_504
DQ9	AK23	PS_DDR_DQ9_504	PS_DDR_DQ41_504
DQ10	AG24	PS_DDR_DQ10_504	PS_DDR_DQ42_504
DQ11	AK24	PS_DDR_DQ11_504	PS_DDR_DQ43_504
DQ12	AJ26	PS_DDR_DQ12_504	PS_DDR_DQ44_504
DQ13	AK25	PS_DDR_DQ13_504	PS_DDR_DQ45_504
DQ14	AG25	PS_DDR_DQ14_504	PS_DDR_DQ46_504
DQ15	AH26	PS_DDR_DQ15_504	PS_DDR_DQ47_504
DQ16	AD22	PS_DDR_DQ16_504	PS_DDR_DQ48_504
DQ17	AE22	PS_DDR_DQ17_504	PS_DDR_DQ49_504
DQ18	AF22	PS_DDR_DQ18_504	PS_DDR_DQ50_504
DQ19	AG21	PS_DDR_DQ19_504	PS_DDR_DQ51_504
DQ20	AD20	PS_DDR_DQ20_504	PS_DDR_DQ52_504
DQ21	AF20	PS_DDR_DQ21_504	PS_DDR_DQ53_504
DQ22	AE20	PS_DDR_DQ22_504	PS_DDR_DQ54_504
DQ23	AG20	PS_DDR_DQ23_504	PS_DDR_DQ55_504
DQ24	AG23	PS_DDR_DQ24_504	PS_DDR_DQ56_504
DQ25	AF23	PS_DDR_DQ25_504	PS_DDR_DQ57_504
DQ26	AF25	PS_DDR_DQ26_504	PS_DDR_DQ58_504
DQ27	AE23	PS_DDR_DQ27_504	PS_DDR_DQ59_504
DQ28	AC22	PS_DDR_DQ28_504	PS_DDR_DQ60_504
DQ29	AC23	PS_DDR_DQ29_504	PS_DDR_DQ61_504
DQ30	AD25	PS_DDR_DQ30_504	PS_DDR_DQ62_504
DQ31	AC24	PS_DDR_DQ31_504	PS_DDR_DQ63_504
DDR4-DQS0_P	AJ21	PS_DDR_DQS_P0_504	PS_DDR_DQ64_504
DDR4-DQS0_N	AK21	PS_DDR_DQS_N0_504	PS_DDR_DQ65_504
DDR4-DQS1_P	AH24	PS_DDR_DQS_P1_504	PS_DDR_DQ66_504
DDR4-DQS1_N	AJ24	PS_DDR_DQS_N1_504	PS_DDR_DQ67_504
DDR4-DQS2_P	AC21	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504
DDR4-DQS2_N	AD21	PS_DDR_DQS_N2_504	PS_DDR_DQ69_504
DDR4-DQS3_P	AD24	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504
DDR4-DQS3_N	AE24	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504
DDR4-DQS4_P	W24	PS_DDR_DQS_P4_504	PS_DDR_DM0_504
DDR4-DQS4_N	W25	PS_DDR_DQS_N4_504	PS_DDR_DM1_504
DDR4-DQS5_P	P25	PS_DDR_DQS_P5_504	PS_DDR_DM2_504
DDR4-DQS5_N	R25	PS_DDR_DQS_N5_504	PS_DDR_DM3_504
DDR4-DQS6_P	U29	PS_DDR_DQS_P6_504	PS_DDR_DM4_504
DDR4-DQS6_N	V29	PS_DDR_DQS_N6_504	PS_DDR_DM5_504
DDR4-DQS7_P	R28	PS_DDR_DQS_P7_504	PS_DDR_DM6_504
DDR4-DQS7_N	R29	PS_DDR_DQS_N7_504	PS_DDR_DM7_504
	Y28	PS_DDR_DQS_P8_504	PS_DDR_DM8_504
	AA28	PS_DDR_DQS_N8_504	

*XCZU7CG-1FBVB900I*



Title: <b>TE0807 - PS_DDR</b>		
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Date: <b>2020-05-08</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>15</b> of <b>29</b>
Filename: <b>PS_DDR.SchDoc</b>		

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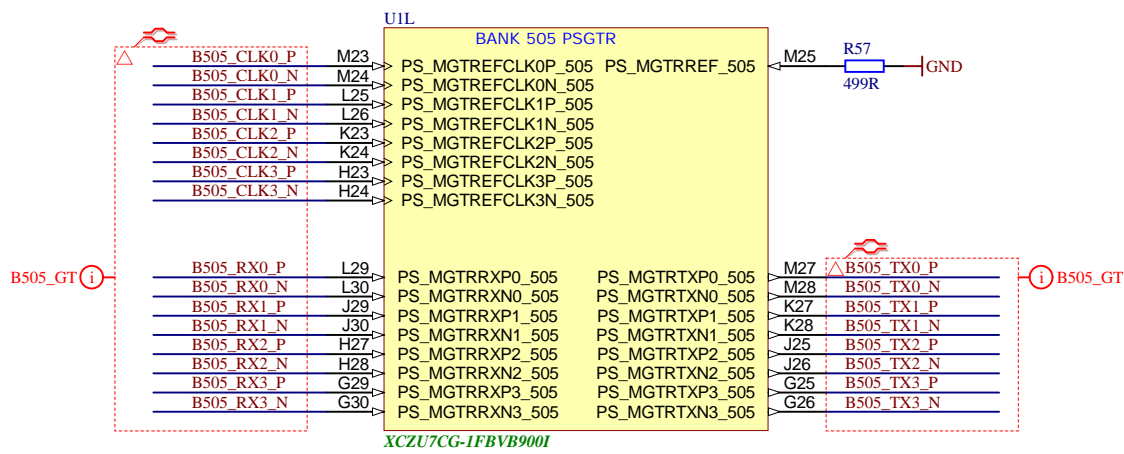
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Title: TE0807 - PS_GT		
A4	Number: TE0807 7AI21-A	Rev. 03
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Filename: B_PS_GT.SchDoc		

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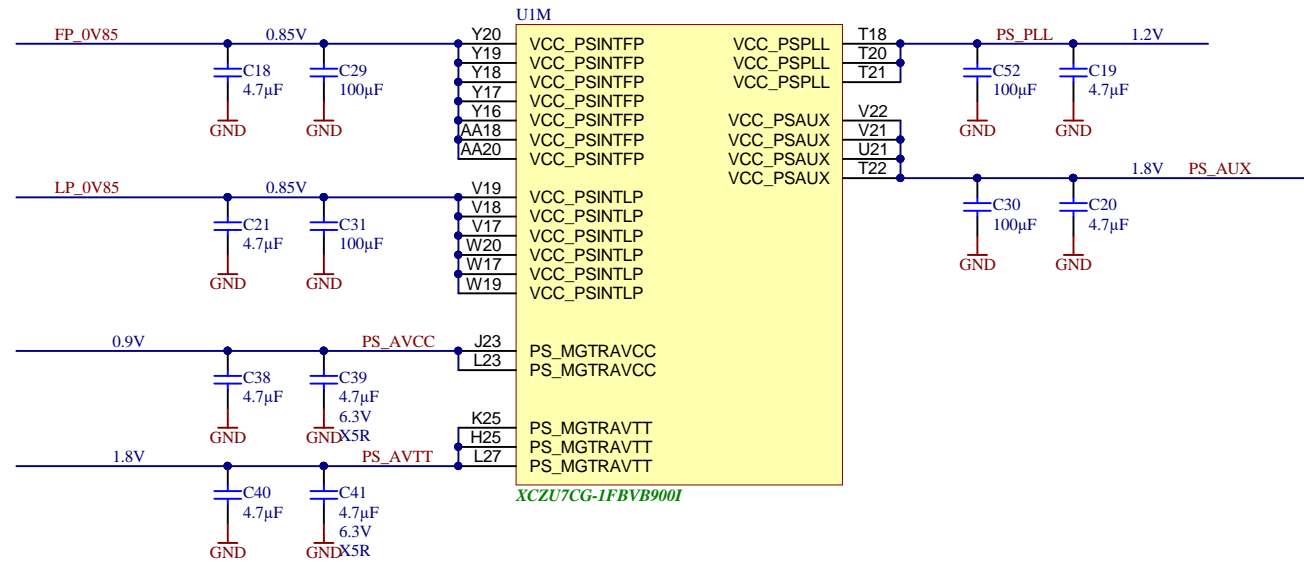
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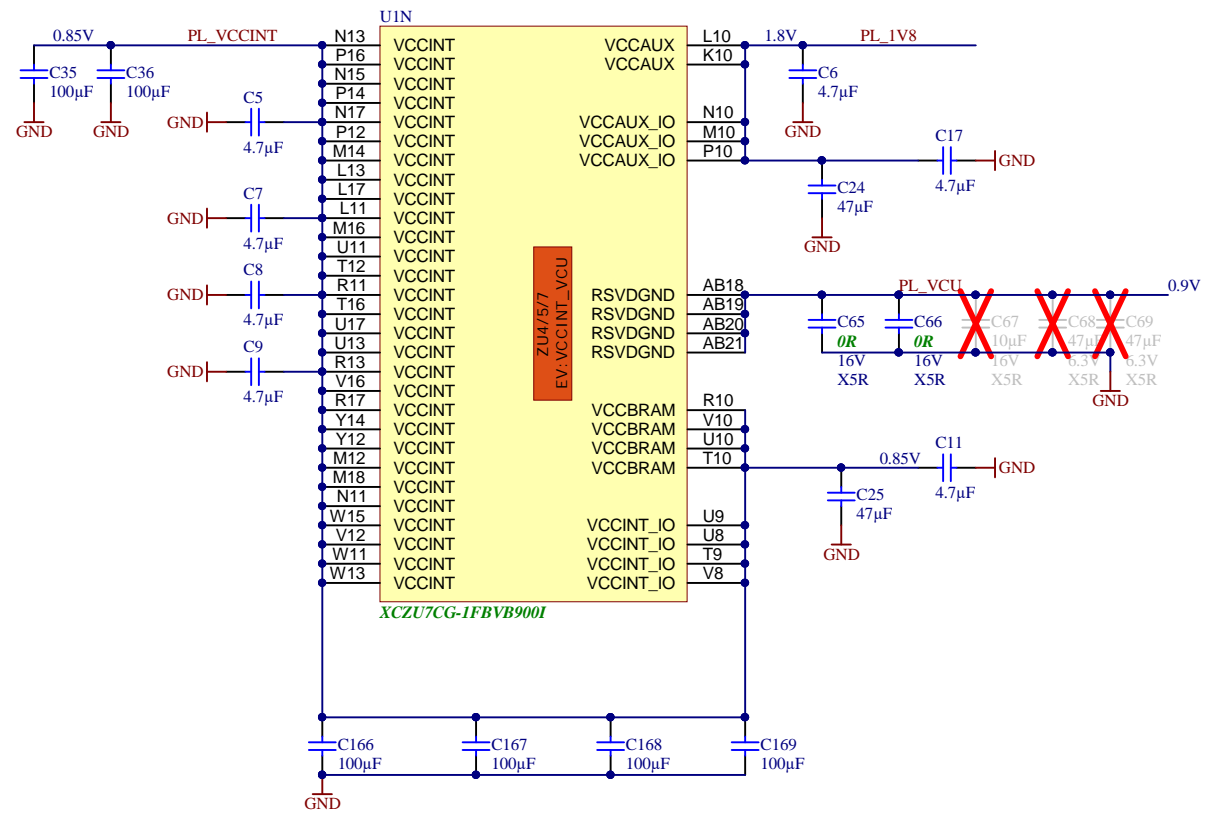
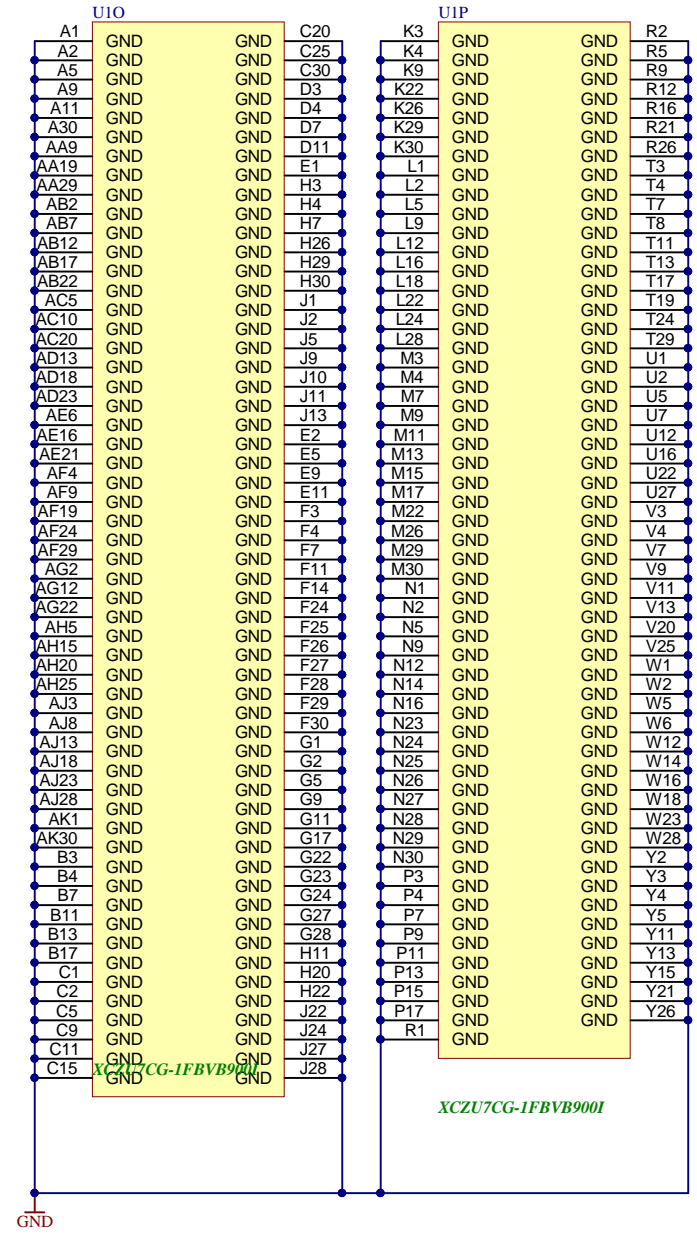

Title: TE0807 - ZU_PS_POWER		
A4	Number: TE0807 7AI21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 17 of 29
Filename: ZU_PS_POWER.SchDoc		

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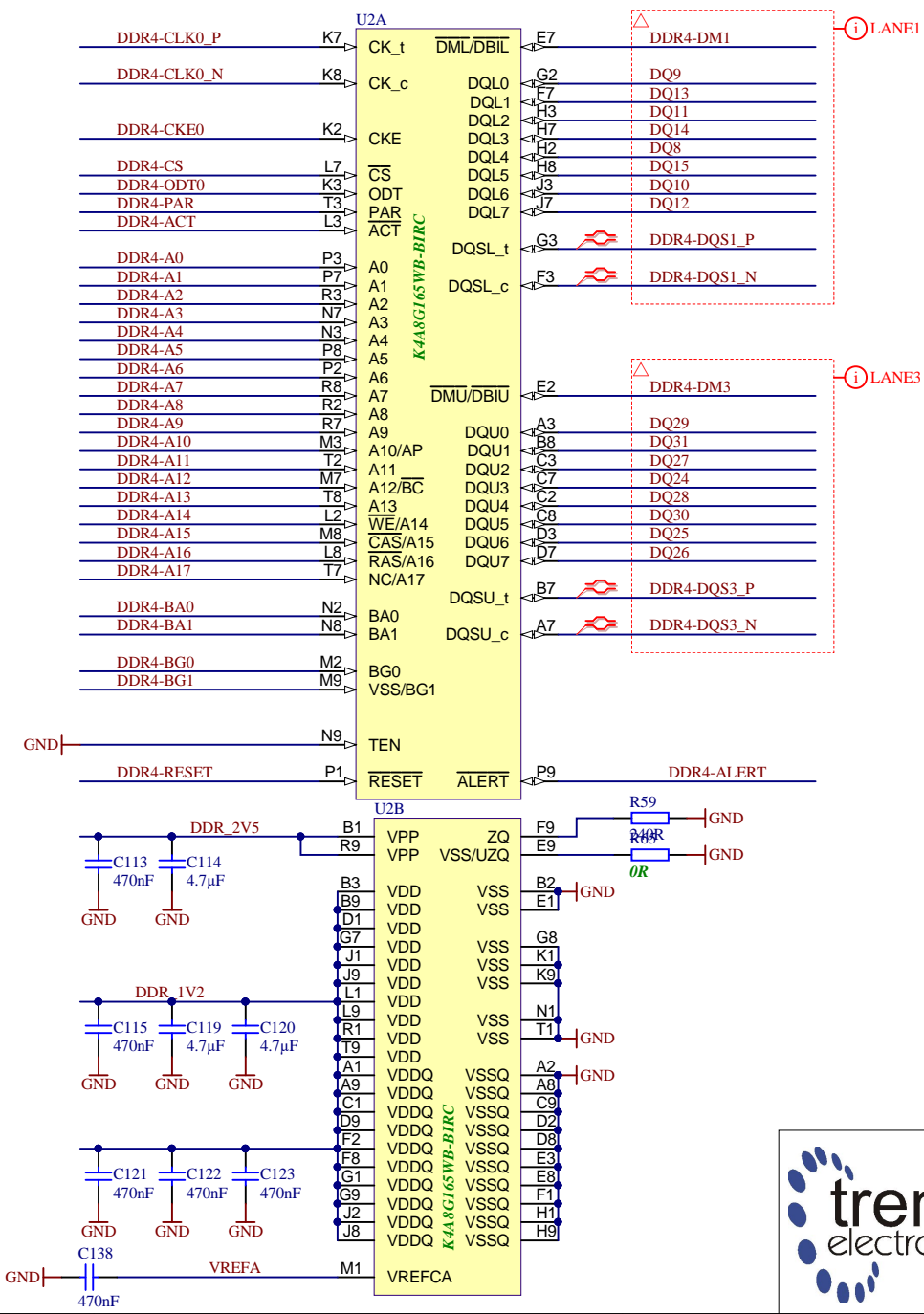
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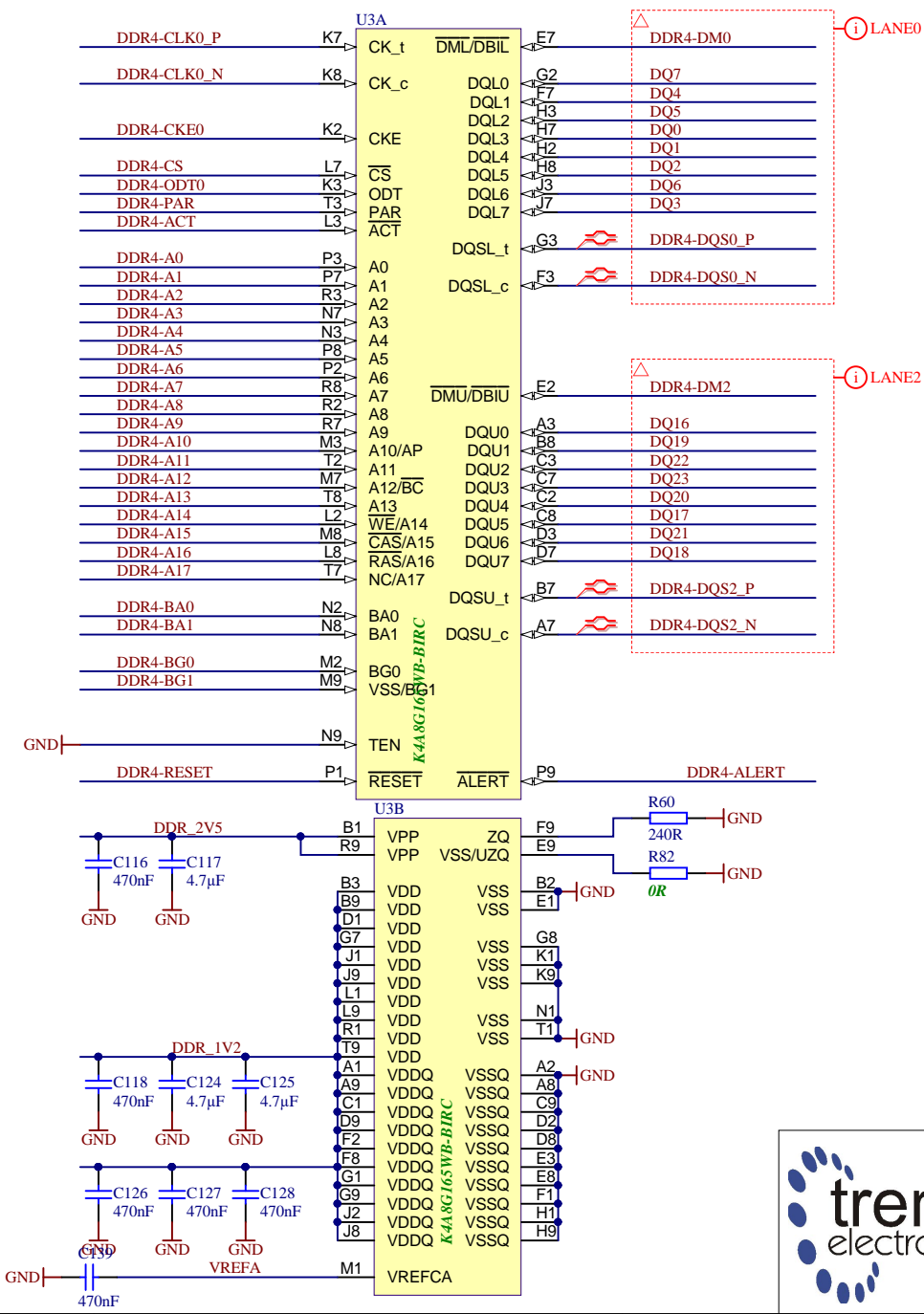

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Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 18 of 29
Filename: ZU_POWER.SchDoc		

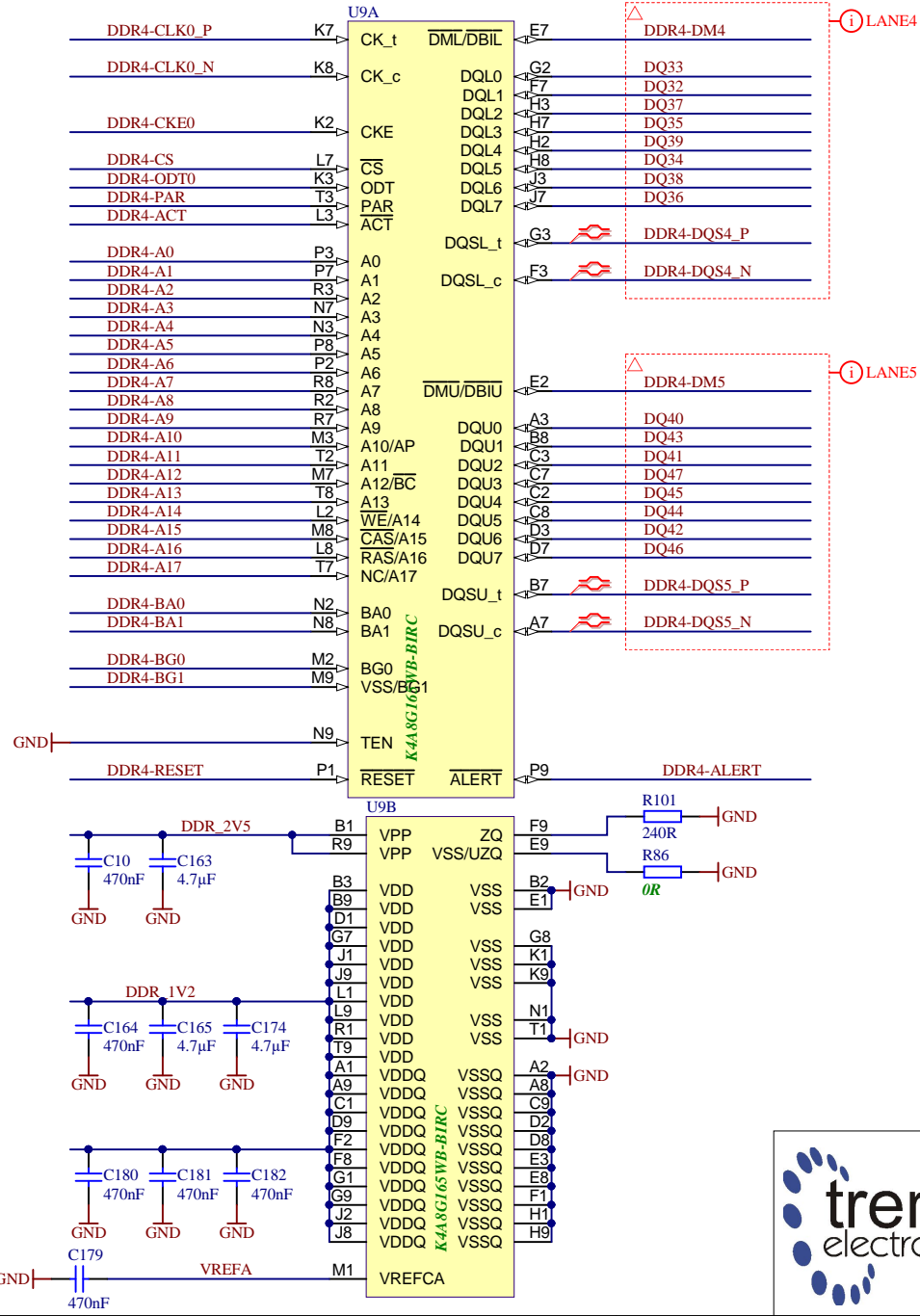


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Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 19 of 29
Filename: DDR4-RAM.SchDoc		

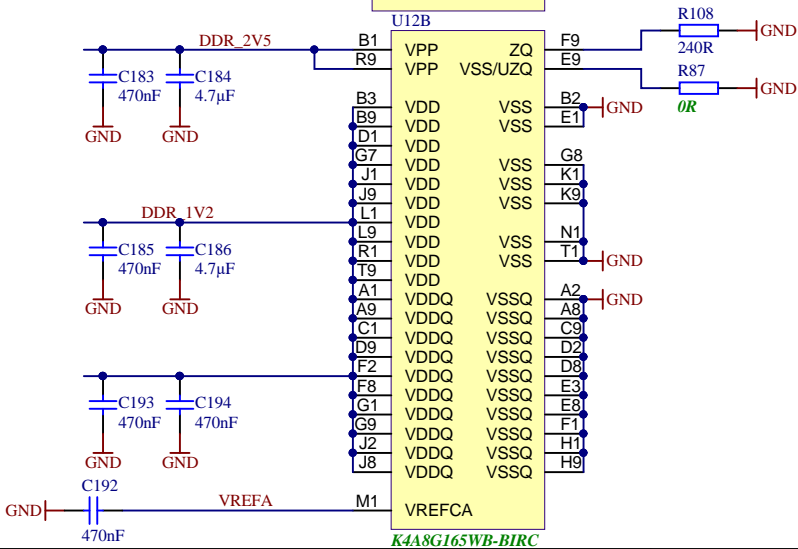
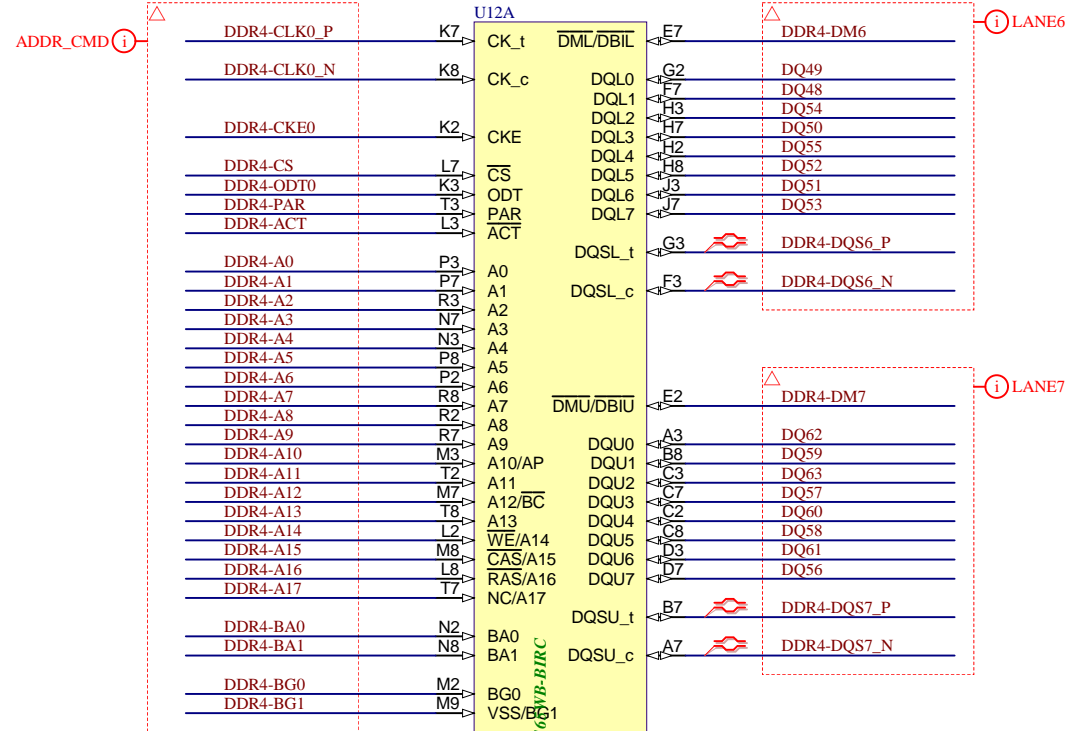



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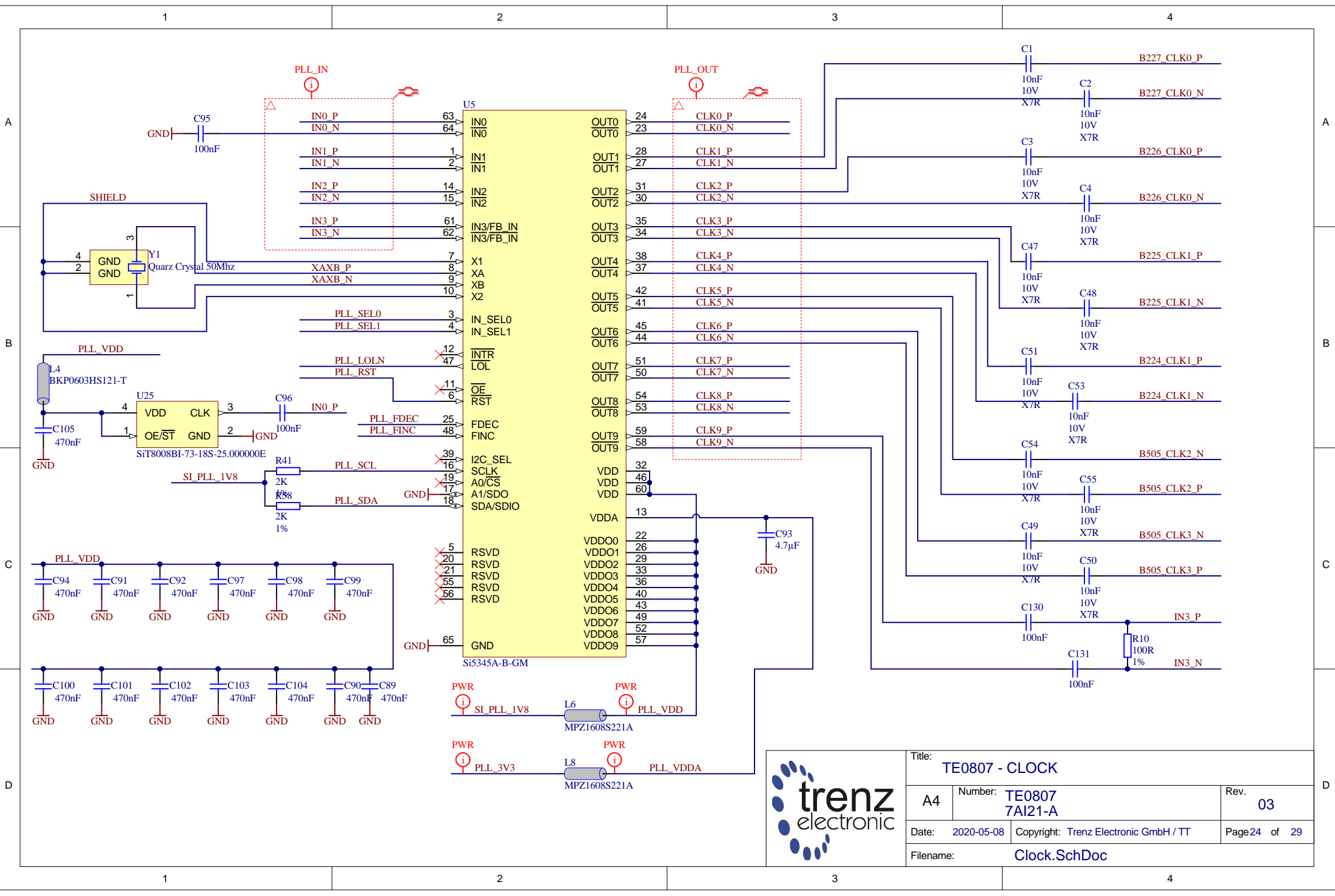


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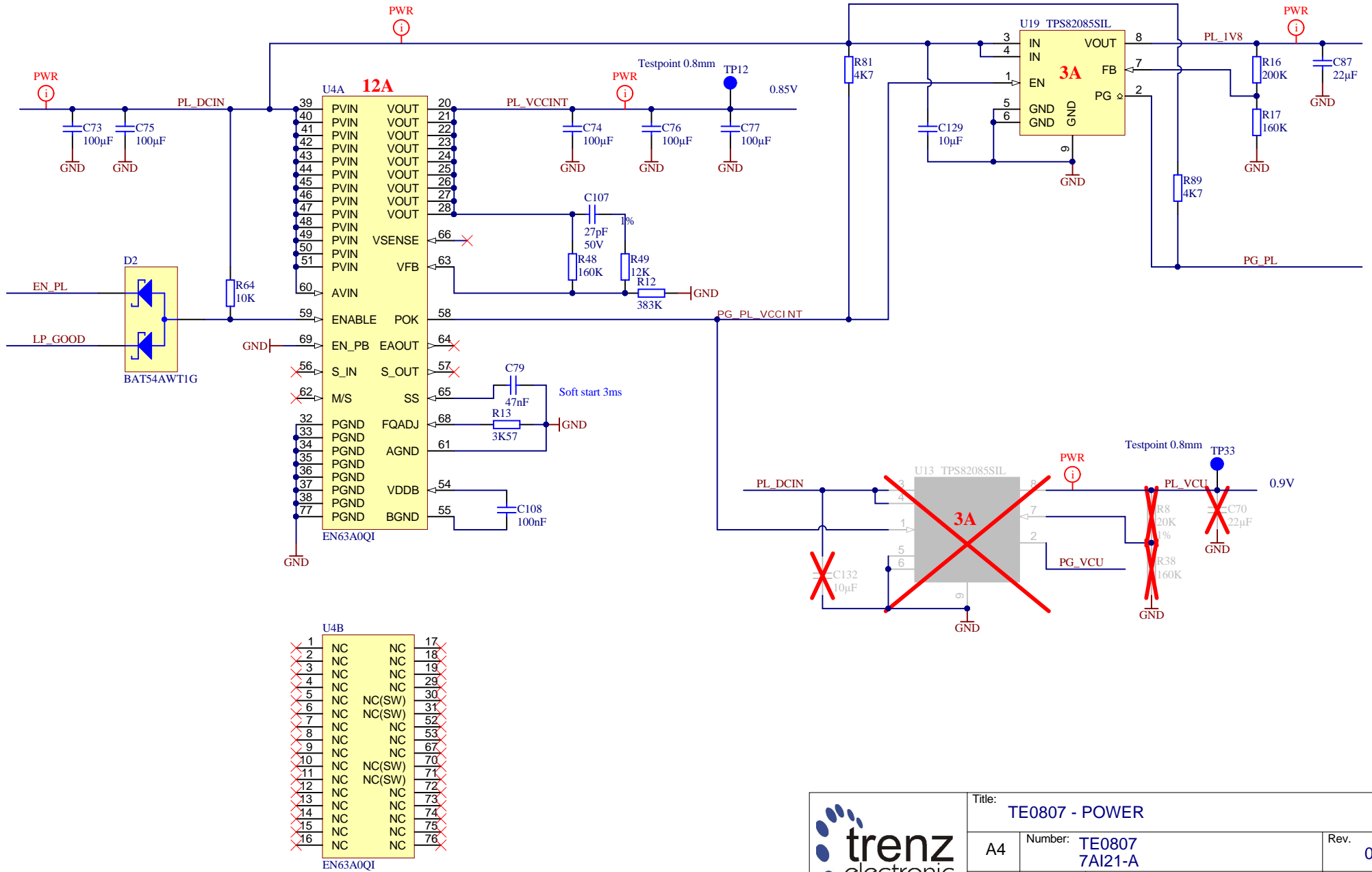


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Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 22 of 29
Filename: <b>DDR4-RAM_4.SchDoc</b>		

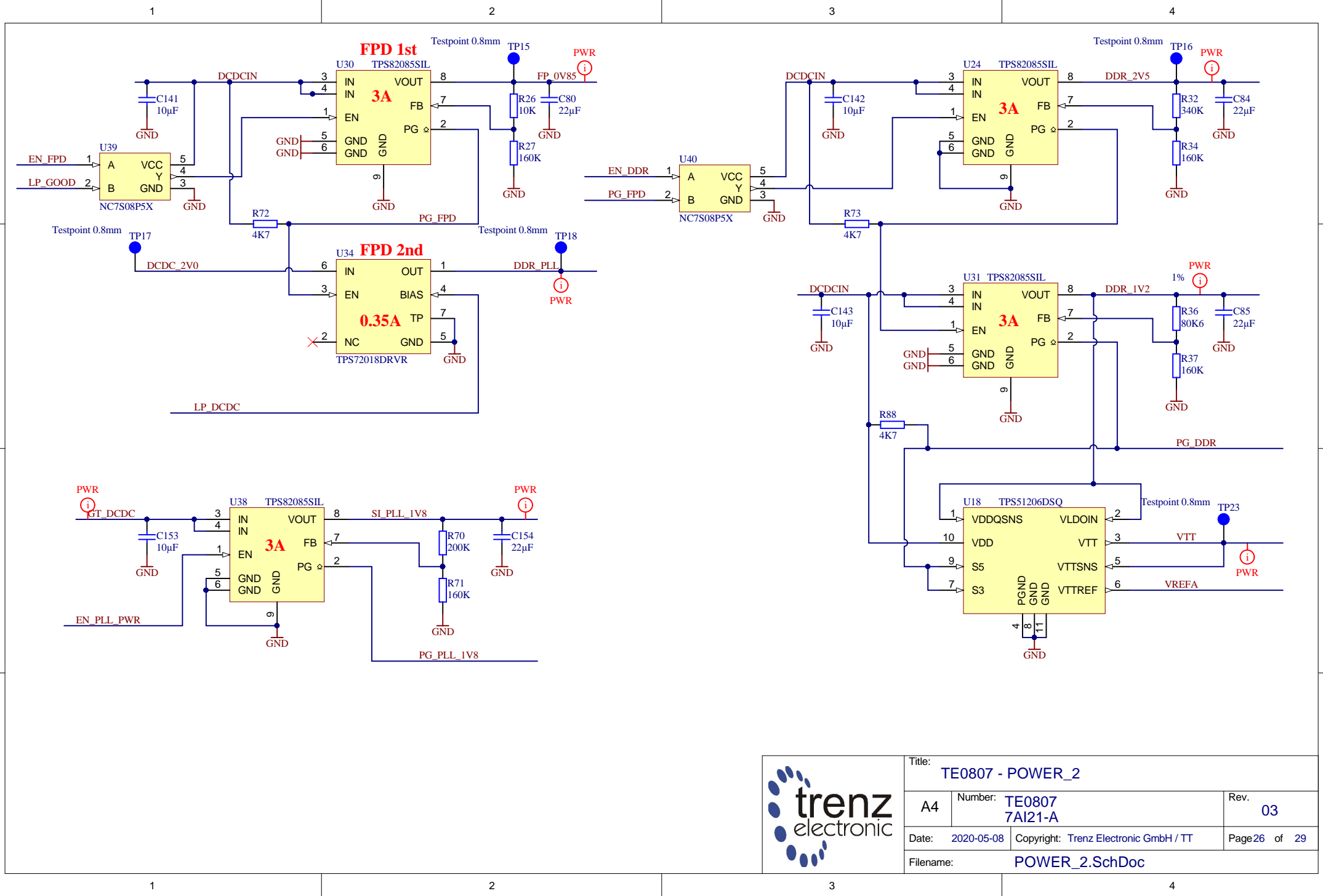





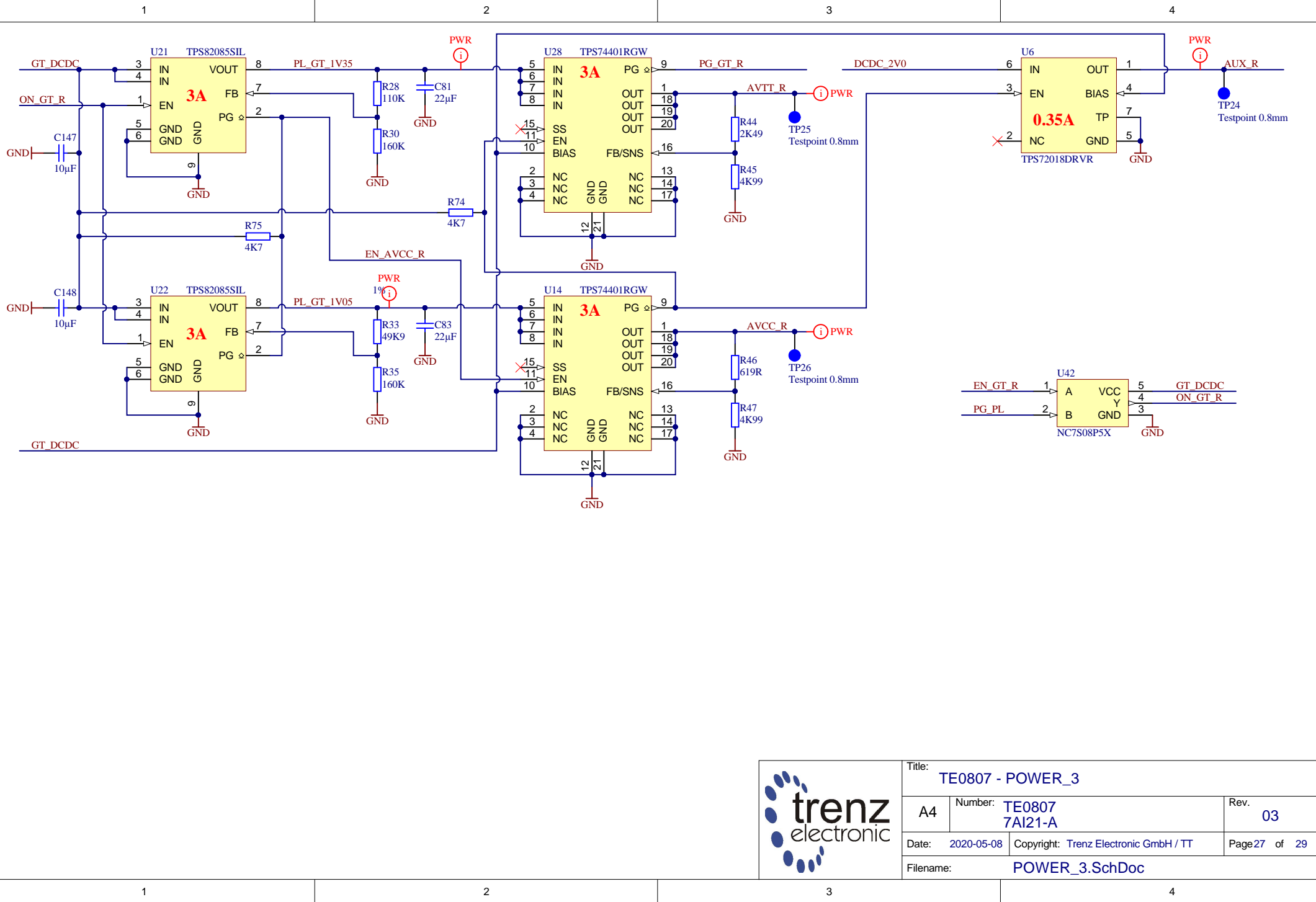
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Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 24 of 29
Filename: Clock.SchDoc		




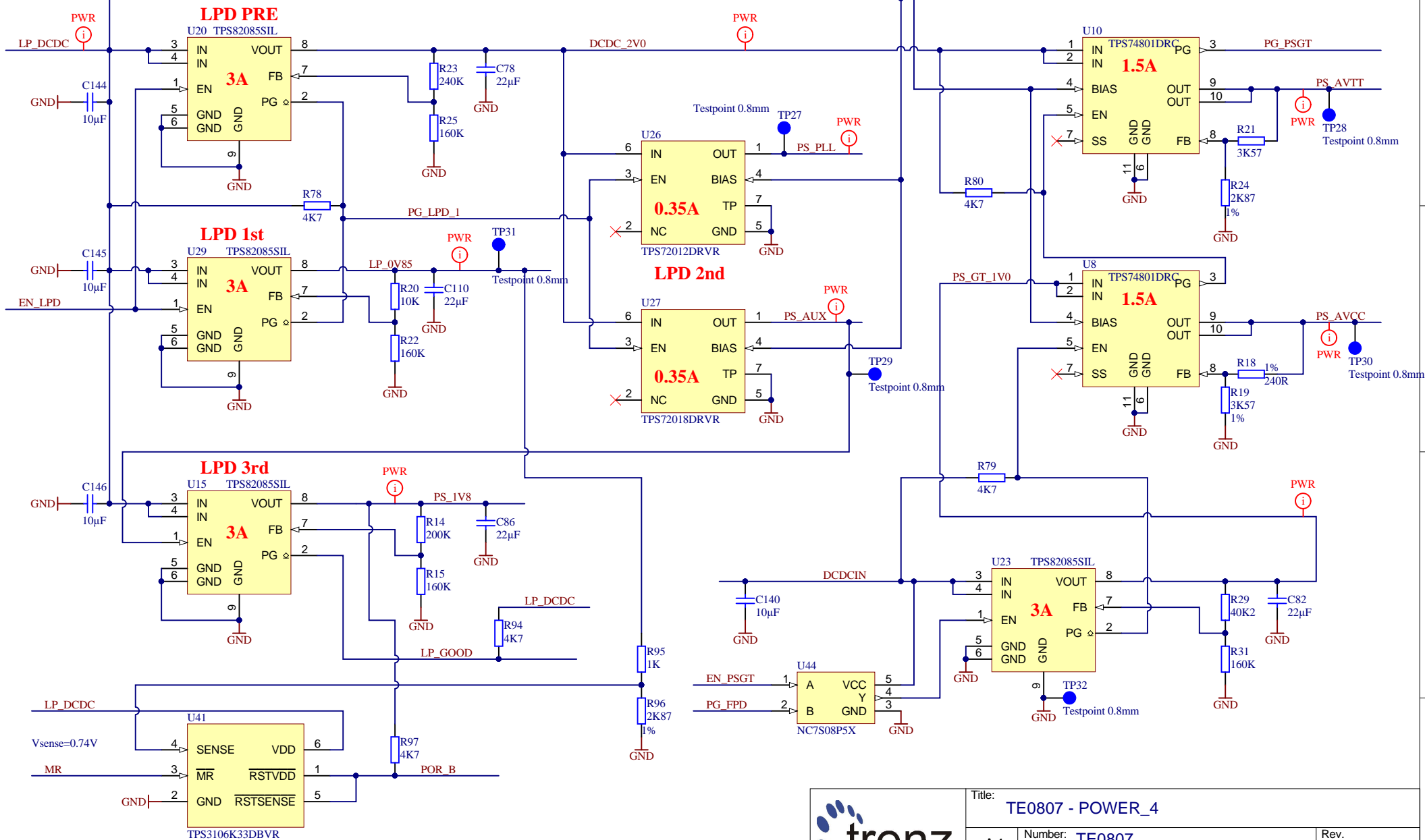
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	Date: <b>2020-05-08</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	
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		Title: TE0807 - POWER_2	
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			Title: TE0807 - POWER_3	
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Title: TE0807 - POWER_4		
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CHANGES REV01 to REV02

- 1) Added EEPROM (U11,24AA025E48T-I/OT)
- 2) Added optional resistors R39/R40 for QSPI flash (do not populated)
- 3) Fixed VCU connection (added additional DCDC and capacitors), recommendation from Xilinx
- 4) Changed obsolete DDR4 chips (NT5AD256M16B2-GN -> K4A8G165WB-BIRC)
- 5) Added net "PG\_VCU" to J2 (pin97)
- 6) full update lib

CHANGES REV02 to REV03 (06.2020)

- VT: 1) Fixed ADC connection  
 2) Fixed DDR4 connection (support B-die DDR4 chips)  
 3) Fixed DDR4 connection (alert\_n pin connection)  
 4) Added U16  
 4) Added testpoints  
 5) Full update LIB

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