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Schematics and other handouts serve for informational purposes only!

	Title: TE0807 - Legal Notices		
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J1.SchDoc

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J2.SchDoc

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J3.SchDoc

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J4.SchDoc

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DDR4-TERM.SchDoc

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Clock.SchDoc

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CONFIG.SchDoc

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U_DDR4-TERM
DDR4-TERM.SchDoc

U_ZU_POWER
ZU_POWER.SchDoc

U_ZU_PS_POWER
ZU_PS_POWER.SchDoc

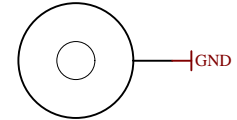
U_POWER
POWER.SchDoc

U_POWER_2
POWER_2.SchDoc

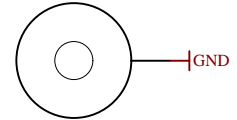
U_POWER_3
POWER_3.SchDoc

U_POWER_4
POWER_4.SchDoc

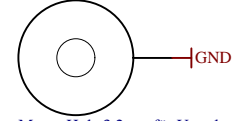
Special notes:



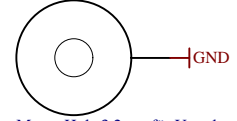
Mount.Hole 3.2mm für Unterlegscheibe



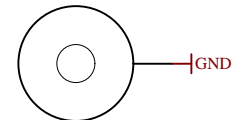
Mount.Hole 3.2mm für Unterlegscheibe



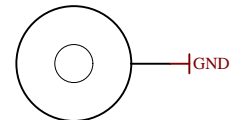
Mount.Hole 3.2mm für Unterlegscheibe



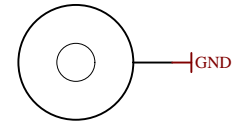
Mount.Hole 3.2mm für Unterlegscheibe



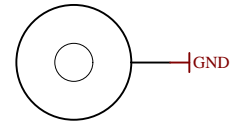
Mount.Hole 3.2mm für Unterlegscheibe



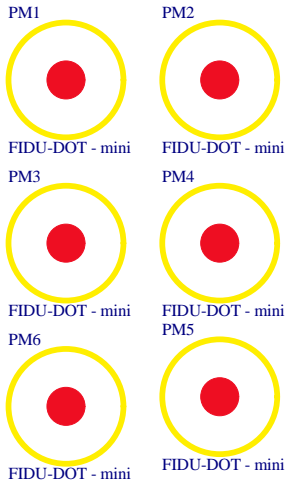
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial
Serialnummer 6,3 x 6.3mm

Assembly variant	7DE21-A
Created by	VY
Modified by	VT
Modified at	2020-03-23
SVN Revision	9271 [Locally Modified]



Title: TE0807		
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1

2

3

4

A

A

B

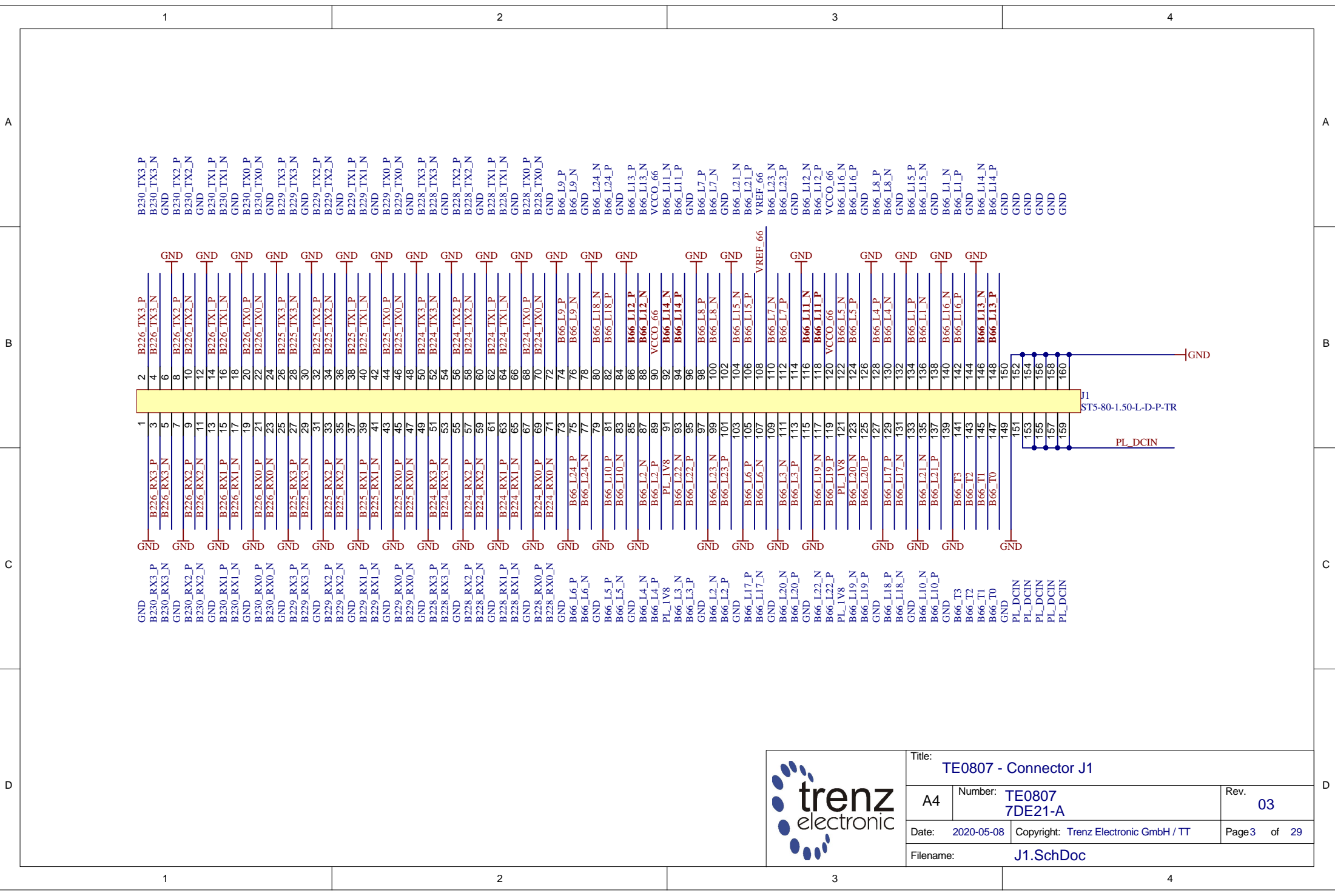
B

C

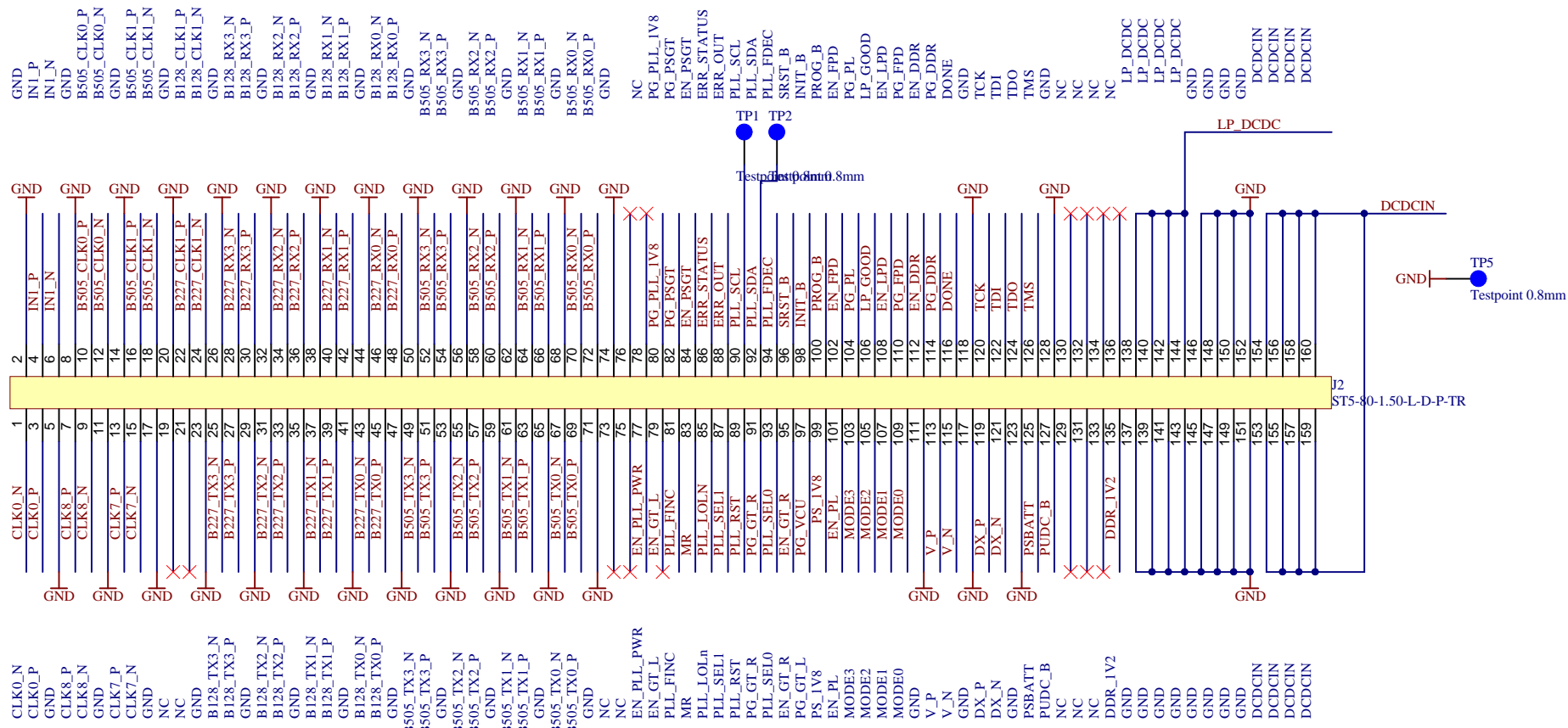
C

D

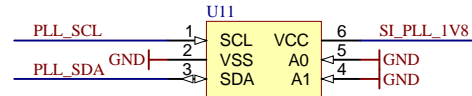
D



Title: TE0807 - Connector J1		
A4	Number: TE0807 7DE21-A	Rev. 03
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Filename: J1.SchDoc		



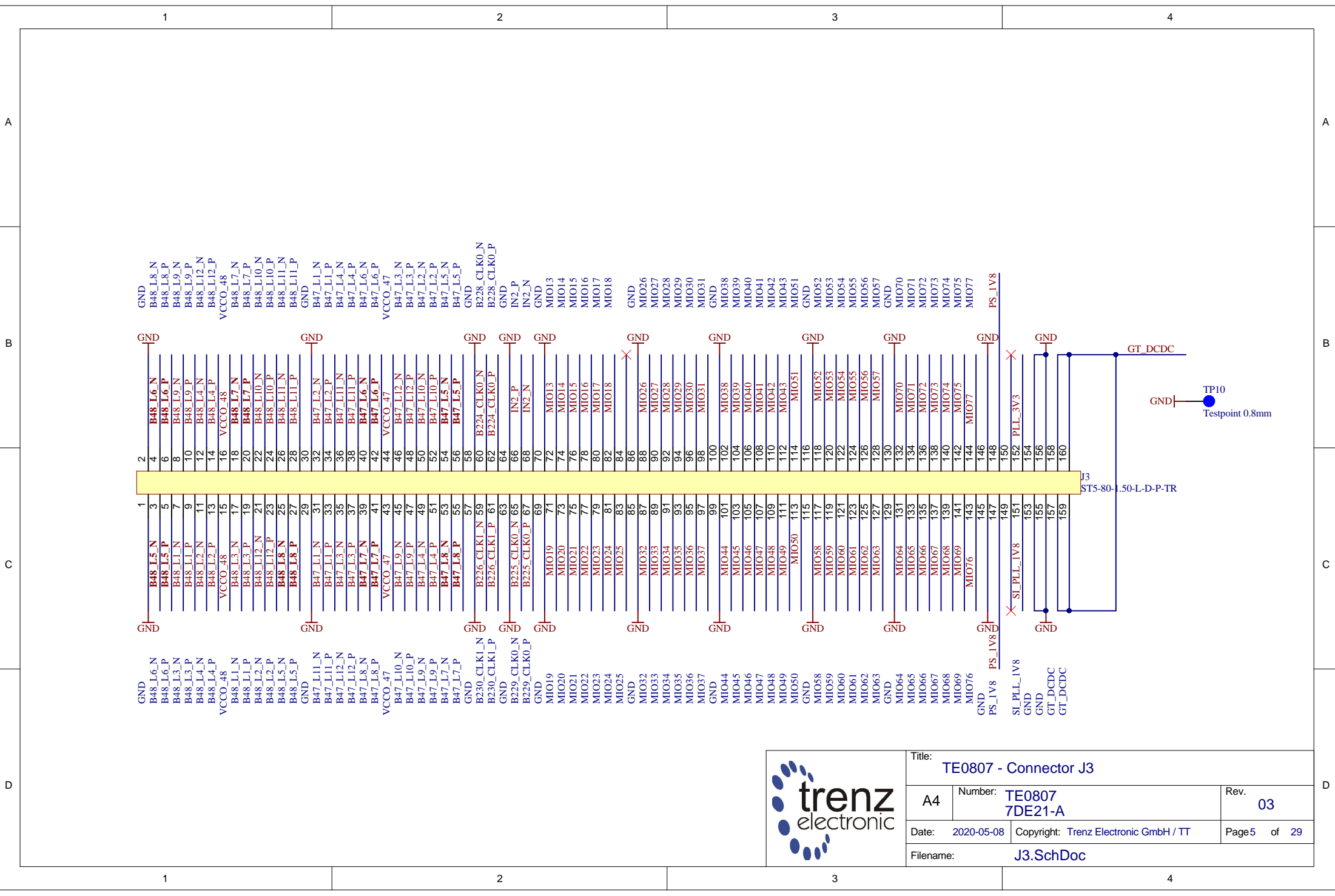
EEPROM for MAC



Slave address: 101000x



Title: TE0807 - Connector J2		
A4	Number: TE0807 7DE21-A	Rev. 03
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Title: TE0807 - Connector J3		
A4	Number: TE0807 7DE21-A	Rev. 03
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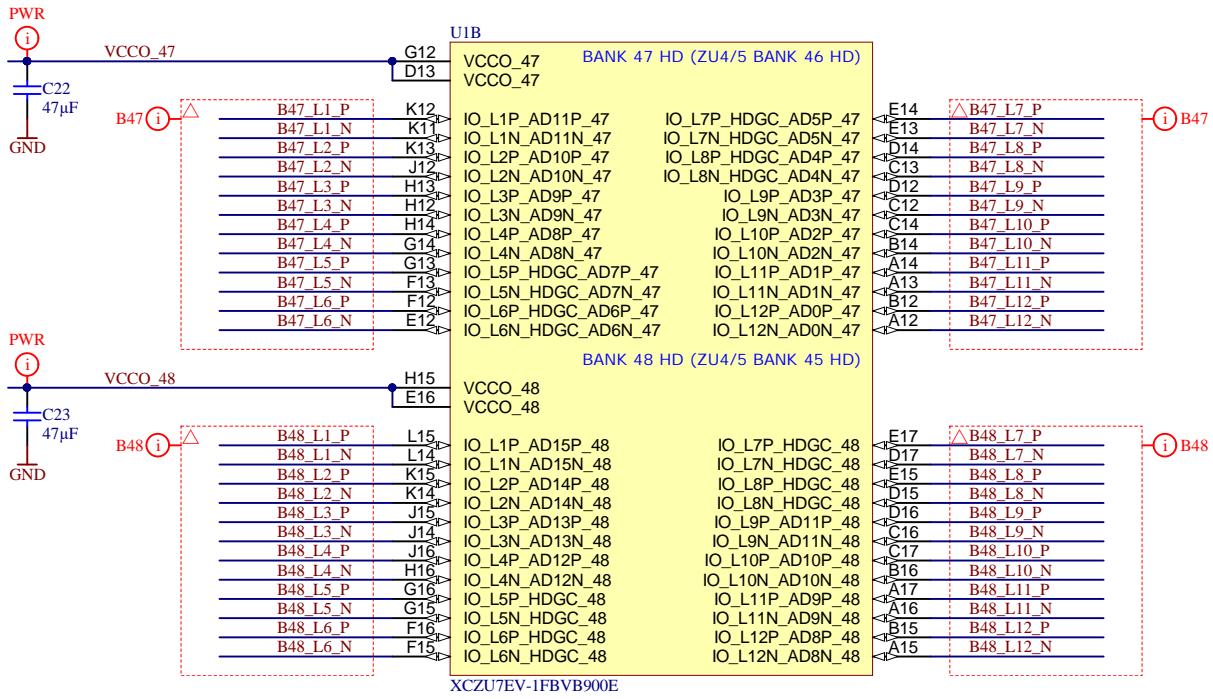
A
B
C
D

1	2	3	4
B65_T3 B65_T2 B65_T1 B65_T0 GND B65_L24_P B65_L24_N VREF_65 B65_L17_P GND B65_L22_P B65_L22_N GND B65_L21_P B65_L21_N GND B65_L20_P B65_L20_N GND B65_L23_P GND B65_L19_P B65_L19_N GND B65_L18_P B65_L18_N GND B65_L24_P B65_L24_N GND B65_L22_P B65_L22_N GND B65_L21_P B65_L21_N GND B65_L20_P B65_L20_N GND B65_L23_P GND B65_L19_P B65_L19_N GND B65_L18_P B65_L18_N GND B65_L15_P GND B65_L12_P B65_L12_N VCCO_65 B65_L7_P GND B65_L11_N B65_L11_P GND B65_L6_P GND B65_L13_P B65_L13_N GND B65_L10_P GND B65_L9_P GND B65_L9_P B65_L4_P GND B65_L14_P GND B65_L8_P B65_L8_N GND B65_L2_P B65_L2_N GND B65_L16_P B65_L16_N GND B65_L3_P B65_L3_P B65_L1_P B65_L1_N GND B65_L5_P GND B65_L5_N NC NC	2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50 52 54 56 58 60 62 64 66 68 70 72 74 76 78 80 82 84 86 88 90 92 94 96 98 100 102 104 106 108 110 112 114 116 118 120 122 124 126 128 130 132 134 136 138 140 142 144 146 148 150 152 154 156 160	B64_T2 B64_T3 B64_T1 B64_T0 GND B64_L24_N B64_L24_P GND B64_L22_P B64_L22_N GND B64_L23_P B64_L23_N GND B64_L19_N B64_L19_P GND B64_L15_P B64_L15_N GND B64_L21_P B64_L21_N GND B64_L20_N B64_L20_P GND B64_L18_P B64_L18_N VCCO_64 B64_L17_P B64_L17_N GND B64_L13_P B64_L13_N GND B64_L14_N B64_L14_P GND B64_L11_P B64_L11_N GND B64_L16_N B64_L16_P VREF_64 B64_L10_N B64_L10_P GND B64_L6_P B64_L6_N GND B64_L5_P B64_L5_N VCCO_64 B64_L9_P GND B64_L4_P B64_L4_N GND B64_L3_N B64_L3_P GND B64_L12_N B64_L12_P GND B64_L2_N B64_L2_P GND B64_L1_N B64_L1_P GND B64_L8_N B64_L8_P GND B64_L7_P B64_L7_N GND NC NC NC	

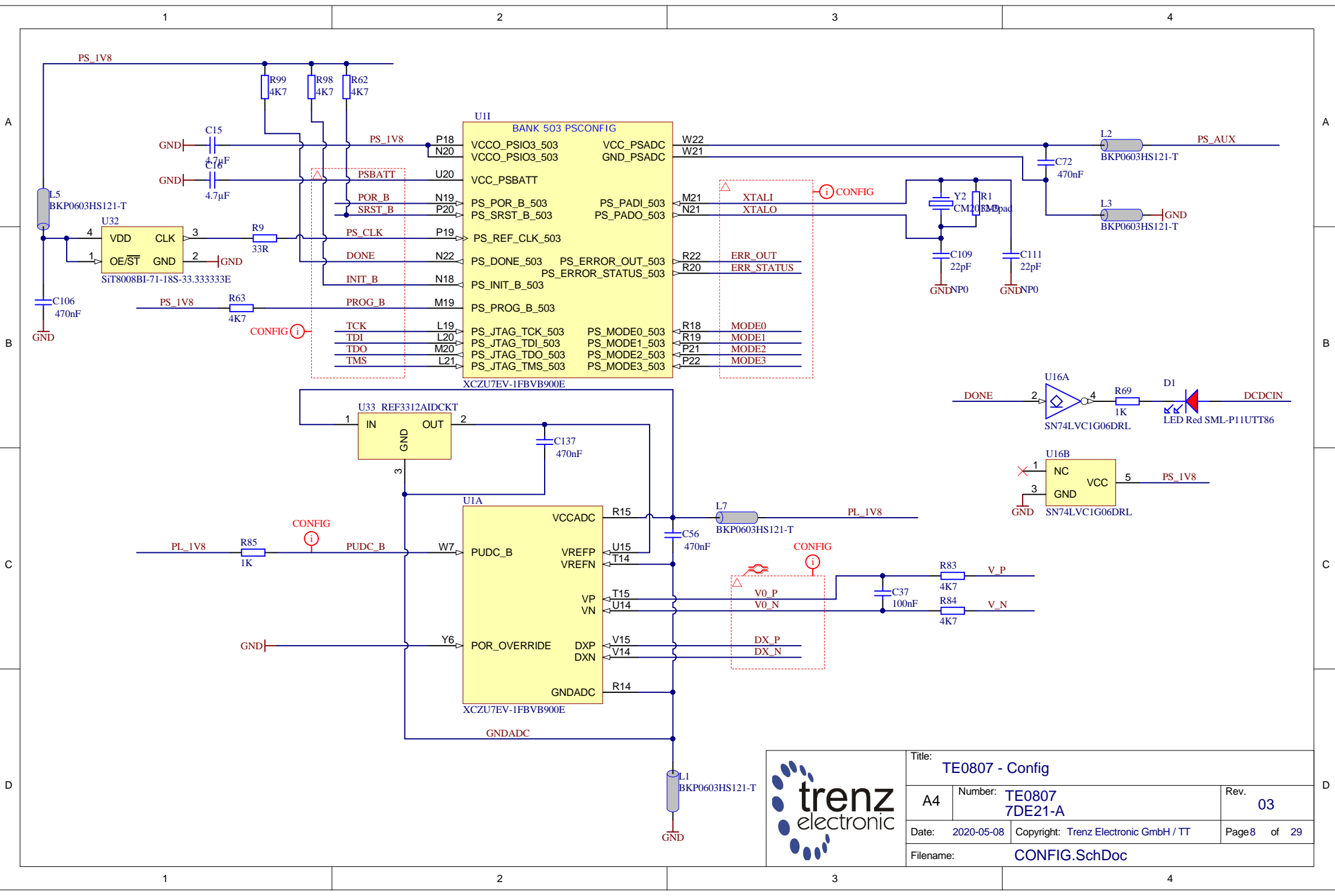
J4 ST5-80-1.50-L-D-P-TR




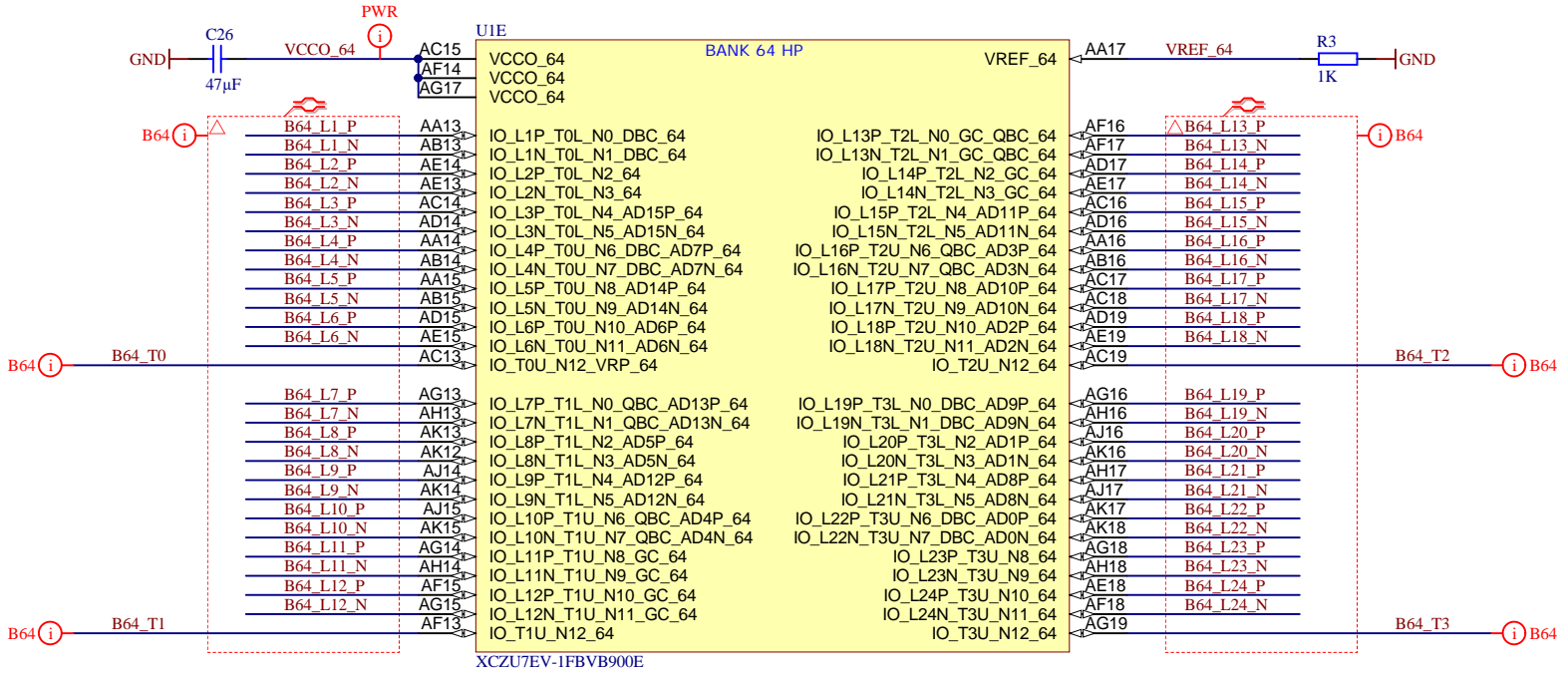
Title: TE0807 - Connector J4		
A4	Number: TE0807 7DE21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 6 of 29
Filename: J4.SchDoc		



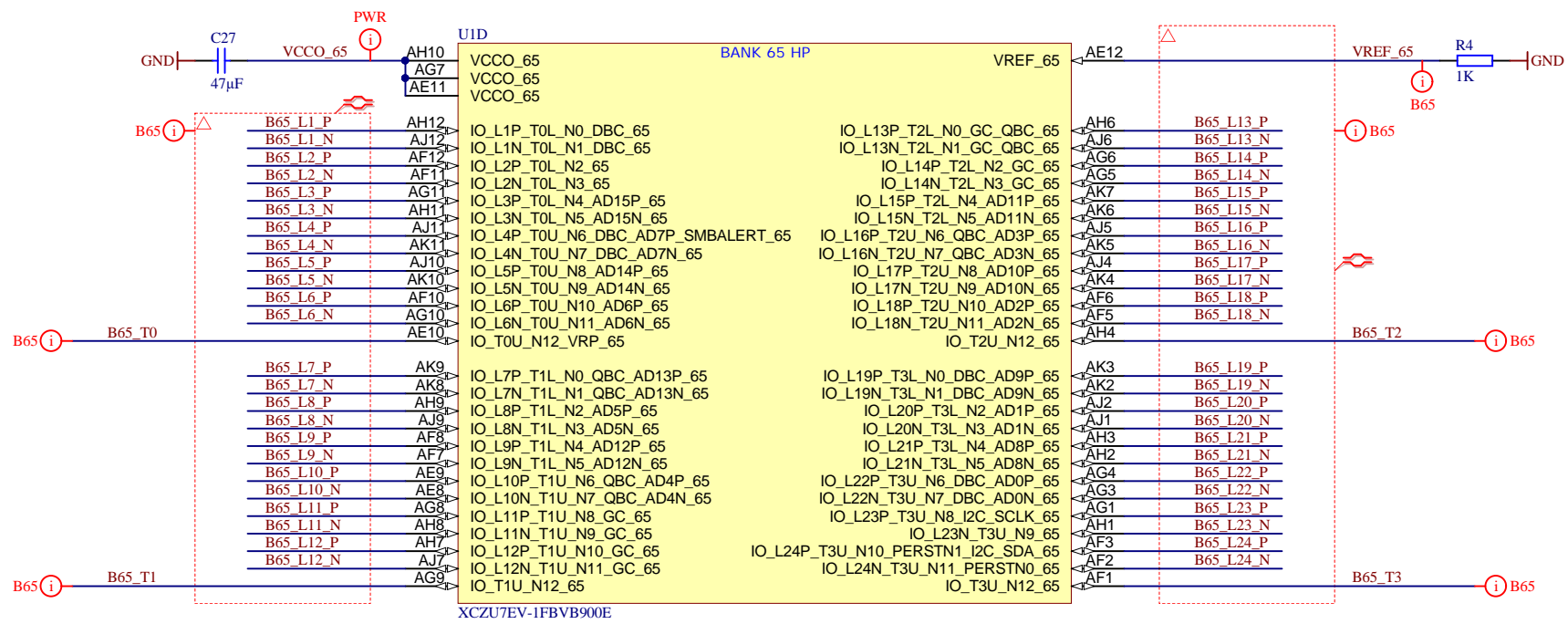
Title: TE0807 - B47HD and B48HD		
A4	Number: TE0807 7DE21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 7 of 29
Filename: B_HD.SchDoc		



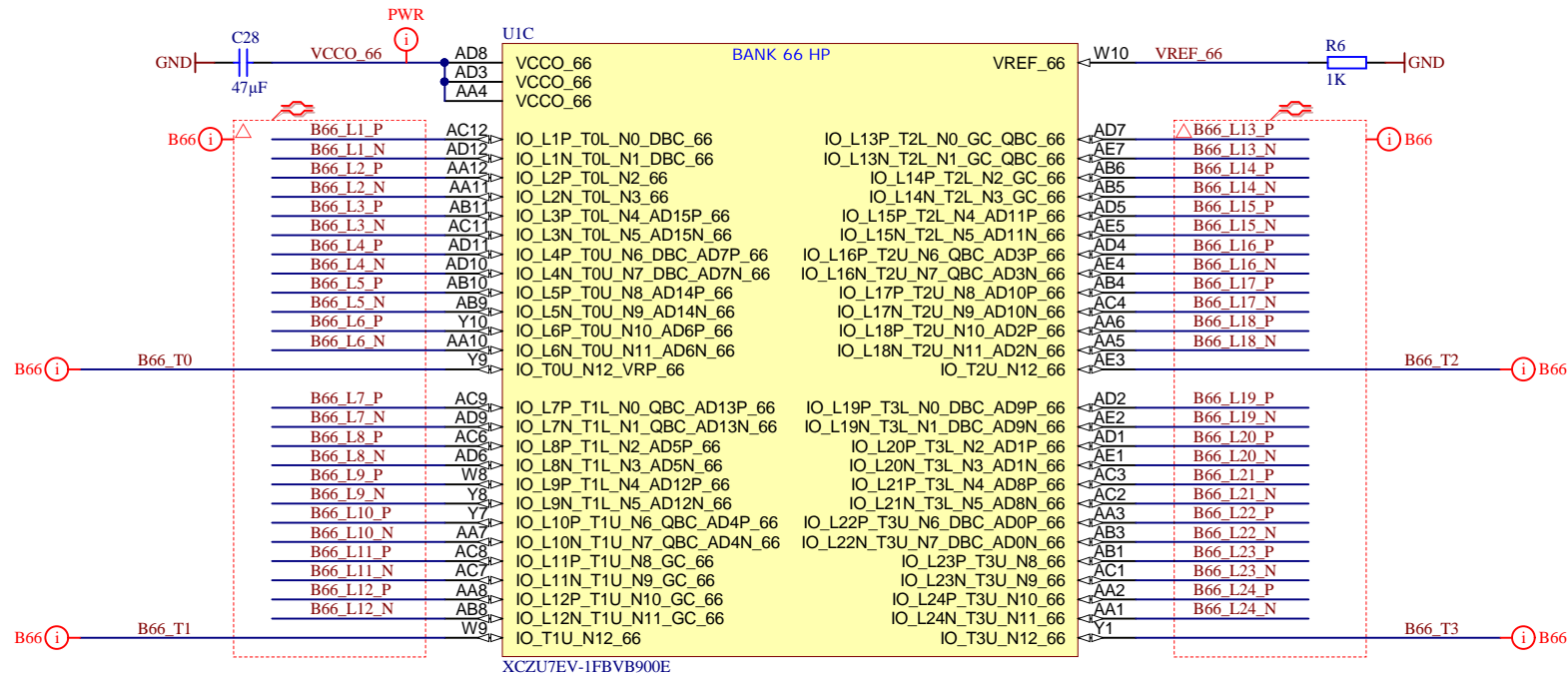
			Title: TE0807 - Config	
			A4	Number: TE0807 7DE21-A
Date: 2020-05-08		Copyright: Trenz Electronic GmbH / TT		Page 8 of 29
Filename: CONFIG.SchDoc				



	Title: TE0807 - B64		
	A4	Number: TE0807 7DE21-A	Rev. 03
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	Filename: B64.SchDoc		



Title: TE0807 - B65		
A4	Number: TE0807 7DE21-A	Rev. 03
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Title: TE0807 - B66		
A4	Number: TE0807 7DE21-A	Rev. 03
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Filename: B66.SchDoc		

A

A

B

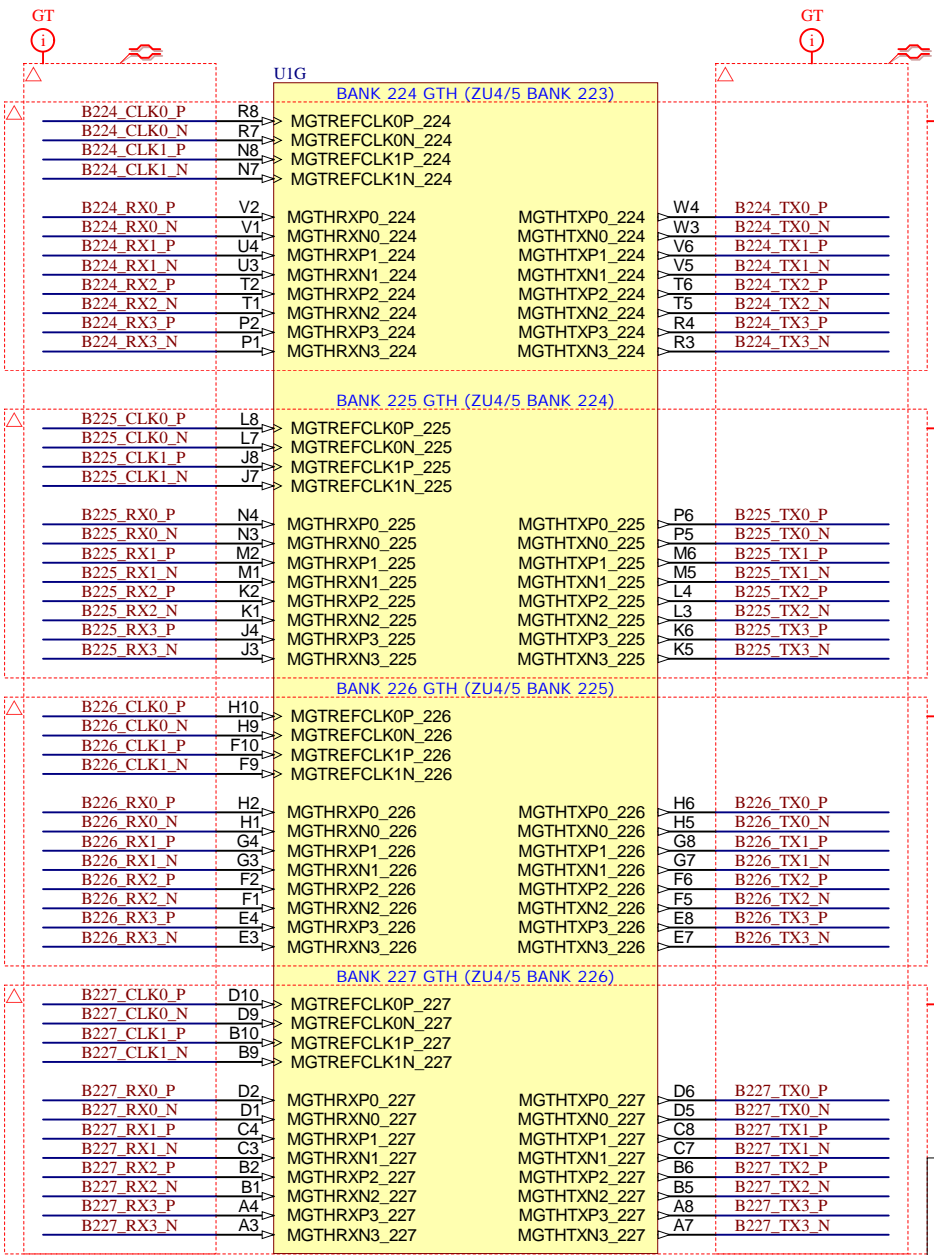
B

C

C

D

D



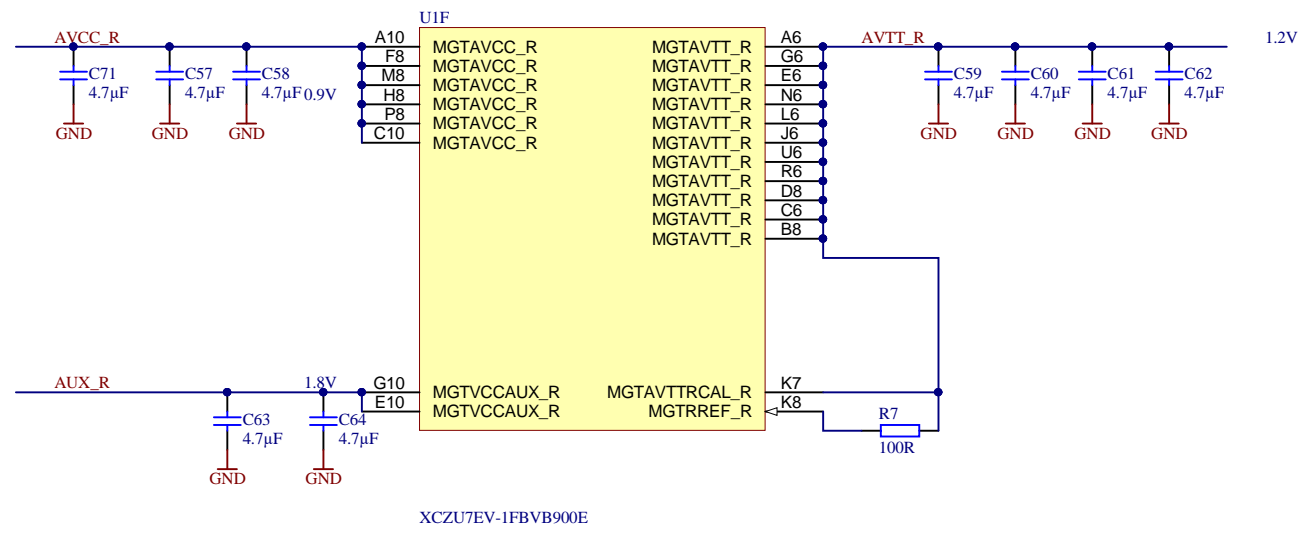
228

229


230

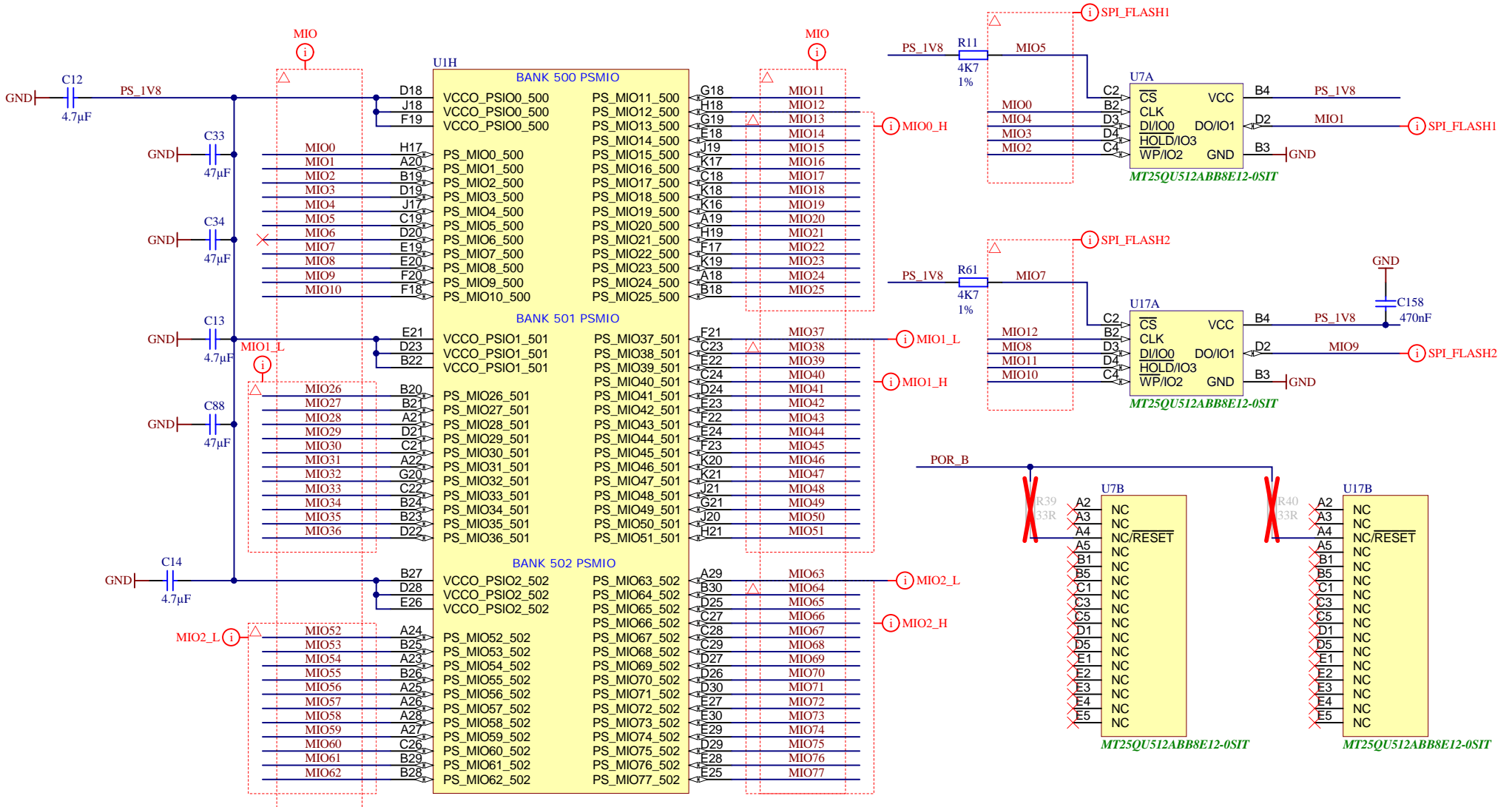


Title: TE0807 - GTH_Banks		
A4	Number: TE0807 7DE21-A	Rev. 03
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Filename: B_GT.SchDoc		




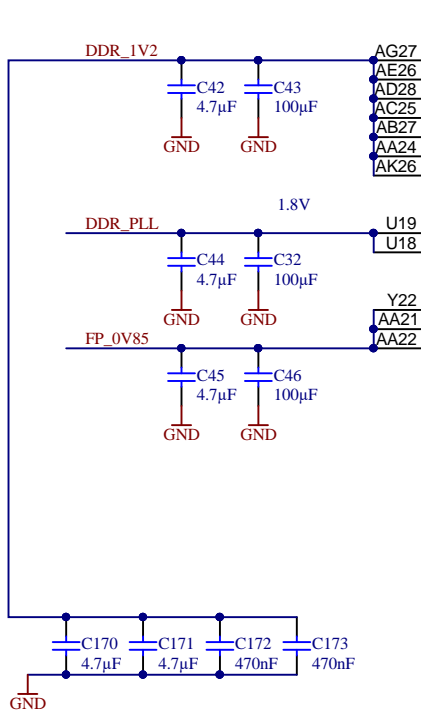
XCZU7EV-1FBVB900E

		Title: TE0807 - GTH_PWR	
		A4	Number: TE0807 7DE21-A
Date: 2020-05-08		Copyright: Trenz Electronic GmbH / TT	
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XCZU7EV-1FBVB900E

		Title: TE0807 - MIO Banks	
		A4	Number: TE0807 7DE21-A
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Filename: B_MIO.SchDoc		Page 14 of 29	



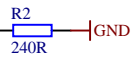
U1J

BANK 504 PSDDR

AG27	VCCO_PSDDR_504	PS_DDR_CK0_504
AE26	VCCO_PSDDR_504	PS_DDR_CK_N0_504
AD28	VCCO_PSDDR_504	PS_DDR_CKE0_504
AC25	VCCO_PSDDR_504	
AB27	VCCO_PSDDR_504	PS_DDR_CK1_504
AA24	VCCO_PSDDR_504	PS_DDR_CK_N1_504
AK26	VCCO_PSDDR_504	PS_DDR_CKE1_504
U19	VCC_PSDDR_PLL	PS_DDR_A0_504
U18	VCC_PSDDR_PLL	PS_DDR_A1_504
		PS_DDR_A2_504
		PS_DDR_A3_504
		PS_DDR_A4_504
		PS_DDR_A5_504
Y22	VCC_PSINTFF_DDR	PS_DDR_A6_504
AA21	VCC_PSINTFF_DDR	PS_DDR_A7_504
AA22	VCC_PSINTFF_DDR	PS_DDR_A8_504
		PS_DDR_A9_504
		PS_DDR_A10_504
		PS_DDR_A11_504
		PS_DDR_A12_504
		PS_DDR_A13_504
		PS_DDR_A14_504
		PS_DDR_A15_504
		PS_DDR_A16_504
		PS_DDR_A17_504
		PS_DDR_CS_N0_504
		PS_DDR_CS_N1_504
		PS_DDR_BA0_504
		PS_DDR_BA1_504
		PS_DDR_BG0_504
		PS_DDR_BG1_504
		PS_DDR_PARITY_504
		PS_DDR_RAM_RST_N_504
		PS_DDR_ACT_N_504
		PS_DDR_ALERT_N_504
		PS_DDR_ZQ_504
		PS_DDR_ODT0_504
		PS_DDR_ODT1_504

XCZU7EV-1FBVB900E

AE30	DDR4-CLK0_P
AF30	DDR4-CLK0_N
AC30	DDR4-CKE0
AF28	
AG28	
AB28	
AH30	DDR4-A0
AG30	DDR4-A1
AK29	DDR4-A2
AJ30	DDR4-A3
AK28	DDR4-A4
AK27	DDR4-A5
AF27	DDR4-A6
AE27	DDR4-A7
AF26	DDR4-A8
AG26	DDR4-A9
AE29	DDR4-A10
AE28	DDR4-A11
AH29	DDR4-A12
AG29	DDR4-A14
AJ29	DDR4-A15
AH27	DDR4-A16
AJ27	DDR4-A17
AD30	DDR4-CS
AD29	
AD27	DDR4-BA0
AC26	DDR4-BA1
AC28	DDR4-BG0
AC27	DDR4-BG1
AB26	DDR4-PAR
AB25	DDR4-RESET
AD26	DDR4-ACT
AB24	DDR4-ALERT
AB23	
AB30	DDR4-ODT0
AC29	



U1K

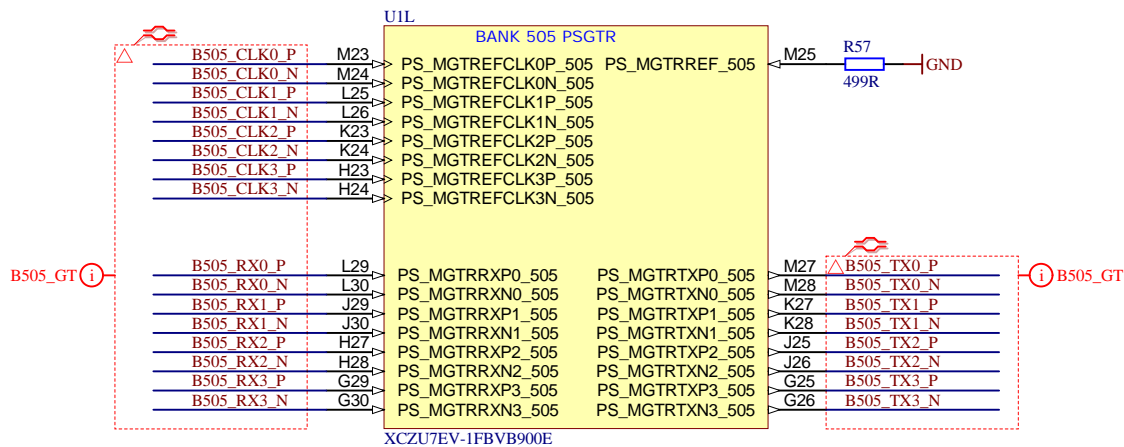
BANK 504 PSDDR


DQ0	AH22	PS_DDR_DQ0_504	PS_DDR_DQ32_504
DQ1	AH21	PS_DDR_DQ1_504	PS_DDR_DQ33_504
DQ2	AJ22	PS_DDR_DQ2_504	PS_DDR_DQ34_504
DQ3	AK22	PS_DDR_DQ3_504	PS_DDR_DQ35_504
DQ4	AK20	PS_DDR_DQ4_504	PS_DDR_DQ36_504
DQ5	AJ19	PS_DDR_DQ5_504	PS_DDR_DQ37_504
DQ6	AK19	PS_DDR_DQ6_504	PS_DDR_DQ38_504
DQ7	AH19	PS_DDR_DQ7_504	PS_DDR_DQ39_504
DQ8	AH23	PS_DDR_DQ8_504	PS_DDR_DQ40_504
DQ9	AK23	PS_DDR_DQ9_504	PS_DDR_DQ41_504
DQ10	AG24	PS_DDR_DQ10_504	PS_DDR_DQ42_504
DQ11	AK24	PS_DDR_DQ11_504	PS_DDR_DQ43_504
DQ12	AJ26	PS_DDR_DQ12_504	PS_DDR_DQ44_504
DQ13	AK25	PS_DDR_DQ13_504	PS_DDR_DQ45_504
DQ14	AG25	PS_DDR_DQ14_504	PS_DDR_DQ46_504
DQ15	AH26	PS_DDR_DQ15_504	PS_DDR_DQ47_504
DQ16	AD22	PS_DDR_DQ16_504	PS_DDR_DQ48_504
DQ17	AE22	PS_DDR_DQ17_504	PS_DDR_DQ49_504
DQ18	AF22	PS_DDR_DQ18_504	PS_DDR_DQ50_504
DQ19	AG21	PS_DDR_DQ19_504	PS_DDR_DQ51_504
DQ20	AD20	PS_DDR_DQ20_504	PS_DDR_DQ52_504
DQ21	AF20	PS_DDR_DQ21_504	PS_DDR_DQ53_504
DQ22	AE20	PS_DDR_DQ22_504	PS_DDR_DQ54_504
DQ23	AG20	PS_DDR_DQ23_504	PS_DDR_DQ55_504
DQ24	AG23	PS_DDR_DQ24_504	PS_DDR_DQ56_504
DQ25	AF23	PS_DDR_DQ25_504	PS_DDR_DQ57_504
DQ26	AF25	PS_DDR_DQ26_504	PS_DDR_DQ58_504
DQ27	AE23	PS_DDR_DQ27_504	PS_DDR_DQ59_504
DQ28	AC22	PS_DDR_DQ28_504	PS_DDR_DQ60_504
DQ29	AC23	PS_DDR_DQ29_504	PS_DDR_DQ61_504
DQ30	AD25	PS_DDR_DQ30_504	PS_DDR_DQ62_504
DQ31	AC24	PS_DDR_DQ31_504	PS_DDR_DQ63_504
		PS_DDR_DQ64_504	PS_DDR_DQ65_504
		PS_DDR_DQ66_504	PS_DDR_DQ67_504
		PS_DDR_DQ68_504	PS_DDR_DQ69_504
		PS_DDR_DQ70_504	PS_DDR_DQ71_504
		PS_DDR_DQS_P0_504	PS_DDR_DQS_P1_504
		PS_DDR_DQS_N0_504	PS_DDR_DQS_N1_504
		PS_DDR_DQS_P2_504	PS_DDR_DQS_P3_504
		PS_DDR_DQS_N2_504	PS_DDR_DQS_N3_504
		PS_DDR_DQS_P4_504	PS_DDR_DQS_N4_504
		PS_DDR_DQS_P5_504	PS_DDR_DQS_N5_504
		PS_DDR_DQS_P6_504	PS_DDR_DQS_N6_504
		PS_DDR_DQS_P7_504	PS_DDR_DQS_N7_504
		PS_DDR_DQS_P8_504	PS_DDR_DQS_N8_504
		PS_DDR_DQS_P9_504	PS_DDR_DQS_N9_504
		PS_DDR_DQS_P10_504	PS_DDR_DQS_N10_504
		PS_DDR_DQS_P11_504	PS_DDR_DQS_N11_504
		PS_DDR_DQS_P12_504	PS_DDR_DQS_N12_504
		PS_DDR_DQS_P13_504	PS_DDR_DQS_N13_504
		PS_DDR_DQS_P14_504	PS_DDR_DQS_N14_504
		PS_DDR_DQS_P15_504	PS_DDR_DQS_N15_504
		PS_DDR_DQS_P16_504	PS_DDR_DQS_N16_504
		PS_DDR_DQS_P17_504	PS_DDR_DQS_N17_504
		PS_DDR_DQS_P18_504	PS_DDR_DQS_N18_504
		PS_DDR_DQS_P19_504	PS_DDR_DQS_N19_504
		PS_DDR_DQS_P20_504	PS_DDR_DQS_N20_504
		PS_DDR_DQS_P21_504	PS_DDR_DQS_N21_504
		PS_DDR_DQS_P22_504	PS_DDR_DQS_N22_504
		PS_DDR_DQS_P23_504	PS_DDR_DQS_N23_504
		PS_DDR_DQS_P24_504	PS_DDR_DQS_N24_504
		PS_DDR_DQS_P25_504	PS_DDR_DQS_N25_504
		PS_DDR_DQS_P26_504	PS_DDR_DQS_N26_504
		PS_DDR_DQS_P27_504	PS_DDR_DQS_N27_504
		PS_DDR_DQS_P28_504	PS_DDR_DQS_N28_504
		PS_DDR_DQS_P29_504	PS_DDR_DQS_N29_504
		PS_DDR_DQS_P30_504	PS_DDR_DQS_N30_504
		PS_DDR_DQS_P31_504	PS_DDR_DQS_N31_504
		PS_DDR_DQS_P32_504	PS_DDR_DQS_N32_504
		PS_DDR_DQS_P33_504	PS_DDR_DQS_N33_504
		PS_DDR_DQS_P34_504	PS_DDR_DQS_N34_504
		PS_DDR_DQS_P35_504	PS_DDR_DQS_N35_504
		PS_DDR_DQS_P36_504	PS_DDR_DQS_N36_504
		PS_DDR_DQS_P37_504	PS_DDR_DQS_N37_504
		PS_DDR_DQS_P38_504	PS_DDR_DQS_N38_504
		PS_DDR_DQS_P39_504	PS_DDR_DQS_N39_504
		PS_DDR_DQS_P40_504	PS_DDR_DQS_N40_504
		PS_DDR_DQS_P41_504	PS_DDR_DQS_N41_504
		PS_DDR_DQS_P42_504	PS_DDR_DQS_N42_504
		PS_DDR_DQS_P43_504	PS_DDR_DQS_N43_504
		PS_DDR_DQS_P44_504	PS_DDR_DQS_N44_504
		PS_DDR_DQS_P45_504	PS_DDR_DQS_N45_504
		PS_DDR_DQS_P46_504	PS_DDR_DQS_N46_504
		PS_DDR_DQS_P47_504	PS_DDR_DQS_N47_504
		PS_DDR_DQS_P48_504	PS_DDR_DQS_N48_504
		PS_DDR_DQS_P49_504	PS_DDR_DQS_N49_504
		PS_DDR_DQS_P50_504	PS_DDR_DQS_N50_504
		PS_DDR_DQS_P51_504	PS_DDR_DQS_N51_504
		PS_DDR_DQS_P52_504	PS_DDR_DQS_N52_504
		PS_DDR_DQS_P53_504	PS_DDR_DQS_N53_504
		PS_DDR_DQS_P54_504	PS_DDR_DQS_N54_504
		PS_DDR_DQS_P55_504	PS_DDR_DQS_N55_504
		PS_DDR_DQS_P56_504	PS_DDR_DQS_N56_504
		PS_DDR_DQS_P57_504	PS_DDR_DQS_N57_504
		PS_DDR_DQS_P58_504	PS_DDR_DQS_N58_504
		PS_DDR_DQS_P59_504	PS_DDR_DQS_N59_504
		PS_DDR_DQS_P60_504	PS_DDR_DQS_N60_504
		PS_DDR_DQS_P61_504	PS_DDR_DQS_N61_504
		PS_DDR_DQS_P62_504	PS_DDR_DQS_N62_504
		PS_DDR_DQS_P63_504	PS_DDR_DQS_N63_504
		PS_DDR_DQS_P64_504	PS_DDR_DQS_N64_504
		PS_DDR_DQS_P65_504	PS_DDR_DQS_N65_504
		PS_DDR_DQS_P66_504	PS_DDR_DQS_N66_504
		PS_DDR_DQS_P67_504	PS_DDR_DQS_N67_504
		PS_DDR_DQS_P68_504	PS_DDR_DQS_N68_504
		PS_DDR_DQS_P69_504	PS_DDR_DQS_N69_504
		PS_DDR_DQS_P70_504	PS_DDR_DQS_N70_504
		PS_DDR_DQS_P71_504	PS_DDR_DQS_N71_504
		PS_DDR_DQS_P72_504	PS_DDR_DQS_N72_504
		PS_DDR_DQS_P73_504	PS_DDR_DQS_N73_504
		PS_DDR_DQS_P74_504	PS_DDR_DQS_N74_504
		PS_DDR_DQS_P75_504	PS_DDR_DQS_N75_504
		PS_DDR_DQS_P76_504	PS_DDR_DQS_N76_504
		PS_DDR_DQS_P77_504	PS_DDR_DQS_N77_504
		PS_DDR_DQS_P78_504	PS_DDR_DQS_N78_504
		PS_DDR_DQS_P79_504	PS_DDR_DQS_N79_504
		PS_DDR_DQS_P80_504	PS_DDR_DQS_N80_504
		PS_DDR_DQS_P81_504	PS_DDR_DQS_N81_504
		PS_DDR_DQS_P82_504	PS_DDR_DQS_N82_504
		PS_DDR_DQS_P83_504	PS_DDR_DQS_N83_504
		PS_DDR_DQS_P84_504	PS_DDR_DQS_N84_504
		PS_DDR_DQS_P85_504	PS_DDR_DQS_N85_504
		PS_DDR_DQS_P86_504	PS_DDR_DQS_N86_504
		PS_DDR_DQS_P87_504	PS_DDR_DQS_N87_504
		PS_DDR_DQS_P88_504	PS_DDR_DQS_N88_504
		PS_DDR_DQS_P89_504	PS_DDR_DQS_N89_504
		PS_DDR_DQS_P90_504	PS_DDR_DQS_N90_504
		PS_DDR_DQS_P91_504	PS_DDR_DQS_N91_504
		PS_DDR_DQS_P92_504	PS_DDR_DQS_N92_504
		PS_DDR_DQS_P93_504	PS_DDR_DQS_N93_504
		PS_DDR_DQS_P94_504	PS_DDR_DQS_N94_504
		PS_DDR_DQS_P95_504	PS_DDR_DQS_N95_504
		PS_DDR_DQS_P96_504	PS_DDR_DQS_N96_504
		PS_DDR_DQS_P97_504	PS_DDR_DQS_N97_504
		PS_DDR_DQS_P98_504	PS_DDR_DQS_N98_504
		PS_DDR_DQS_P99_504	PS_DDR_DQS_N99_504

XCZU7EV-1FBVB900E



Title: TE0807 - PS_DDR		
A4	Number: TE0807 7DE21-A	Rev. 03
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	Title: TE0807 - PS_GT		
	A4	Number: TE0807 7DE21-A	Rev. 03
	Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 16 of 29
	Filename: B_PS_GT.SchDoc		

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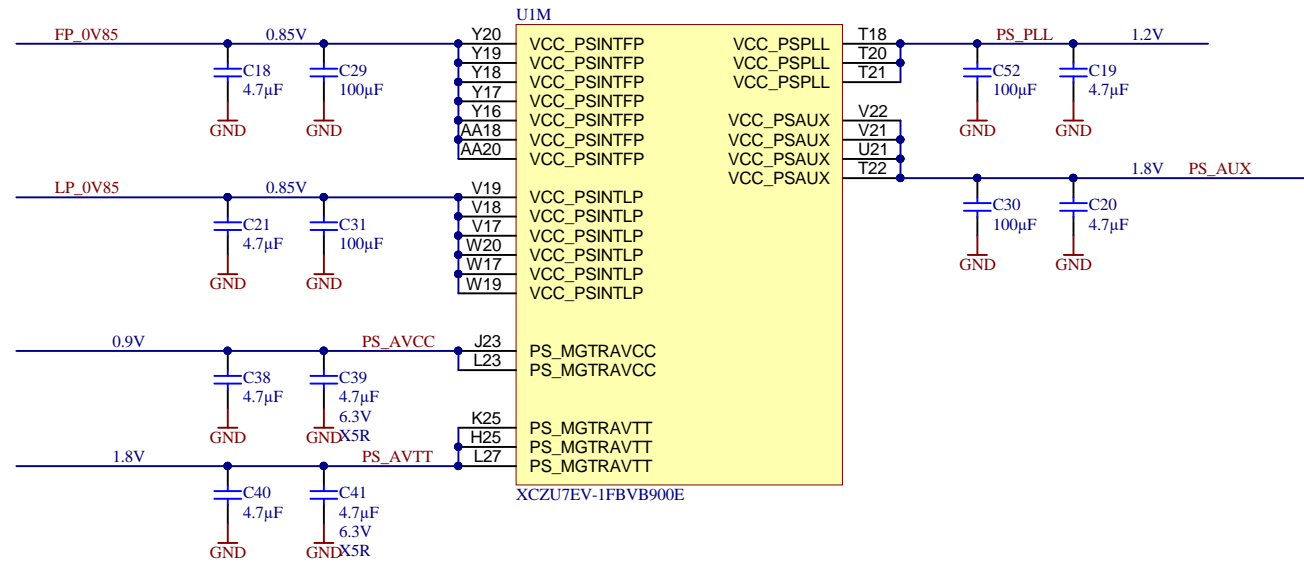
B

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VCC_PSINTFP	VCC_PSPLL
VCC_PSINTFP	VCC_PSPLL
VCC_PSINTFP	VCC_PSPLL
VCC_PSINTFP	VCC_PSPLL
VCC_PSINTFP	VCC_PSAUX
VCC_PSINTFP	VCC_PSAUX
VCC_PSINTFP	VCC_PSAUX
VCC_PSINTFP	VCC_PSAUX
VCC_PSINTLP	VCC_PSPLL
VCC_PSINTLP	VCC_PSPLL
VCC_PSINTLP	VCC_PSAUX
VCC_PSINTLP	VCC_PSAUX
VCC_PSINTLP	VCC_PSAUX
VCC_PSINTLP	VCC_PSAUX
VCC_PSINTLP	VCC_PSAUX
VCC_PSINTLP	VCC_PSAUX
PS_MGTRAVCC	
PS_MGTRAVCC	
PS_MGTRAVTT	
PS_MGTRAVTT	
PS_MGTRAVTT	

XCZU7EV-1FBVB900E



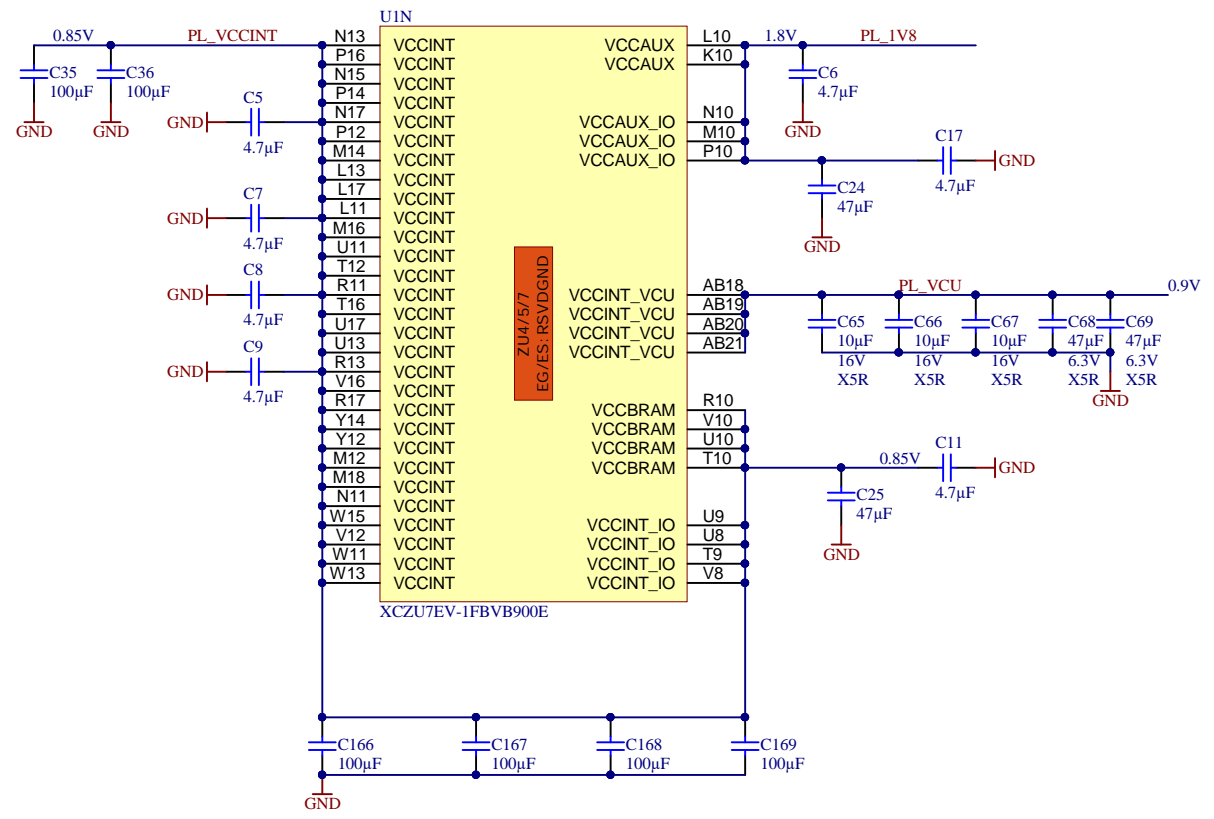
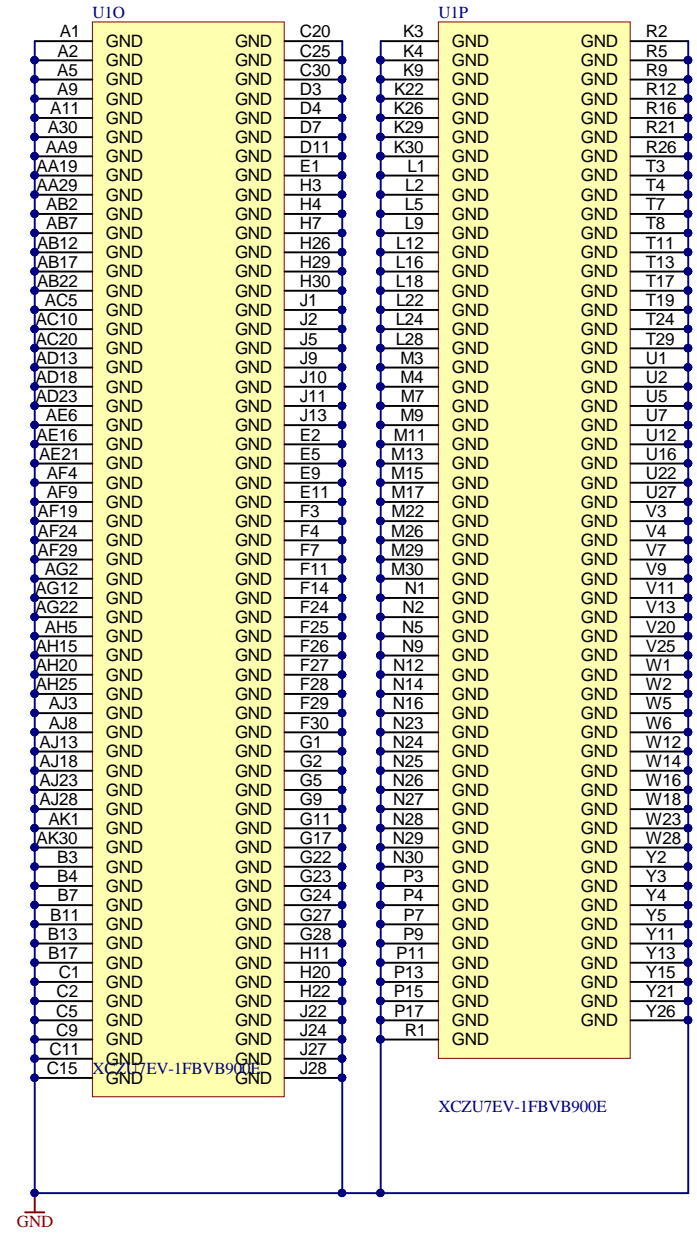

Title: TE0807 - ZU_PS_POWER		
A4	Number: TE0807 7DE21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 17 of 29
Filename: ZU_PS_POWER.SchDoc		

1

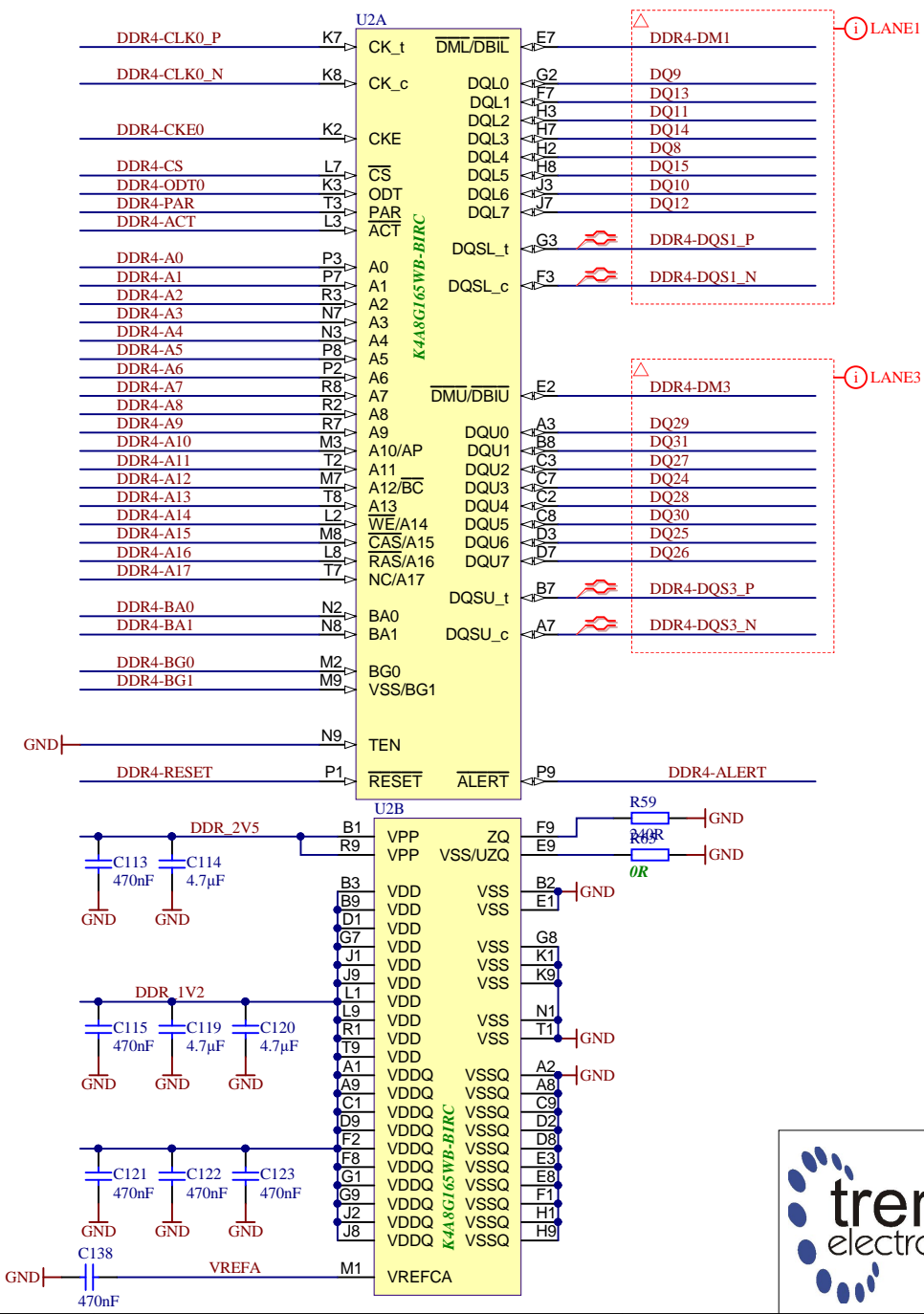
2

3

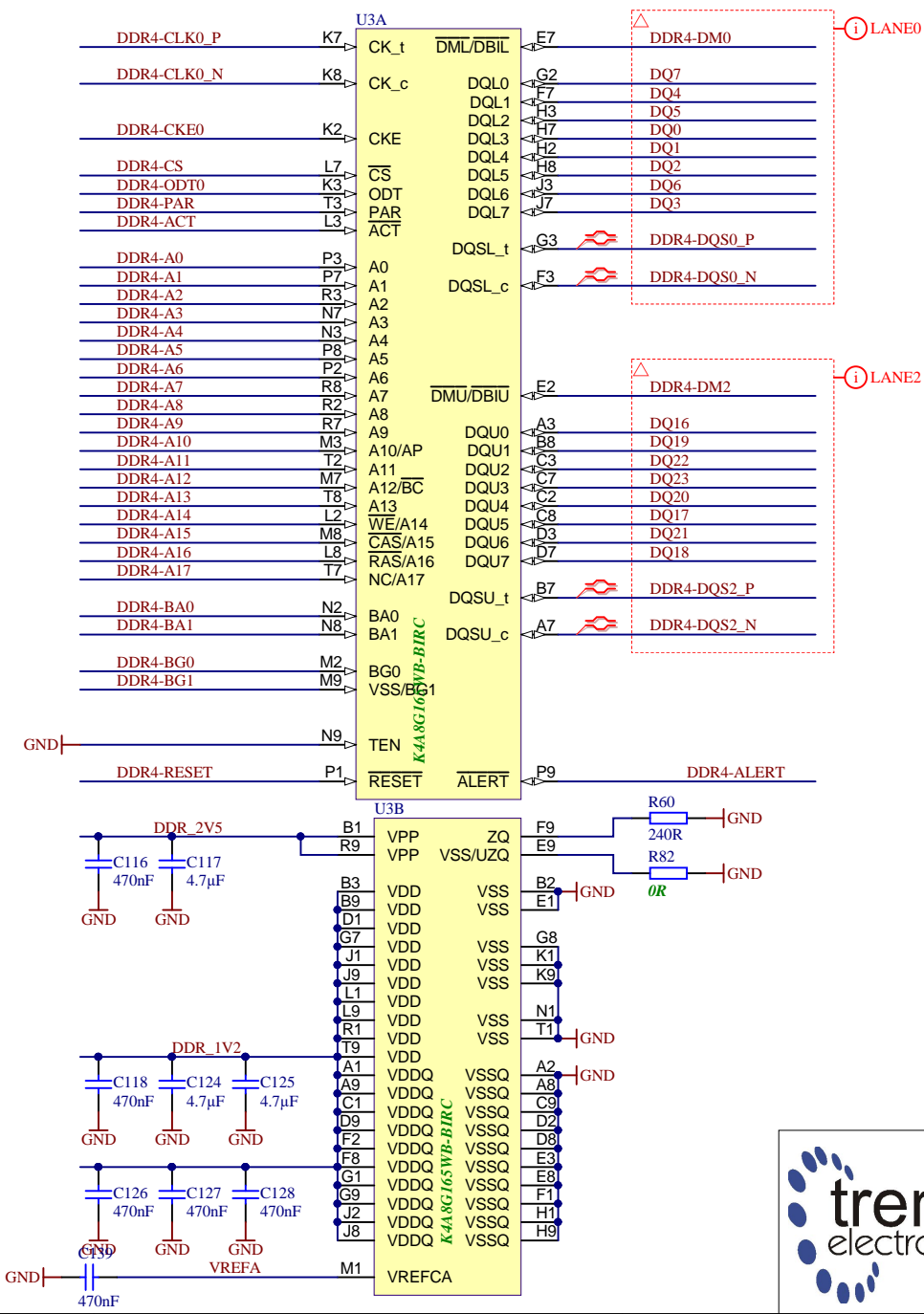

4

Title: TE0807 - ZU_POWER		
A4	Number: TE0807 7DE21-A	Rev. 03
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Title: TE0807 - DDR4_1_RAM		
A4	Number: TE0807 7DE21-A	Rev. 03
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Filename: DDR4-RAM.SchDoc		

Title: TE0807 - DDR4_2_RAM		
A4	Number: TE0807 7DE21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 20 of 29
Filename: DDR4-RAM_2.SchDoc		

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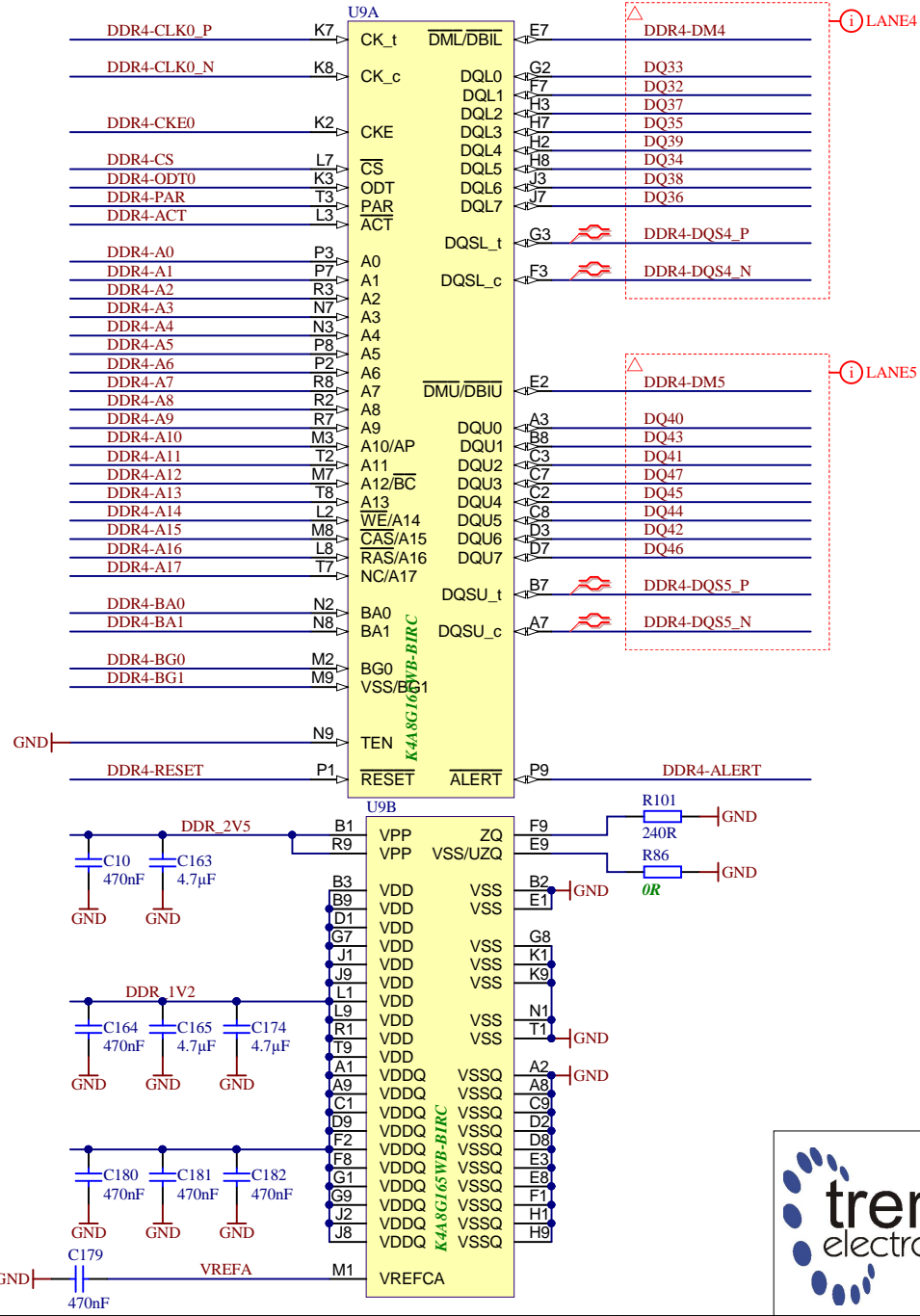
B


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			Title: TE0807 - DDR4_3_RAM	
			A4	Number: TE0807 7DE21-A
Date: 2020-05-08		Copyright: Trenz Electronic GmbH / TT		Page 21 of 29
Filename: DDR4-RAM_3.SchDoc				

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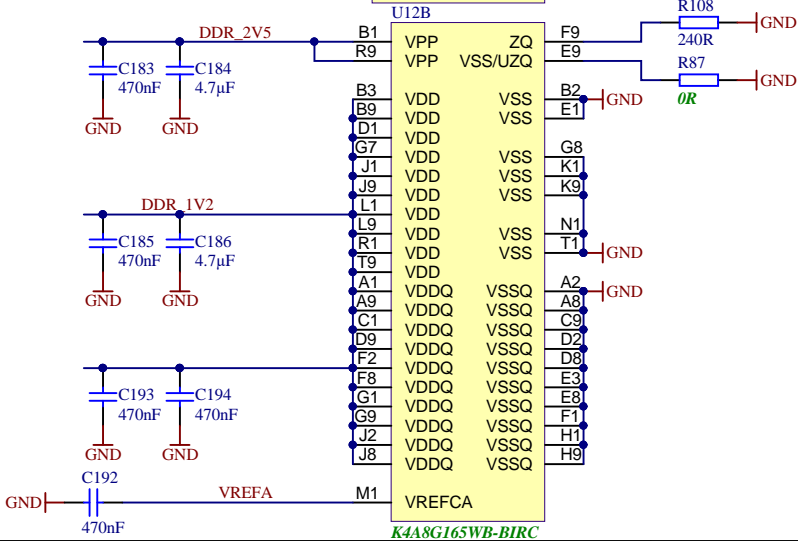
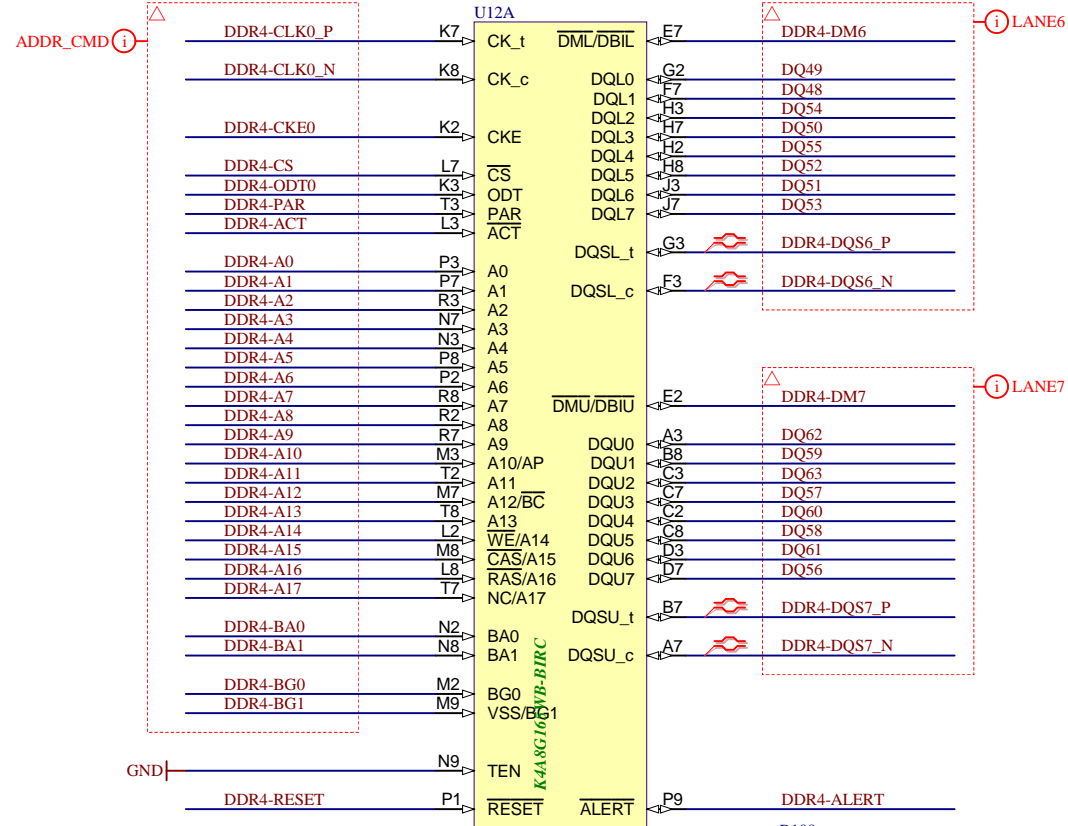
B

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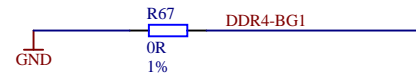
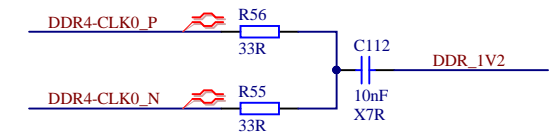
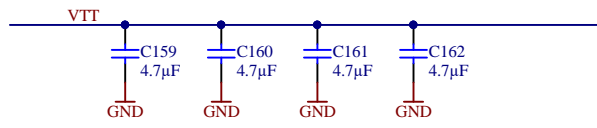
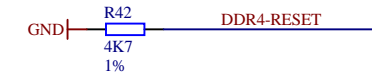
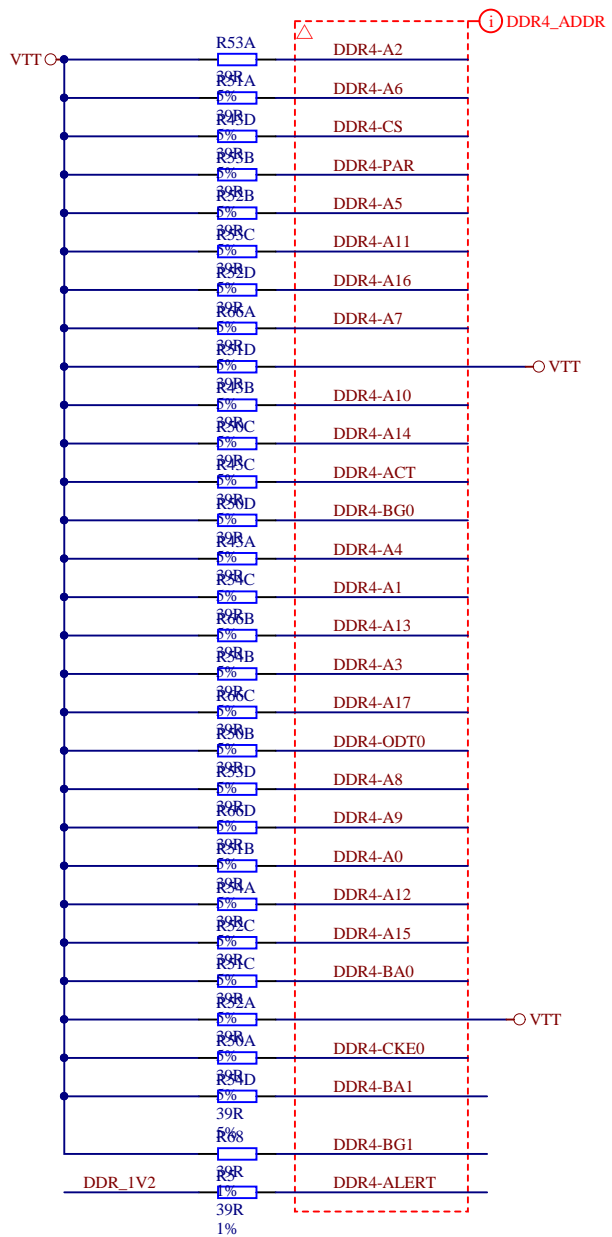
Title: TE0807 - DDR4_4_RAM		
A4	Number: TE0807 7DE21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 22 of 29
Filename: DDR4-RAM_4.SchDoc		

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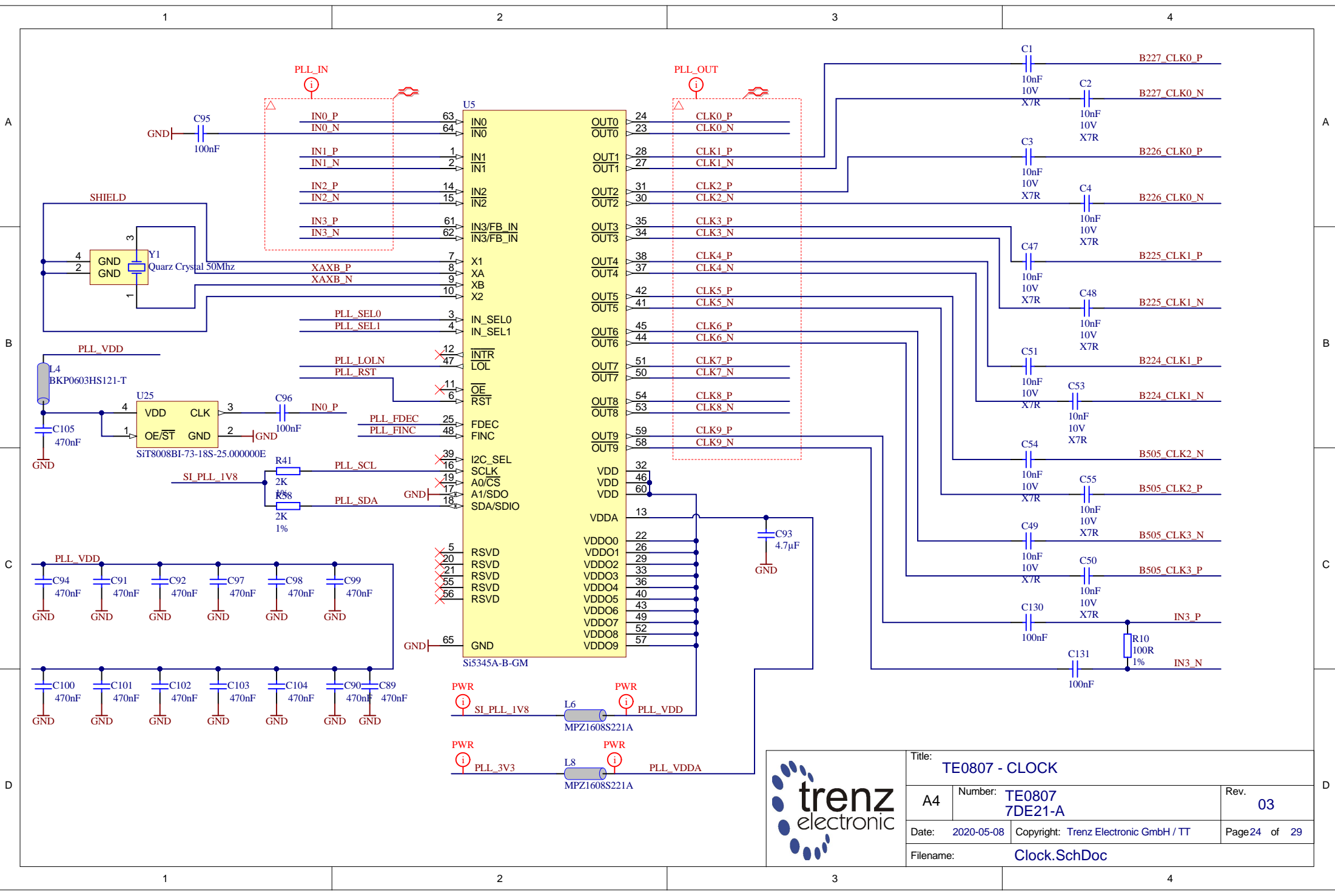
2

3

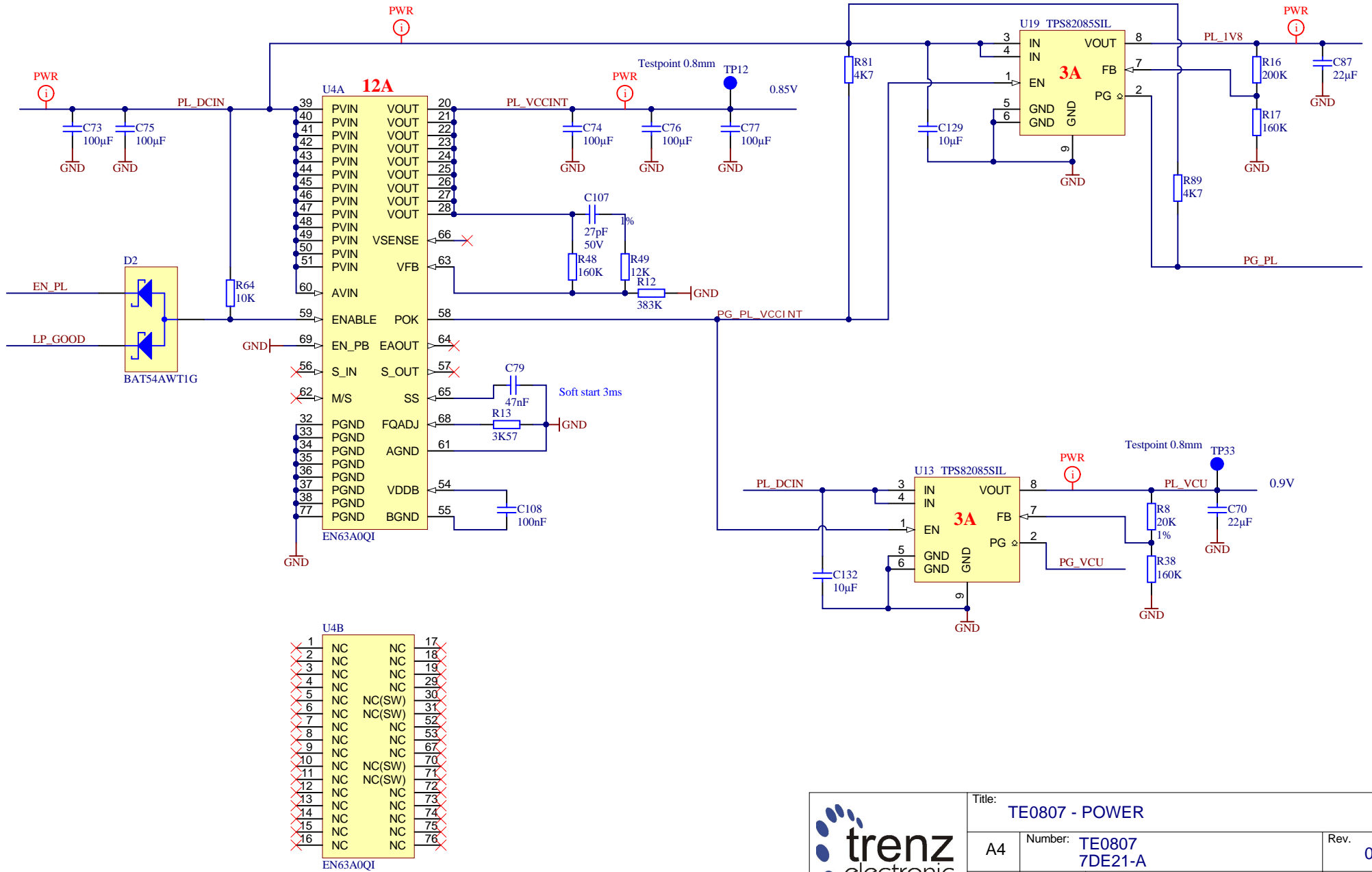
4



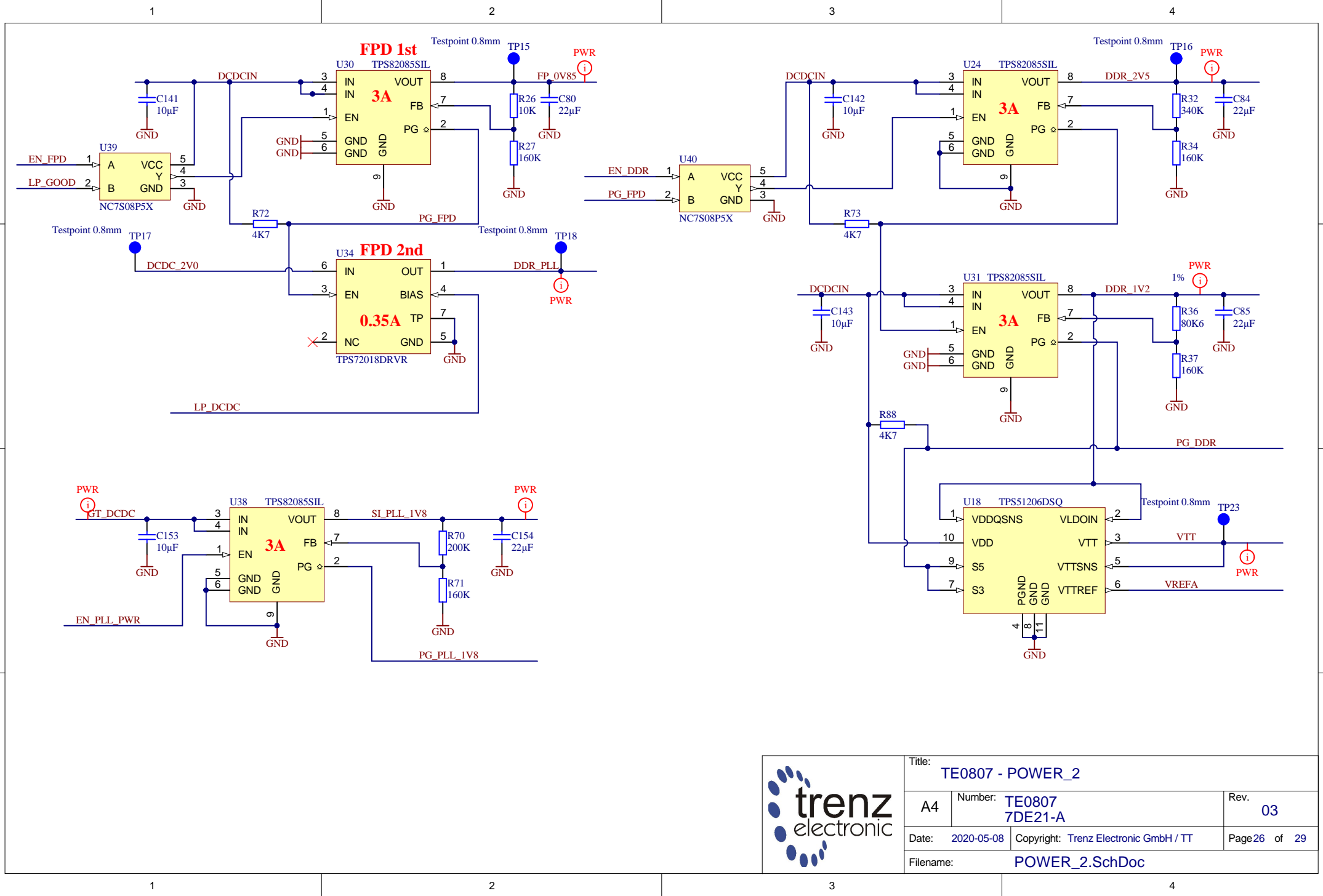
Title: TE0807 - DDR4_TERM		
A4	Number: TE0807 7DE21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 23 of 29
Filename: DDR4-TERM.SchDoc		




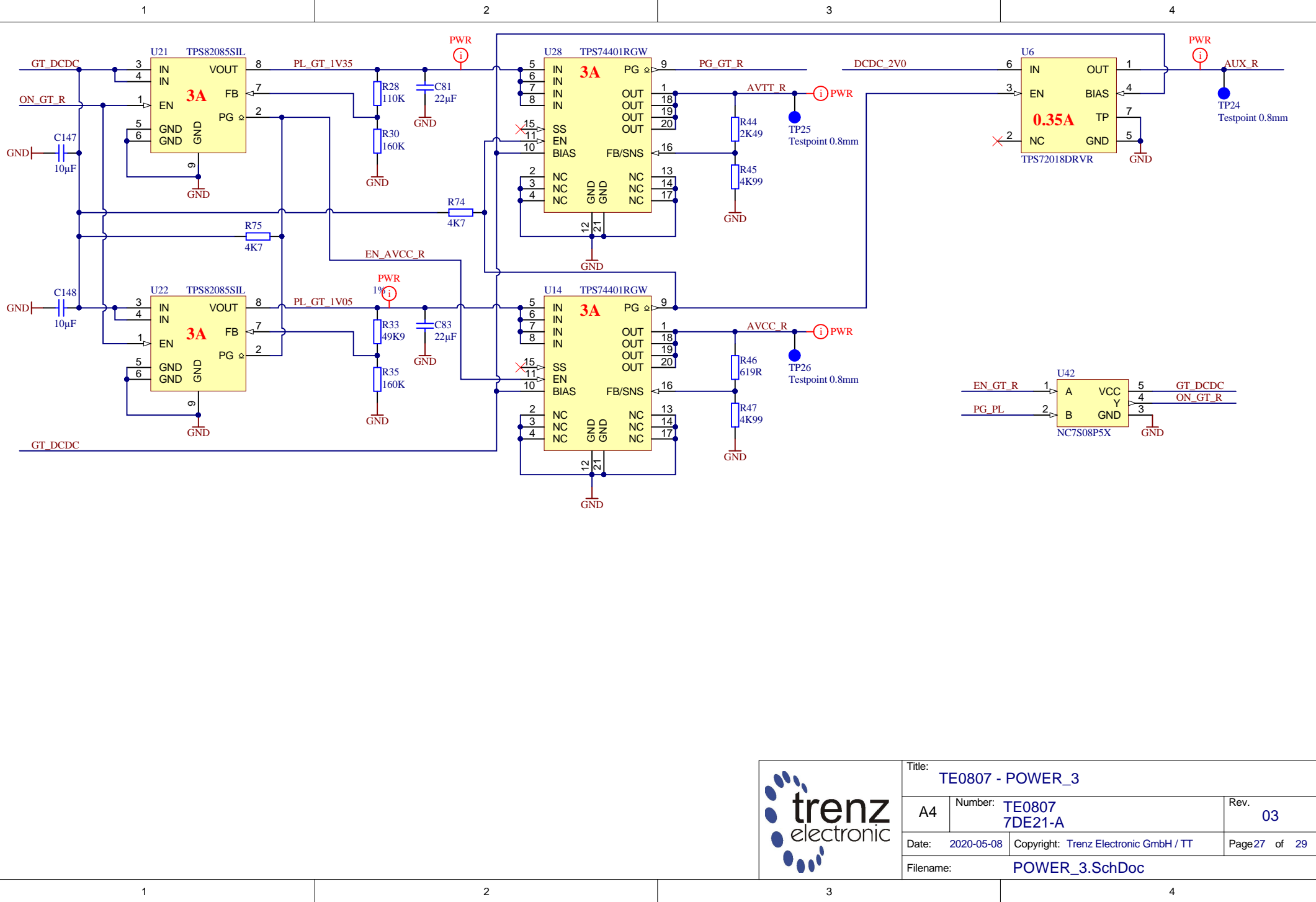
Title: TE0807 - CLOCK		
A4	Number: TE0807 7DE21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 24 of 29
Filename: Clock.SchDoc		




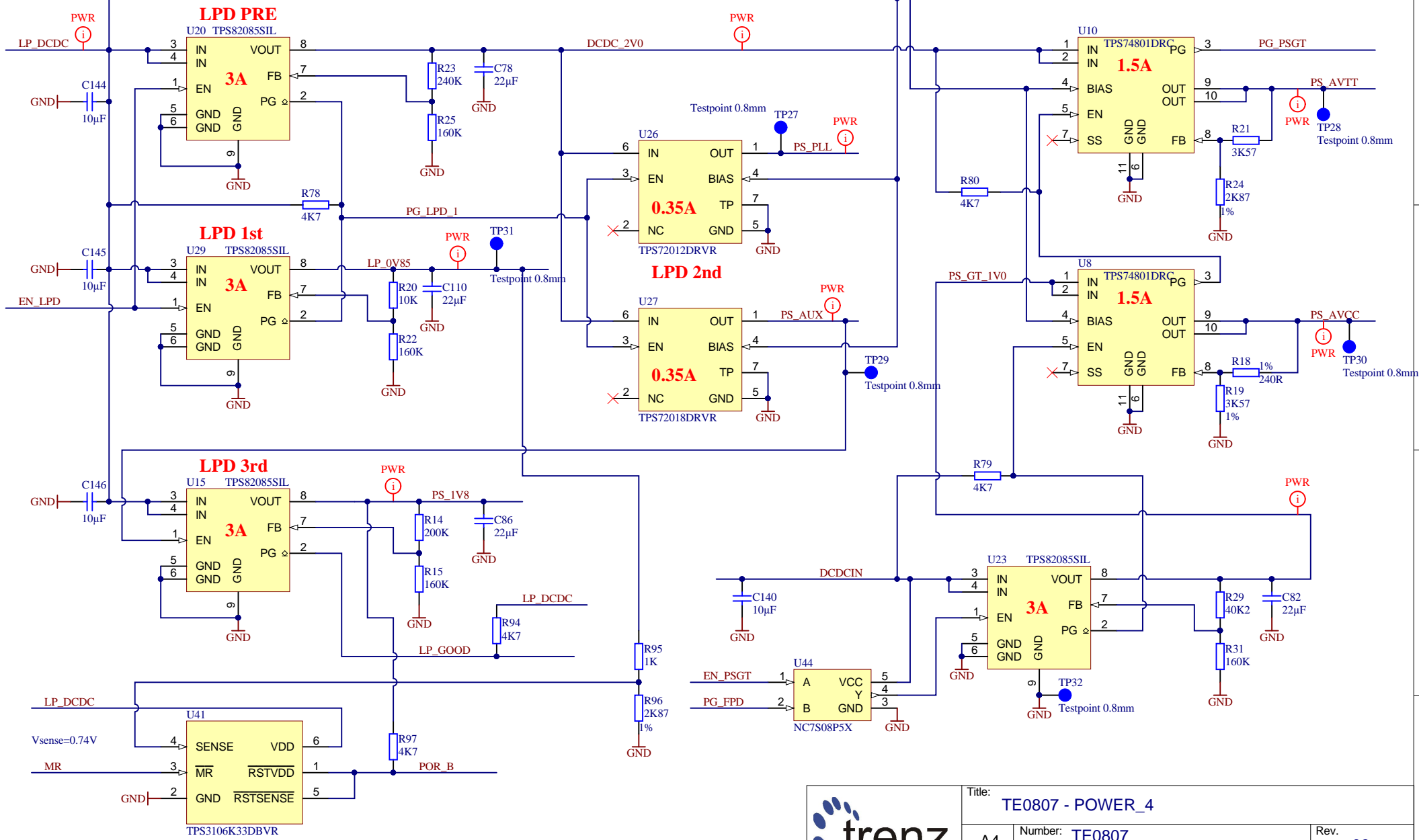
	Title: TE0807 - POWER		
	A4	Number: TE0807 7DE21-A	Rev. 03
	Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	
	Filename: POWER.SchDoc	Page 25 of 29	



		Title: TE0807 - POWER_2	
		A4	Number: TE0807 7DE21-A
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			Title: TE0807 - POWER_3	
A4	Number: TE0807 7DE21-A	Rev. 03		
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Title: TE0807 - POWER_4		
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CHANGES REV01 to REV02

- 1) Added EEPROM (U11,24AA025E48T-I/OT)
- 2) Added optional resistors R39/R40 for QSPI flash (do not populated)
- 3) Fixed VCU connection (added additional DCDC and capacitors), recommendation from Xilinx
- 4) Changed obsolete DDR4 chips (NT5AD256M16B2-GN -> K4A8G165WB-BIRC)
- 5) Added net "PG_VCU" to J2 (pin97)
- 6) full update lib

CHANGES REV02 to REV03 (06.2020)

- VT: 1) Fixed ADC connection
 2) Fixed DDR4 connection (support B-die DDR4 chips)
 3) Fixed DDR4 connection (alert_n pin connection)
 4) Added U16
 4) Added testpoints
 5) Full update LIB

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	Title: TE0807 - Changes list		
	A4	Number: TE0807 7DE21-A	Rev. 03
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	Filename: Revision_Changes.SchDoc		

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