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Schematics and other handouts serve for informational purposes only!

	Title: <b>TE0807 - Legal Notices</b>		
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J1.SchDoc

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J3.SchDoc

U\_J4  
J4.SchDoc

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DDR4-TERM.SchDoc

U\_B64  
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U\_ZU\_POWER  
ZU\_POWER.SchDoc

U\_ZU\_PS\_POWER  
ZU\_PS\_POWER.SchDoc

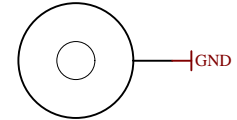
U\_POWER  
POWER.SchDoc

U\_POWER\_2  
POWER\_2.SchDoc

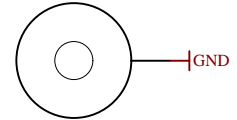
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POWER\_3.SchDoc

U\_POWER\_4  
POWER\_4.SchDoc

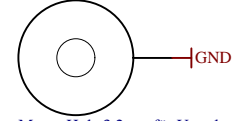
Special notes:



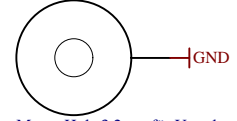
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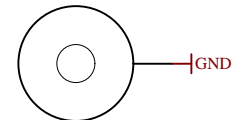
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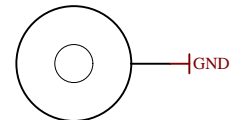
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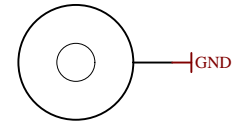
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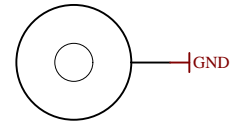
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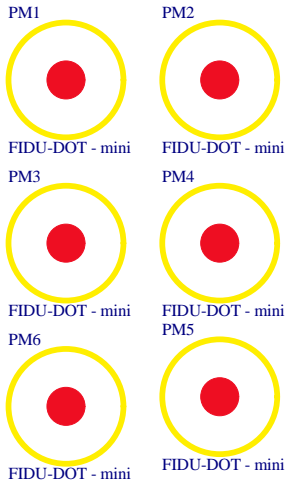
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



LOGO1  
TE Logo PRINT Layer  
LOGO PRINT

Serial  
Serialnummer 6,3 x 6.3mm

Assembly variant	7DI21-A
Created by	VT
Modified by	VT
Modified at	2020-03-23
SVN Revision	9271 [Locally Modified]



Title: TE0807		
A4	Number: TE0807 7DI21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 2 of 29
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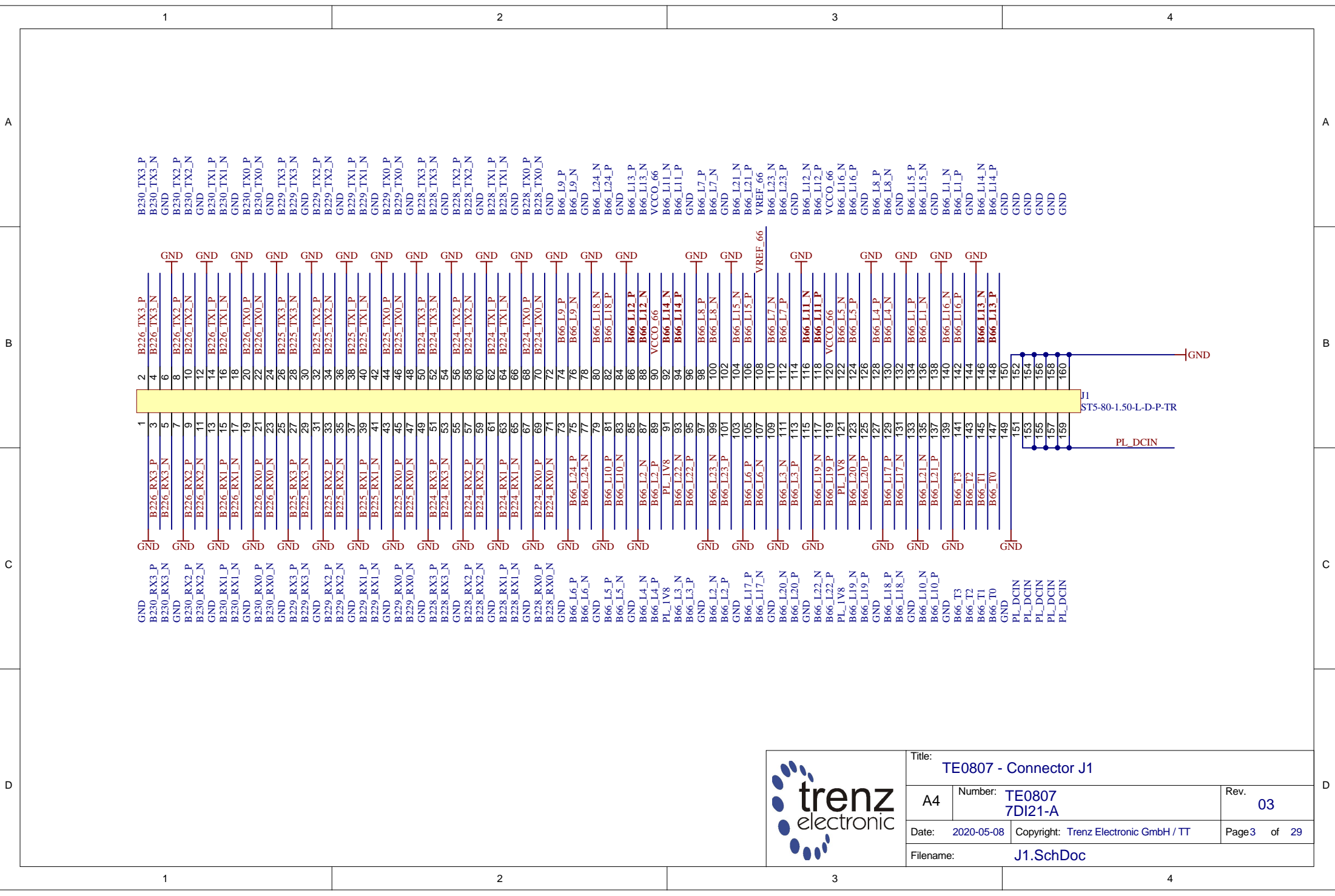

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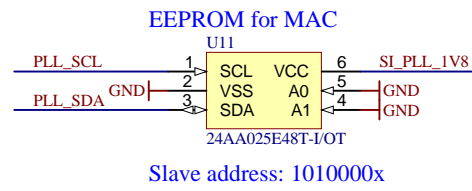
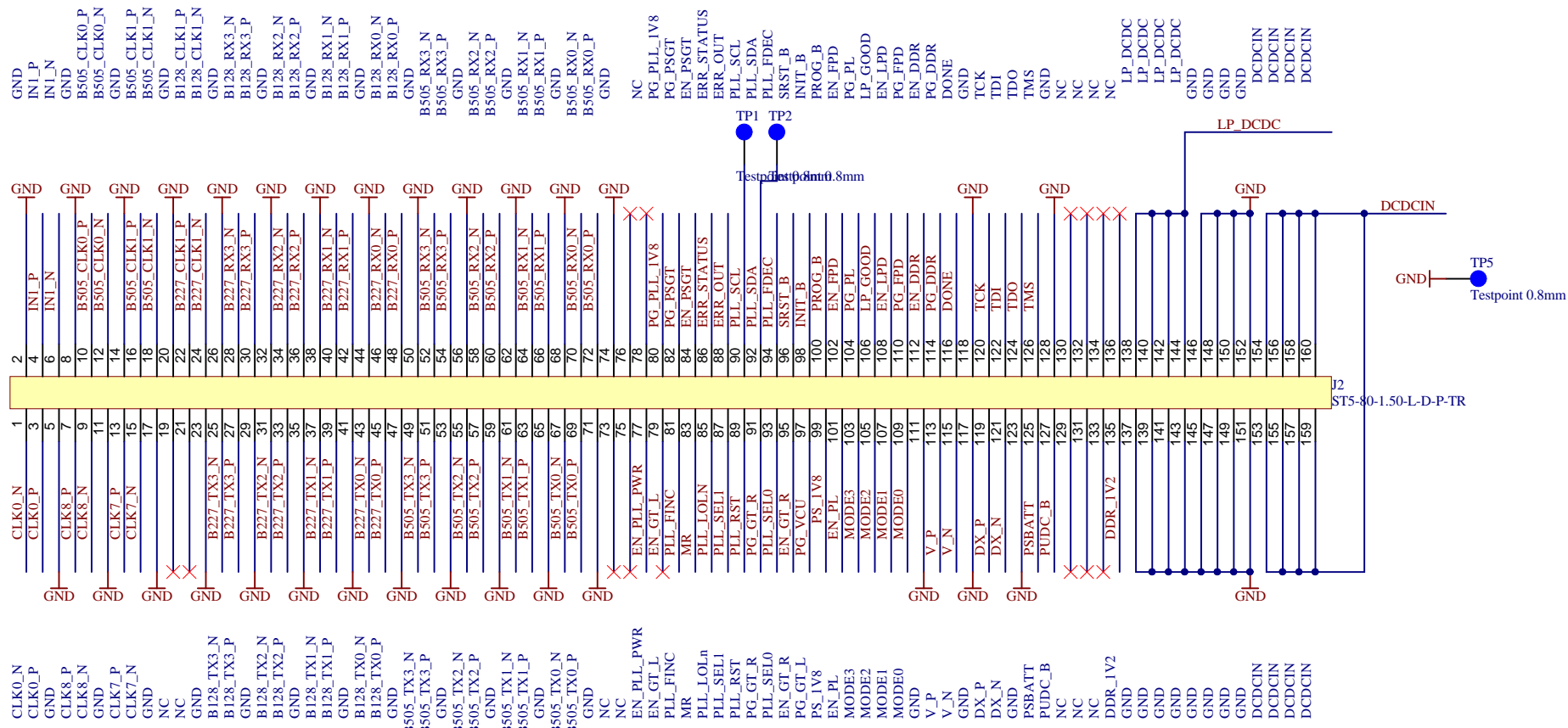
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D

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A4	Number: TE0807 7DI21-A	Rev. 03
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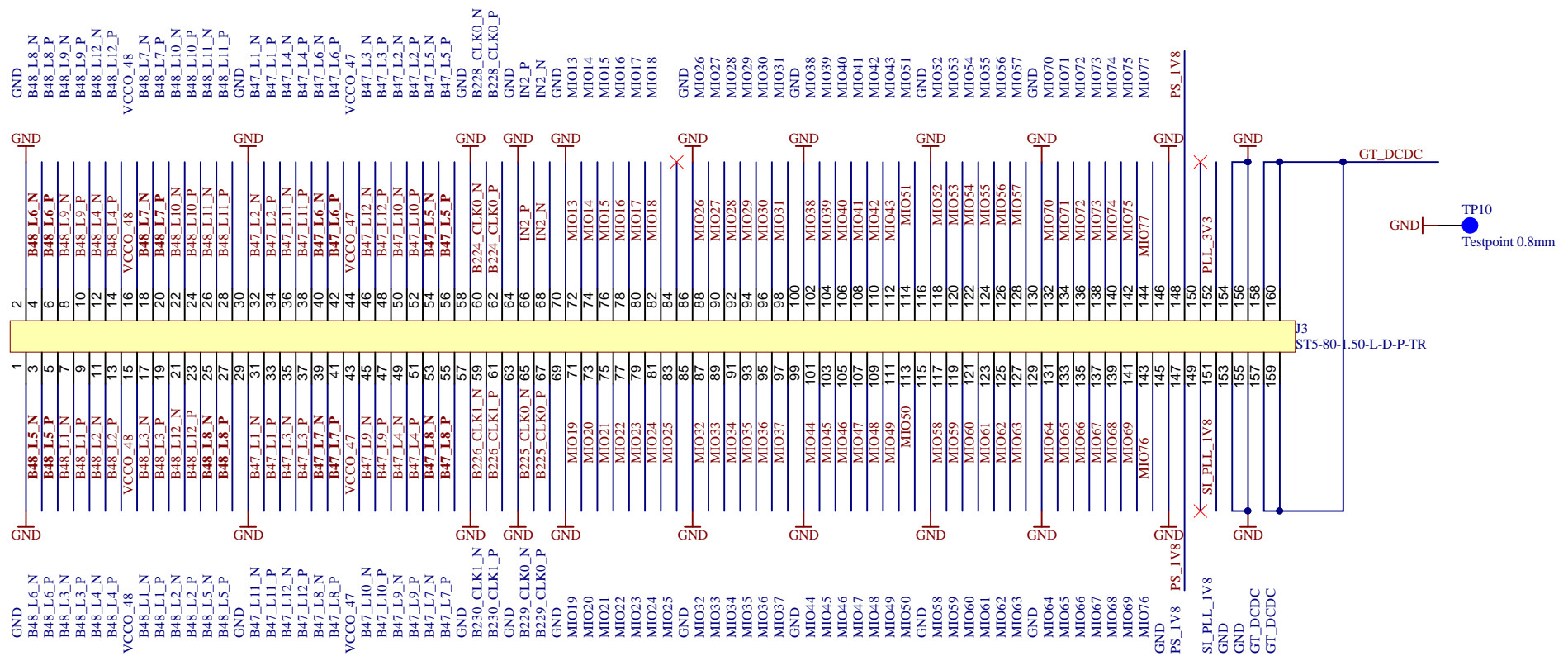
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A4	Number: TE0807 7DI21-A	Rev. 03
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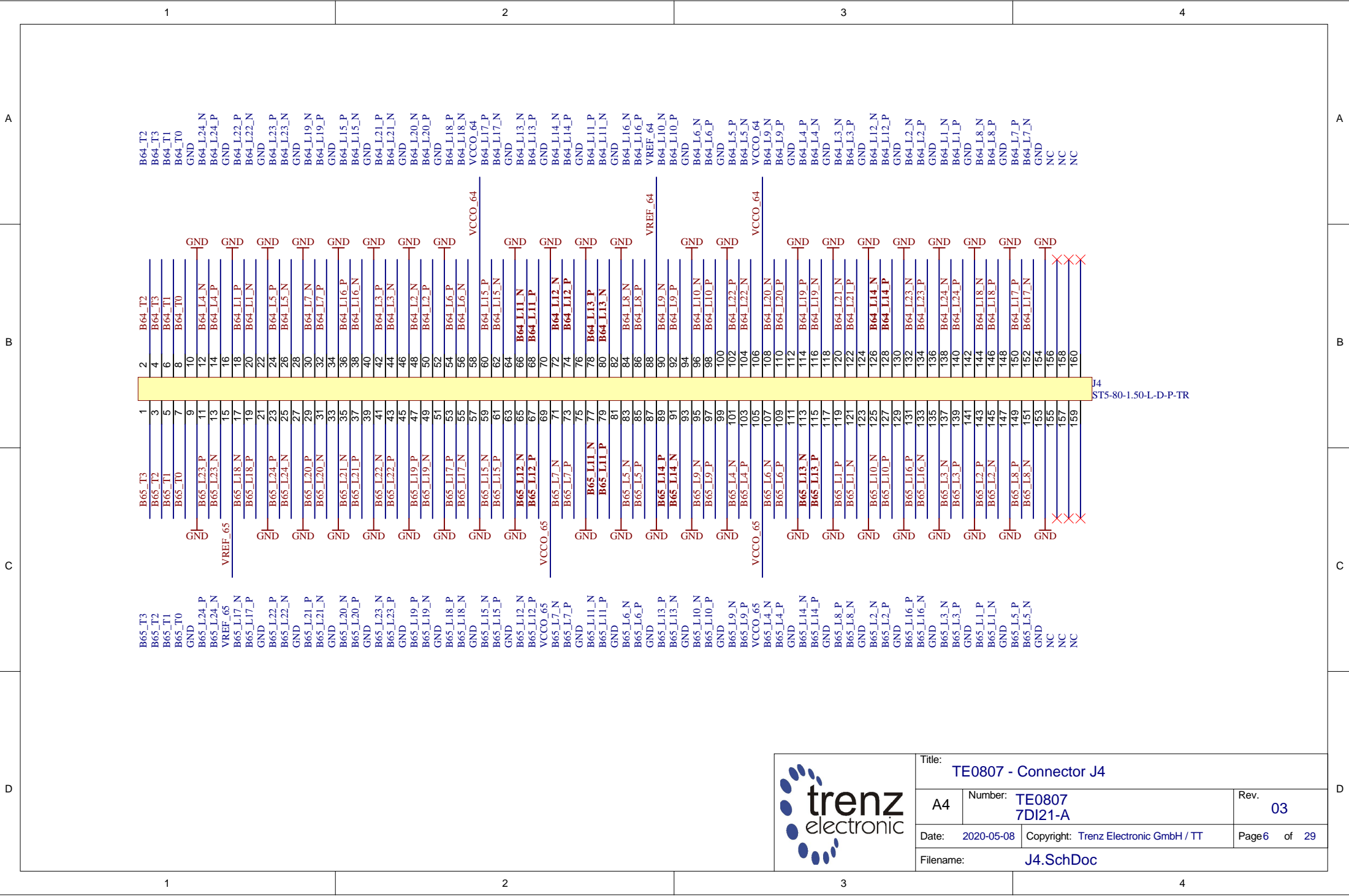
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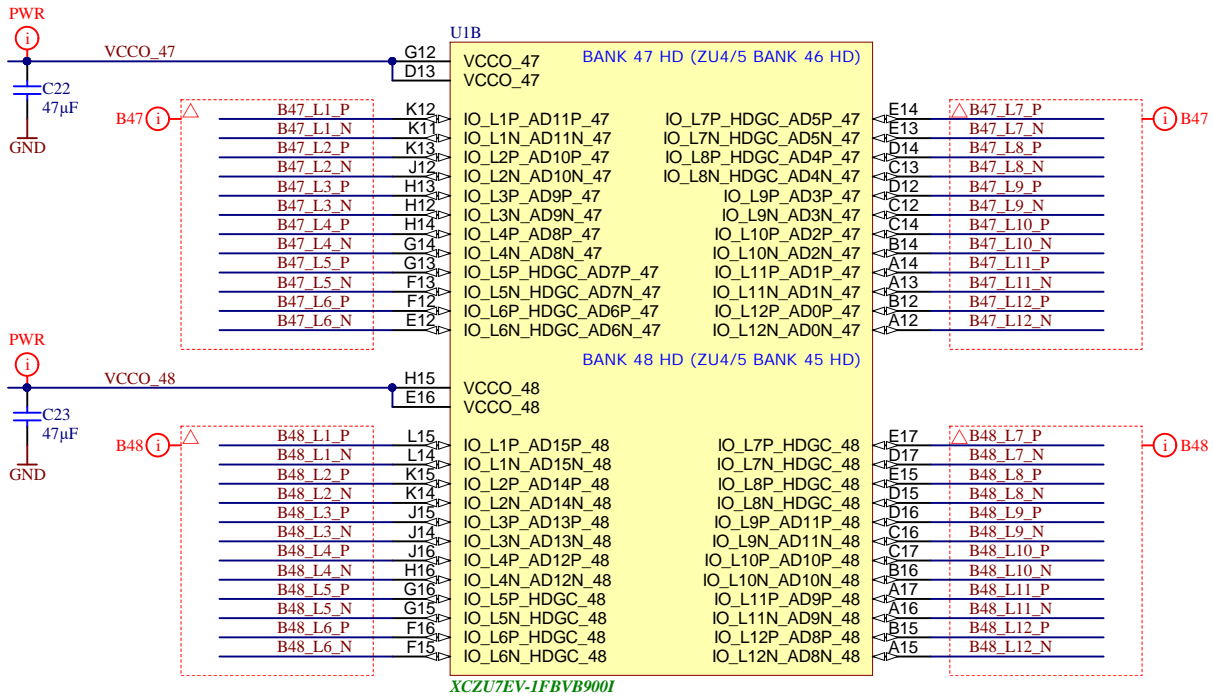
D

A  
B  
C  
D

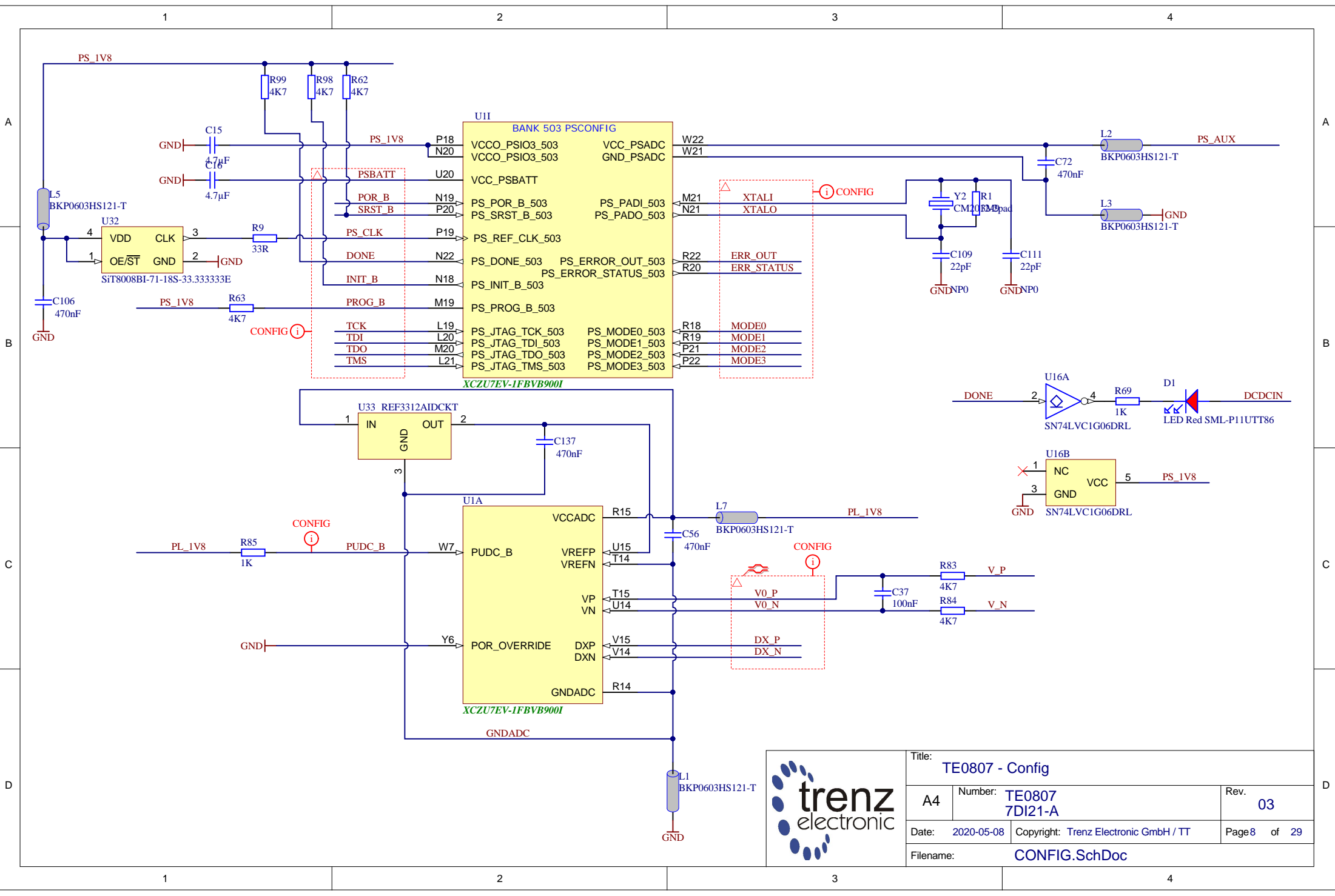



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			Title: TE0807 - Config	
			A4	Number: TE0807 7DI21-A
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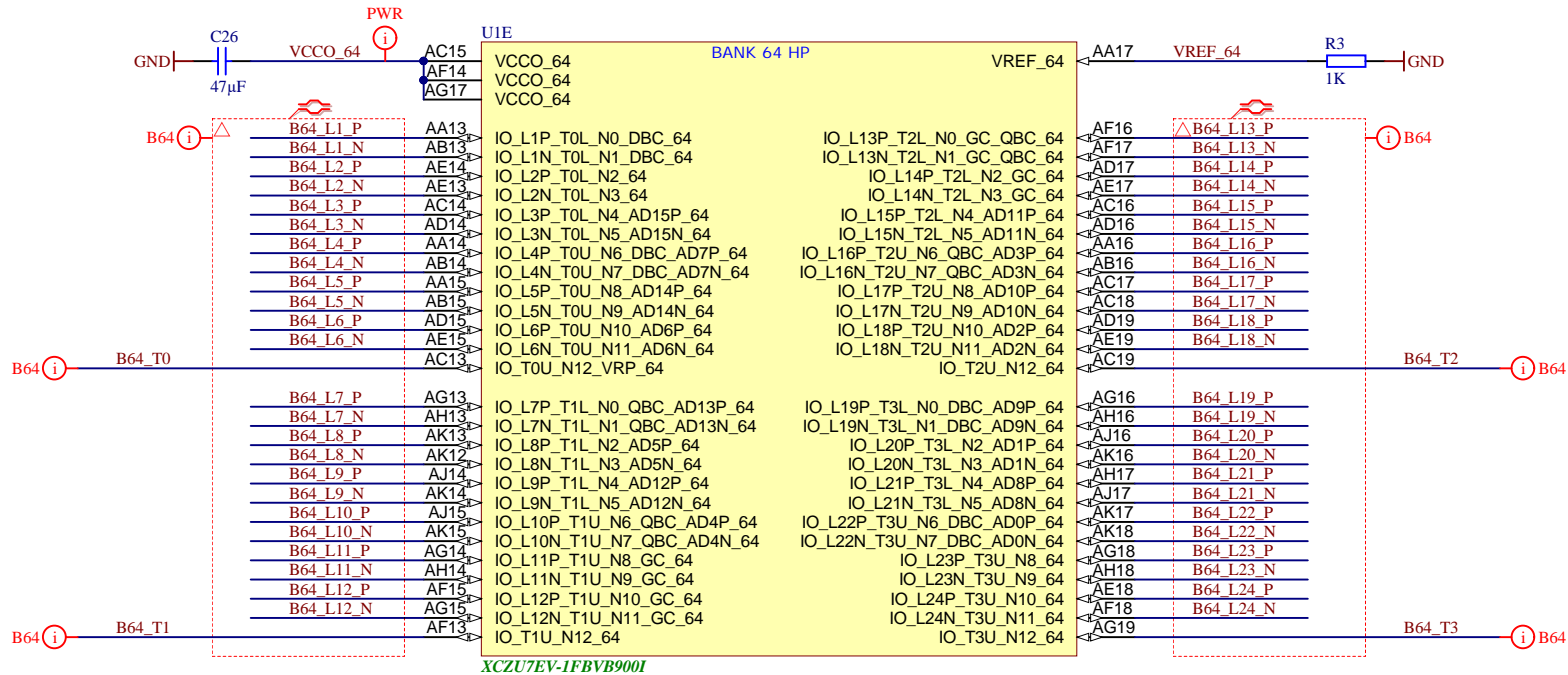
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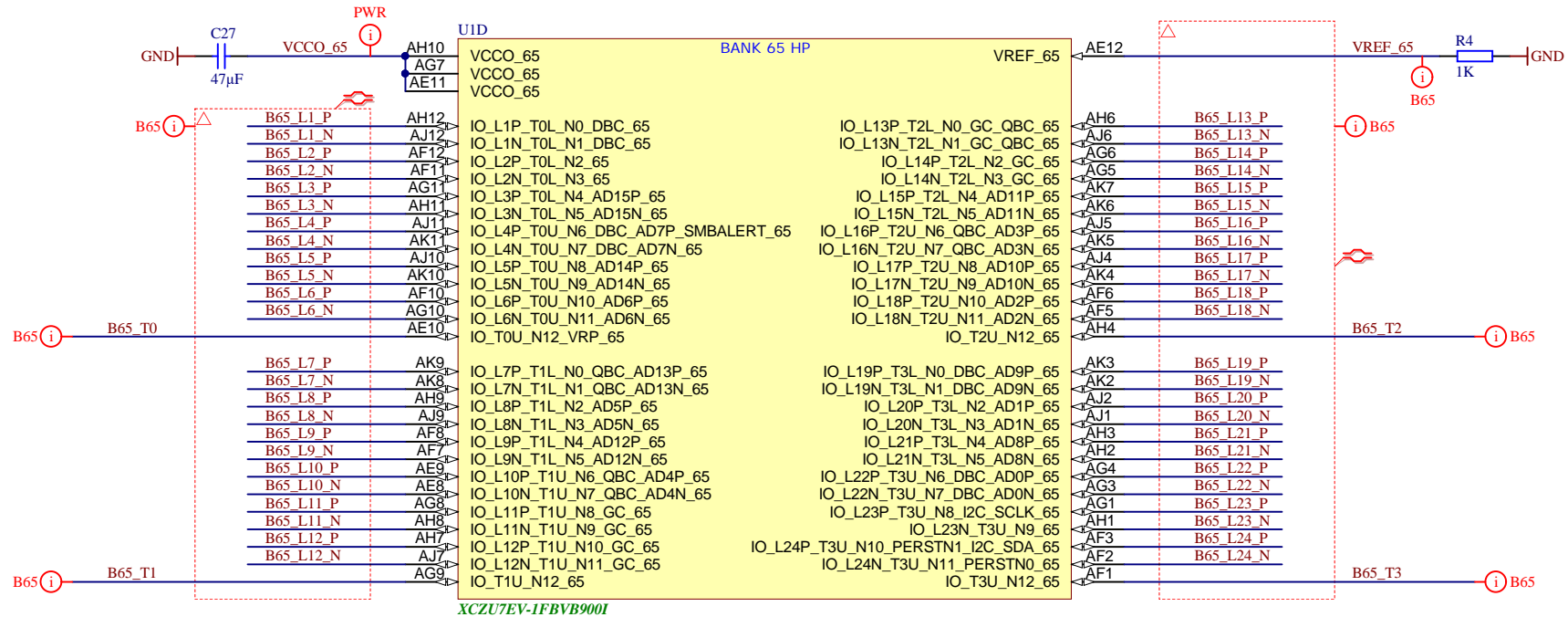
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	A4	Number: <b>TE0807 7DI21-A</b>	Rev. <b>03</b>
	Date: <b>2020-05-08</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>9</b> of <b>29</b>
	Filename: <b>B64.SchDoc</b>		

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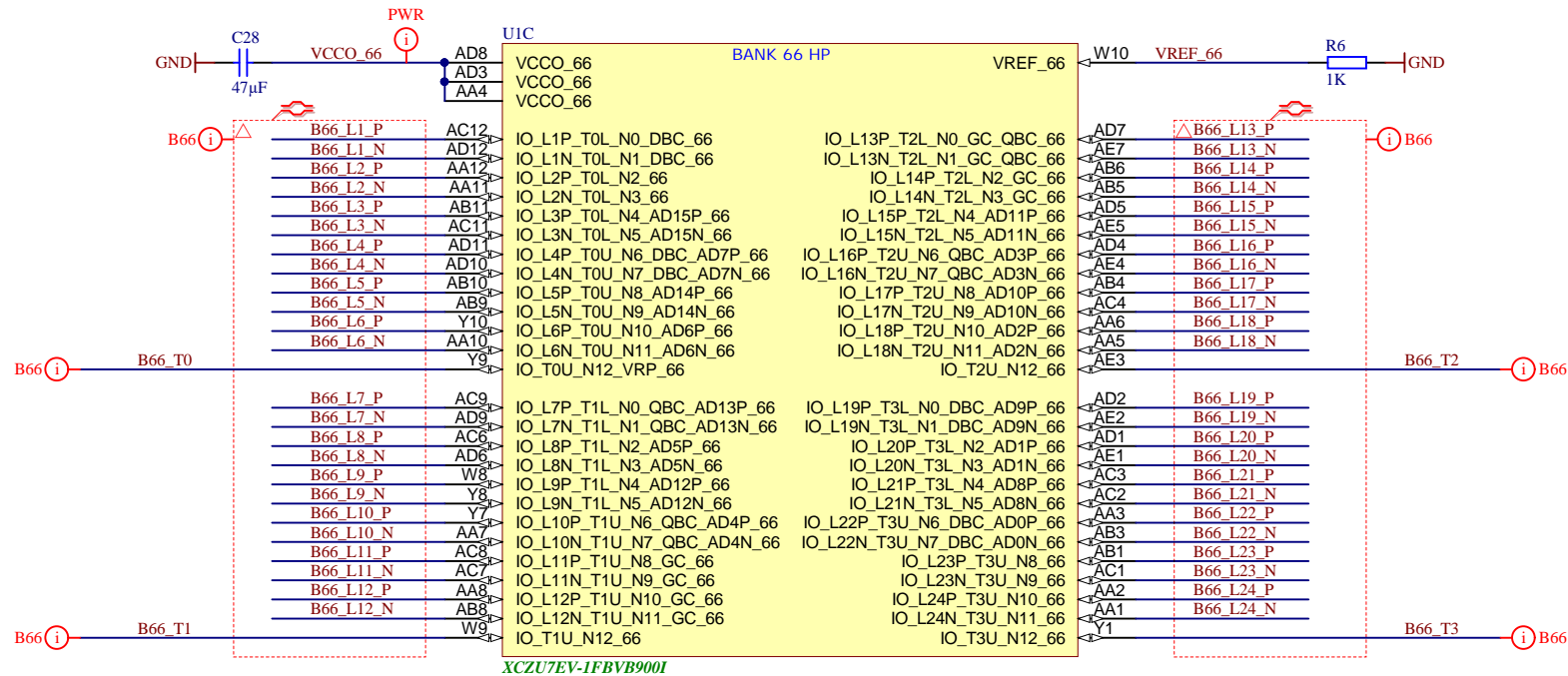

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Date: <b>2020-05-08</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>10</b> of <b>29</b>
Filename: <b>B65.SchDoc</b>		

Title: <b>TE0807 - B66</b>		
A4	Number: <b>TE0807 7DI21-A</b>	Rev. <b>03</b>
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Filename: <b>B66.SchDoc</b>		

A

A

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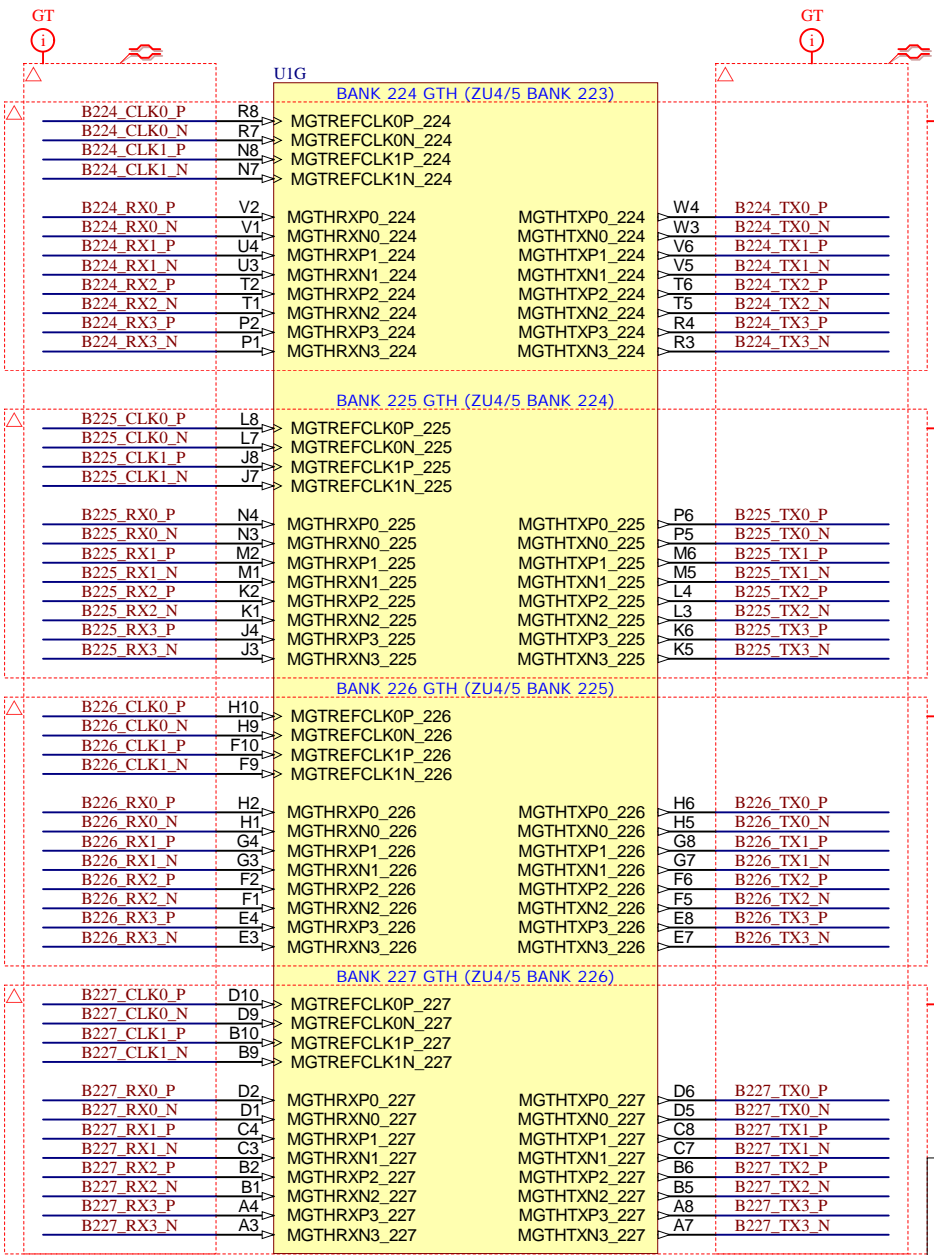
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C

D

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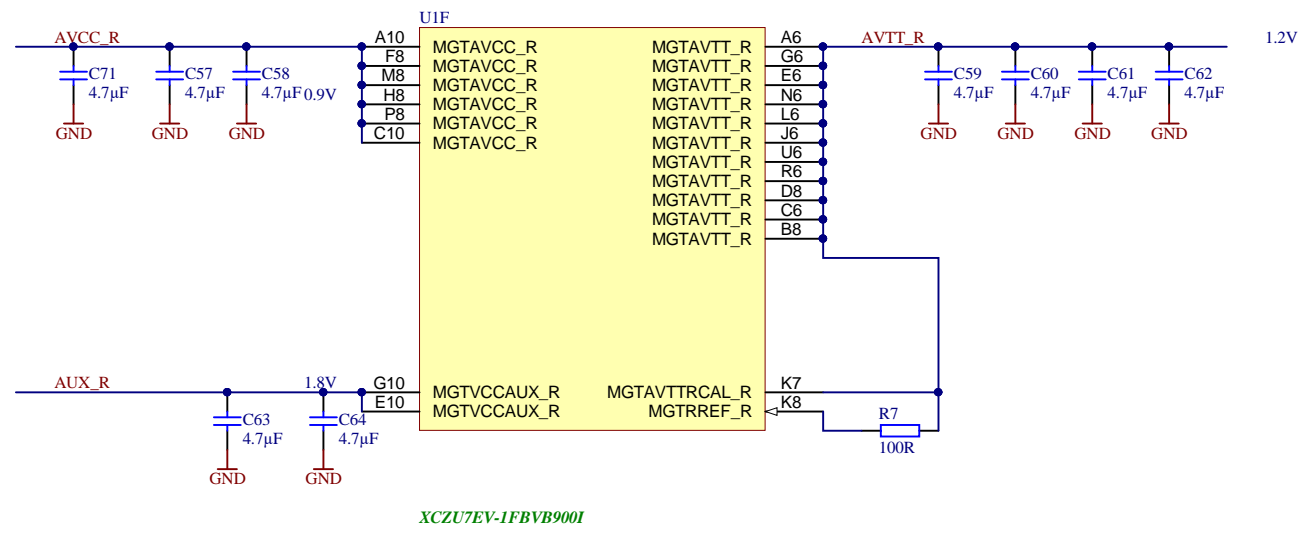
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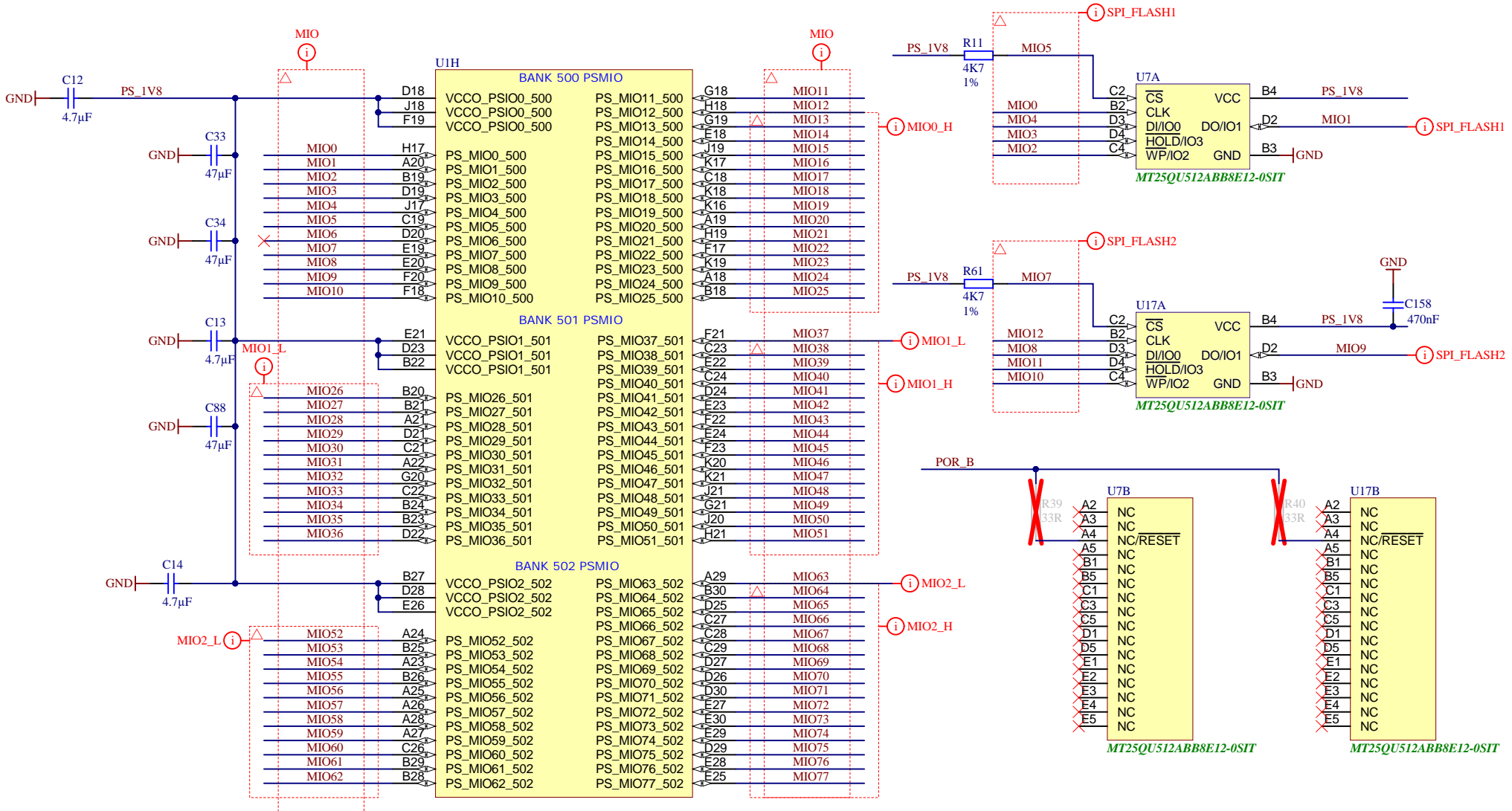


Title: TE0807 - GTH_Banks		
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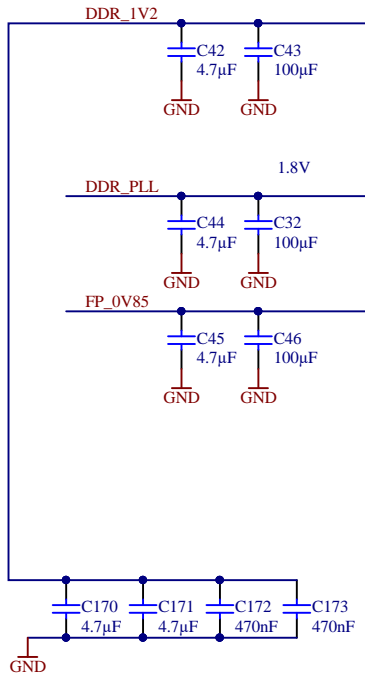
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	Title: TE0807 - GTH_PWR		
	A4	Number: TE0807 7DI21-A	Rev. 03
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		Title: TE0807 - MIO Banks	
		A4	Number: TE0807 7DI21-A
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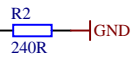


**UIJ**

**BANK 504 PSDDR**

VCCO_PSDDR_504	PS_DDR_CK0_504	AE30	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	AF30	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0_504	AC30	DDR4-CKE0
VCCO_PSDDR_504		AF28	
VCCO_PSDDR_504	PS_DDR_CK1_504	AG28	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	AB28	
VCCO_PSDDR_504	PS_DDR_CKE1_504		
VCC_PSDDR_PLL	PS_DDR_A0_504	AH30	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	AG30	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AK29	DDR4-A2
VCC_PSDDR_PLL	PS_DDR_A3_504	AJ30	DDR4-A3
VCC_PSDDR_PLL	PS_DDR_A4_504	AK28	DDR4-A4
VCC_PSDDR_PLL	PS_DDR_A5_504	AK27	DDR4-A5
VCC_PSDDR_PLL	PS_DDR_A6_504	AF27	DDR4-A6
VCC_PSDDR_PLL	PS_DDR_A7_504	AE27	DDR4-A7
VCC_PSDDR_PLL	PS_DDR_A8_504	AF26	DDR4-A8
VCC_PSDDR_PLL	PS_DDR_A9_504	AG26	DDR4-A9
VCC_PSDDR_PLL	PS_DDR_A10_504	AE29	DDR4-A10
VCC_PSDDR_PLL	PS_DDR_A11_504	AE28	DDR4-A11
VCC_PSDDR_PLL	PS_DDR_A12_504	AH29	DDR4-A12
VCC_PSDDR_PLL	PS_DDR_A13_504	AG29	DDR4-A13
VCC_PSDDR_PLL	PS_DDR_A14_504	AJ29	DDR4-A14
VCC_PSDDR_PLL	PS_DDR_A15_504	AH27	DDR4-A15
VCC_PSDDR_PLL	PS_DDR_A16_504	AJ27	DDR4-A16
VCC_PSDDR_PLL	PS_DDR_A17_504		
VCC_PSINTFF_DDR	PS_DDR_CS_N0_504	AD30	DDR4-CS
VCC_PSINTFF_DDR	PS_DDR_CS_N1_504	AD29	
VCC_PSINTFF_DDR	PS_DDR_BA0_504	AD27	DDR4-BA0
VCC_PSINTFF_DDR	PS_DDR_BA1_504	AC26	DDR4-BA1
VCC_PSINTFF_DDR	PS_DDR_BG0_504	AC28	DDR4-BG0
VCC_PSINTFF_DDR	PS_DDR_BG1_504	AC27	DDR4-BG1
VCC_PSINTFF_DDR	PS_DDR_PARITY_504	AB26	DDR4-PAR
VCC_PSINTFF_DDR	PS_DDR_RAM_RST_N_504	AB25	DDR4-RESET
VCC_PSINTFF_DDR	PS_DDR_ACT_N_504	AD26	DDR4-ACT
VCC_PSINTFF_DDR	PS_DDR_ALERT_N_504	AB24	DDR4-ALERT
VCC_PSINTFF_DDR	PS_DDR_ZQ_504	AB23	
VCC_PSINTFF_DDR	PS_DDR_ODT0_504	AB30	DDR4-ODT0
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**UIK**

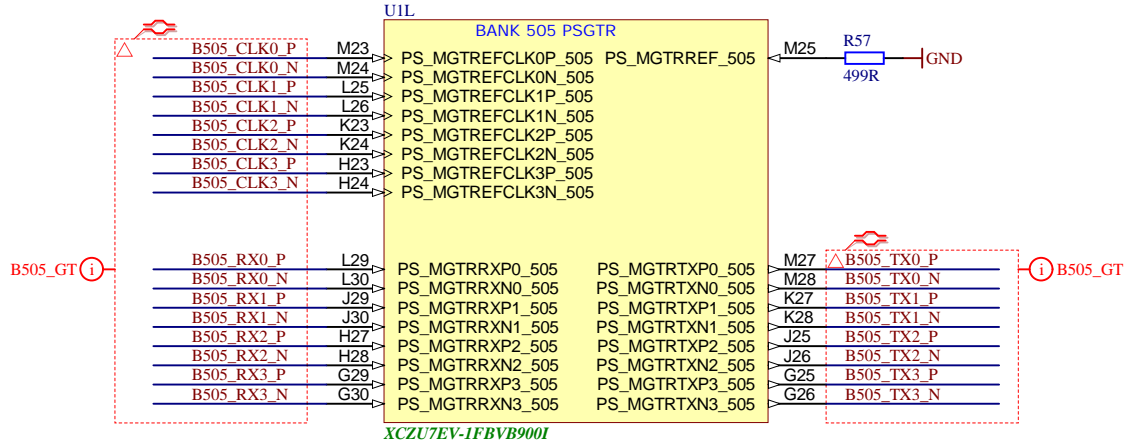
**BANK 504 PSDDR**

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DQ1	AH21	PS_DDR_DQ1_504	PS_DDR_DQ33_504	V23	DQ33
DQ2	AJ22	PS_DDR_DQ2_504	PS_DDR_DQ34_504	U25	DQ34
DQ3	AK22	PS_DDR_DQ3_504	PS_DDR_DQ35_504	V24	DQ35
DQ4	AK20	PS_DDR_DQ4_504	PS_DDR_DQ36_504	Y25	DQ36
DQ5	AJ19	PS_DDR_DQ5_504	PS_DDR_DQ37_504	AA23	DQ37
DQ6	AK19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	AA25	DQ38
DQ7	AH19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	Y23	DQ39
DQ8	AH23	PS_DDR_DQ8_504	PS_DDR_DQ40_504	P23	DQ40
DQ9	AK23	PS_DDR_DQ9_504	PS_DDR_DQ41_504	R23	DQ41
DQ10	AG24	PS_DDR_DQ10_504	PS_DDR_DQ42_504	T23	DQ42
DQ11	AK24	PS_DDR_DQ11_504	PS_DDR_DQ43_504	P26	DQ43
DQ12	AJ26	PS_DDR_DQ12_504	PS_DDR_DQ44_504	T25	DQ44
DQ13	AK25	PS_DDR_DQ13_504	PS_DDR_DQ45_504	U23	DQ45
DQ14	AG25	PS_DDR_DQ14_504	PS_DDR_DQ46_504	T26	DQ46
DQ15	AH26	PS_DDR_DQ15_504	PS_DDR_DQ47_504	P24	DQ47
DQ16	AD22	PS_DDR_DQ16_504	PS_DDR_DQ48_504	U26	DQ48
DQ17	AE22	PS_DDR_DQ17_504	PS_DDR_DQ49_504	U26	DQ49
DQ18	AF22	PS_DDR_DQ18_504	PS_DDR_DQ50_504	U28	DQ50
DQ19	AG21	PS_DDR_DQ19_504	PS_DDR_DQ51_504	V27	DQ51
DQ20	AD20	PS_DDR_DQ20_504	PS_DDR_DQ52_504	U30	DQ52
DQ21	AF20	PS_DDR_DQ21_504	PS_DDR_DQ53_504	V30	DQ53
DQ22	AE20	PS_DDR_DQ22_504	PS_DDR_DQ54_504	W30	DQ54
DQ23	AG20	PS_DDR_DQ23_504	PS_DDR_DQ55_504	W29	DQ55
DQ24	AG23	PS_DDR_DQ24_504	PS_DDR_DQ56_504	R30	DQ56
DQ25	AF23	PS_DDR_DQ25_504	PS_DDR_DQ57_504	T30	DQ57
DQ26	AF25	PS_DDR_DQ26_504	PS_DDR_DQ58_504	P30	DQ58
DQ27	AE23	PS_DDR_DQ27_504	PS_DDR_DQ59_504	P29	DQ59
DQ28	AC22	PS_DDR_DQ28_504	PS_DDR_DQ60_504	T28	DQ60
DQ29	AC23	PS_DDR_DQ29_504	PS_DDR_DQ61_504	T27	DQ61
DQ30	AD25	PS_DDR_DQ30_504	PS_DDR_DQ62_504	P27	DQ62
DQ31	AC24	PS_DDR_DQ31_504	PS_DDR_DQ63_504	R27	DQ63
		PS_DDR_DQ64_504	PS_DDR_DQ64_504	AB29	
		PS_DDR_DQ65_504	PS_DDR_DQ65_504	AA30	
DDR4-DQS0_P	AJ21	PS_DDR_DQS_P0_504	PS_DDR_DQ66_504	Y30	
DDR4-DQS0_N	AK21	PS_DDR_DQS_N0_504	PS_DDR_DQ67_504	Y29	
DDR4-DQS1_P	AH24	PS_DDR_DQS_P1_504	PS_DDR_DQ68_504	AA26	
DDR4-DQS1_N	AJ24	PS_DDR_DQS_N1_504	PS_DDR_DQ69_504	W27	
DDR4-DQS2_P	AC21	PS_DDR_DQS_P2_504	PS_DDR_DQ70_504	Y27	
DDR4-DQS2_N	AD21	PS_DDR_DQS_N2_504	PS_DDR_DQ71_504	W26	
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DDR4-DQS5_P	P25	PS_DDR_DQS_P5_504	PS_DDR_DM1_504	AJ25	DDR4-DM1
DDR4-DQS5_N	R25	PS_DDR_DQS_N5_504	PS_DDR_DM2_504	AF21	DDR4-DM2
DDR4-DQS6_P	U29	PS_DDR_DQS_P6_504	PS_DDR_DM3_504	AE25	DDR4-DM3
DDR4-DQS6_N	V29	PS_DDR_DQS_N6_504	PS_DDR_DM4_504	Y24	DDR4-DM4
DDR4-DQS7_P	R28	PS_DDR_DQS_P7_504	PS_DDR_DM5_504	R24	DDR4-DM5
DDR4-DQS7_N	R29	PS_DDR_DQS_N7_504	PS_DDR_DM6_504	V28	DDR4-DM6
	Y28	PS_DDR_DQS_P8_504	PS_DDR_DM7_504	P28	DDR4-DM7
	AA28	PS_DDR_DQS_N8_504	PS_DDR_DM8_504	AA27	

*XCZU7EV-1FBVB900I*



Title: <b>TE0807 - PS_DDR</b>		
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Date: <b>2020-05-08</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>15</b> of <b>29</b>
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A

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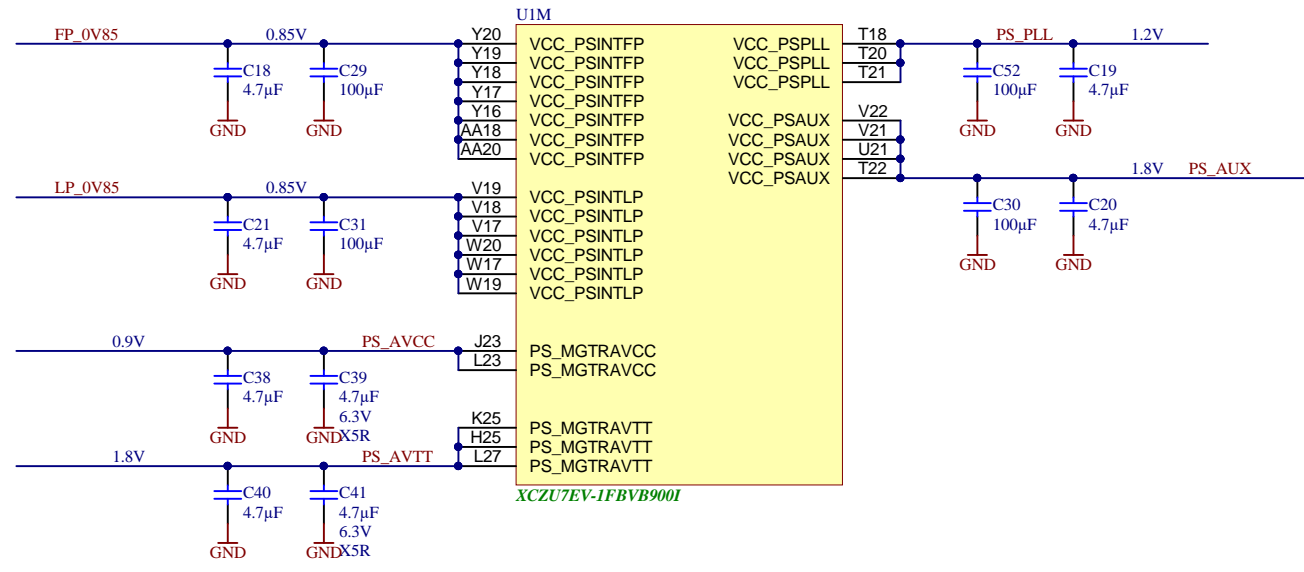
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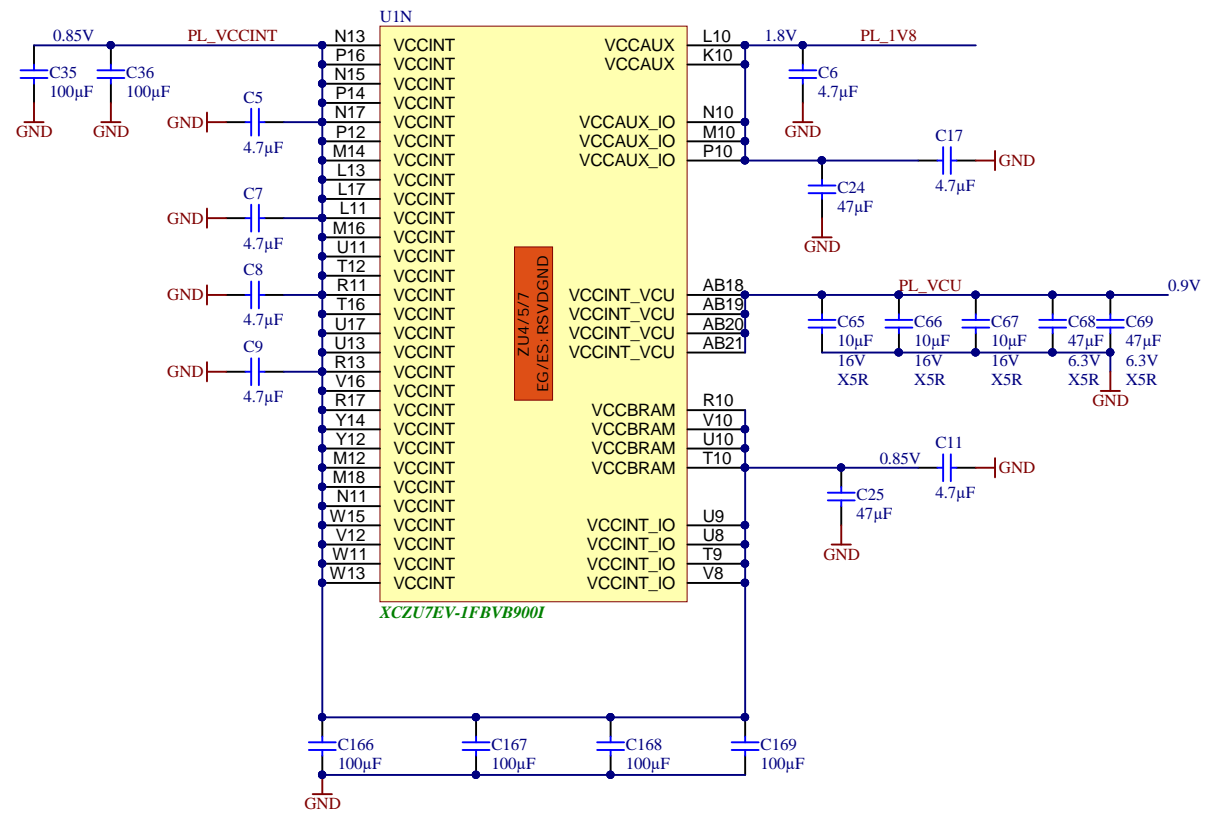
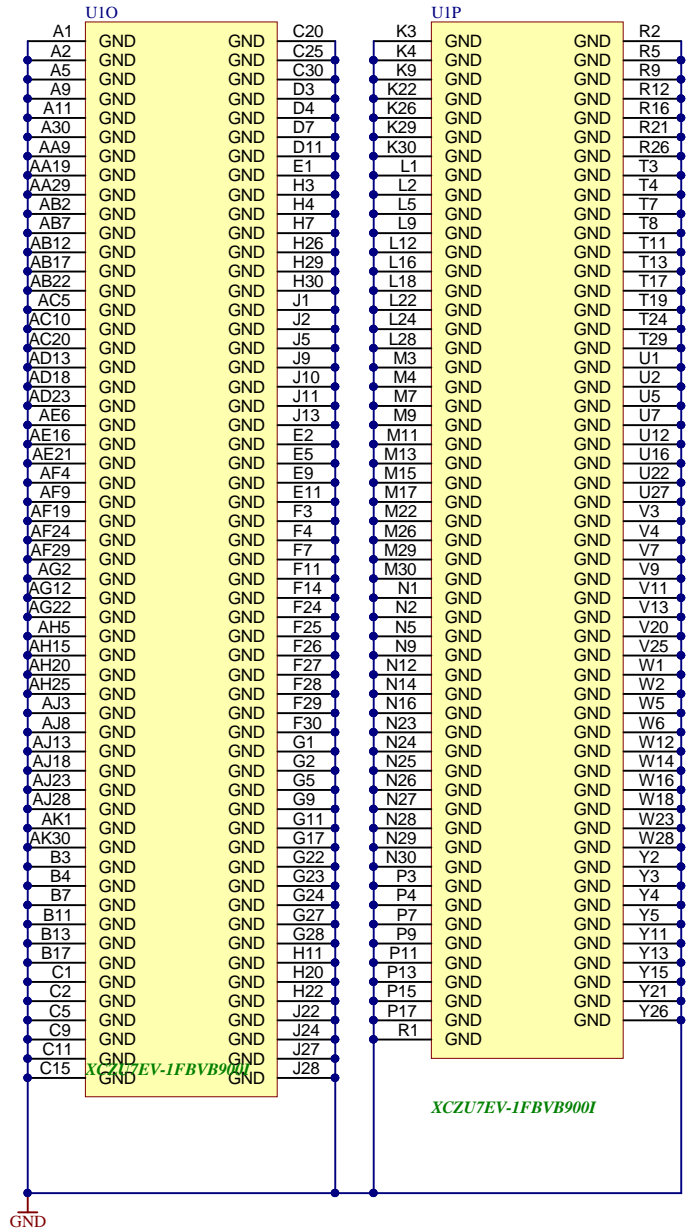
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A4	Number: TE0807 7DI21-A	Rev. 03
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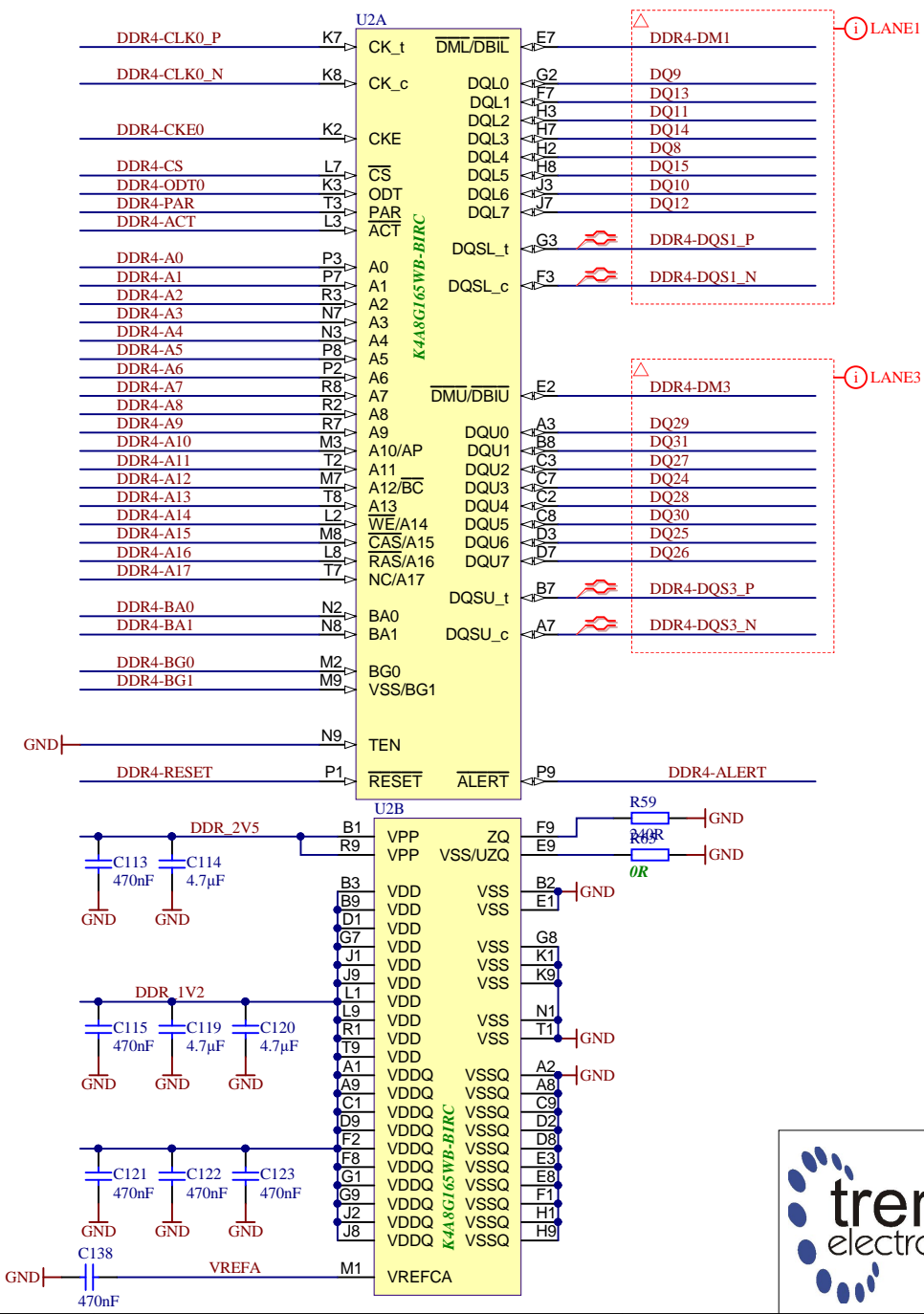
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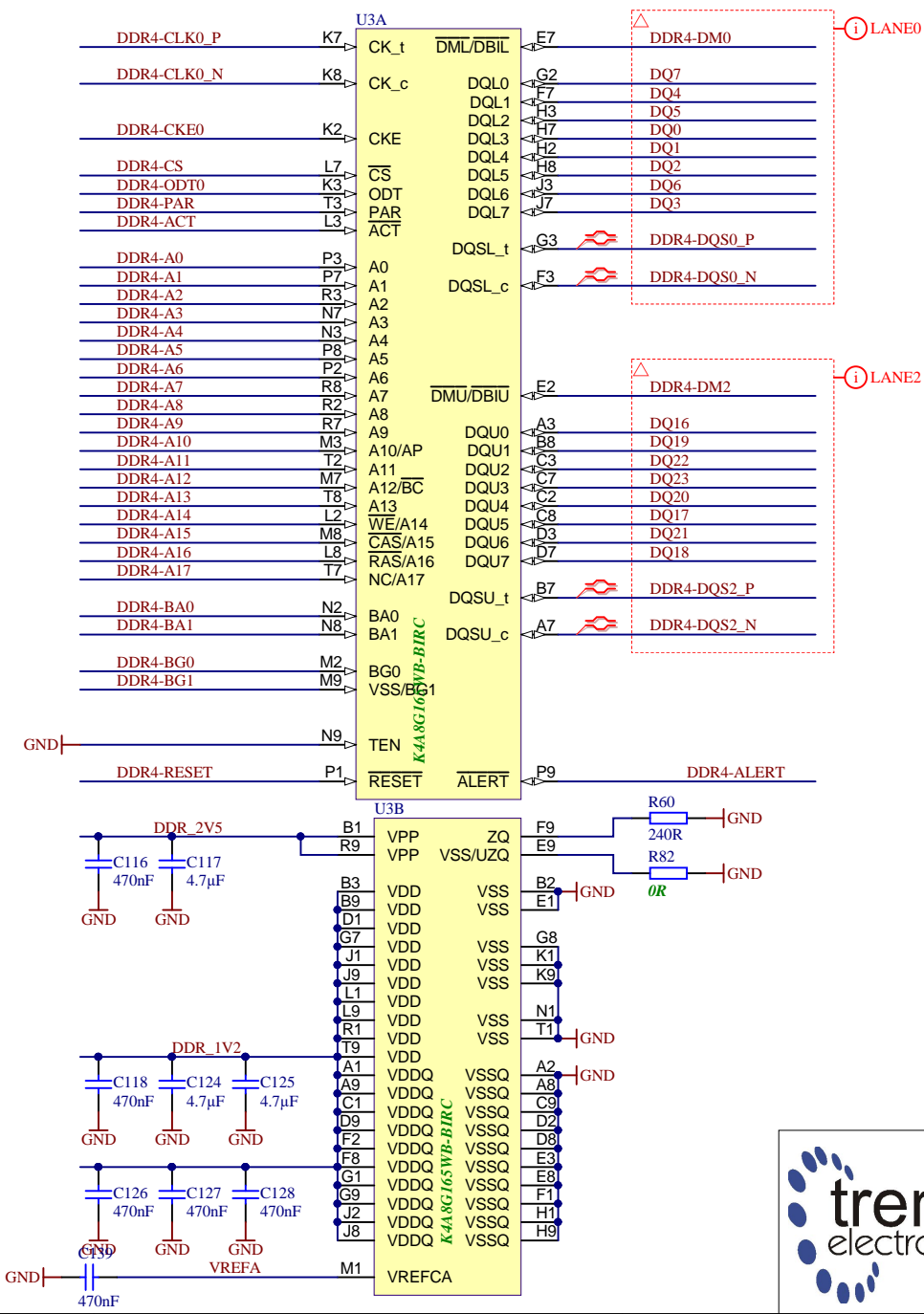

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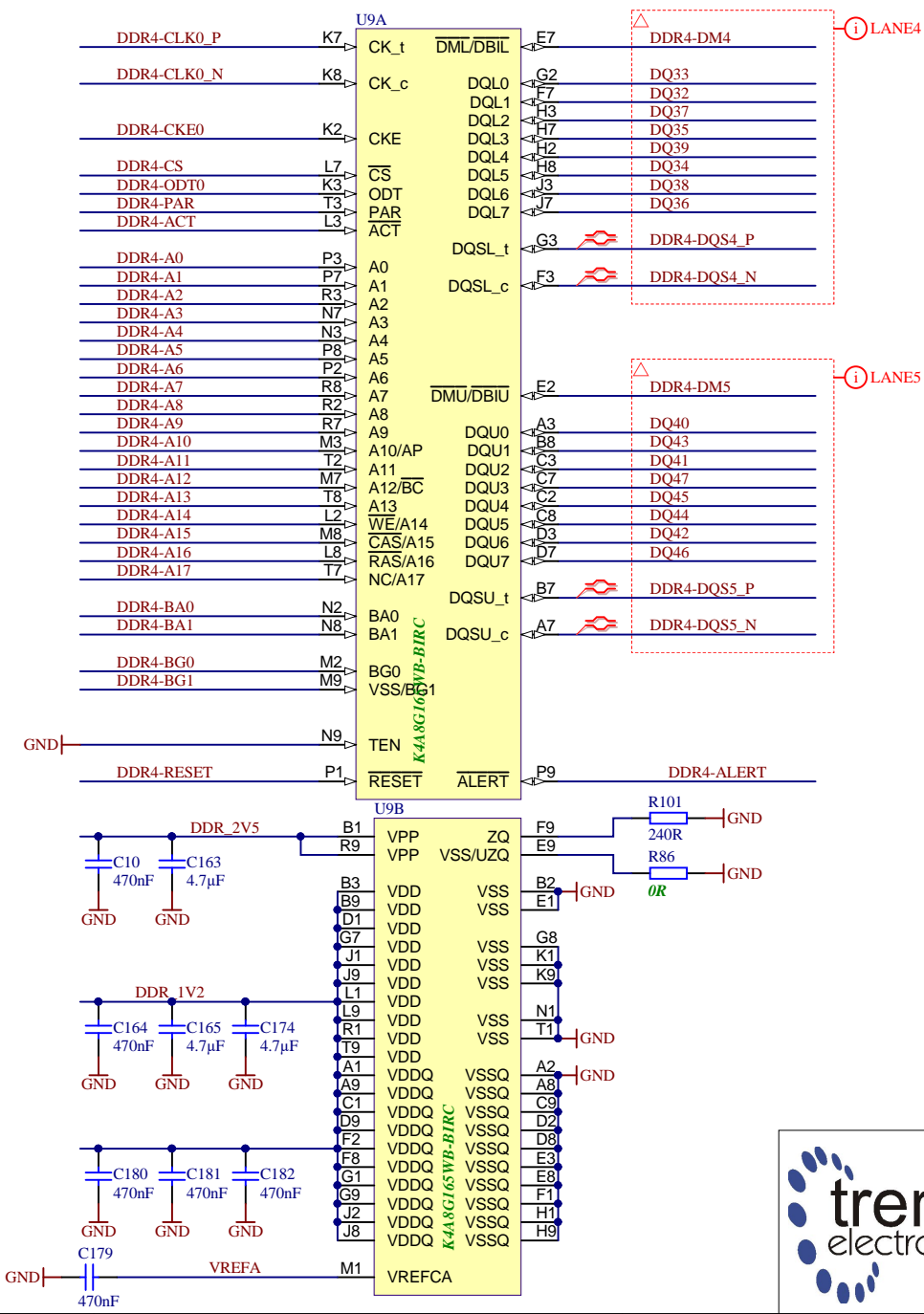
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	A4	Number: TE0807 7DI21-A	Rev. 03
	Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 18 of 29
	Filename: ZU_POWER.SchDoc		



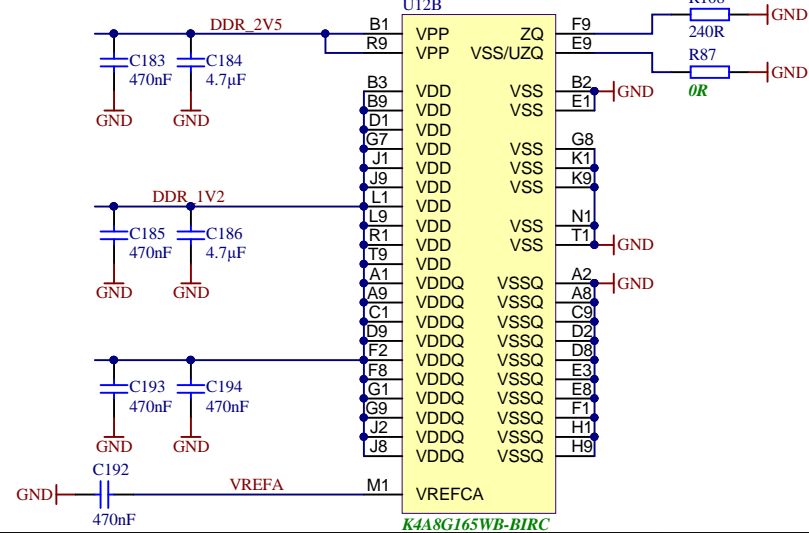
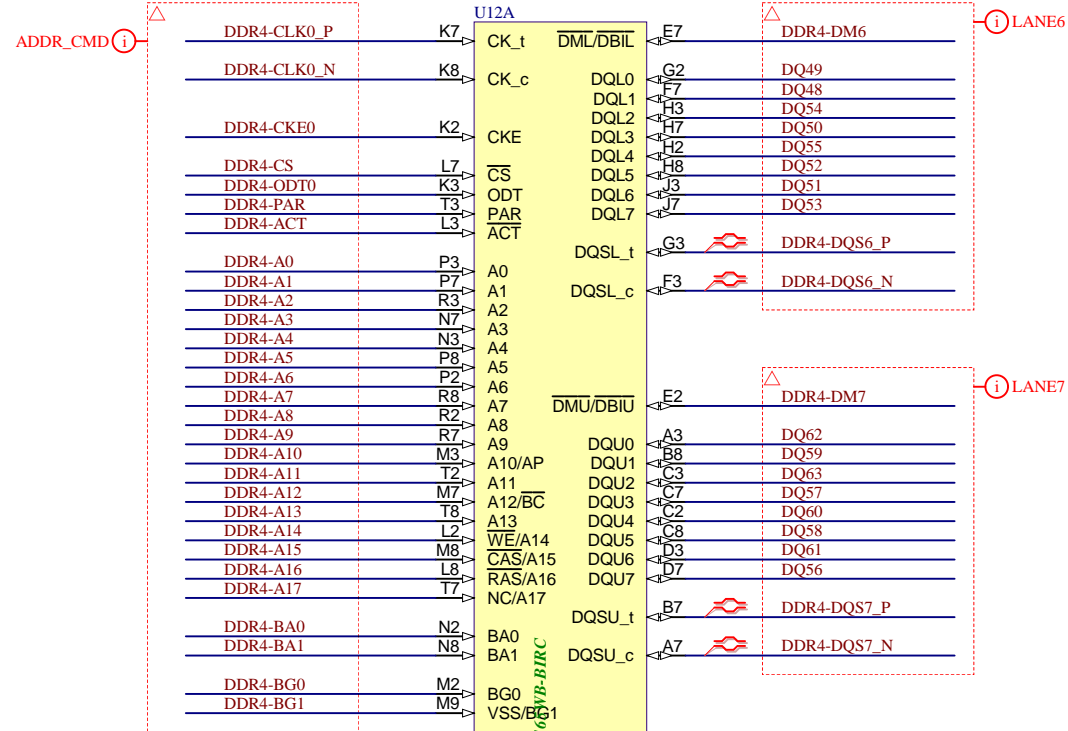

Title: TE0807 - DDR4_1_RAM		
A4	Number: TE0807 7DI21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 19 of 29
Filename: DDR4-RAM.SchDoc		

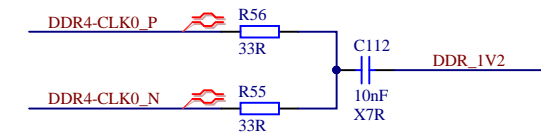
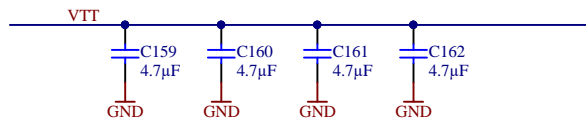
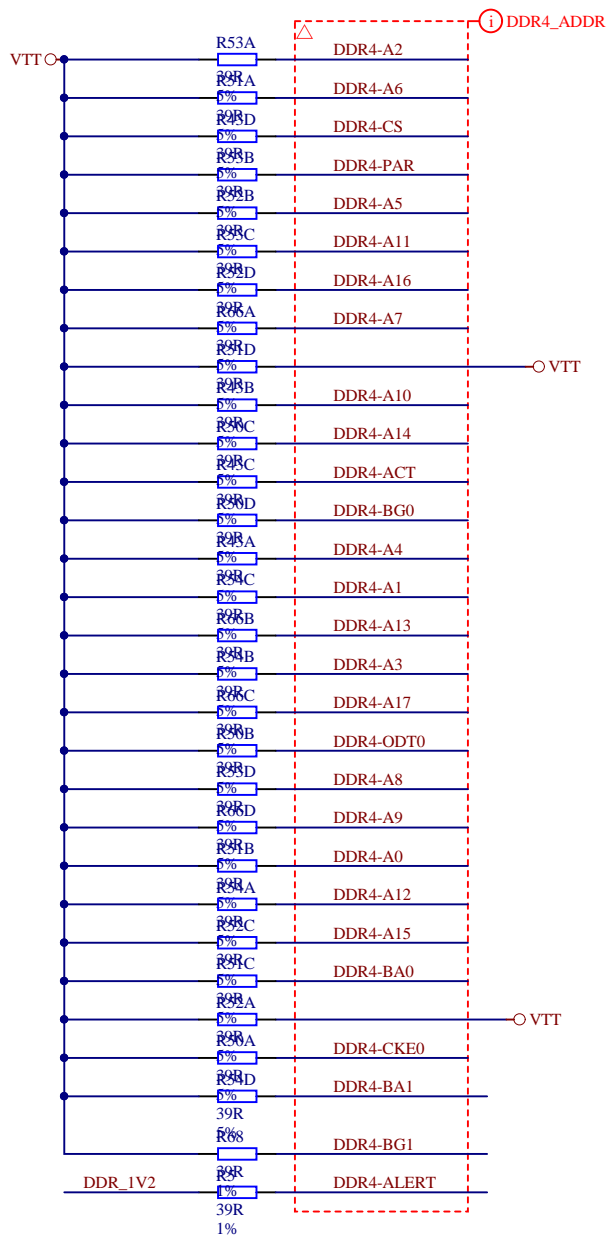
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A4	Number: TE0807 7DI21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 20 of 29
Filename: DDR4-RAM_2.SchDoc		



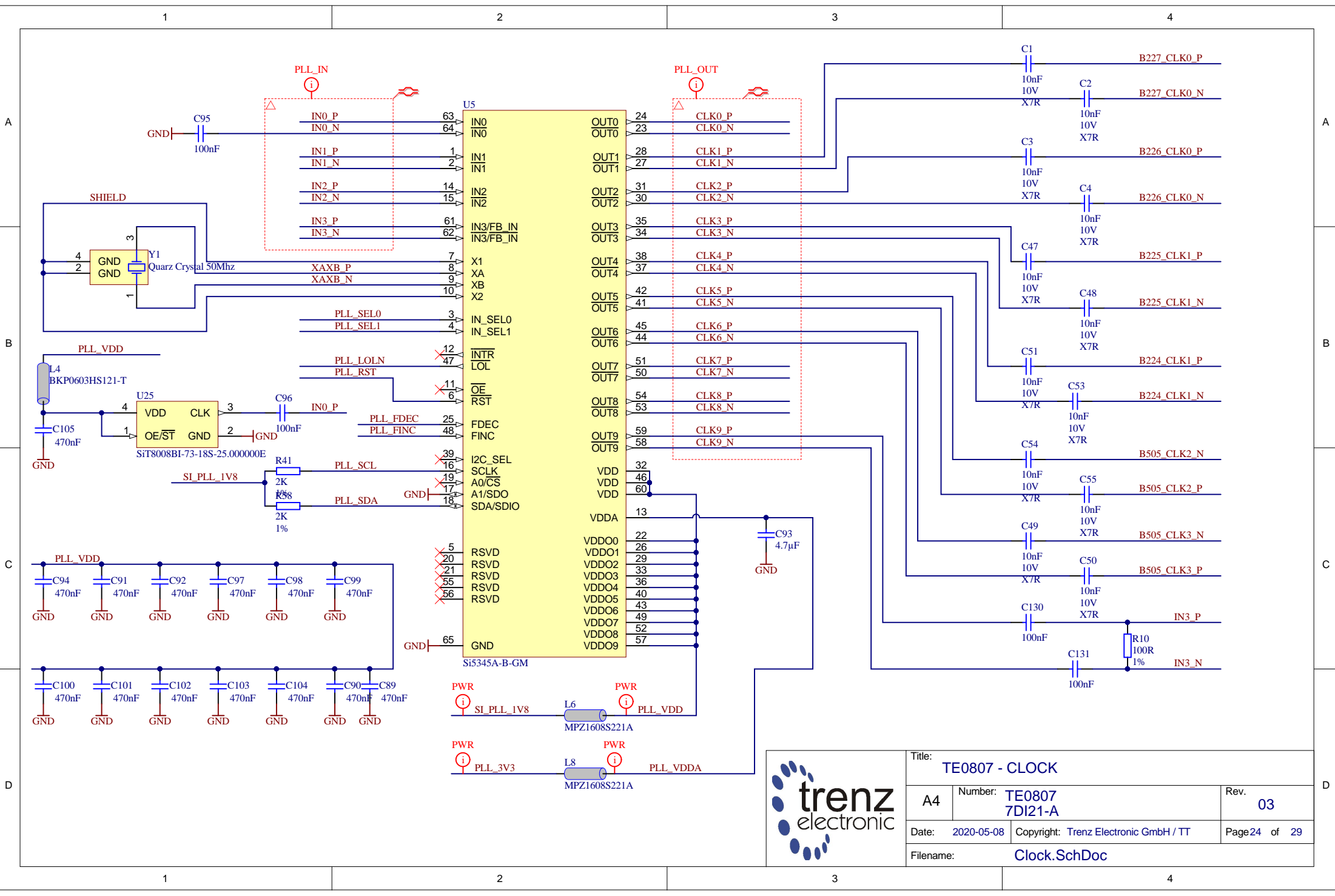
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A4	Number: TE0807 7DI21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 21 of 29
Filename: DDR4-RAM_3.SchDoc		

Title: TE0807 - DDR4_4_RAM		
A4	Number: TE0807 7DI21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 22 of 29
Filename: DDR4-RAM_4.SchDoc		

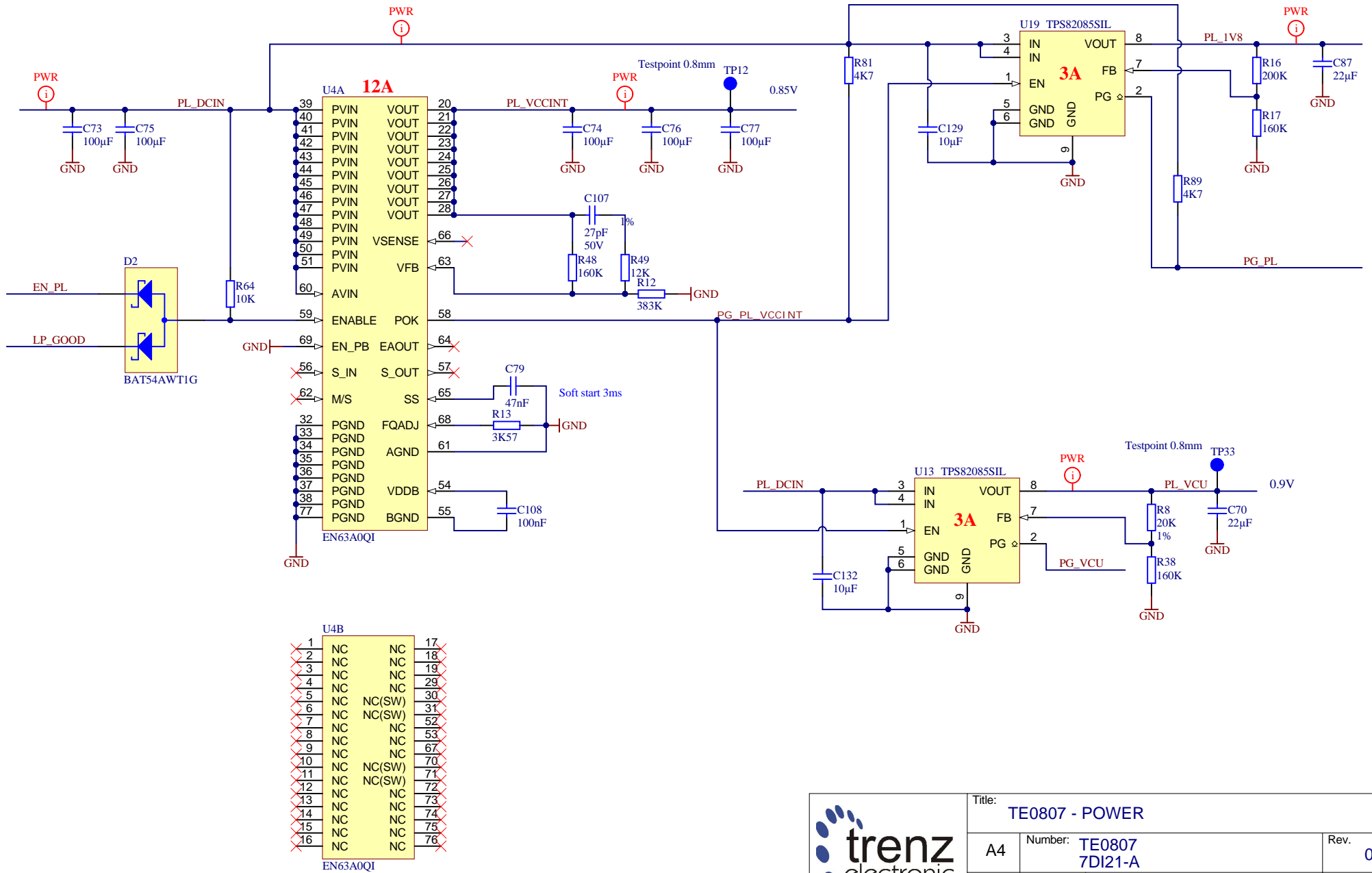


Title: TE0807 - DDR4_TERM		
A4	Number: TE0807 7DI21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 23 of 29
Filename: DDR4-TERM.SchDoc		

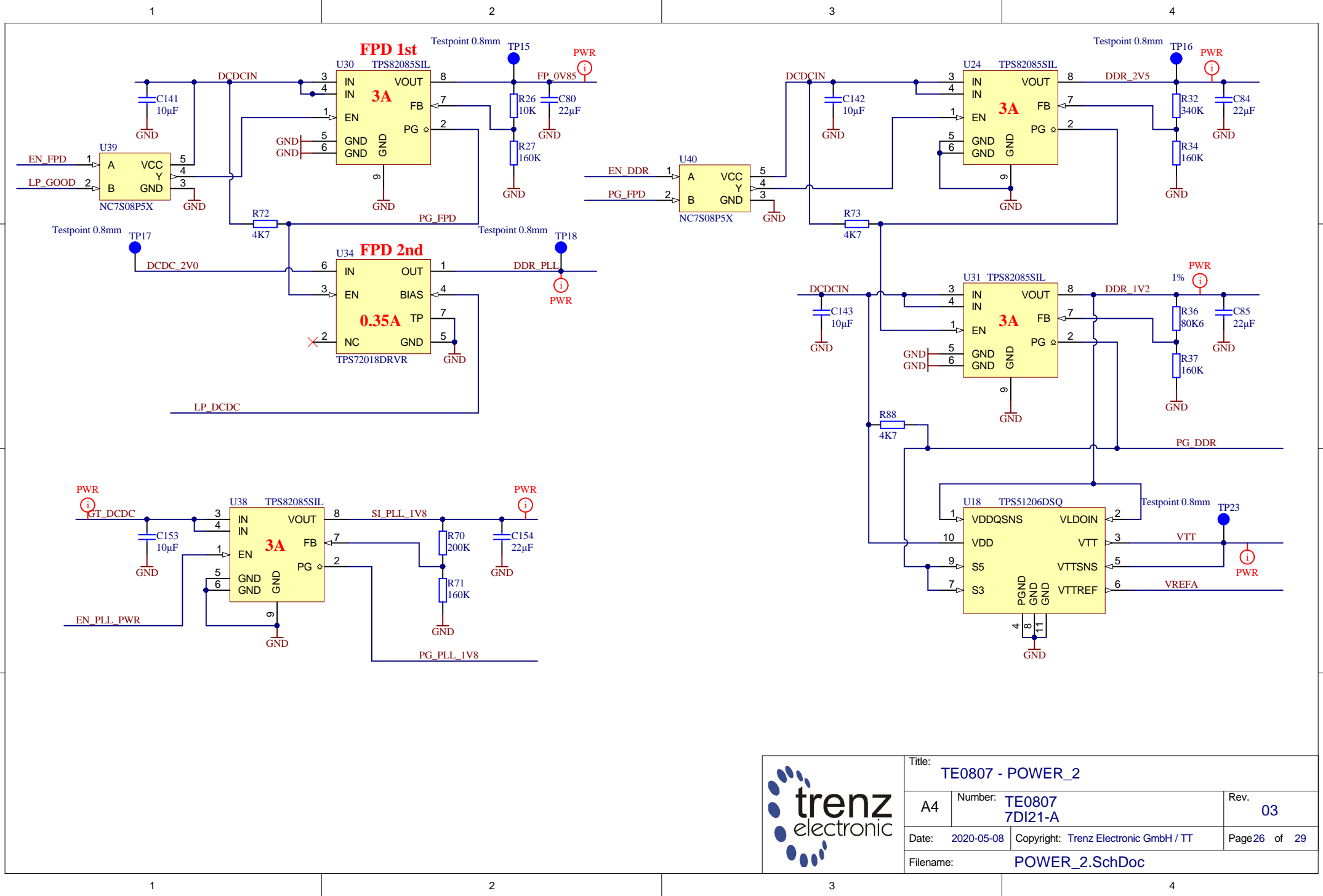



Title: TE0807 - CLOCK		
A4	Number: TE0807 7DI21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 24 of 29
Filename: Clock.SchDoc		

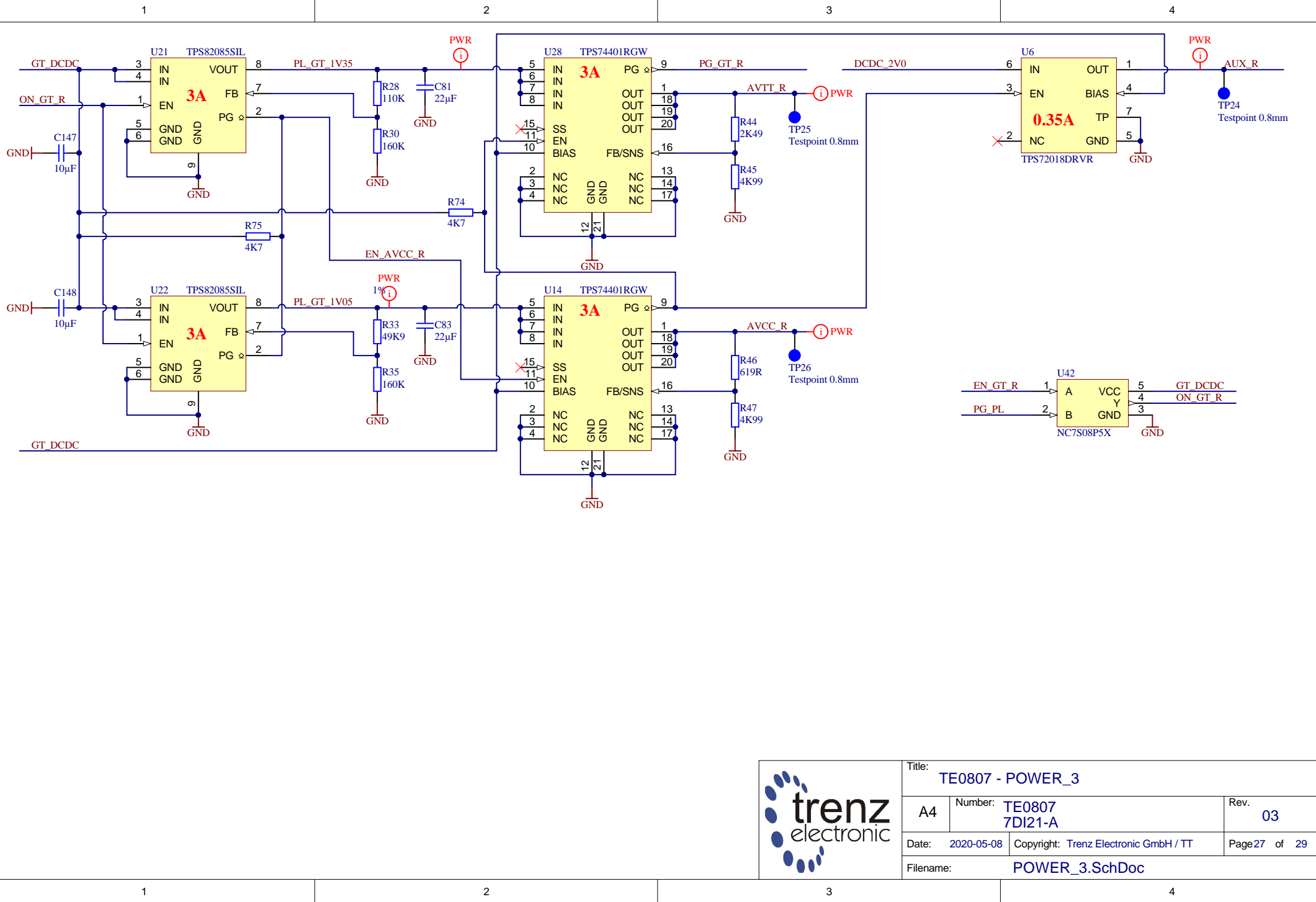





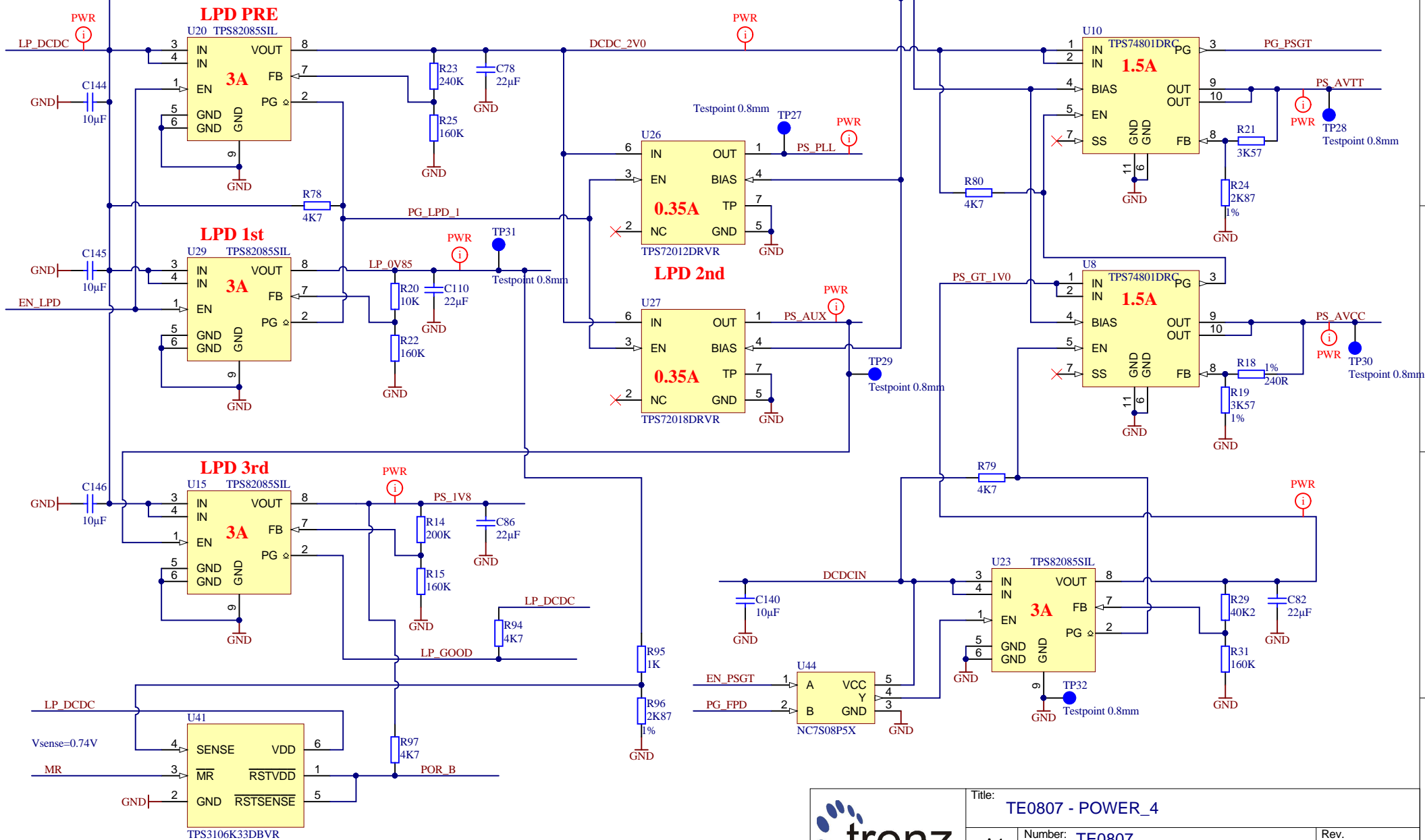
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	A4	Number: <b>TE0807 7DI21-A</b>	Rev. <b>03</b>
	Date: <b>2020-05-08</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	
	Filename: <b>POWER.SchDoc</b>	Page <b>25</b> of <b>29</b>	



		Title: TE0807 - POWER_2	
		A4	Number: TE0807 7DI21-A
Date: 2020-05-08		Copyright: Trenz Electronic GmbH / TT	
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		Title: TE0807 - POWER_3	
		A4	Number: TE0807 7DI21-A
Date: 2020-05-08		Copyright: Trenz Electronic GmbH / TT	
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Title: TE0807 - POWER_4		
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CHANGES REV01 to REV02

- 1) Added EEPROM (U11,24AA025E48T-I/OT)
- 2) Added optional resistors R39/R40 for QSPI flash (do not populated)
- 3) Fixed VCU connection (added additional DCDC and capacitors), recommendation from Xilinx
- 4) Changed obsolete DDR4 chips (NT5AD256M16B2-GN -> K4A8G165WB-BIRC)
- 5) Added net "PG\_VCU" to J2 (pin97)
- 6) full update lib

CHANGES REV02 to REV03 (06.2020)

- VT: 1) Fixed ADC connection  
 2) Fixed DDR4 connection (support B-die DDR4 chips)  
 3) Fixed DDR4 connection (alert\_n pin connection)  
 4) Added U16  
 4) Added testpoints  
 5) Full update LIB

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	Title: <b>TE0807 - Changes list</b>		
	A4	Number: <b>TE0807 7DI21-A</b>	Rev. <b>03</b>
	Date: <b>2020-05-08</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>29</b> of <b>29</b>
	Filename: <b>Revision_Changes.SchDoc</b>		

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