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	Title: TE0807 - Legal Notices		
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U_J1
J1.SchDoc

U_J2
J2.SchDoc

U_J3
J3.SchDoc

U_J4
J4.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

U_B64
B64.SchDoc

U_B65
B65.SchDoc

U_B66
B66.SchDoc

U_B_GT
B_GT.SchDoc

U_B_GT_2
B_GT_2.SchDoc

U_B_PS_GT
B_PS_GT.SchDoc

U_PS_DDR
PS_DDR.SchDoc

U_B_MIO
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U_B_HD
B_HD.SchDoc

U_Clock
Clock.SchDoc

U_CONFIG
CONFIG.SchDoc

U_DDR4-RAM
DDR4-RAM.SchDoc

U_DDR4-RAM_2
DDR4-RAM_2.SchDoc

U_DDR4-RAM_3
DDR4-RAM_3.SchDoc

U_DDR4-RAM_4
DDR4-RAM_4.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

U_ZU_POWER
ZU_POWER.SchDoc

U_ZU_PS_POWER
ZU_PS_POWER.SchDoc

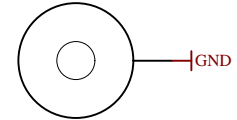
U_POWER
POWER.SchDoc

U_POWER_2
POWER_2.SchDoc

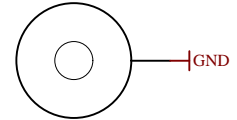
U_POWER_3
POWER_3.SchDoc

U_POWER_4
POWER_4.SchDoc

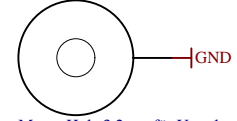
Special notes:



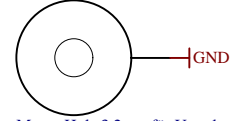
Mount.Hole 3.2mm für Unterlegscheibe



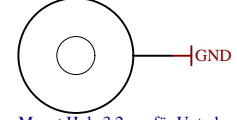
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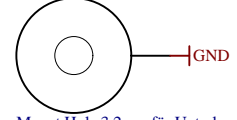
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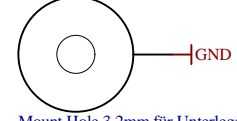
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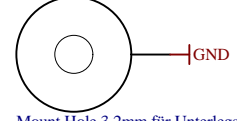
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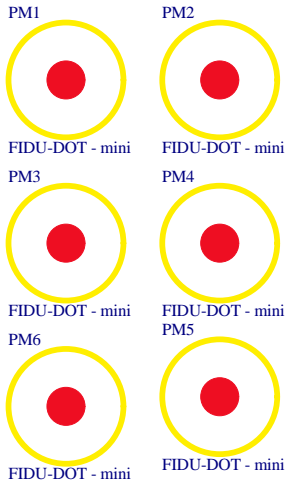
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



LOGO1
TE Logo PRINT Layer
LOGO PRINT

Serial
Serialnummer 6,3 x 6.3mm

Assembly variant	7NE21-A
Created by	VT
Modified by	VT
Modified at	2020-06-16
SVN Revision	9271 [Locally Modified]



Title: TE0807		
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1

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A

A

B

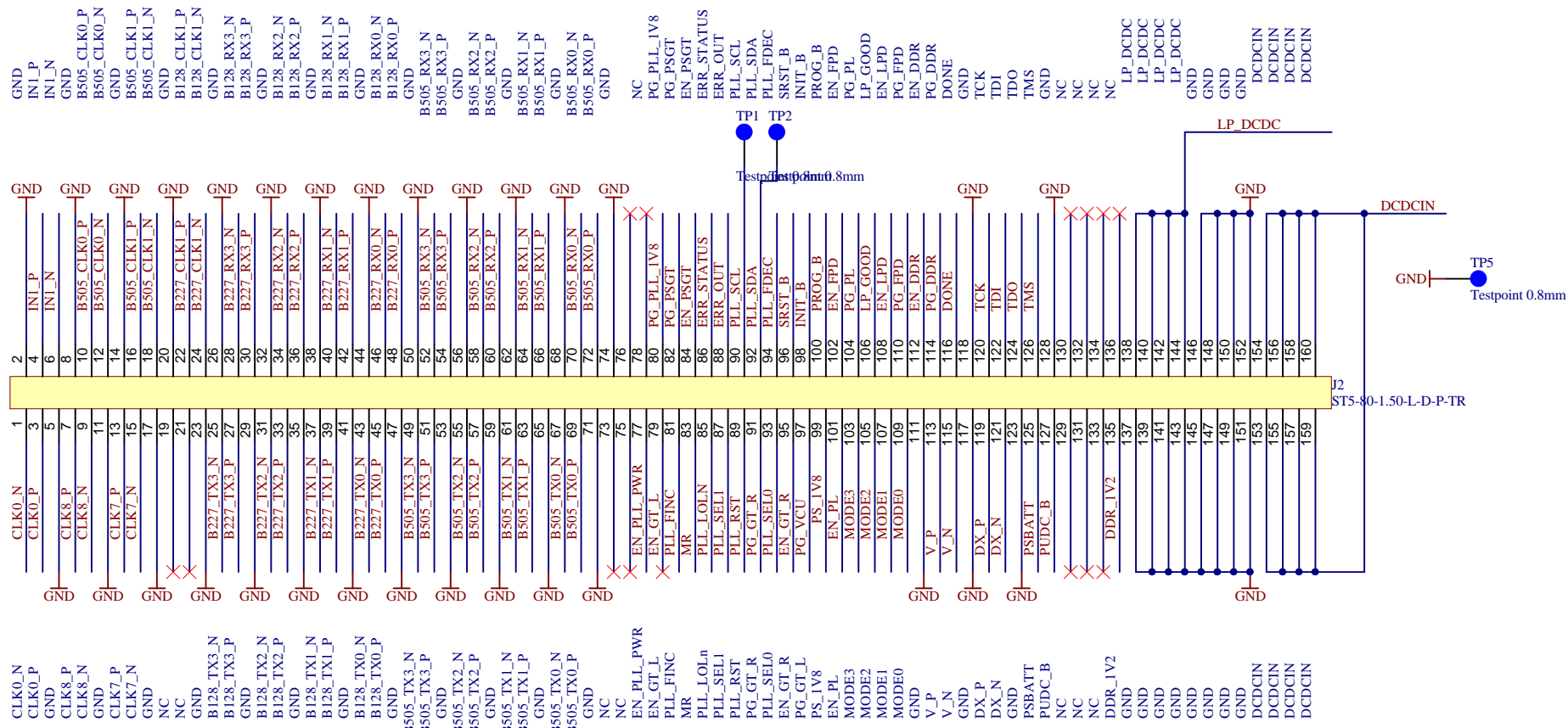
B

C

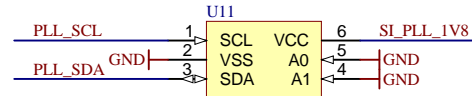
C

D

D



EEPROM for MAC

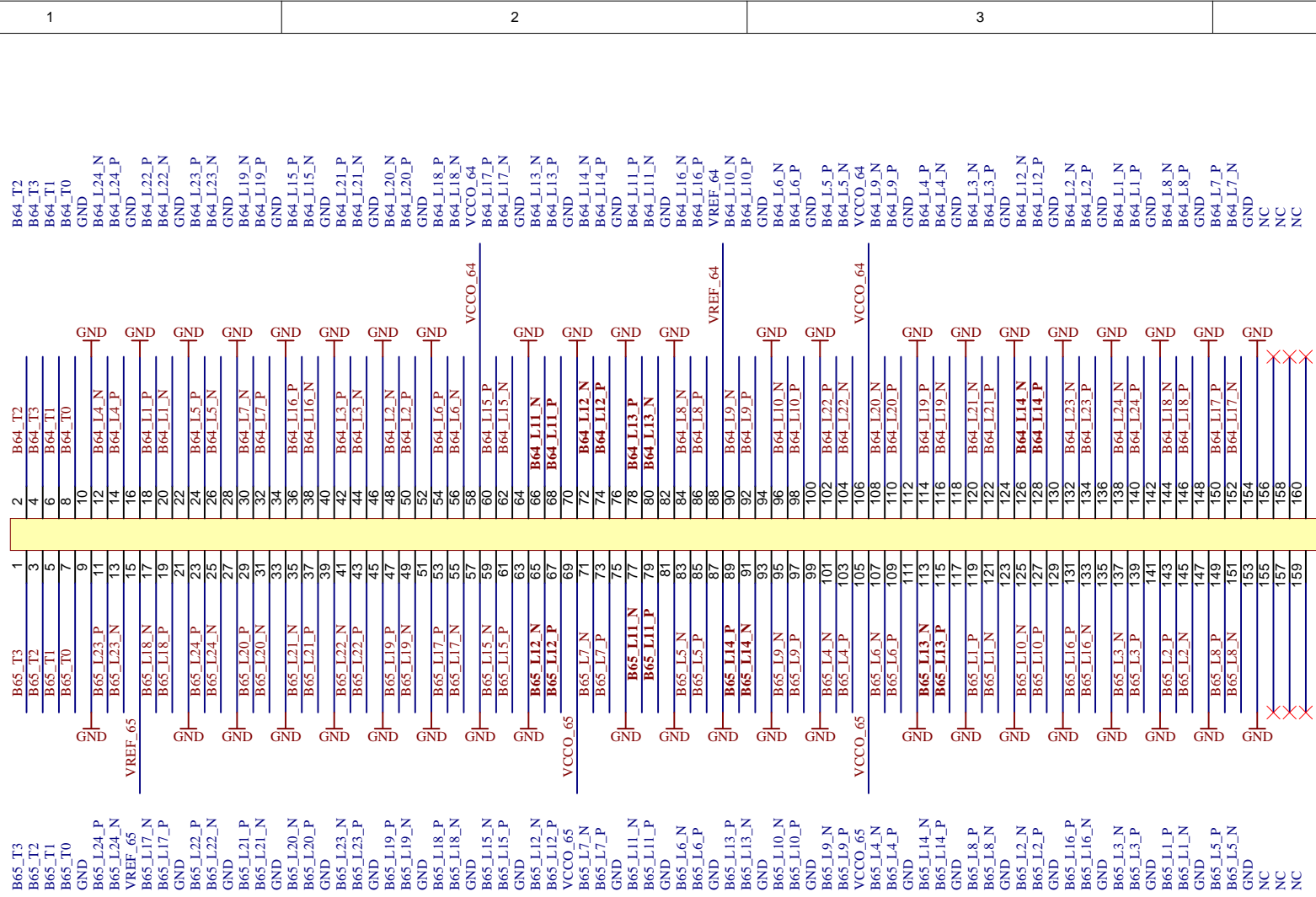


Slave address: 101000x




Title: TE0807 - Connector J2		
A4	Number: TE0807 7NE21-A	Rev. 03
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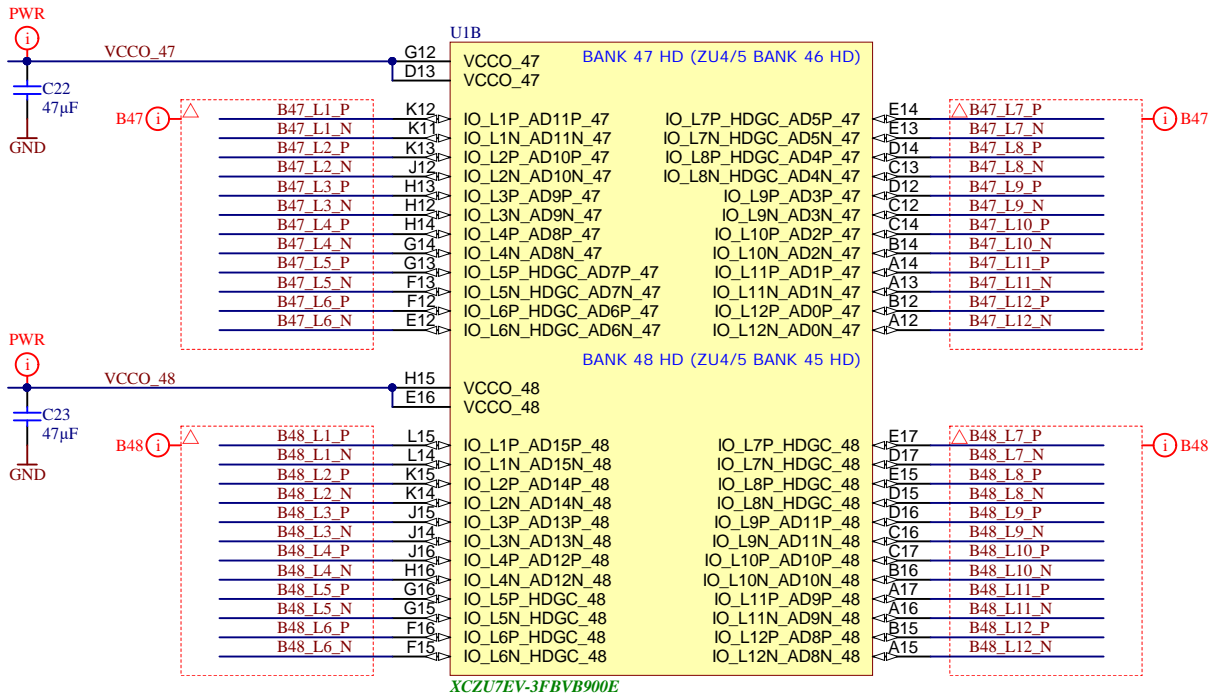
A
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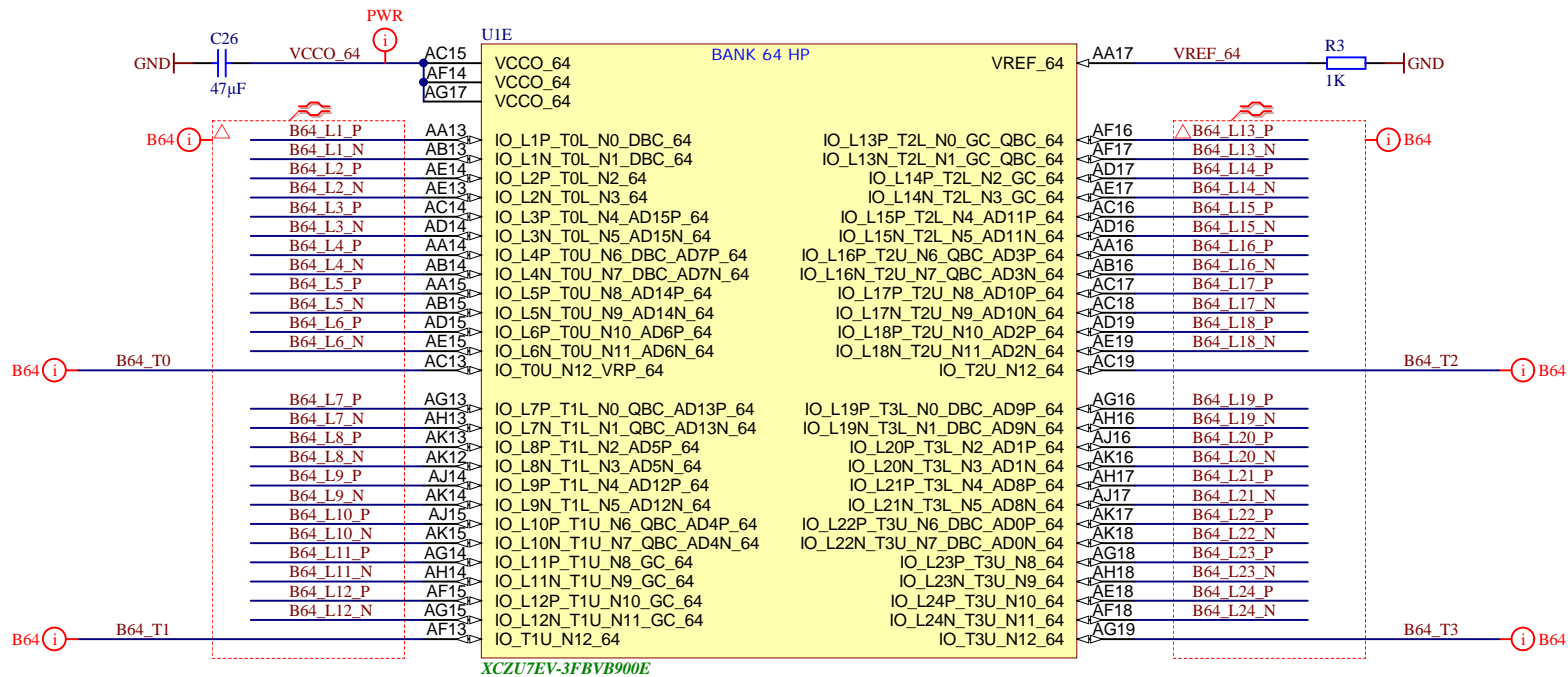
J4
ST5-80-1.50-L-D-P-TR



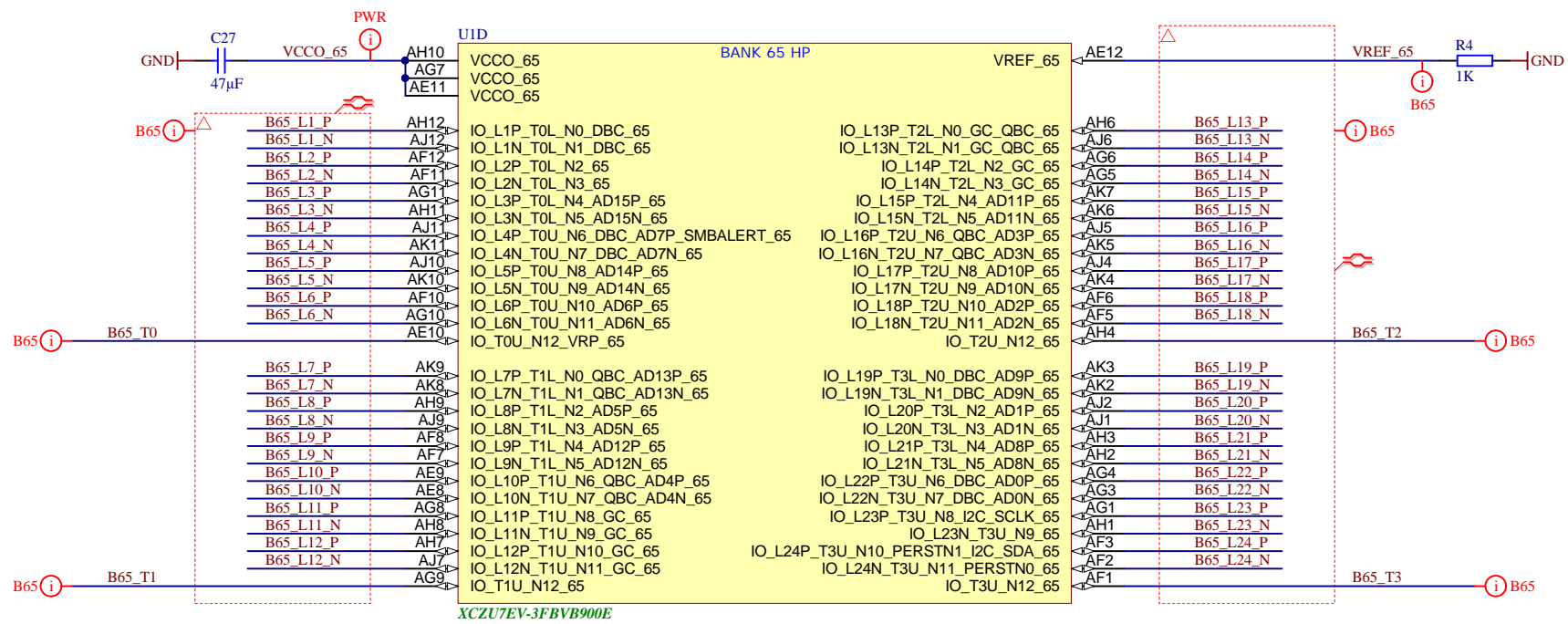
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A4	Number: TE0807 7NE21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 6 of 29
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Title: TE0807 - B47HD and B48HD		
A4	Number: TE0807 7NE21-A	Rev. 03
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Filename: B_HD.SchDoc		



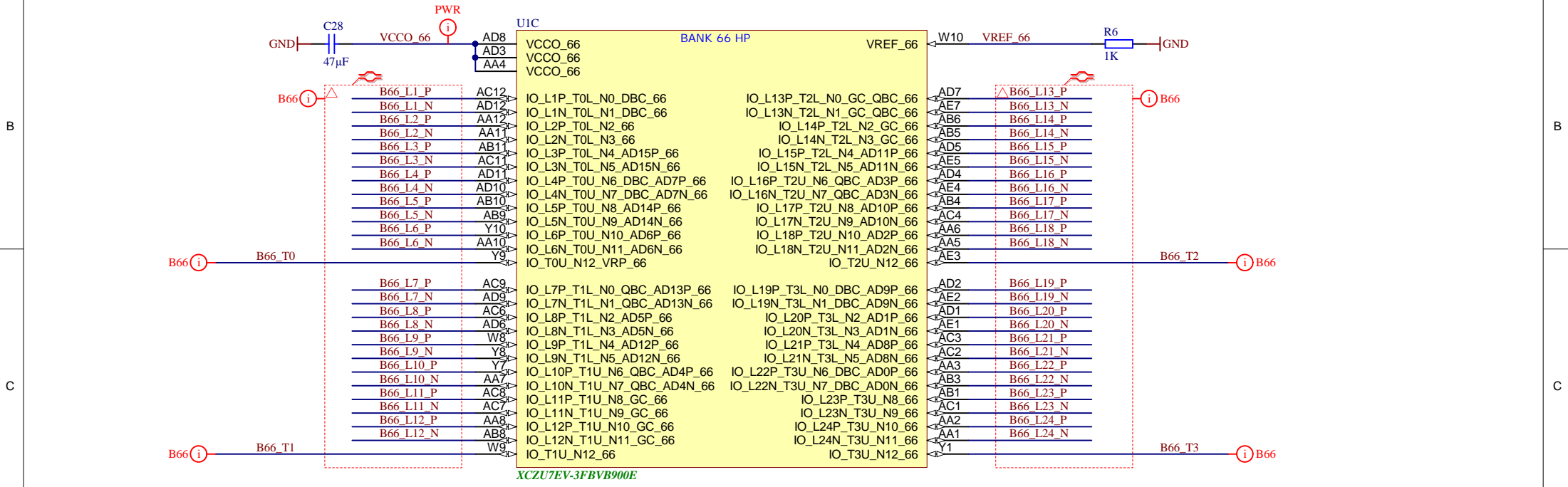
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A4	Number: TE0807 7NE21-A	Rev. 03
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XCZU7EV-3FBVB900E



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Title: TE0807 - B66		
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A

A

B

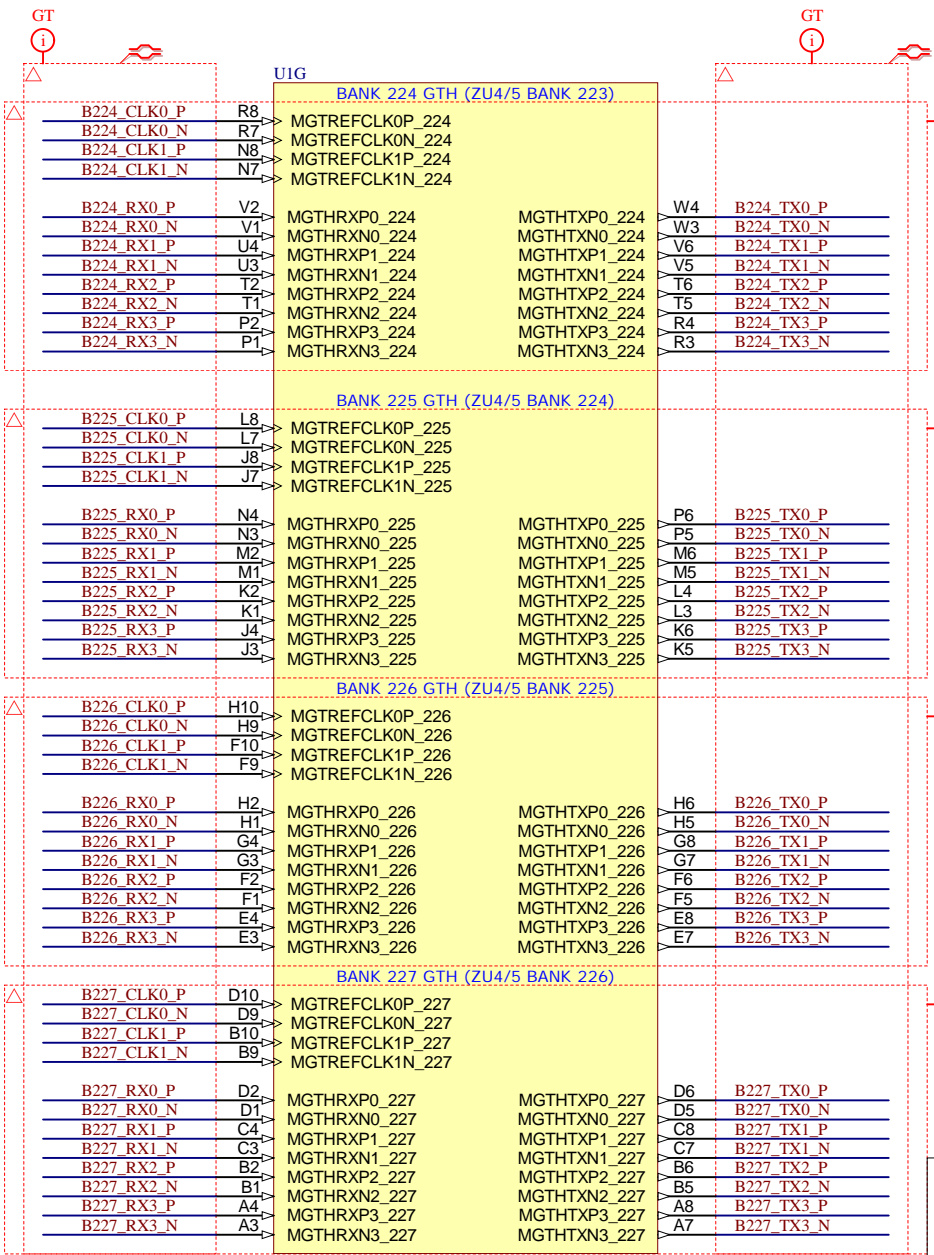
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C

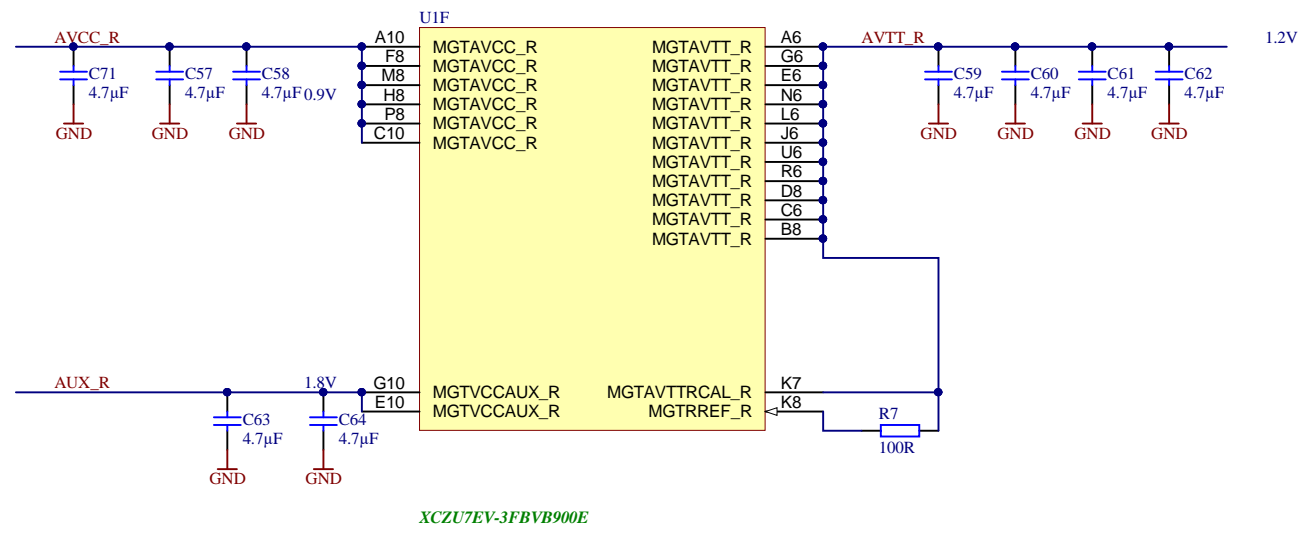
C


D

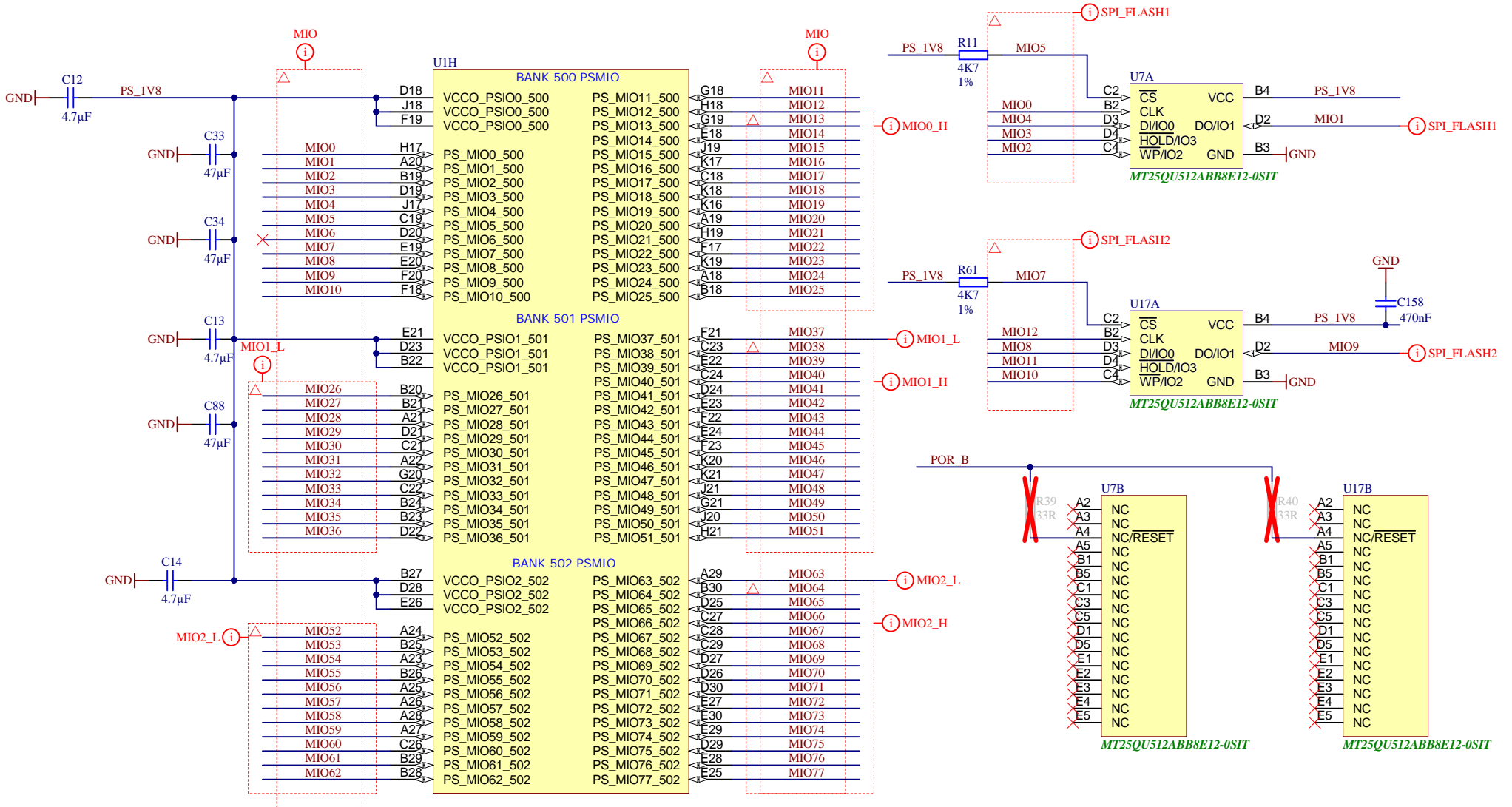
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Title: TE0807 - GTH_Banks		
A4	Number: TE0807 7NE21-A	Rev. 03
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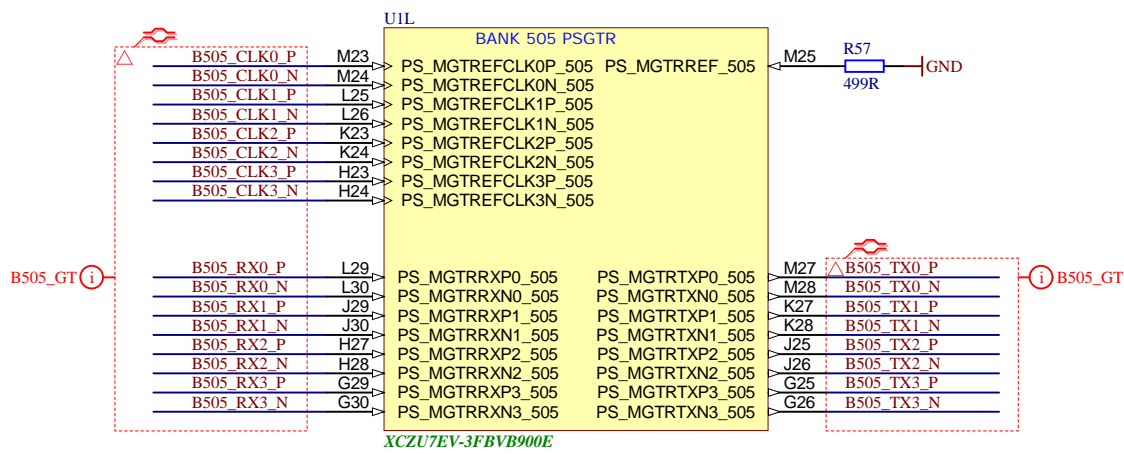


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		A4	Number: TE0807 7NE21-A
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Filename: B_GT_2.SchDoc		Page 13 of 29	



XCZU7EV-3FBVB900E

	Title: TE0807 - MIO Banks		
	A4	Number: TE0807 7NE21-A	Rev. 03
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	Title: TE0807 - PS_GT		
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	Filename: B_PS_GT.SchDoc		

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A

B

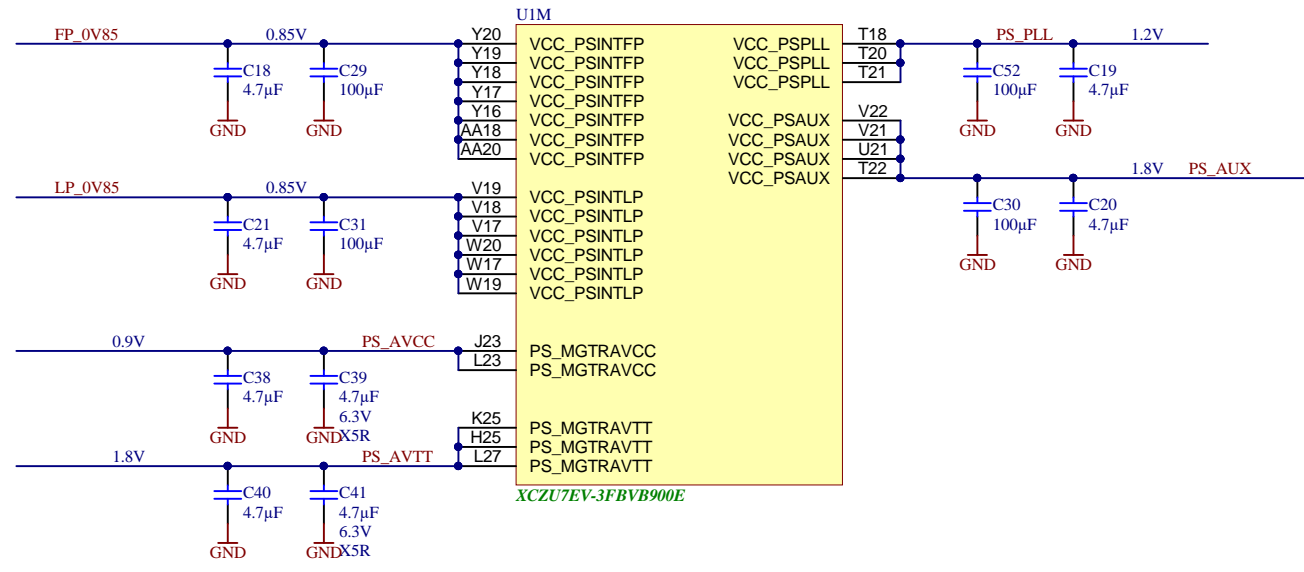
B

C

C

D

D



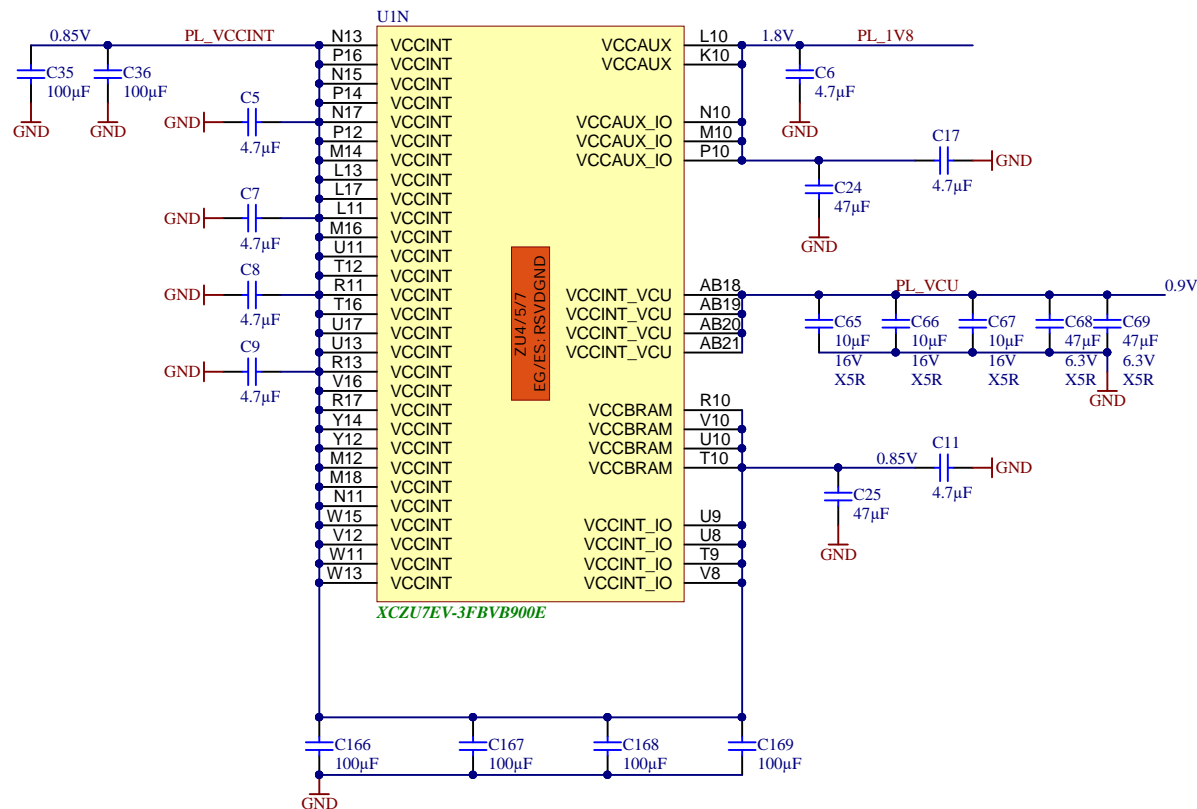
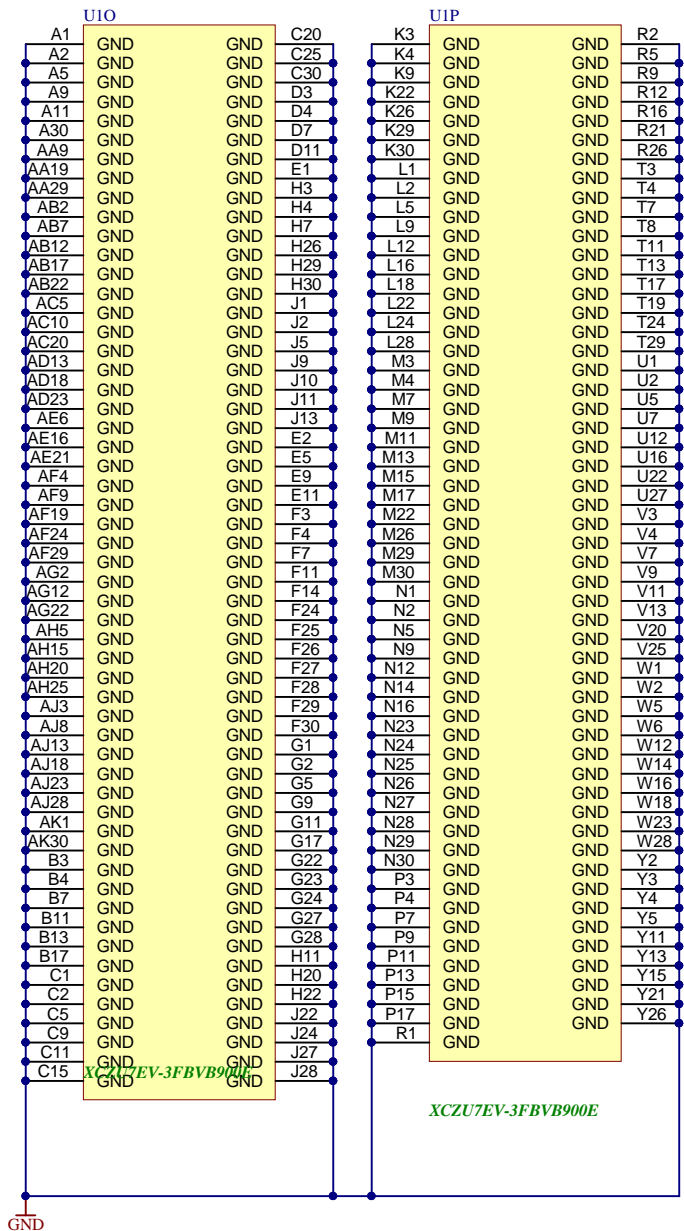
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A4	Number: TE0807 7NE21-A	Rev. 03
Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	Page 17 of 29
Filename: ZU_PS_POWER.SchDoc		


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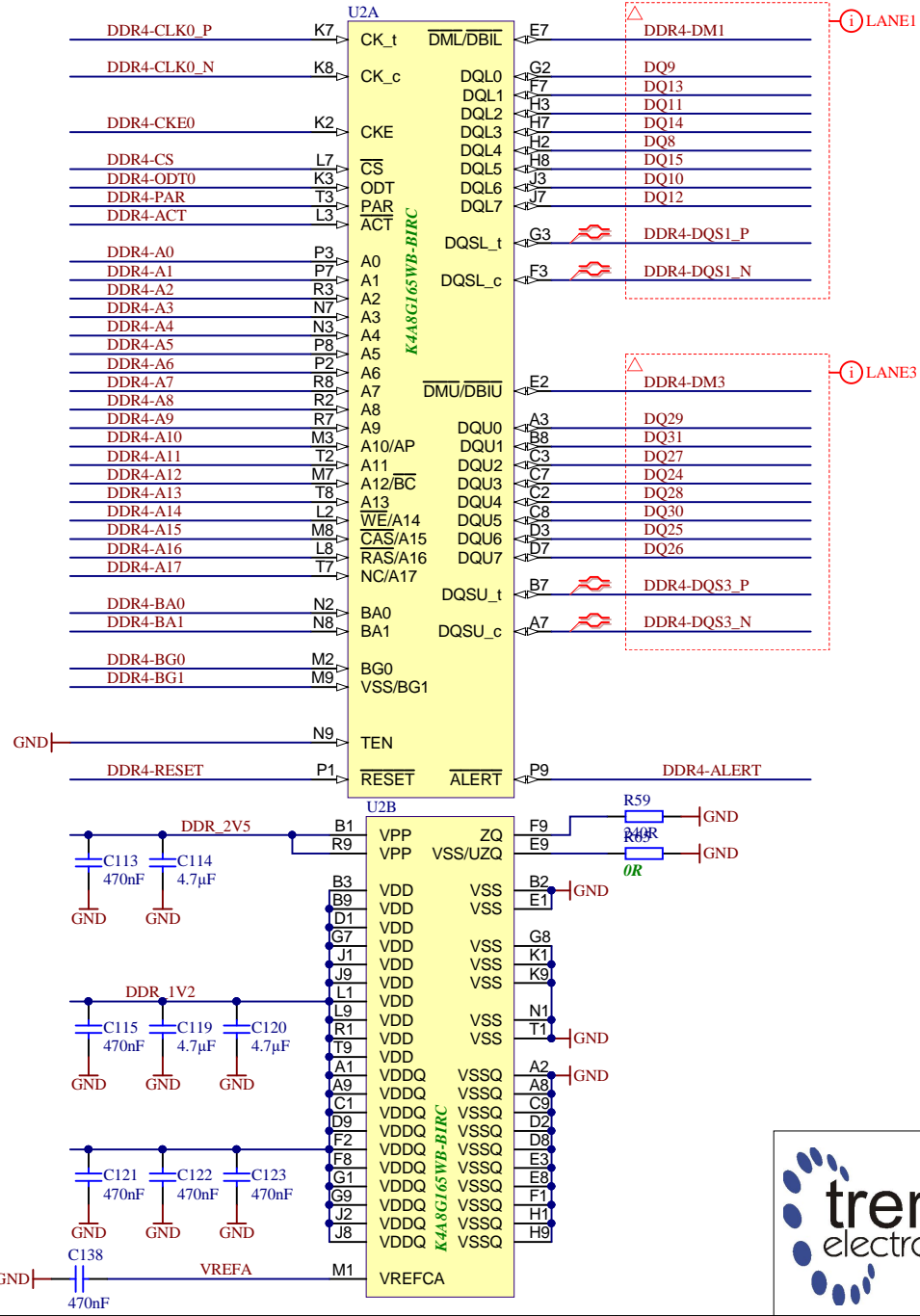
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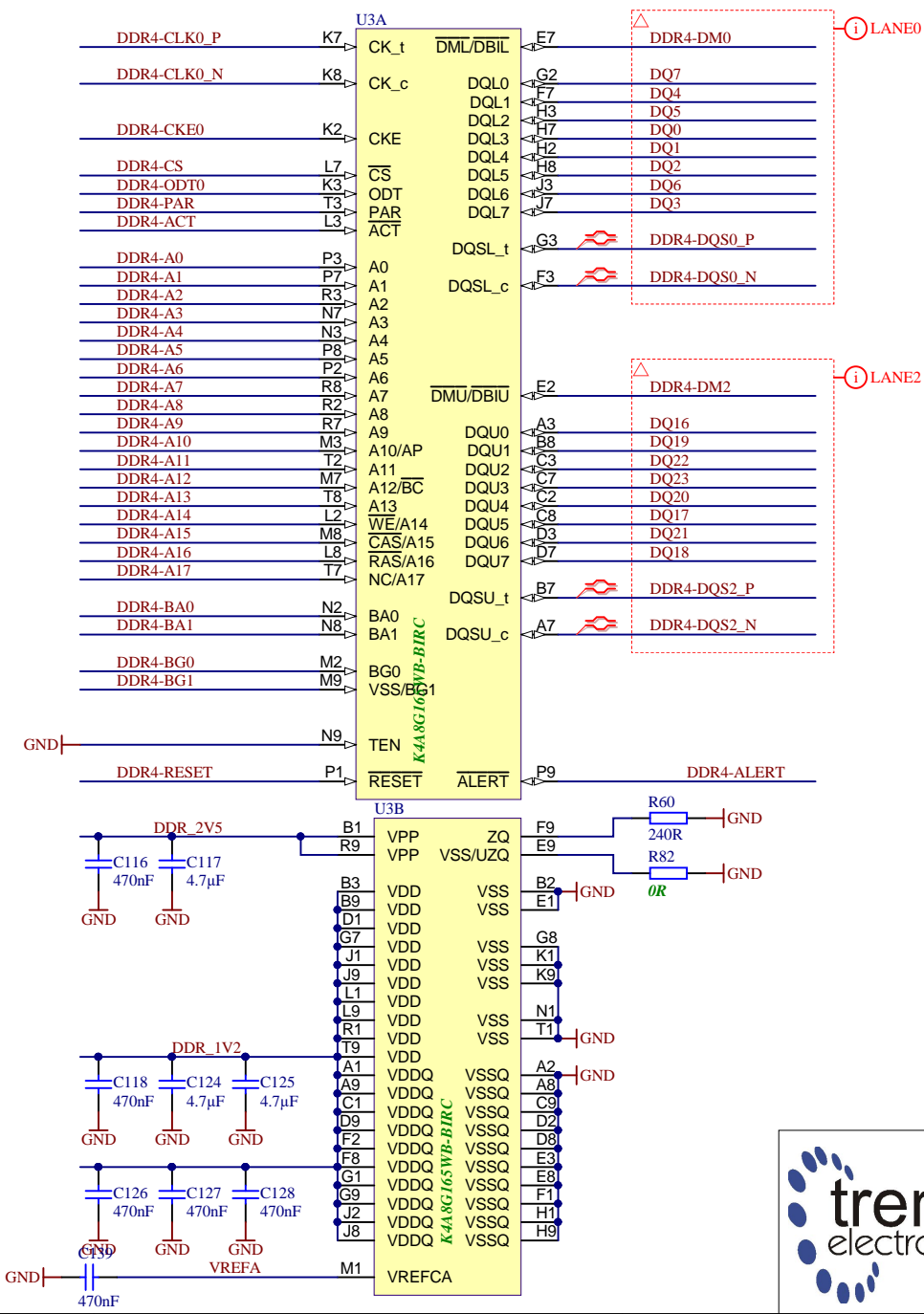

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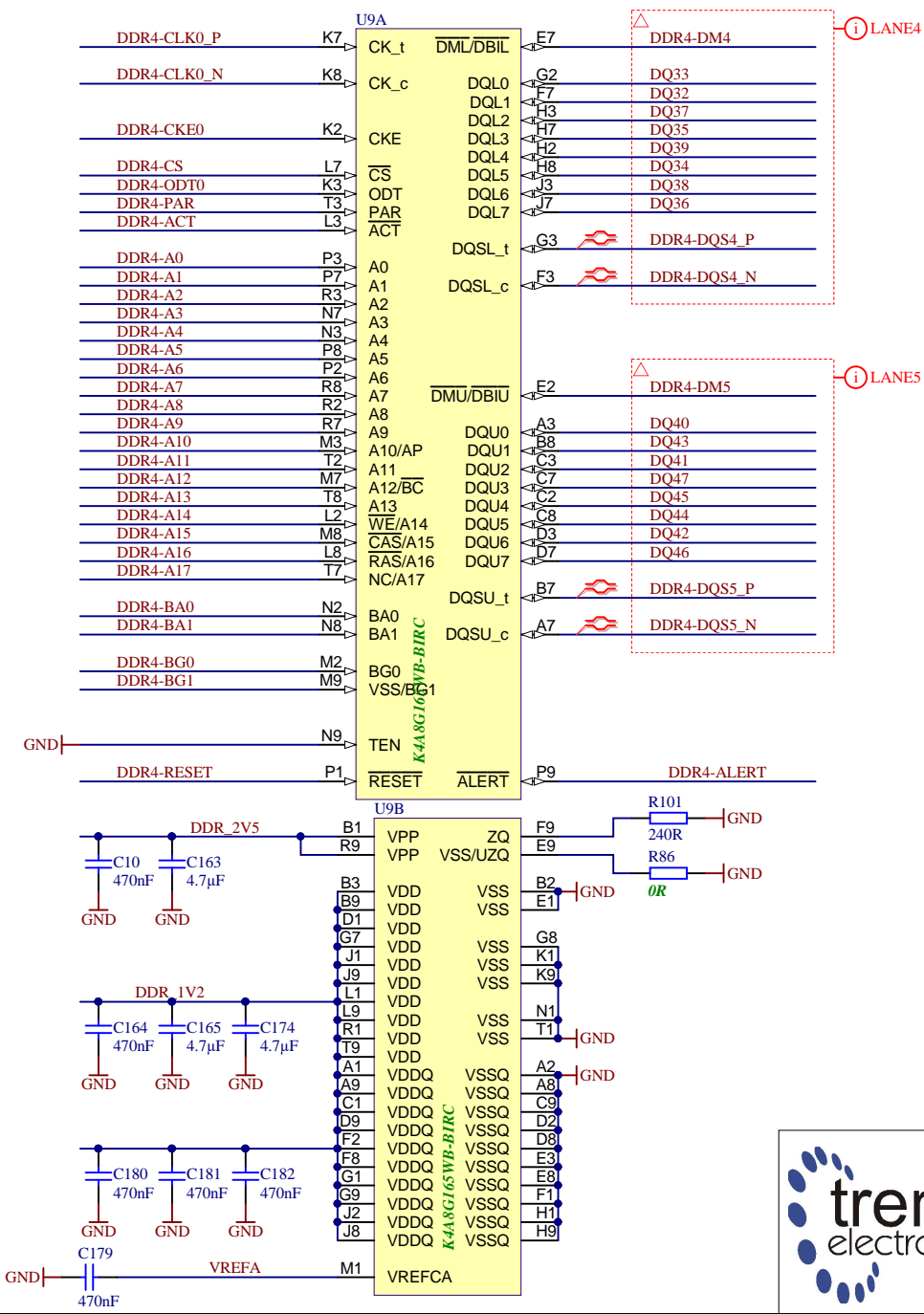
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			A4	Number: TE0807 7NE21-A
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Filename: ZU_POWER.SchDoc				



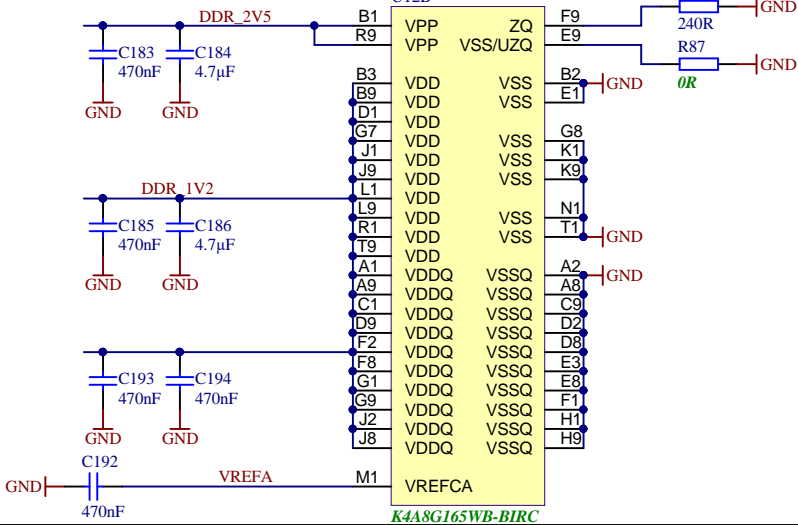
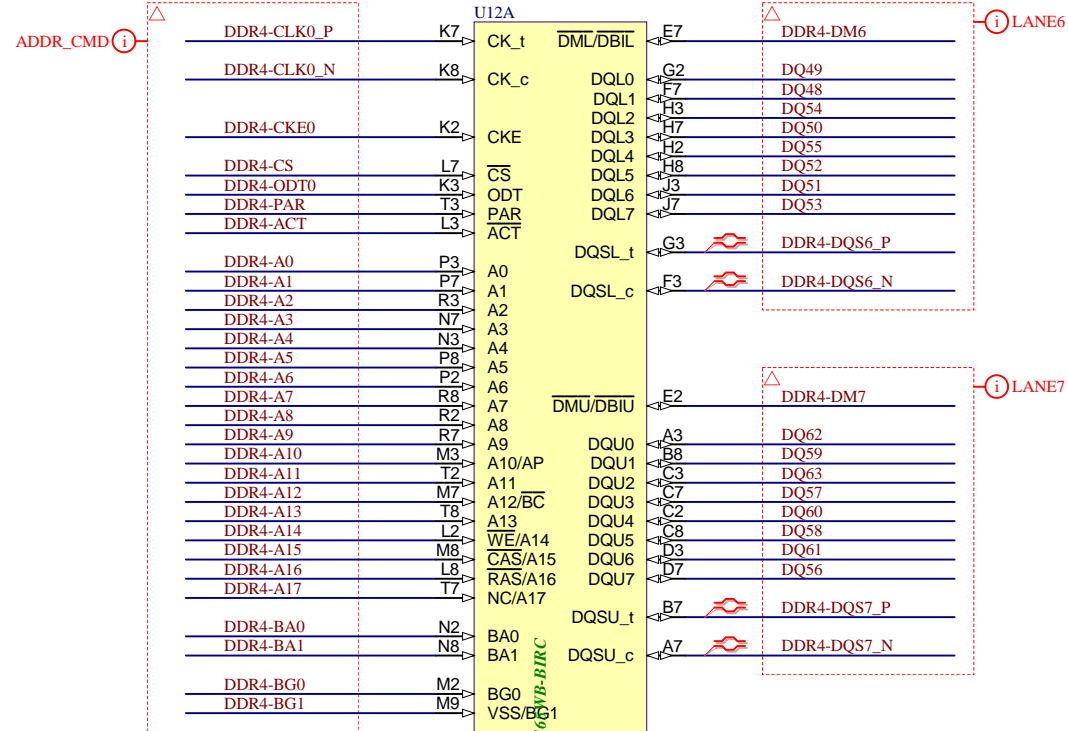

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Filename: DDR4-RAM.SchDoc		

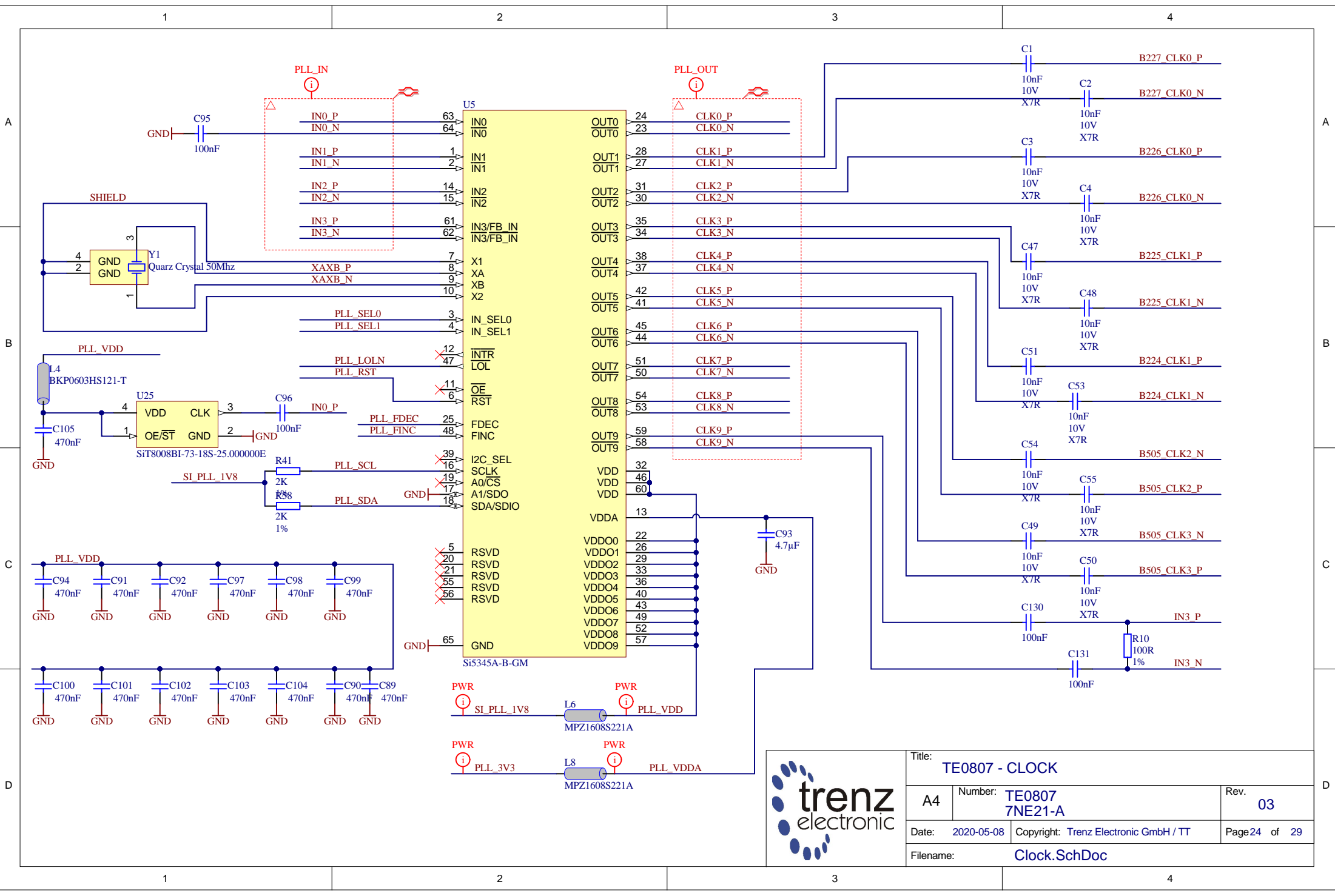
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Filename: DDR4-RAM_2.SchDoc		



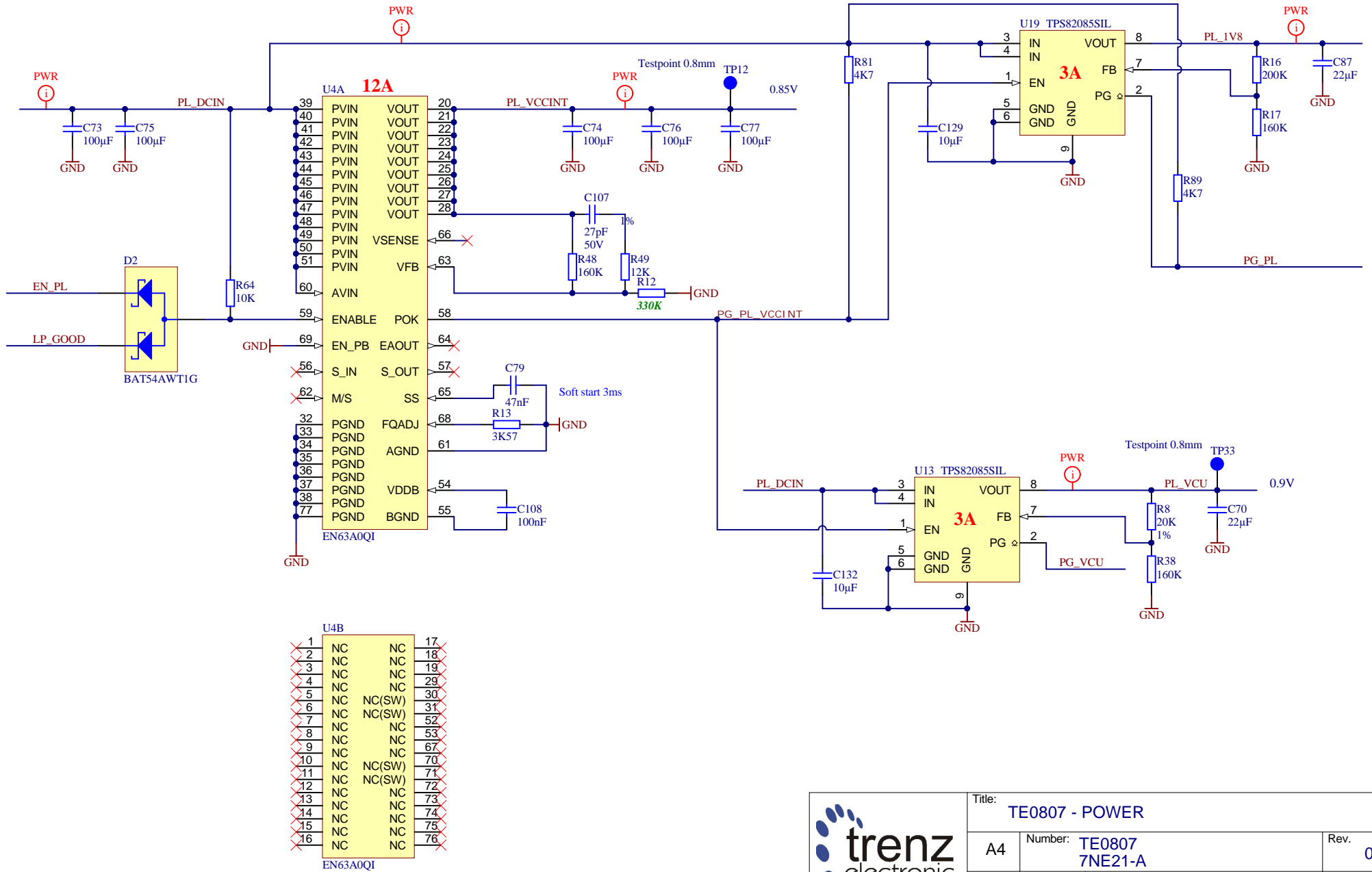

Title: TE0807 - DDR4_3_RAM		
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Filename: DDR4-RAM_3.SchDoc		

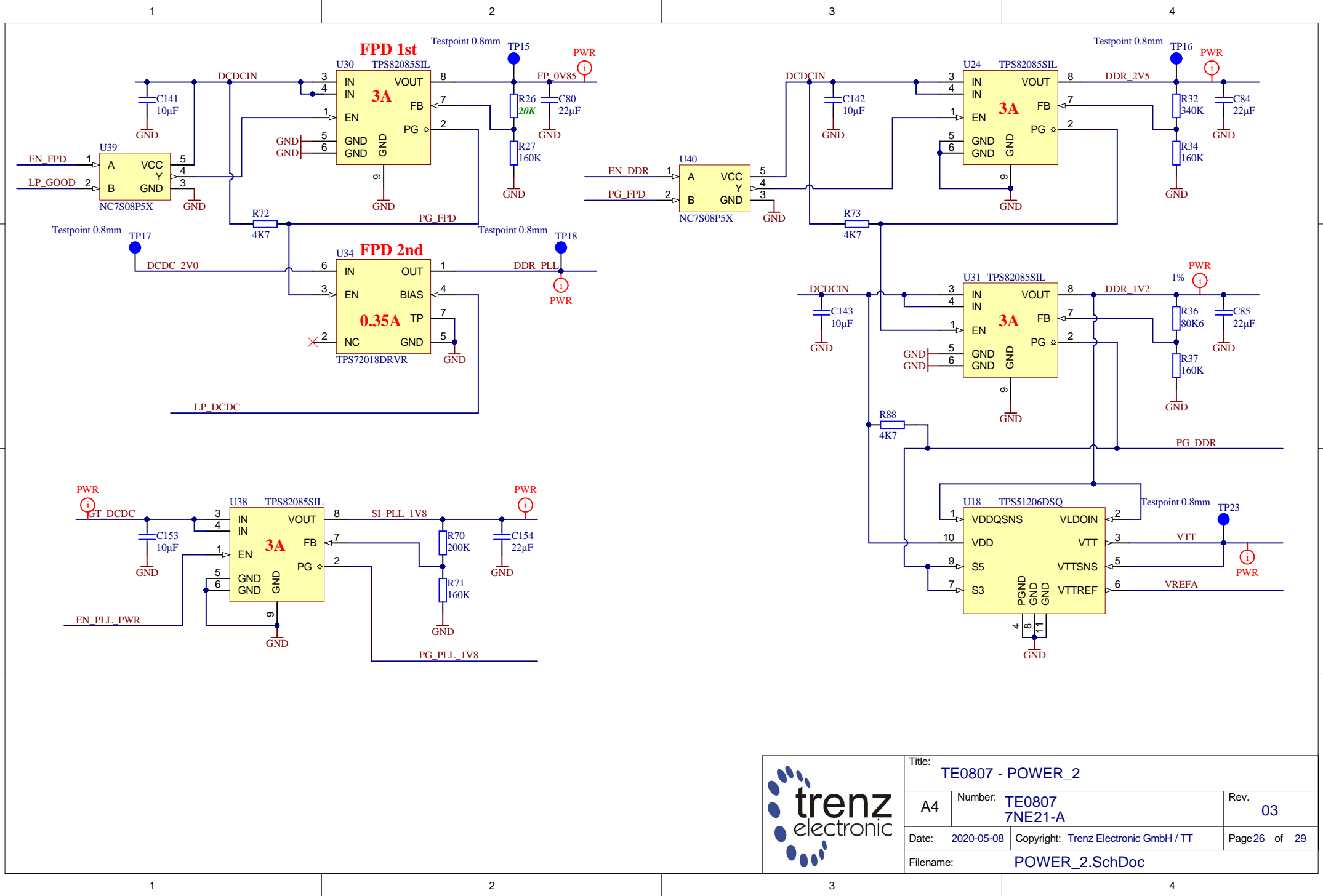
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Filename: DDR4-RAM_4.SchDoc		




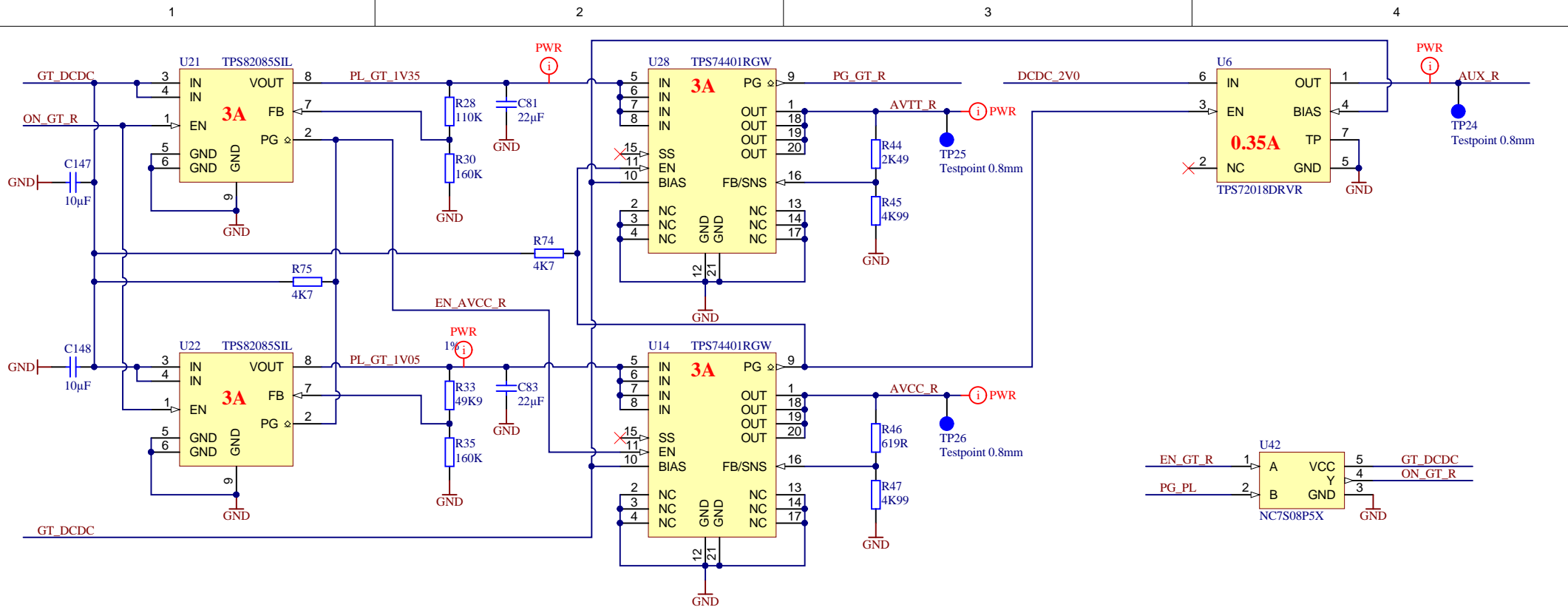
Title: TE0807 - CLOCK		
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Date: 2020-05-08	Copyright: Trenz Electronic GmbH / TT	
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Filename: Clock.SchDoc		





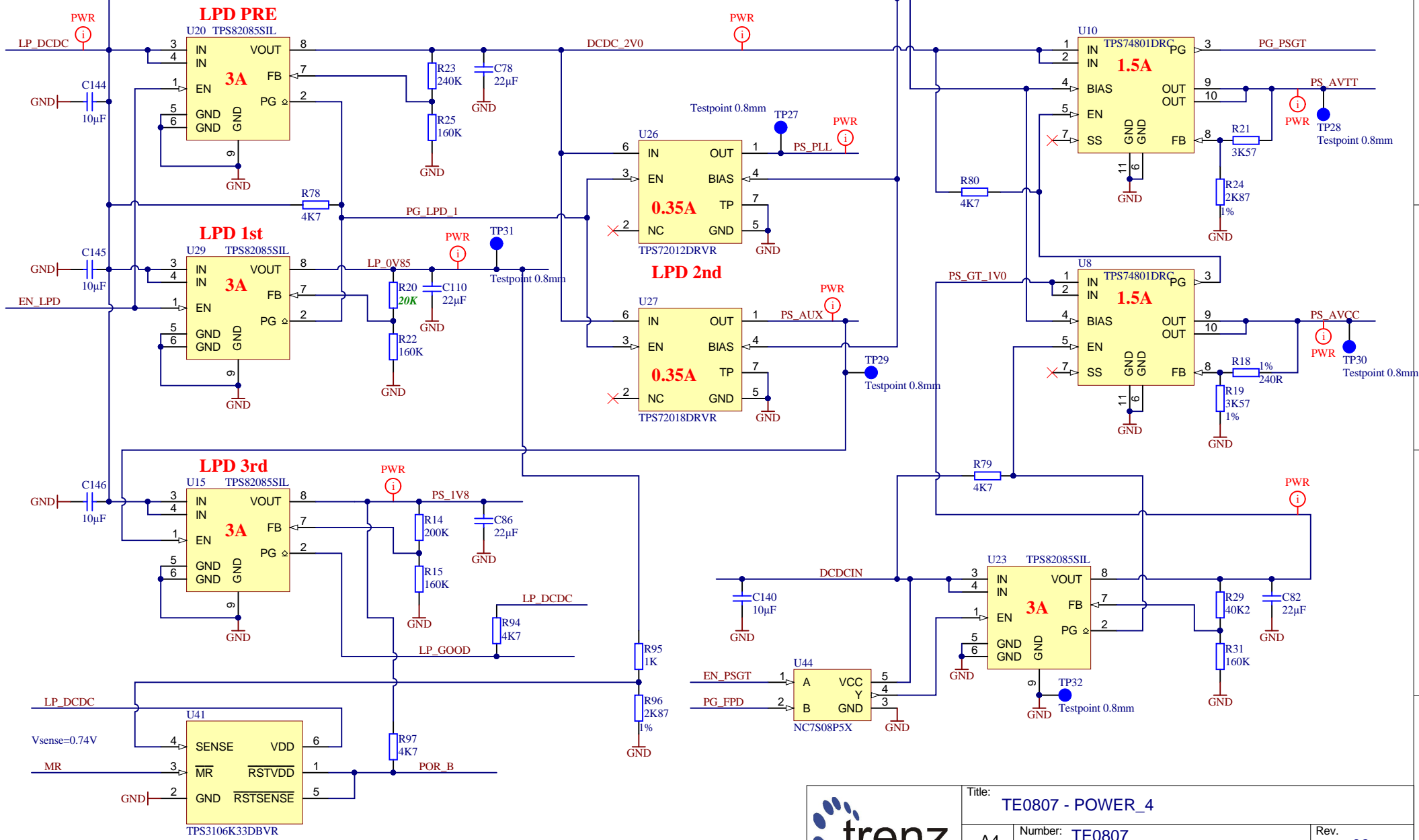
Title: TE0807 - POWER		
A4	Number: TE0807 7NE21-A	Rev. 03
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		Title: TE0807 - POWER_2	
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			Title: TE0807 - POWER_3	
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Title: TE0807 - POWER_4		
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CHANGES REV01 to REV02

- 1) Added EEPROM (U11,24AA025E48T-I/OT)
- 2) Added optional resistors R39/R40 for QSPI flash (do not populated)
- 3) Fixed VCU connection (added additional DCDC and capacitors), recommendation from Xilinx
- 4) Changed obsolete DDR4 chips (NT5AD256M16B2-GN -> K4A8G165WB-BIRC)
- 5) Added net "PG_VCU" to J2 (pin97)
- 6) full update lib

CHANGES REV02 to REV03 (06.2020)

- VT: 1) Fixed ADC connection
 2) Fixed DDR4 connection (support B-die DDR4 chips)
 3) Fixed DDR4 connection (alert_n pin connection)
 4) Added U16
 4) Added testpoints
 5) Full update LIB

A

A

B


B

C

C

D

D

	Title: TE0807 - Changes list		
	A4	Number: TE0807 7NE21-A	Rev. 03
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