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Schematics and other handouts serve for informational purposes only!

	Title: <b>TE0807 – Legal Notices Modules</b>		
	A4	Number: <b>TE0807 4A181-A</b>	Rev. <b>04</b>
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	Filename: <b>Legal Notices Modules.SchDoc</b>		

REV	DATE	Description	
-01	-	Initial revision	-
-02	-	1) Added EEPROM <b>U11</b> (24AA025E48T-I/OT). 2) Added optional resistors <b>R39</b> / <b>R40</b> for QSPI flash (default: not populated). 3) Fixed VCU connection (added additional DCDC and capacitors), recommendation from AMD. 4) Changed obsolete DDR4 chips (NT5AD256M16B2-GN -> K4A8G165WB-BIRC). 5) Added net "PG_VCU" to <b>J2</b> (pin97). 6) Full update LIB.	-
-03	2020-06	1) Fixed ADC connection. 2) Fixed DDR4 connection (support B-die DDR4 chips). 3) Fixed DDR4 connection (alert_n pin connection). 4) Added U16. 5) Added testpoints. 6) Full update LIB.	VT
-04	2024-05	1) Changed DCDC ( <b>U4</b> ) from EN63A0QI to MPQ8633 and adapted according circuit. 2) Changed DCDC ( <b>U13</b> ) from TPS82085SIL/MUN3CAD03-SE to MPM3860GQW-Z and adapted according circuit. 3) Changed DCDC ( <b>U15</b> , <b>U19</b> , <b>U20</b> , <b>U21</b> , <b>U22</b> , <b>U23</b> , <b>U24</b> , <b>U29</b> , <b>U30</b> , <b>U31</b> , <b>U38</b> ) from TPS82085SIL/MUN3CAD03-SE to MPM3834CGPA and adapted according circuit. 4) Changed voltage rail from 1.35 V to 1.45 V via adaption voltage divider resistor <b>R28</b> and <b>R30</b> and changed voltage rail name PL_GT_1V35 to <b>PL_GT_1V45</b> . 5) Changed voltage rail from 1.05 V to 1.15 V via adaption voltage divider resistors <b>R33</b> and <b>R35</b> and changed voltage rail name PL_GT_1V05 to <b>PL_GT_1V15</b> . 6) Changed PLL ( <b>U5</b> ) from Si5345A-B to Si5345A-D-GM. 7) Changed inverted buffer SN74LVC1G06DRL to not inverted buffer SN74LVC1G07DRL ( <b>U16A</b> / <b>U16B</b> ). 8) Added diode <b>D3</b> between <b>U41</b> pin 3 net <b>MR</b> and voltage rail <b>LP_DCDC</b> . 9) Added capacitors <b>C213</b> ... <b>C215</b> for VTT voltage rail <b>VTT</b> . 10) Replaced DDR4 memory chips to use bigger chip sizes. 11) Connected DDR4-TEN signals together for <b>U2A</b> , <b>U3A</b> , <b>U9A</b> , and <b>U12A</b> and pulled them low via 499 Ohm resistor <b>R103</b> . Added testpoint <b>TP3</b> for signal DDR4-TEN. 12) Added remote sense option (default: not fitted): 12.1) <b>R13</b> for <b>U29</b> . 12.2) <b>R90</b> for <b>U30</b> . 12.3) <b>R106</b> for <b>U31</b> . 13) Added decoupling capacitors: 13.1) <b>C136</b> , <b>C149</b> for <b>U1B</b> . 13.2) <b>C155</b> for <b>U1C</b> . 13.3) <b>C151</b> for <b>U1E</b> . 13.4) <b>C152</b> for <b>U1D</b> . 13.5) <b>C205</b> ... <b>C212</b> , <b>C217</b> , and <b>C234</b> for <b>U1N</b> . 13.6) <b>C226</b> ... <b>C228</b> for <b>U6</b> . 13.7) <b>C233</b> for <b>U8</b> . 13.8) <b>C232</b> for <b>U10</b> . 13.9) <b>C156</b> for <b>U11</b> . 13.10) <b>C225</b> for <b>U14</b> . 13.11) <b>C150</b> for <b>U16B</b> . 13.12) <b>C216</b> , <b>C219</b> , and <b>C220</b> ... <b>C223</b> for <b>U18</b> . 13.13) <b>C230</b> for <b>U26</b> . 13.14) <b>C231</b> for <b>U27</b> . 13.15) <b>C224</b> for <b>U28</b> . 13.16) <b>C218</b> for <b>U34</b> . 13.17) <b>C201</b> for <b>U39</b> . 13.18) <b>C202</b> for <b>U40</b> . 13.19) <b>C229</b> for <b>U41</b> . 13.20) <b>C203</b> for <b>U42</b> . 13.21) <b>C204</b> for <b>U44</b> . 14) Added pull-up resistors for HOLD ( <b>R92</b> ) and WP ( <b>R93</b> ) signals for Flash <b>U7A</b> .	ED/MR

A

A

B

B

C

C


D

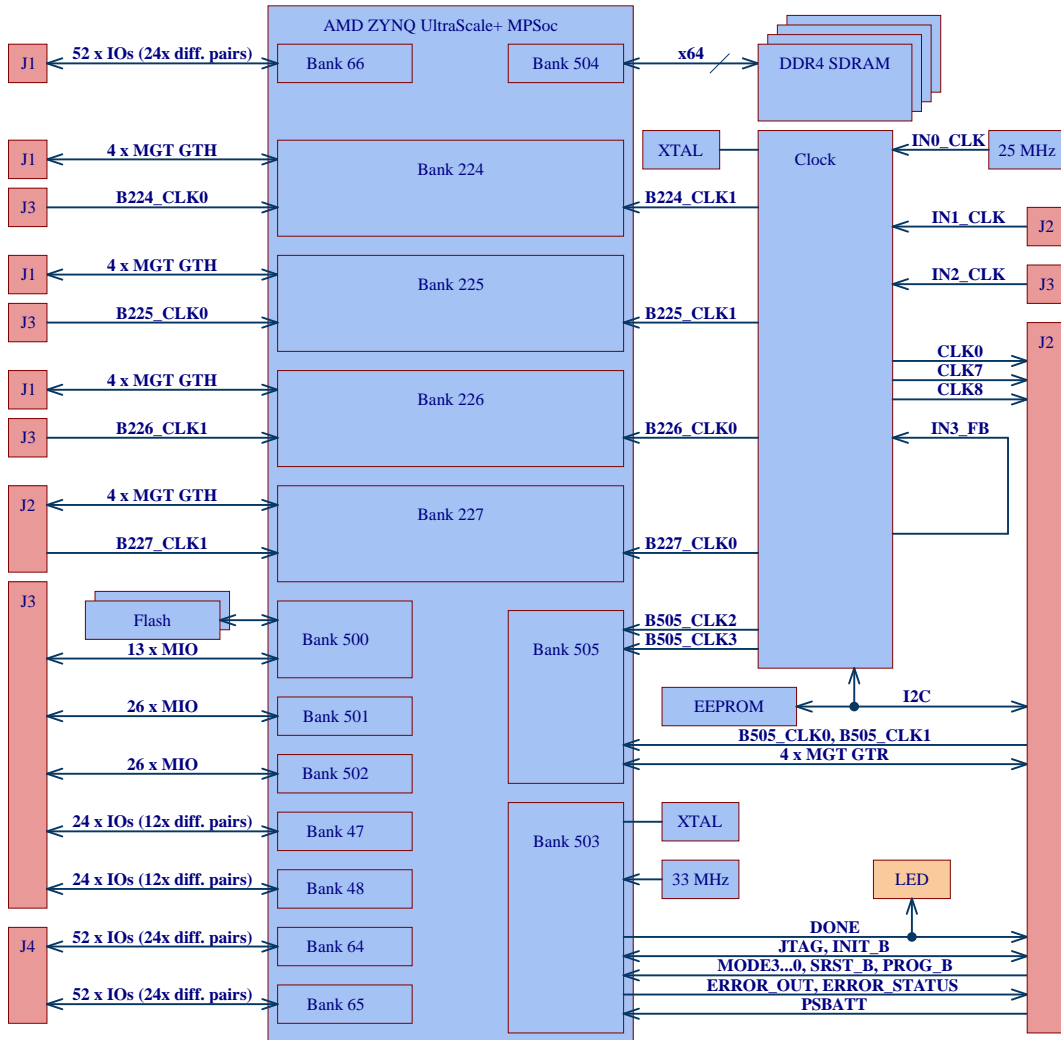
D



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REV	DATE	Description (continued...)	
-04	2024-05	<p>15) Added pull-up resistors for HOLD (R100) and WP (R102) signals for Flash U17A.</p> <p>16) Added pull-up resistor (R107) (default: not fitted) and pull-down resistor (R109) (default: fitted) for signal POR_OVERRIDE (U1A).</p> <p>17) Changed 10 nF capacitor (C112) from 16 V, 0402 to 10 V, 0201.</p> <p>18) Changed 100 nF capacitor (C37, C79, C95, C96, C130, C131, C133) from 6.3 V, X5R, 0201 to 50 V, X7R, 0402.</p> <p>19) Changed capacitor (C12, C13, C14, C15, C16, C18, C19, C20, C21, C42, C44, C45, C170, C171) from 4.7 µF to 10 µF.</p> <p>20) Changed 10 µF capacitor (C65, C66, C67) from 16 V, 0603 to 6.3 V, 0402.</p> <p>21) Changed 100 µF capacitor (C29, C30, C31, C32, C35, C36, C43, C46, C52, C166, C167, C168, C169) from 6.3 V, 1206 to 4 V, 0805.</p> <p>22) Changed 47 µF capacitor (C22, C23, C24, C25, C26, C27, C28, C33, C34, C68, C69, C70, C74, C76, C77, C78, C80, C81, C82, C83, C84, C85, C86, C87, C88, C110, C154, C198, C199, C200, C205) from 0805 to 0603.</p> <p>23) Changed ferrid bead (L1, L2, L3, L4, L5, L7) from BKP0603HS121-T to MPZ0603S121HT000.</p> <p>24) Changed resistor (R41, R58) from 2 kOhm to 2.49 kOhm.</p> <p>25) Changed resistor (R74) from 4.7 kOhm, 0201 to 10 kOhm, 0402.</p> <p>26) Added testpoints TP4, TP6...TP9, TP11, TP13, TP14, TP19...TP22, TP34...TP67.</p> <p>27) Added Trezz address on PCB.</p> <p>28) Added CE-, UKCA- RoHS-, and WEEE-logo.</p> <p>29) Updated components from library.</p> <p>30) Changed signal trace length.</p> <p>31) Updated documentation.</p>	ED/MR

	Title: TE0807 – Revision_Changes_2		
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### Supported Voltage Ranges:

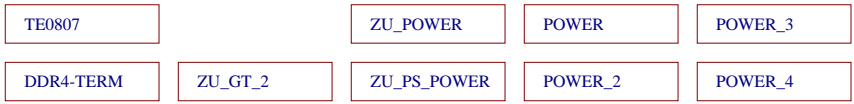
Power Rail	Direction	Range	Tolerance	Description	Note
PL_DCIN	IN	3.3 V	+/- 3 %	Micromodule Power	Programmable Logic
LP_DCDC	IN	3.3 V	+/- 3 %	Micromodule Power	Low-Power Domain
GT_DCDC	IN	3.3 V	+/- 3 %	Micromodule Power	GTH/GTY Transceiver
DCDCIN	IN	3.3 V	+/- 5 %	Micromodule Power	Full-Power Domain and GTR
VCCO_64	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 64	-
VCCO_65	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 65	-
VCCO_66	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 66	-
VCCO_47	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 47	-
VCCO_48	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 48	-
PSBATT	IN	1.2 V - 1.5 V	-	RTC / BBRAM	-
PLL_3V3	IN	3.3 V	+/- 5 %	PLL Core Power	-
PL_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Programmable Logic
PS_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Processing System
SI_PLL_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Clock Supply
DDR_1V2	OUT	1.2 V	+/- 3 %	Power for Carrier	PS DDR I/O Supply

### I2C Address:

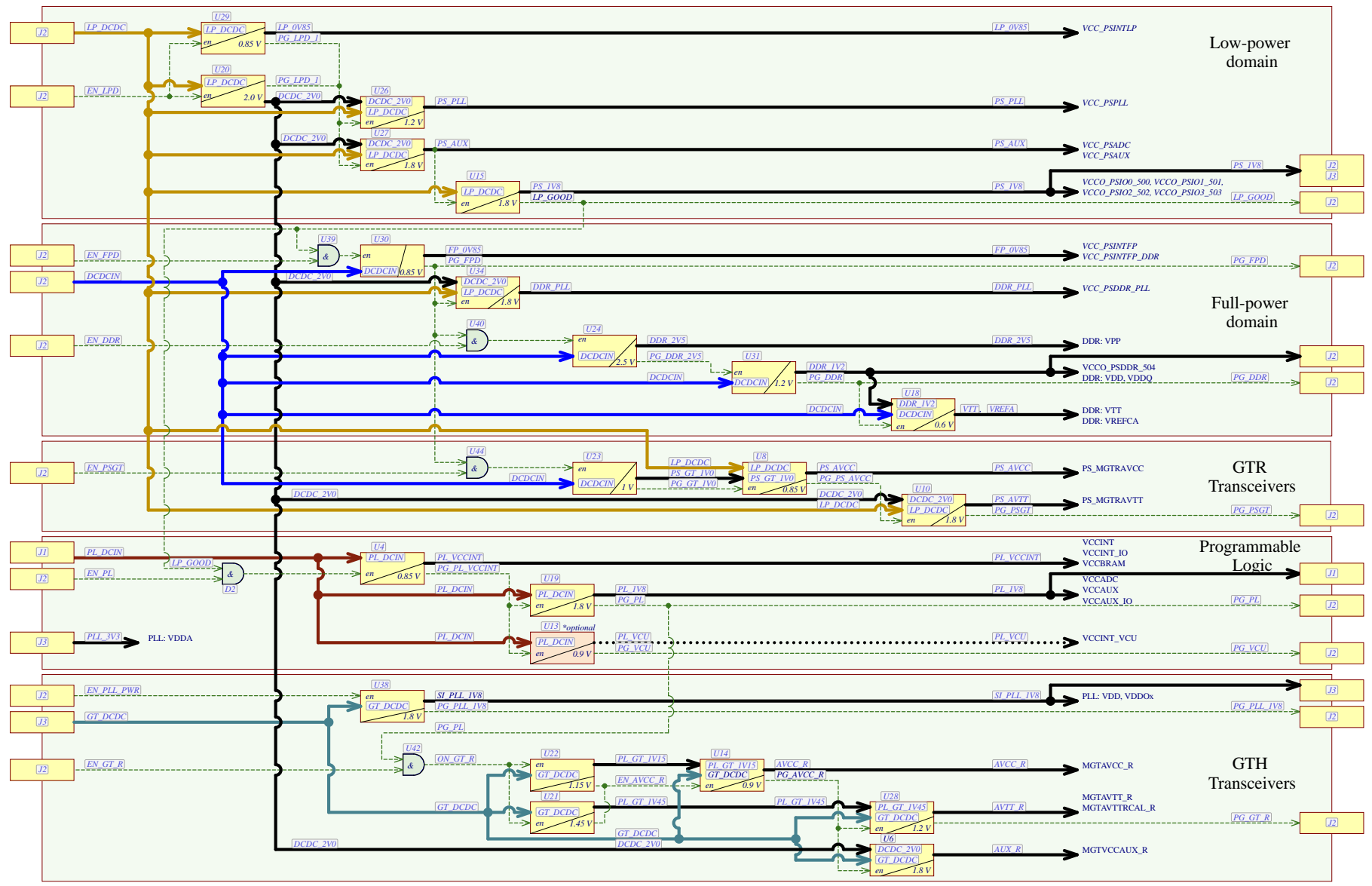
Device	I2C ADDR	Note
PLL <b>U5</b>	0x69	-
EEPROM <b>U11</b>	0x50	-

### Legend:

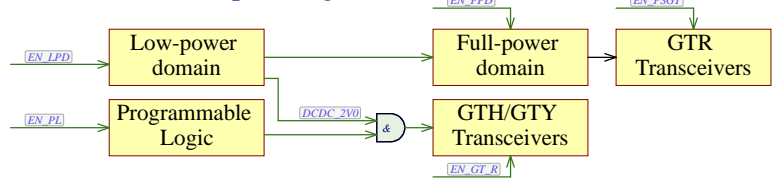
- B2B Connector
- LED Interface
- On-board Components



Title: <b>TE0807 – Overview</b>		
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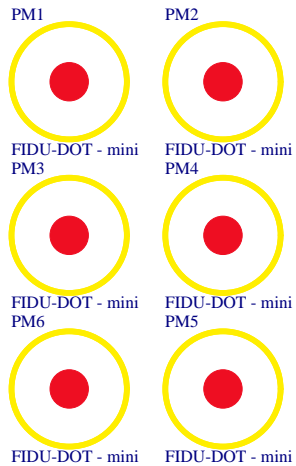
Power-on sequencing:



Title: TE0807 - Power_Diagram		
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Special notes:



Serial  
Serialnummer 6,3 x 6.3mm  
LOGO1

TE Logo PRINT Layer

LOGO PRINT  
MECH1

TE Address Overlay

LOGO ADDRESS  
CE1

CE Logo on Top Overlay

CE-TOPOVERLAY  
UKCA1

UKCA Logo on Top Overlay

UKCA-TOPOVERLAY

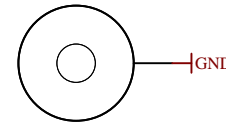
RoHS1

RoHS Logo on Top Overlay

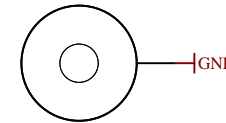
RoHS-TOPOVERLAY  
WEEE1

WEEE Logo on Top Overlay

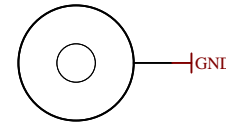
WEEE-TOPOVERLAY



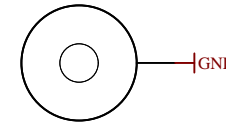
Mount.Hole 3.2mm für Unterlegscheibe



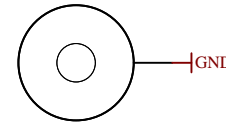
Mount.Hole 3.2mm für Unterlegscheibe



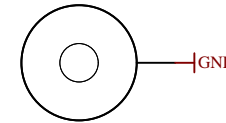
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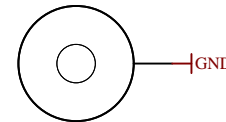
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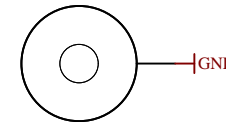
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe

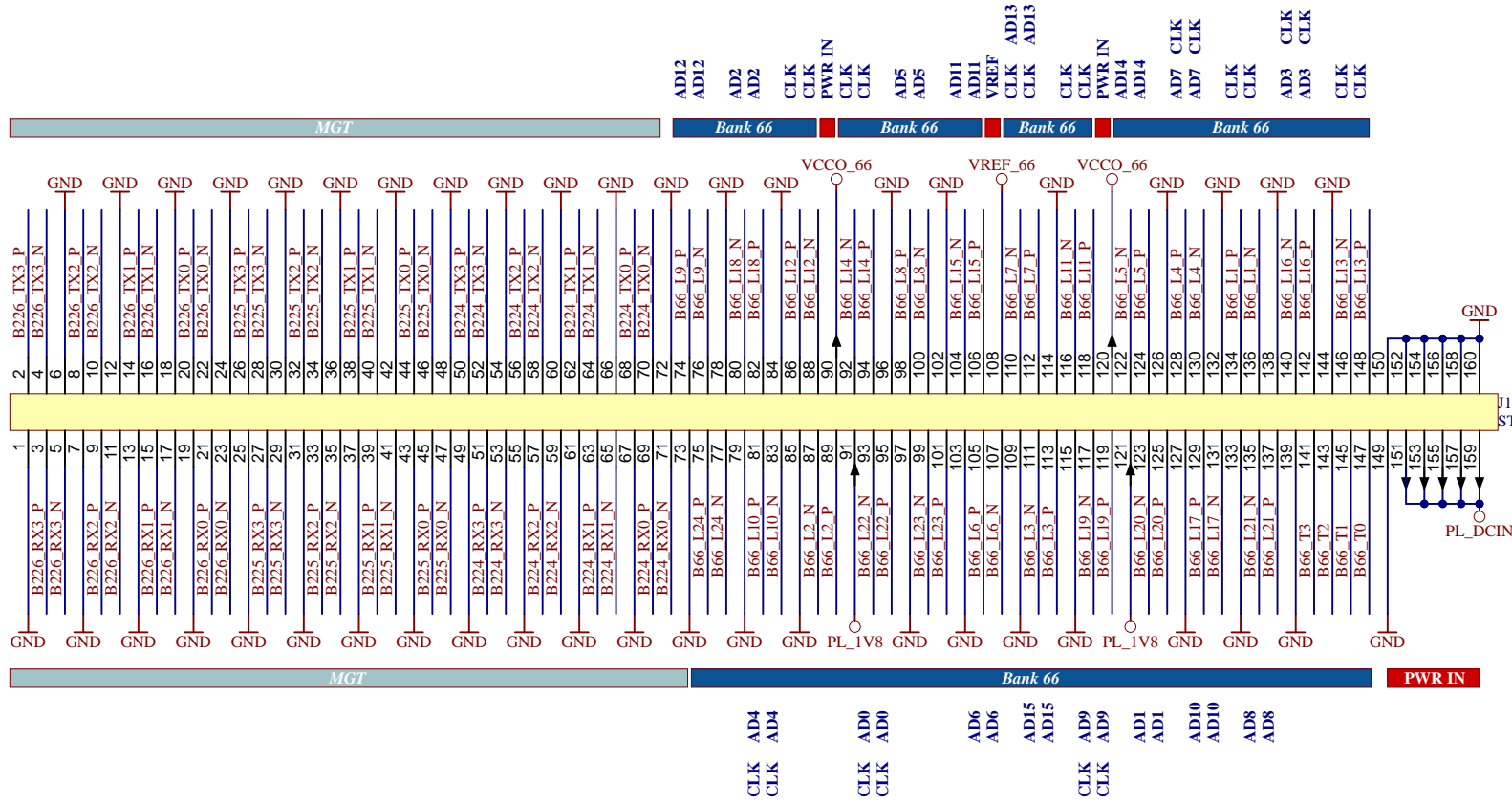
Design drawn by: ED/MR  
Checked by: MT  
Assembly variant: 4AI81-A  
Created by: ED  
Modified by: ED  
Modified at: 2024-05-01



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B224 GTH 4 Lanes  
 B225 GTH 4 Lanes  
 B226 GTH 4 Lanes  
 B66 52 IO, 24 LVDS Pairs

Consider AC coupling for MGT signals!



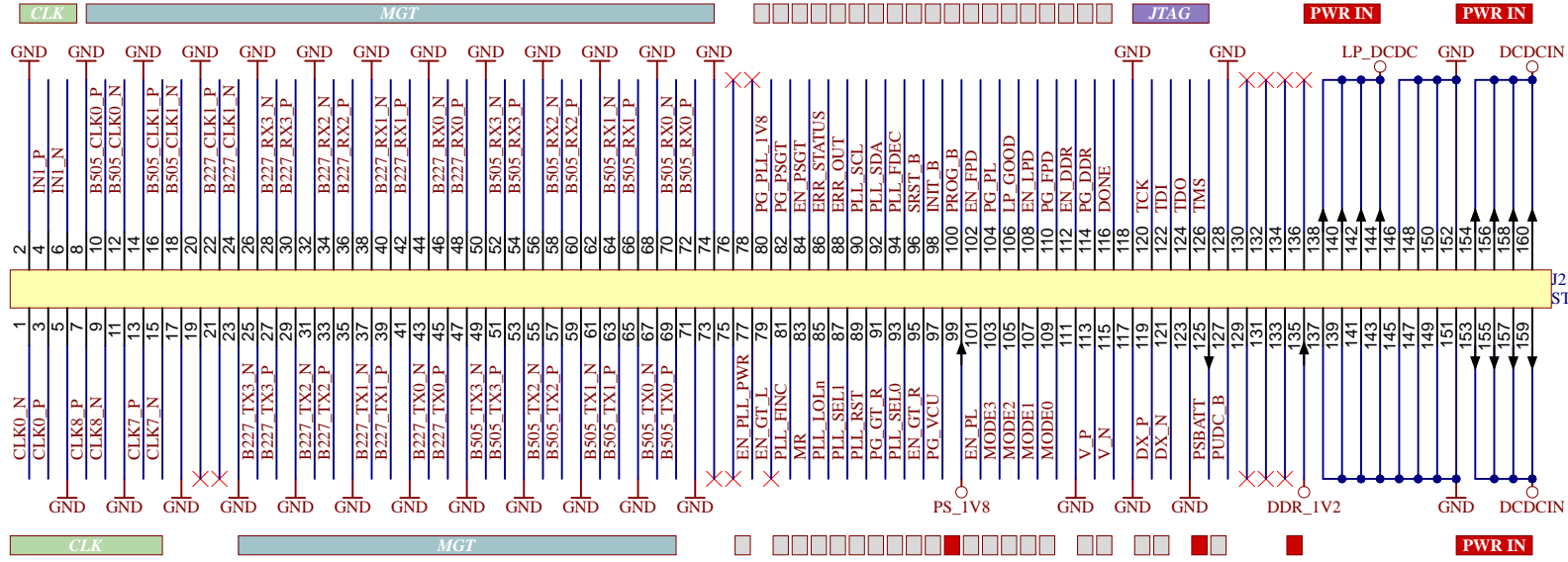
- Bank 47 HD 0..VCCO47
- Bank 48 HD 0..VCCO48
- Bank 64 HP 0..VCCO64
- Bank 65 HP 0..VCCO65
- Bank 66 HP 0..VCCO66



Title: TE0807 – Connector J1		
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JTAG I2C  
 PLL CLK IN  
 3x PLL CLK OUT  
 B505 GTR 2 CLK IN  
 B505 GTR 4 Lanes  
 B227 GTH 4 Lanes  
 B227 GTH CLK IN

Consider AC coupling for MGT signals!



- Bank 47 HD 0..VCC047
- Bank 48 HD 0..VCC048
- Bank 64 HP 0..VCC064
- Bank 65 HP 0..VCC065
- Bank 66 HP 0..VCC066



Title: TE0807 – Connector J2		
A4	Number: TE0807 4AI81-A	Rev. 04
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1

2

3

4

1

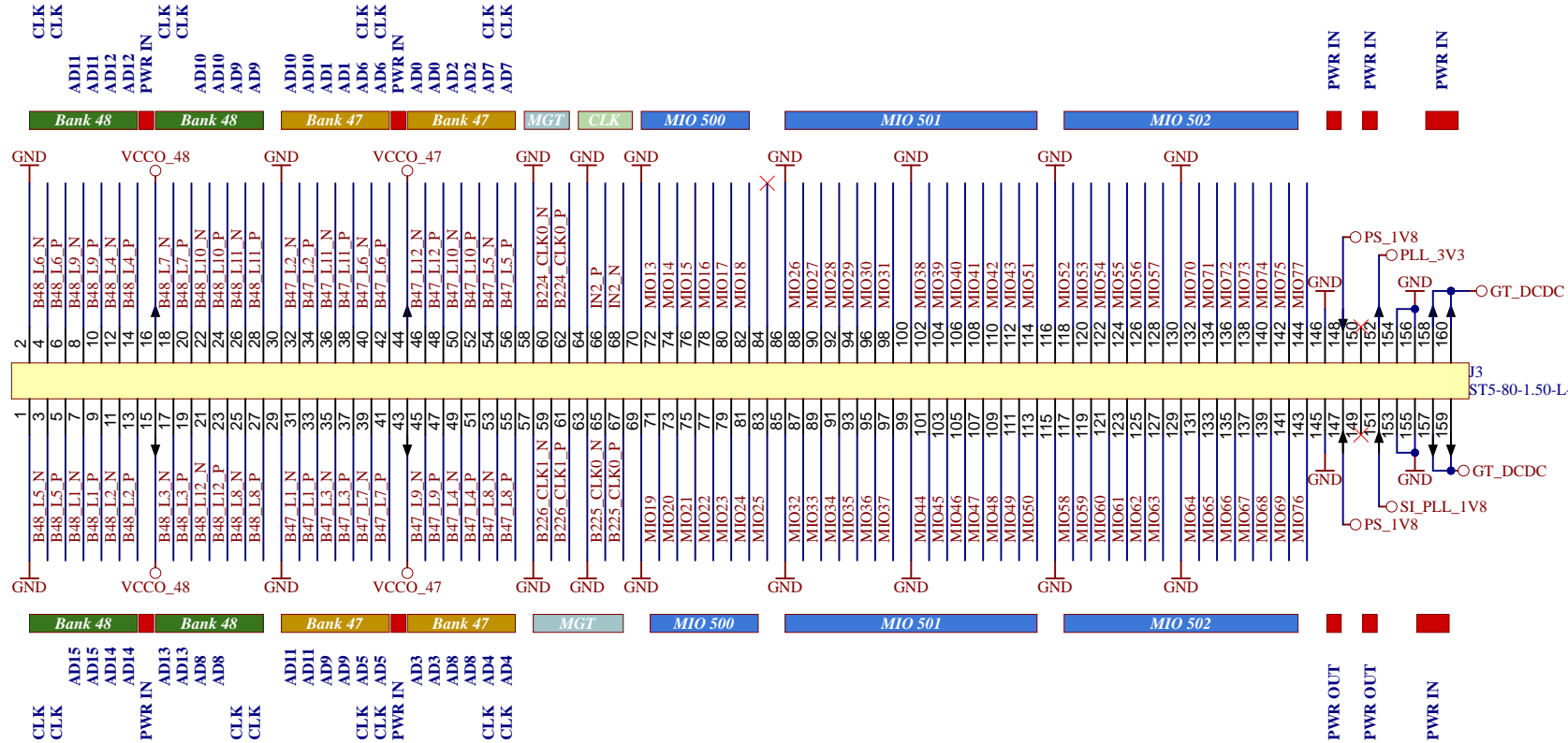
2

3

4

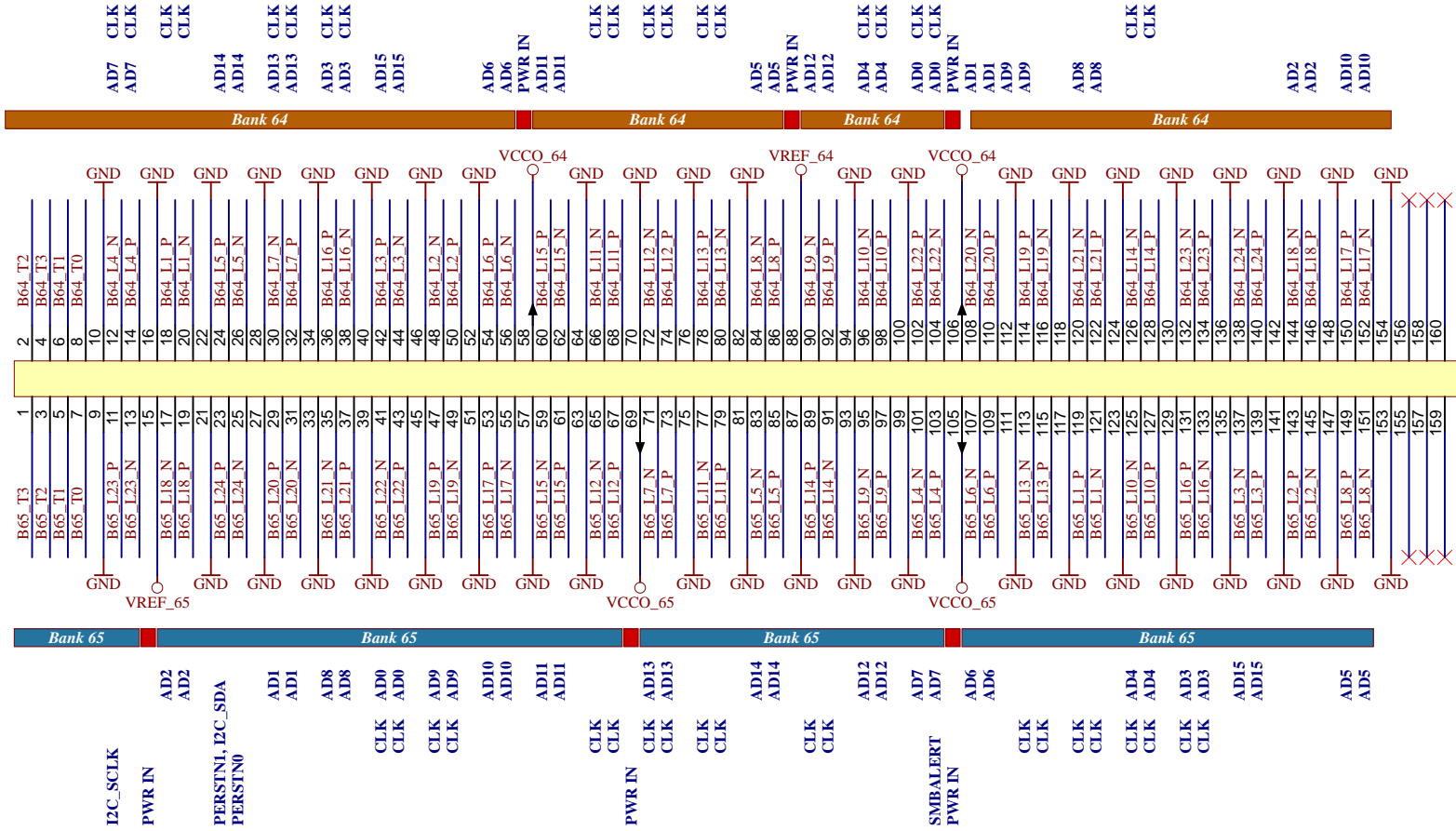


B47 24 IO, 12 LVDS Pairs  
 B48 24 IO, 12 LVDS Pairs  
 B224 GTH CLK IN  
 B225 GTH CLK IN  
 B226 GTH CLK IN  
 65 MIO  
 PLL CLK IN



Title: TE0807 – Connector J3		
A4	Number: TE0807 4AI81-A	Rev. 04
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B64 52 IO, 24 LVDS Pairs  
 B65 52 IO, 24 LVDS Pairs

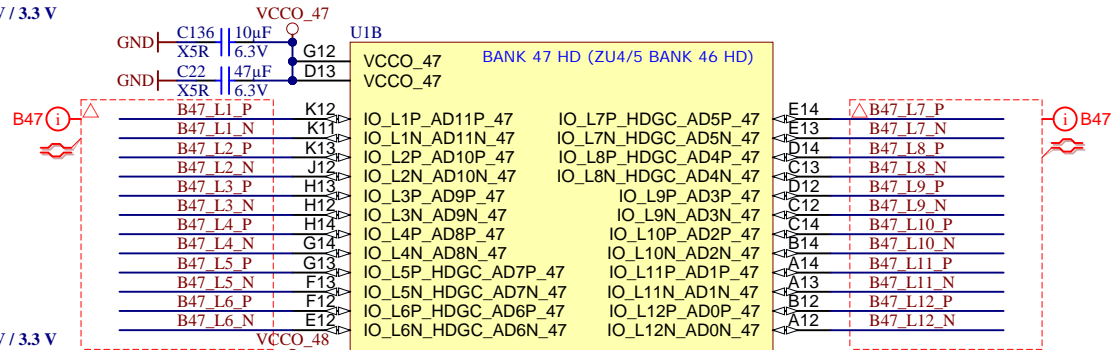


- Bank 47 HD 0..VCCO47
- Bank 48 HD 0..VCCO48
- Bank 64 HP 0..VCCO64
- Bank 65 HP 0..VCCO65
- Bank 66 HP 0..VCCO66

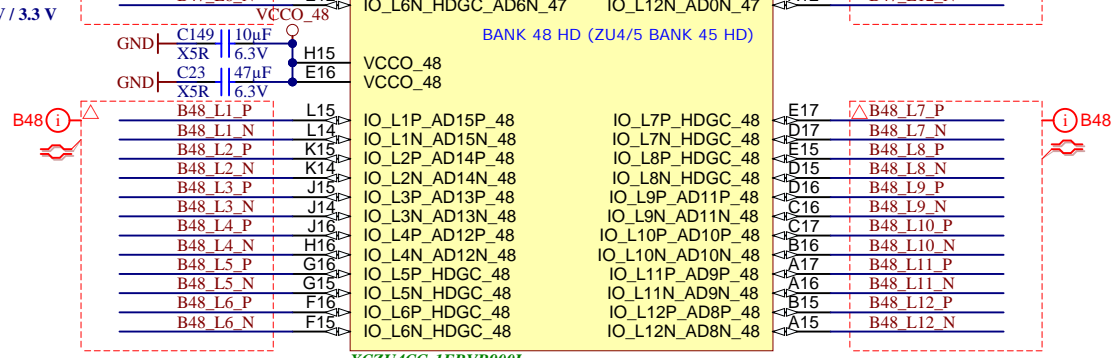


Title: TE0807 – Connector J4		
A4	Number: TE0807 4AI81-A	Rev. 04
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1.2 V / 1.35 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V



1.2 V / 1.35 V / 1.5 V / 1.8 V / 2.5 V / 3.3 V



XCZU4CG-1FBV9001



Title: TE0807 – HD Banks		
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1

2

3

4

A

A

B

B

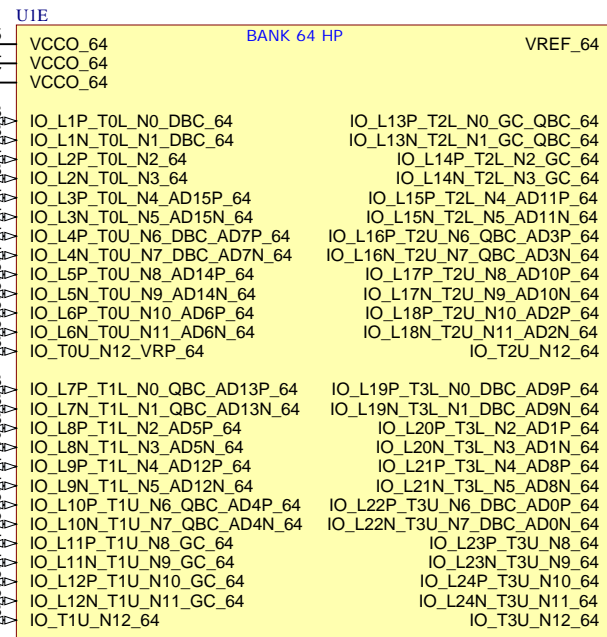
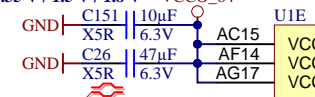
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C

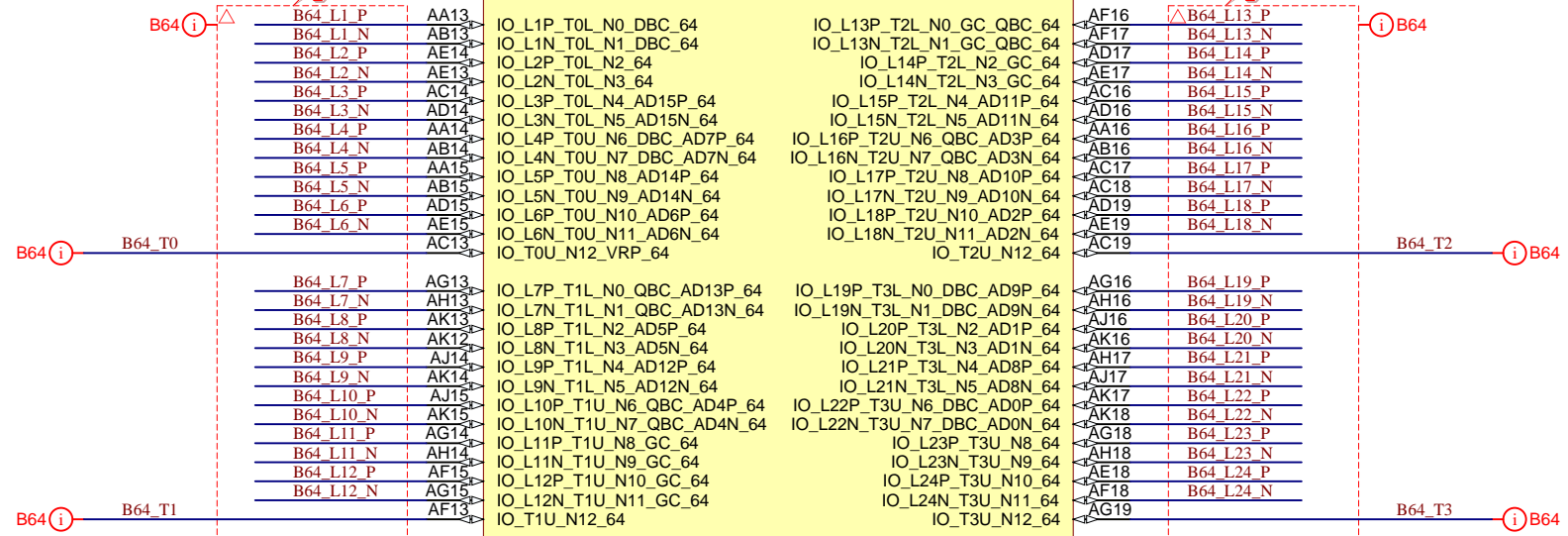
D

D

1.0 V / 1.2 V / 1.35 V / 1.5 V / 1.8 V VCCO\_64



XCZU4CG-1FBVB9001



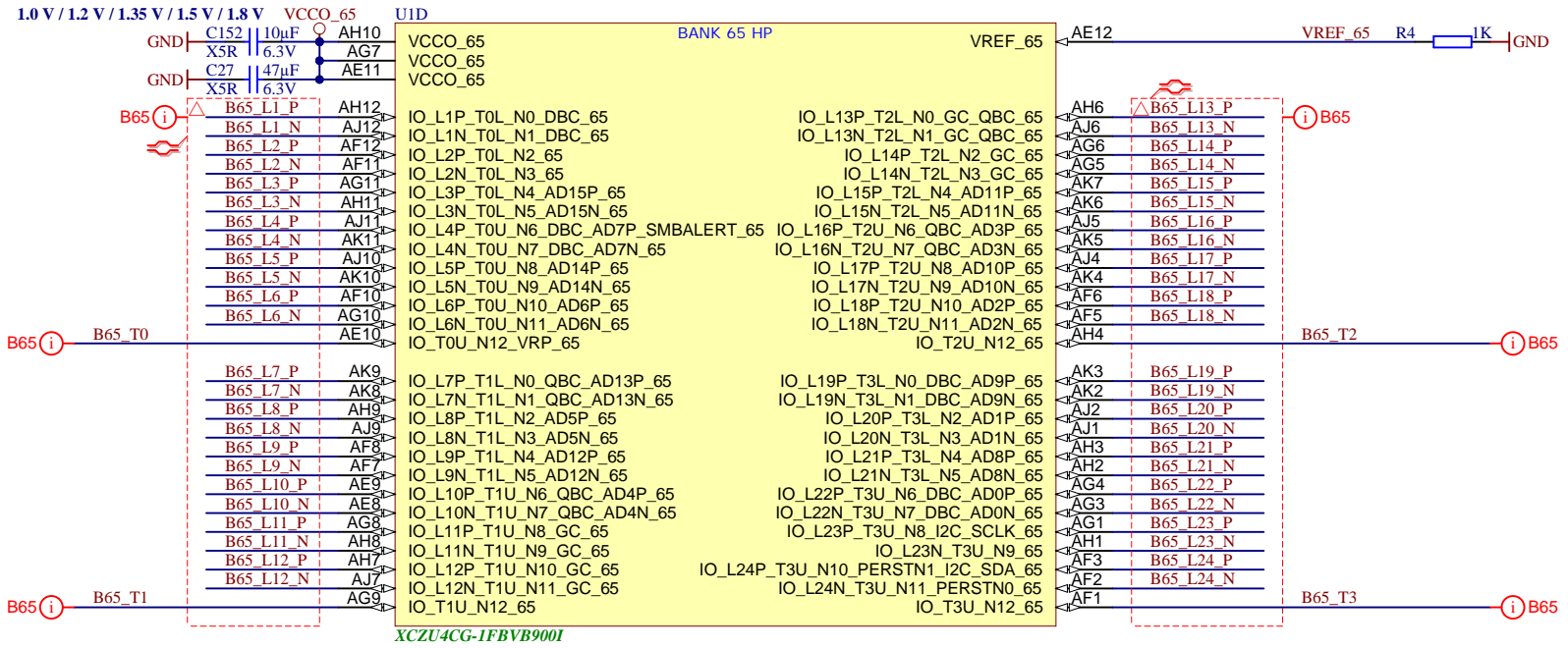
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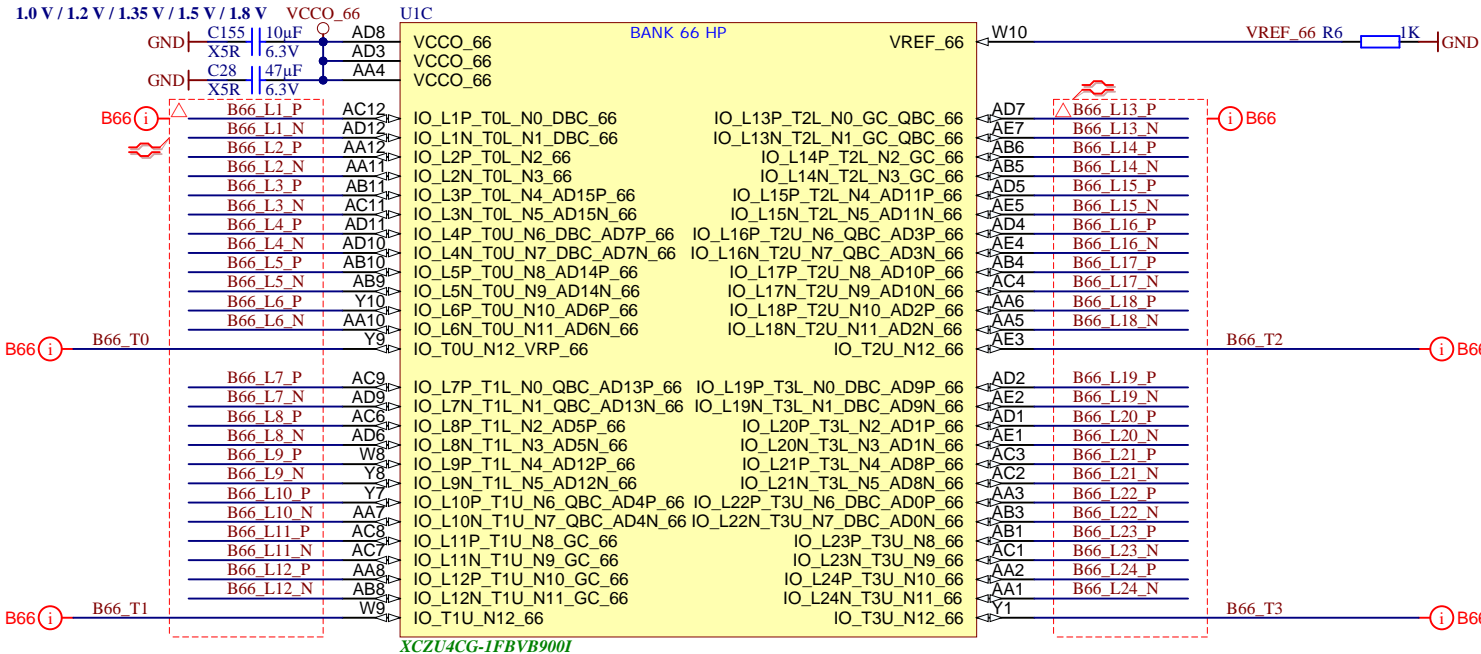

2

3

4

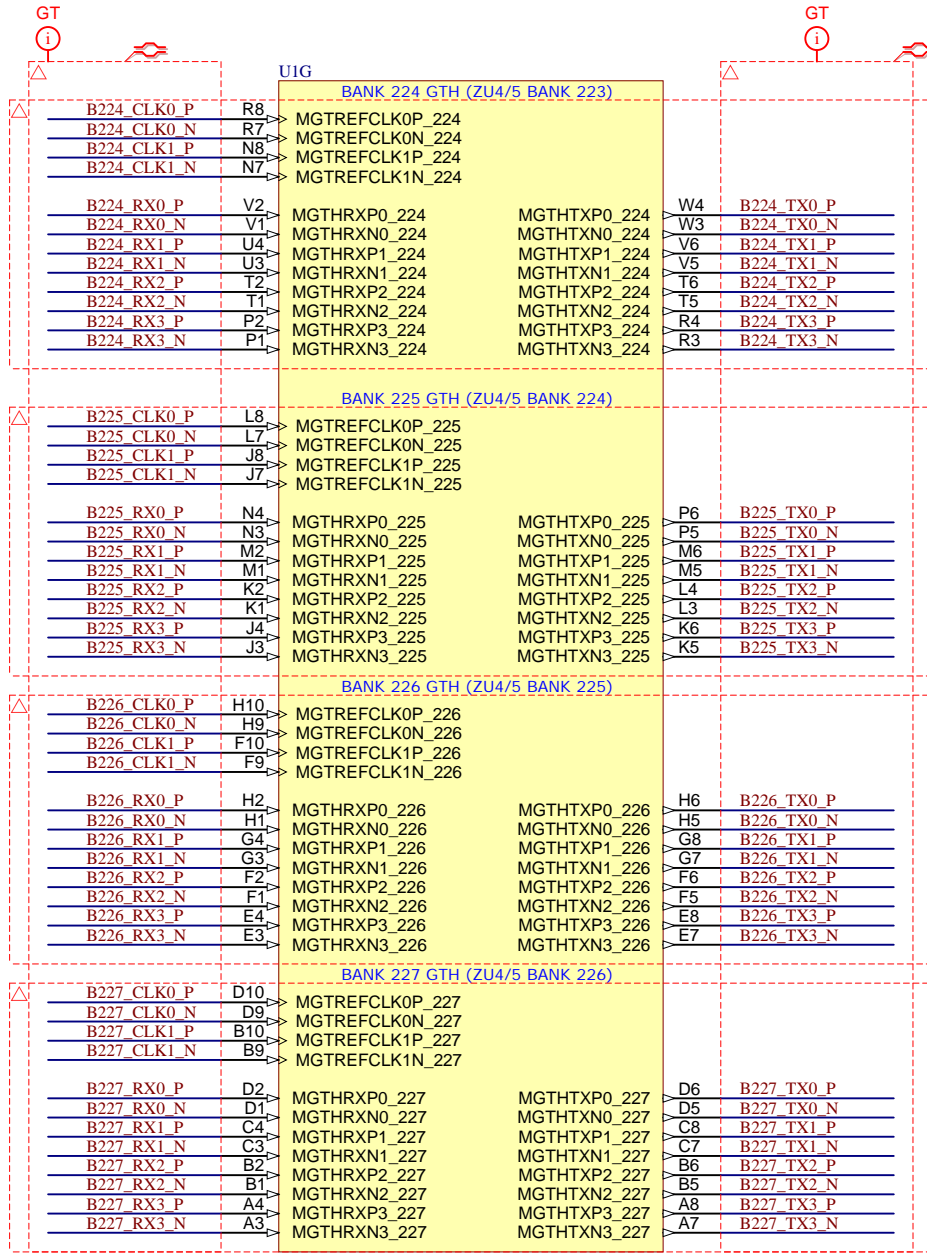


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228

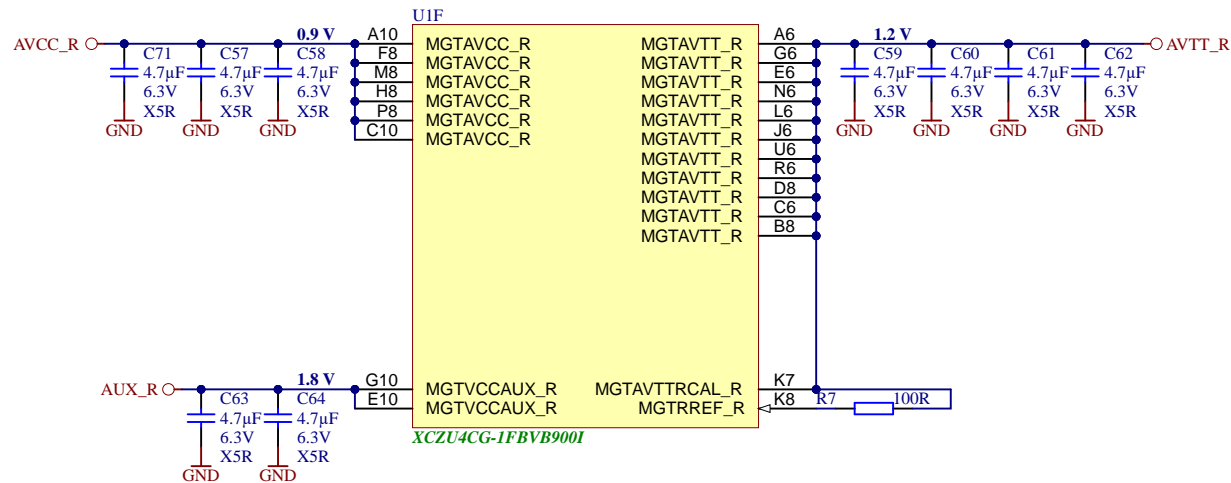
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230

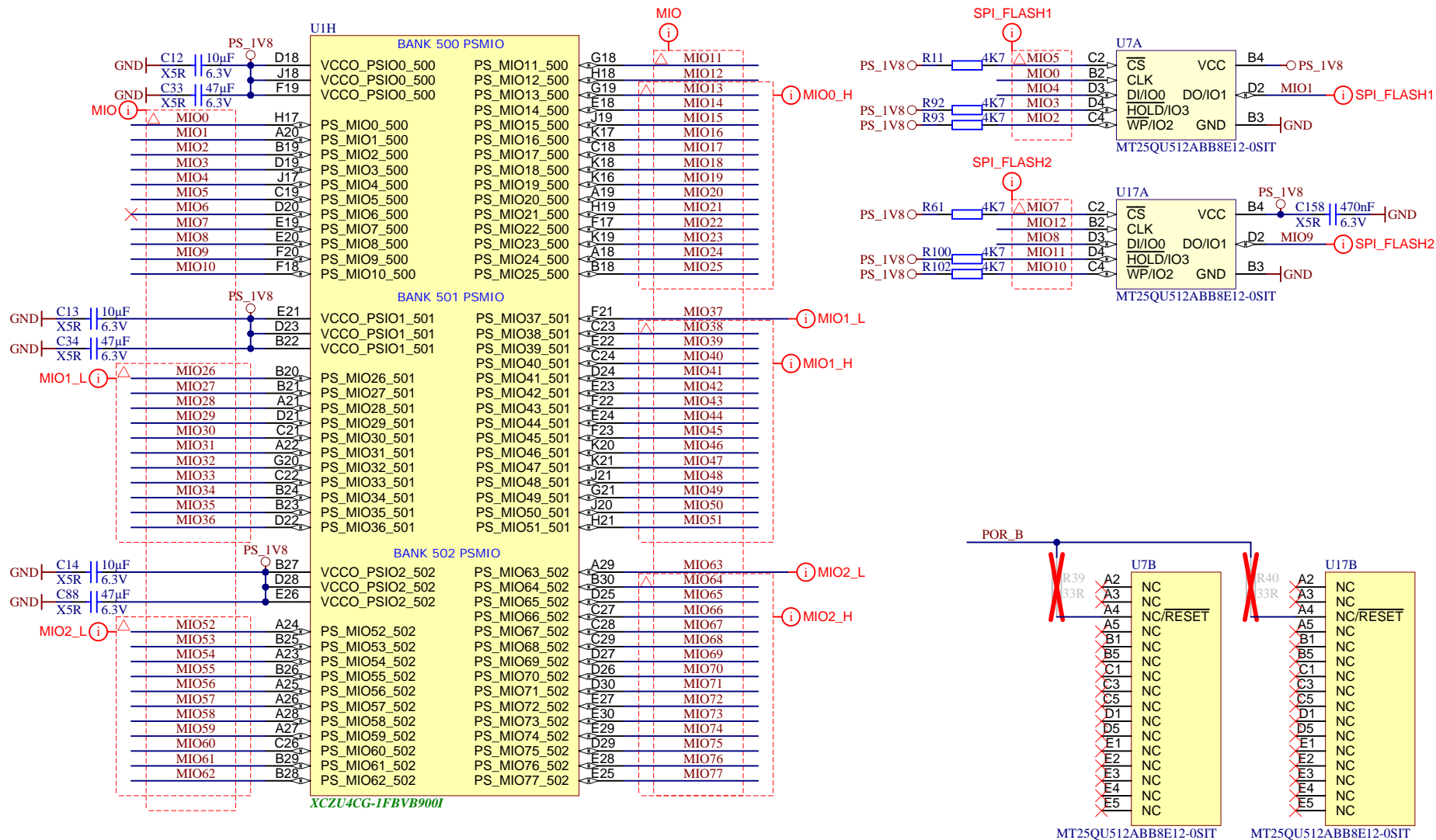
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Title: TE0807 – GTH Banks		
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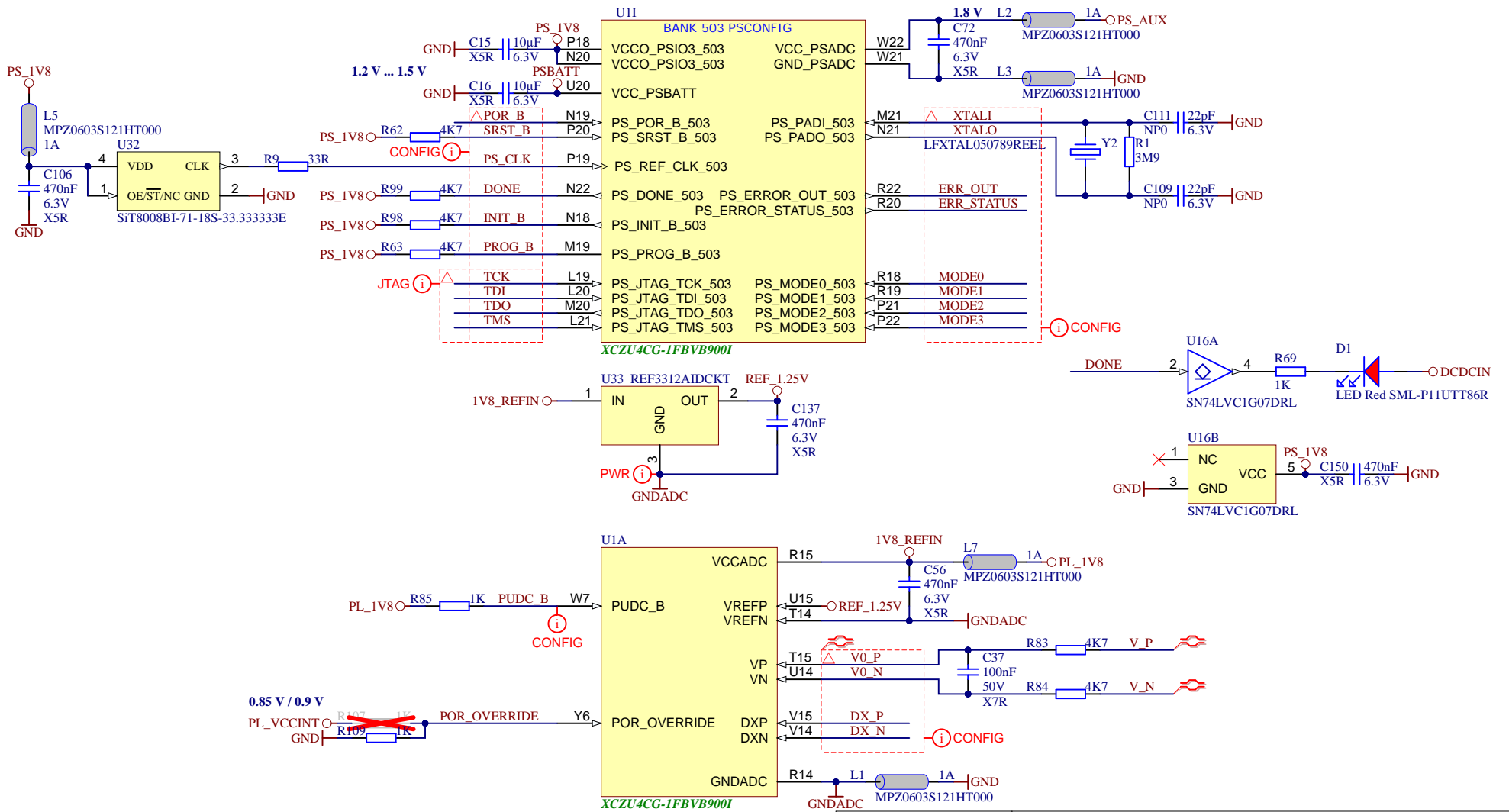


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			Title: <b>TE0807 – Config</b>	
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A

A

B

B

C

C

D

D

**UIJ**

**BANK 504 PSDDR**

VCCO_PSDDR_504	PS_DDR_CK0_504	AE30	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK_N0_504	AF30	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0_504	AC30	DDR4-CKE0
VCCO_PSDDR_504	PS_DDR_CK1_504	AF28	
VCCO_PSDDR_504	PS_DDR_CK_N1_504	AG28	
VCCO_PSDDR_504	PS_DDR_CKE1_504	AB28	
VCC_PSDDR_PLL	PS_DDR_A0_504	AH30	DDR4-A0
VCC_PSDDR_PLL	PS_DDR_A1_504	AG30	DDR4-A1
VCC_PSDDR_PLL	PS_DDR_A2_504	AK29	DDR4-A2
VCC_PSDDR_PLL	PS_DDR_A3_504	AJ30	DDR4-A3
VCC_PSDDR_PLL	PS_DDR_A4_504	AK28	DDR4-A4
VCC_PSDDR_PLL	PS_DDR_A5_504	AK27	DDR4-A5
VCC_PSDDR_PLL	PS_DDR_A6_504	AF27	DDR4-A6
VCC_PSDDR_PLL	PS_DDR_A7_504	AE27	DDR4-A7
VCC_PSDDR_PLL	PS_DDR_A8_504	AF26	DDR4-A8
VCC_PSDDR_PLL	PS_DDR_A9_504	AG26	DDR4-A9
VCC_PSDDR_PLL	PS_DDR_A10_504	AE29	DDR4-A10
VCC_PSDDR_PLL	PS_DDR_A11_504	AE28	DDR4-A11
VCC_PSDDR_PLL	PS_DDR_A12_504	AH29	DDR4-A12
VCC_PSDDR_PLL	PS_DDR_A13_504	AG29	DDR4-A14
VCC_PSDDR_PLL	PS_DDR_A14_504	AJ29	DDR4-A15
VCC_PSDDR_PLL	PS_DDR_A15_504	AH27	DDR4-A16
VCC_PSDDR_PLL	PS_DDR_A16_504	AJ27	DDR4-A17
VCC_PSDDR_PLL	PS_DDR_A17_504	AJ27	DDR4-A17
PS_DDR_CS_N0_504	PS_DDR_CS_N1_504	AD30	DDR4-CS
PS_DDR_CS_N0_504	PS_DDR_CS_N1_504	AD29	
PS_DDR_BA0_504	PS_DDR_BA1_504	AD27	DDR4-BA0
PS_DDR_BA0_504	PS_DDR_BA1_504	AC26	DDR4-BA1
PS_DDR_BG0_504	PS_DDR_BG1_504	AC28	DDR4-BG0
PS_DDR_BG0_504	PS_DDR_BG1_504	AC27	DDR4-BG1
PS_DDR_PARITY_504	PS_DDR_RAM_RST_N_504	AB26	DDR4-PAR
PS_DDR_RAM_RST_N_504	PS_DDR_ACT_N_504	AB25	DDR4-RESET
PS_DDR_ACT_N_504	PS_DDR_ALERT_N_504	AD26	DDR4-ACT
PS_DDR_ALERT_N_504	PS_DDR_ALERT_N_504	AB24	DDR4-ALERT
PS_DDR_ZQ_504	PS_DDR_ZQ_504	AB23	R2 240R
PS_DDR_ODT0_504	PS_DDR_ODT1_504	AB30	DDR4-ODT0
PS_DDR_ODT0_504	PS_DDR_ODT1_504	AC29	

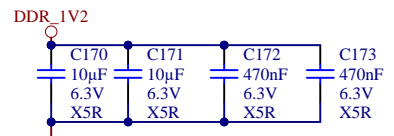
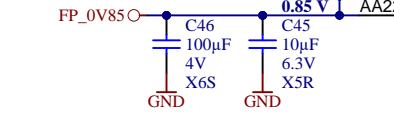
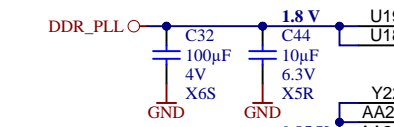
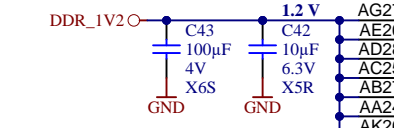
*XCZU4CG-1FBVB900I*

**UIK**

**BANK 504 PSDDR**

PS_DDR_DQ0_504	PS_DDR_DQ32_504	AH22	DQ0
PS_DDR_DQ1_504	PS_DDR_DQ33_504	AH21	DQ1
PS_DDR_DQ2_504	PS_DDR_DQ34_504	AJ22	DQ2
PS_DDR_DQ3_504	PS_DDR_DQ35_504	AK22	DQ3
PS_DDR_DQ4_504	PS_DDR_DQ36_504	AK20	DQ4
PS_DDR_DQ5_504	PS_DDR_DQ37_504	AJ19	DQ5
PS_DDR_DQ6_504	PS_DDR_DQ38_504	AK19	DQ6
PS_DDR_DQ7_504	PS_DDR_DQ39_504	AH19	DQ7
PS_DDR_DQ8_504	PS_DDR_DQ40_504	AH23	DQ8
PS_DDR_DQ9_504	PS_DDR_DQ41_504	AK23	DQ9
PS_DDR_DQ10_504	PS_DDR_DQ42_504	AG24	DQ10
PS_DDR_DQ11_504	PS_DDR_DQ43_504	AJ24	DQ11
PS_DDR_DQ12_504	PS_DDR_DQ44_504	AJ26	DQ12
PS_DDR_DQ13_504	PS_DDR_DQ45_504	AK25	DQ13
PS_DDR_DQ14_504	PS_DDR_DQ46_504	AG25	DQ14
PS_DDR_DQ15_504	PS_DDR_DQ47_504	AH26	DQ15
PS_DDR_DQ16_504	PS_DDR_DQ48_504	AD22	DQ16
PS_DDR_DQ17_504	PS_DDR_DQ49_504	AE22	DQ17
PS_DDR_DQ18_504	PS_DDR_DQ50_504	AF22	DQ18
PS_DDR_DQ19_504	PS_DDR_DQ51_504	AG21	DQ19
PS_DDR_DQ20_504	PS_DDR_DQ52_504	AD20	DQ20
PS_DDR_DQ21_504	PS_DDR_DQ53_504	AF20	DQ21
PS_DDR_DQ22_504	PS_DDR_DQ54_504	AE20	DQ22
PS_DDR_DQ23_504	PS_DDR_DQ55_504	AG20	DQ23
PS_DDR_DQ24_504	PS_DDR_DQ56_504	AG23	DQ24
PS_DDR_DQ25_504	PS_DDR_DQ57_504	AF23	DQ25
PS_DDR_DQ26_504	PS_DDR_DQ58_504	AF25	DQ26
PS_DDR_DQ27_504	PS_DDR_DQ59_504	AE23	DQ27
PS_DDR_DQ28_504	PS_DDR_DQ60_504	AC22	DQ28
PS_DDR_DQ29_504	PS_DDR_DQ61_504	AC23	DQ29
PS_DDR_DQ30_504	PS_DDR_DQ62_504	AD25	DQ30
PS_DDR_DQ31_504	PS_DDR_DQ63_504	AC24	DQ31
PS_DDR_DQ31_504	PS_DDR_DQ64_504	AC24	DQ31
PS_DDR_DQ31_504	PS_DDR_DQ65_504	AC24	DQ31
PS_DDR_DQS_P0_504	PS_DDR_DQS_P0_504	AJ21	DDR4-DQS0_P
PS_DDR_DQS_N0_504	PS_DDR_DQS_N0_504	AK21	DDR4-DQS0_N
PS_DDR_DQS_P1_504	PS_DDR_DQS_P1_504	AH24	DDR4-DQS1_P
PS_DDR_DQS_N1_504	PS_DDR_DQS_N1_504	AJ24	DDR4-DQS1_N
PS_DDR_DQS_P2_504	PS_DDR_DQS_P2_504	AC21	DDR4-DQS2_P
PS_DDR_DQS_N2_504	PS_DDR_DQS_N2_504	AD21	DDR4-DQS2_N
PS_DDR_DQS_P3_504	PS_DDR_DQS_P3_504	AD24	DDR4-DQS3_P
PS_DDR_DQS_N3_504	PS_DDR_DQS_N3_504	AE24	DDR4-DQS3_N
PS_DDR_DQS_P4_504	PS_DDR_DQS_P4_504	W24	DDR4-DQS4_P
PS_DDR_DQS_N4_504	PS_DDR_DQS_N4_504	W25	DDR4-DQS4_N
PS_DDR_DQS_P5_504	PS_DDR_DQS_P5_504	P25	DDR4-DQS5_P
PS_DDR_DQS_N5_504	PS_DDR_DQS_N5_504	R25	DDR4-DQS5_N
PS_DDR_DQS_P6_504	PS_DDR_DQS_P6_504	U29	DDR4-DQS6_P
PS_DDR_DQS_N6_504	PS_DDR_DQS_N6_504	V29	DDR4-DQS6_N
PS_DDR_DQS_P7_504	PS_DDR_DQS_P7_504	R28	DDR4-DQS7_P
PS_DDR_DQS_N7_504	PS_DDR_DQS_N7_504	R29	DDR4-DQS7_N
PS_DDR_DQS_P8_504	PS_DDR_DQS_P8_504	R29	DDR4-DQS7_N
PS_DDR_DQS_N8_504	PS_DDR_DQS_N8_504	R29	DDR4-DQS7_N
PS_DDR_DQS_P8_504	PS_DDR_DQS_P8_504	Y28	
PS_DDR_DQS_N8_504	PS_DDR_DQS_N8_504	AA28	

*XCZU4CG-1FBVB900I*



Title: <b>TE0807 - PS_DDR</b>		
A4	Number: <b>TE0807 4AI81-A</b>	Rev. <b>04</b>
Date: <b>19.06.2024</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>19</b> of <b>32</b>
Filename: <b>PS_DDR.SchDoc</b>		

1

2

3

4

A

A

B

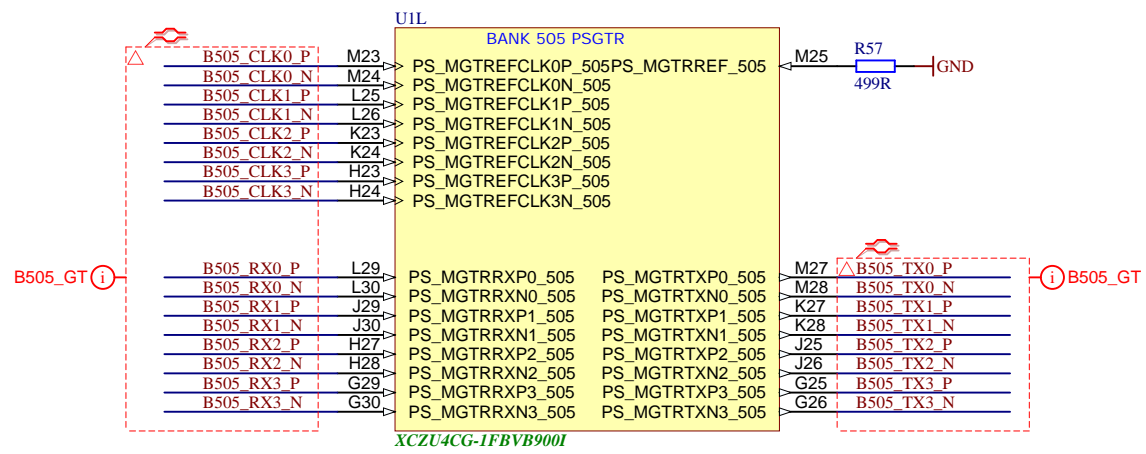
B


C

C

D

D



	Title: TE0807 – B_PS_GT		
	A4	Number: TE0807 4AI81-A	Rev. 04
	Date: 19.06.2024	Copyright: Trenz Electronic GmbH	Page 20 of 32
	Filename: B_PS_GT.SchDoc		

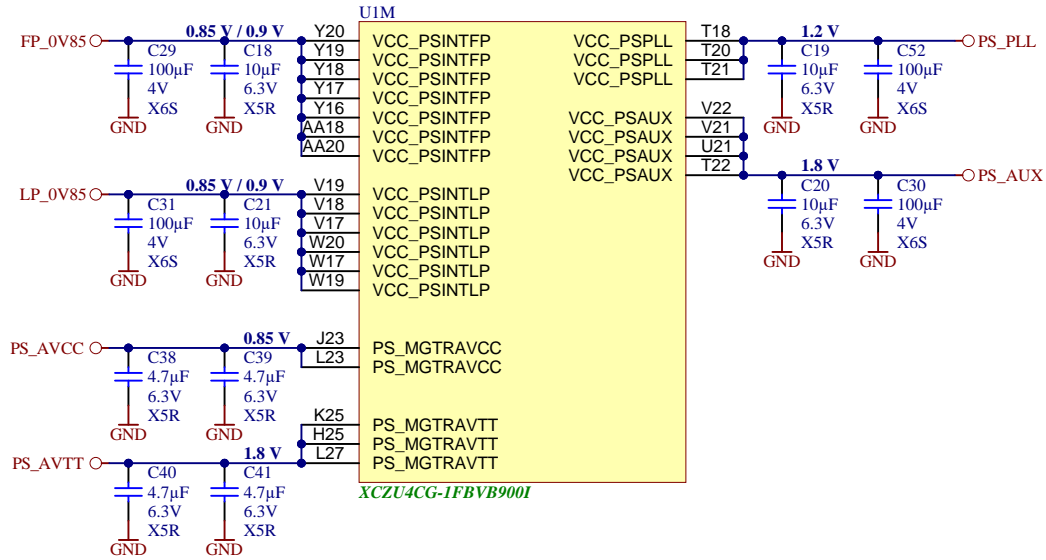
1


2

3

4





	Title: TE0807 – ZU_PS_POWER		
	A4	Number: TE0807 4A181-A	Rev. 04
	Date: 19.06.2024	Copyright: Trenz Electronic GmbH	Page 21 of 32
	Filename: ZU_PS_POWER.SchDoc		

A

B

C

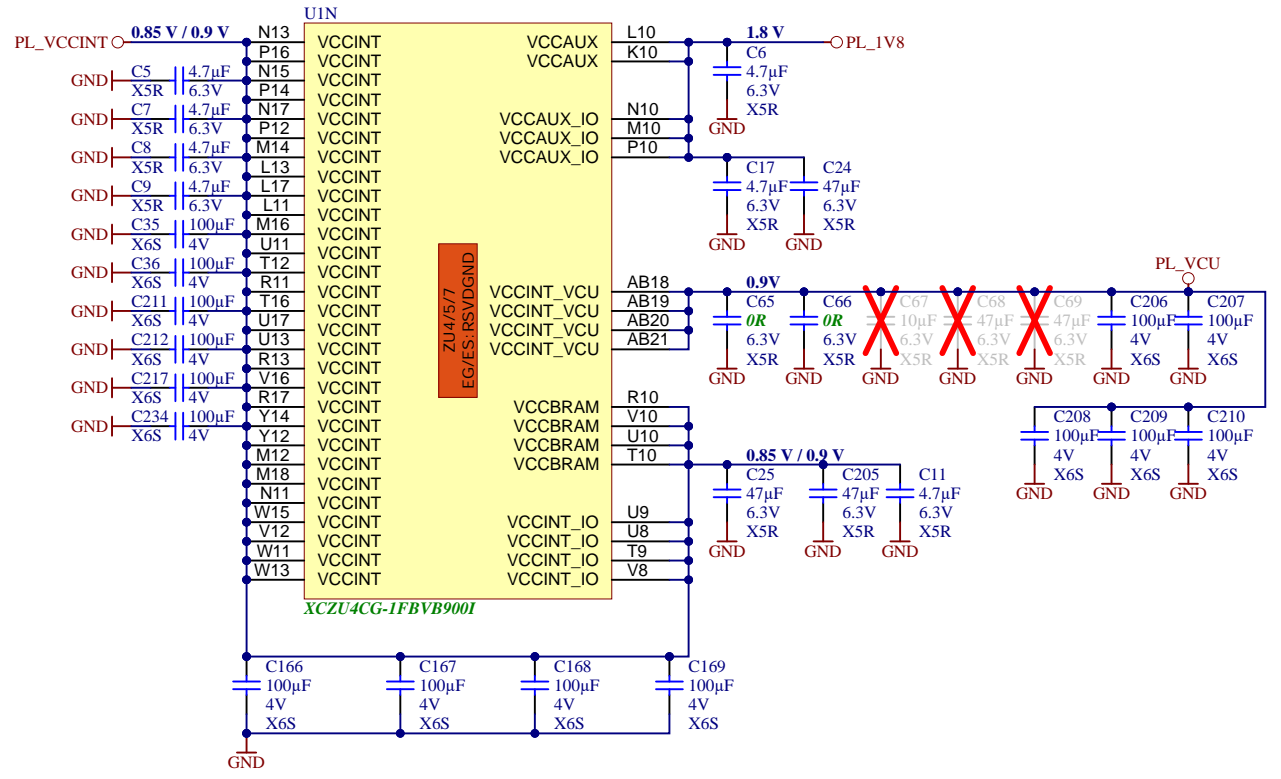
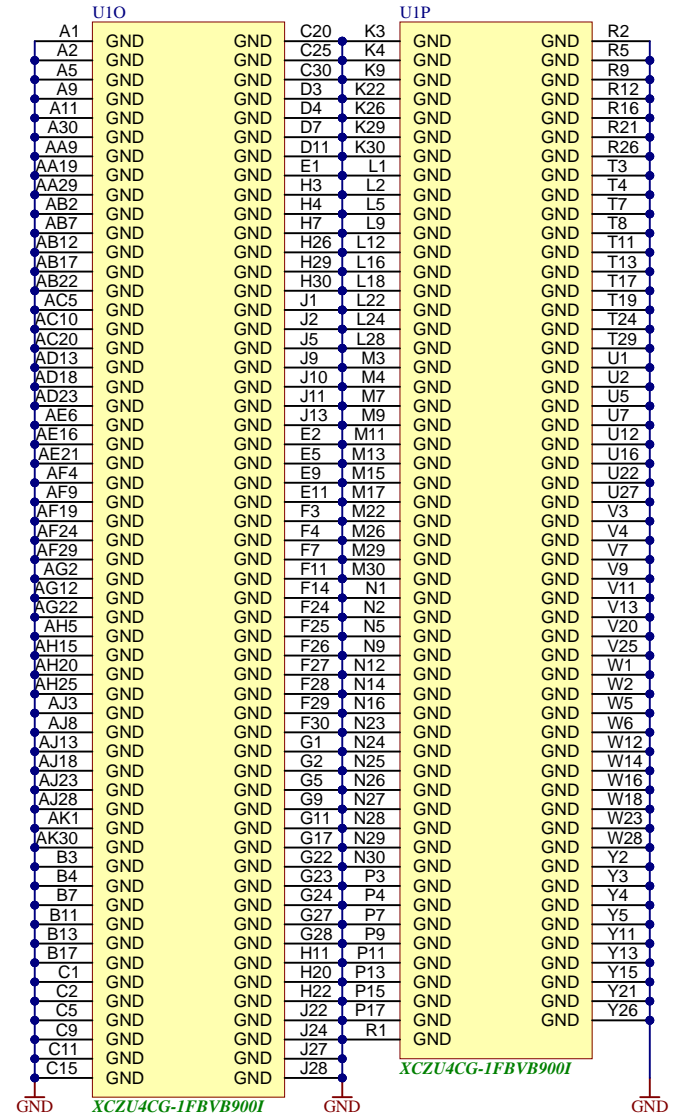
D

A

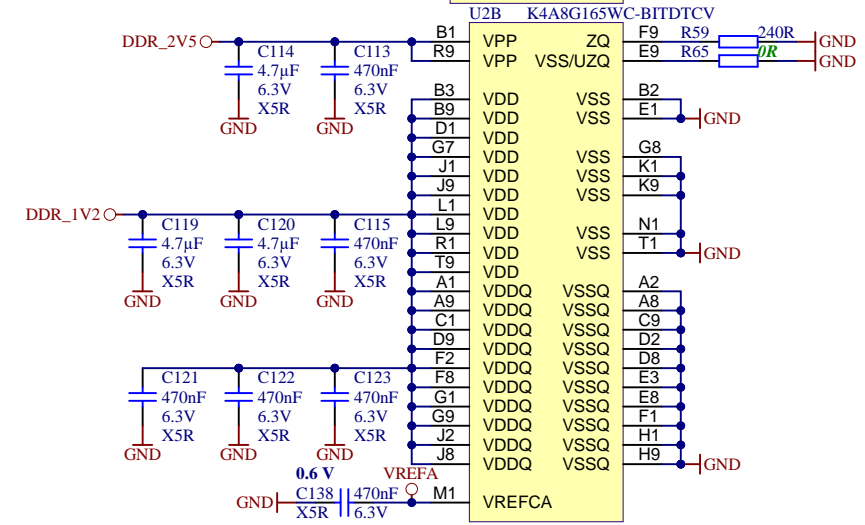
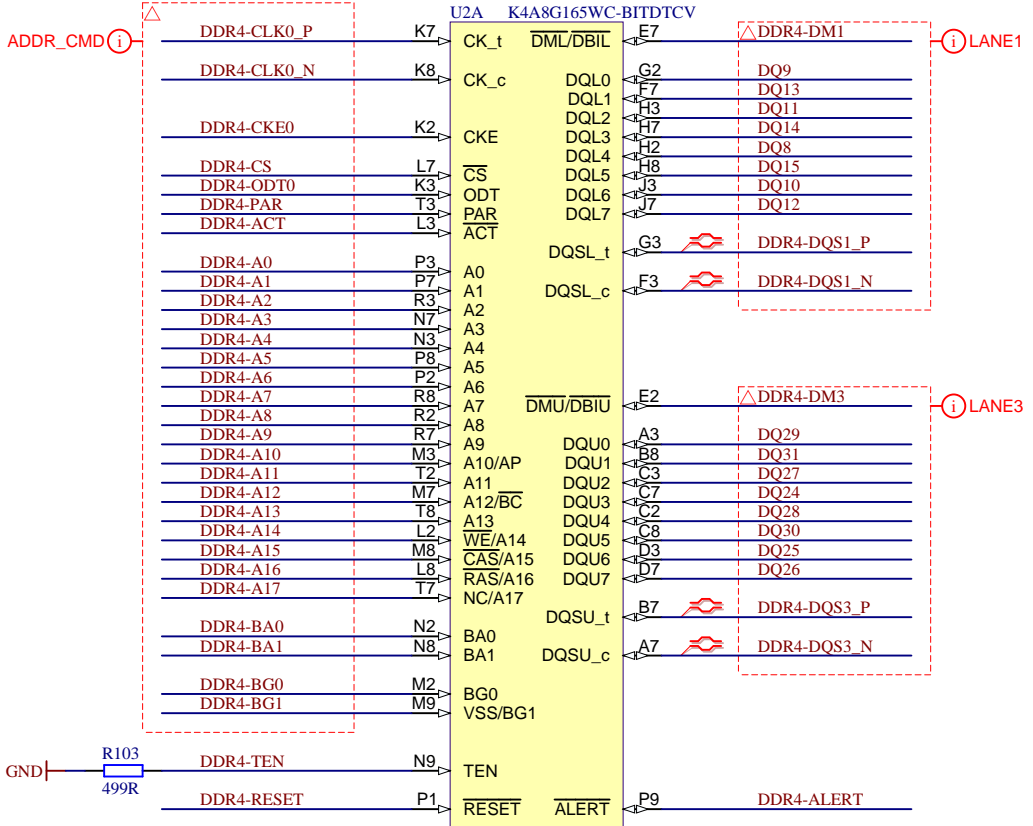
B

C

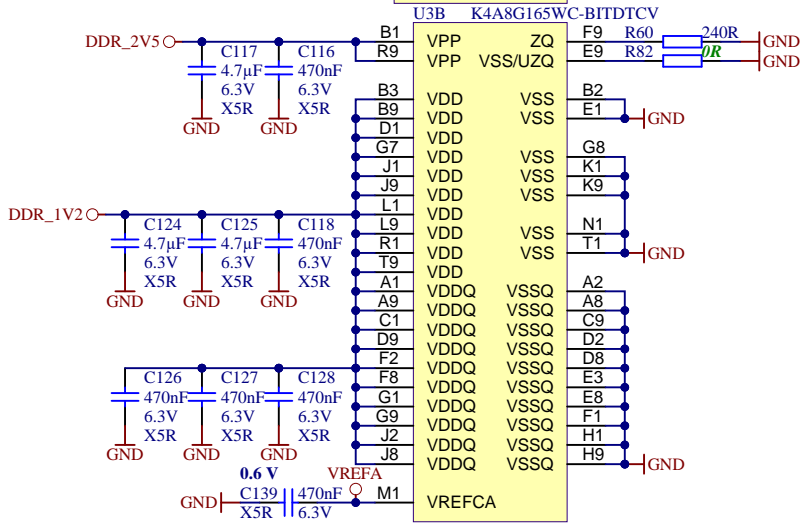
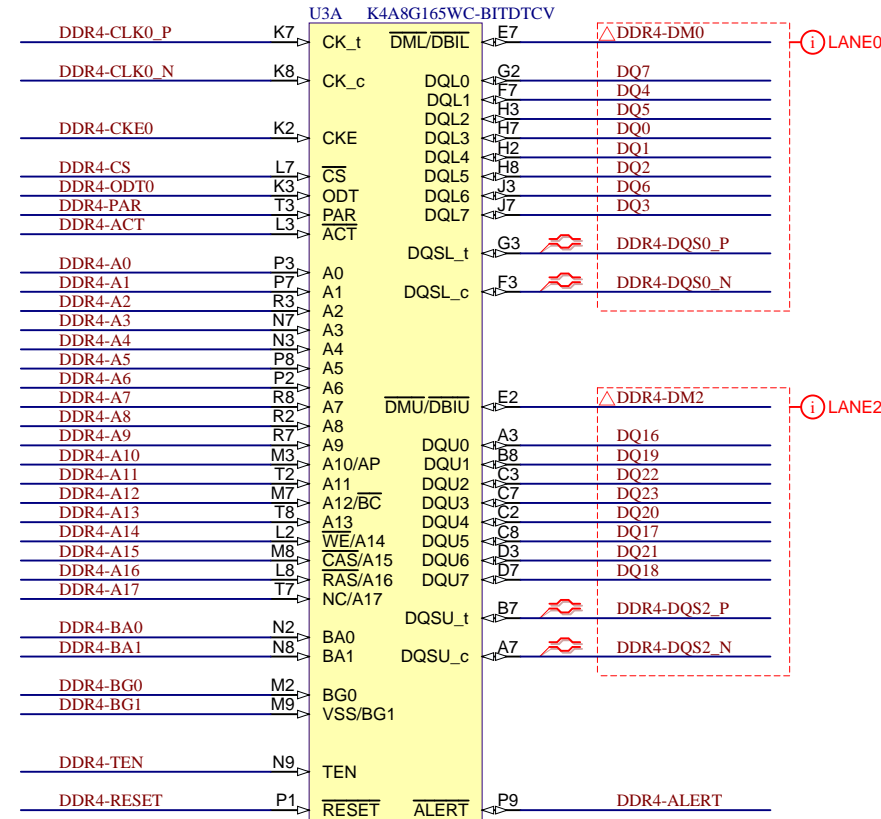
D



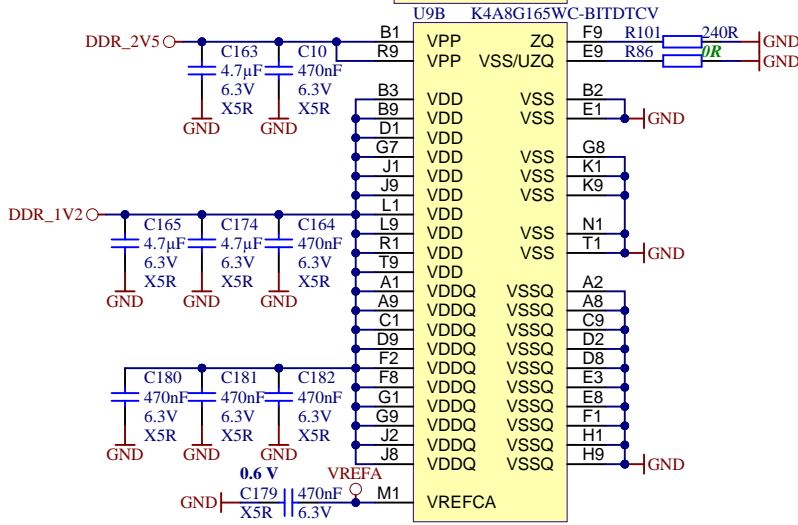
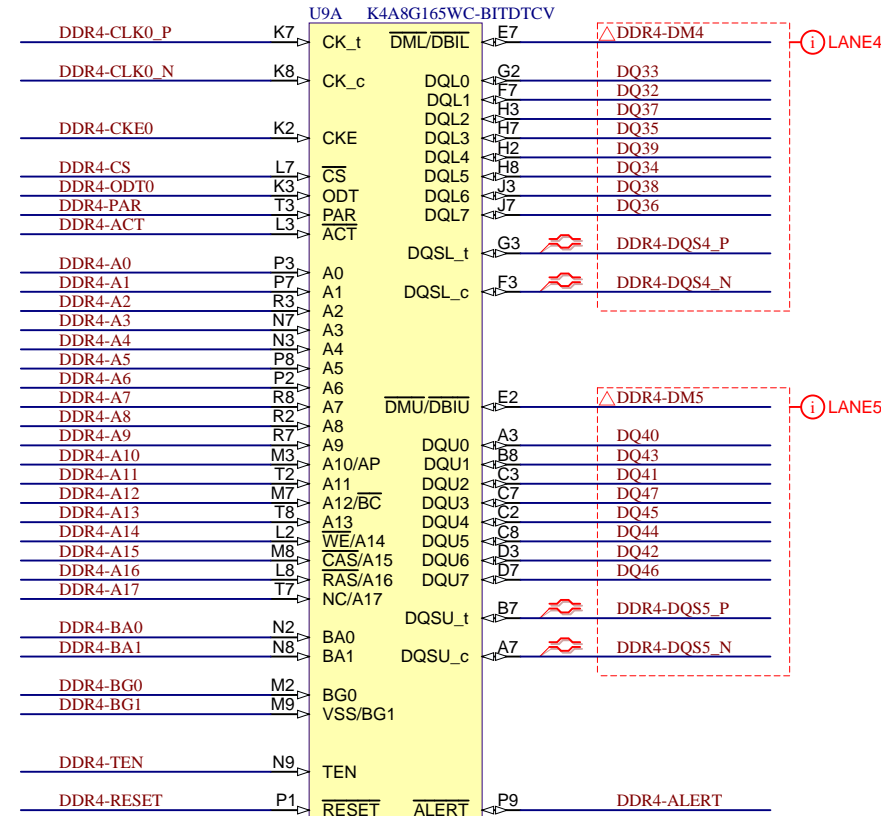
Title: TE0807 – ZU_POWER		
A4	Number: TE0807 4AI81-A	Rev. 04
Date: 19.06.2024	Copyright: Trenz Electronic GmbH	Page 22 of 32
Filename: ZU_POWER.SchDoc		



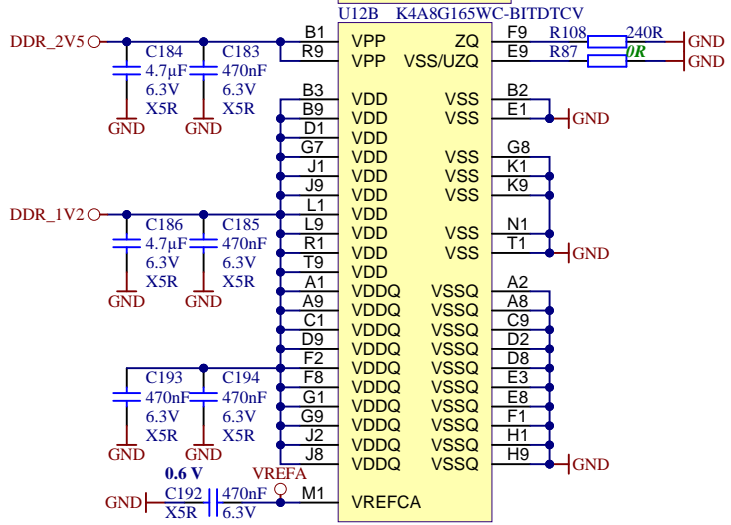
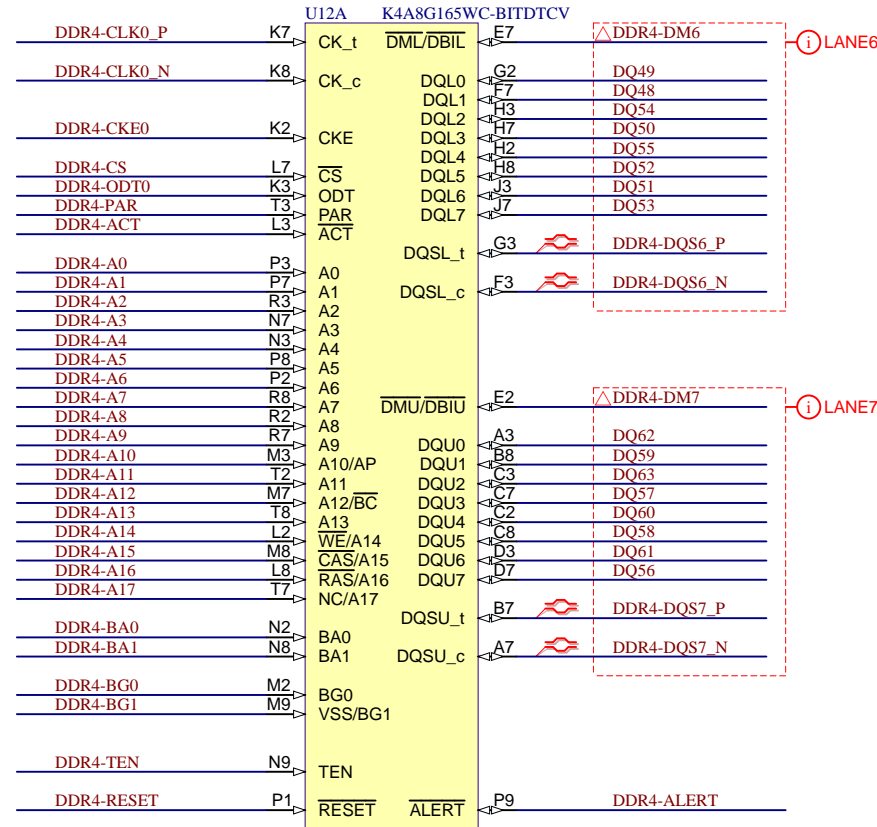
Title: TE0807 – DDR4-RAM_1		
A4	Number: TE0807 4A181-A	Rev. 04
Date: 19.06.2024	Copyright: Trenz Electronic GmbH	Page 23 of 32
Filename: DDR4-RAM.SchDoc		



Title: TE0807 – DDR4-RAM_2		
A4	Number: TE0807 4A181-A	Rev. 04
Date: 19.06.2024	Copyright: Trenz Electronic GmbH	Page 24 of 32
Filename: DDR4-RAM_2.SchDoc		

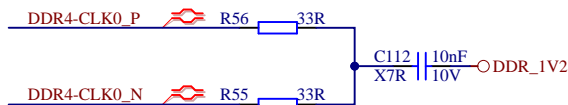
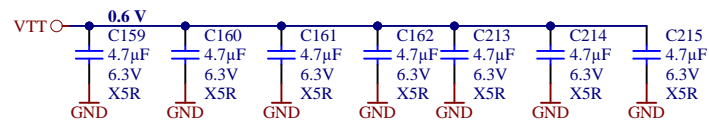
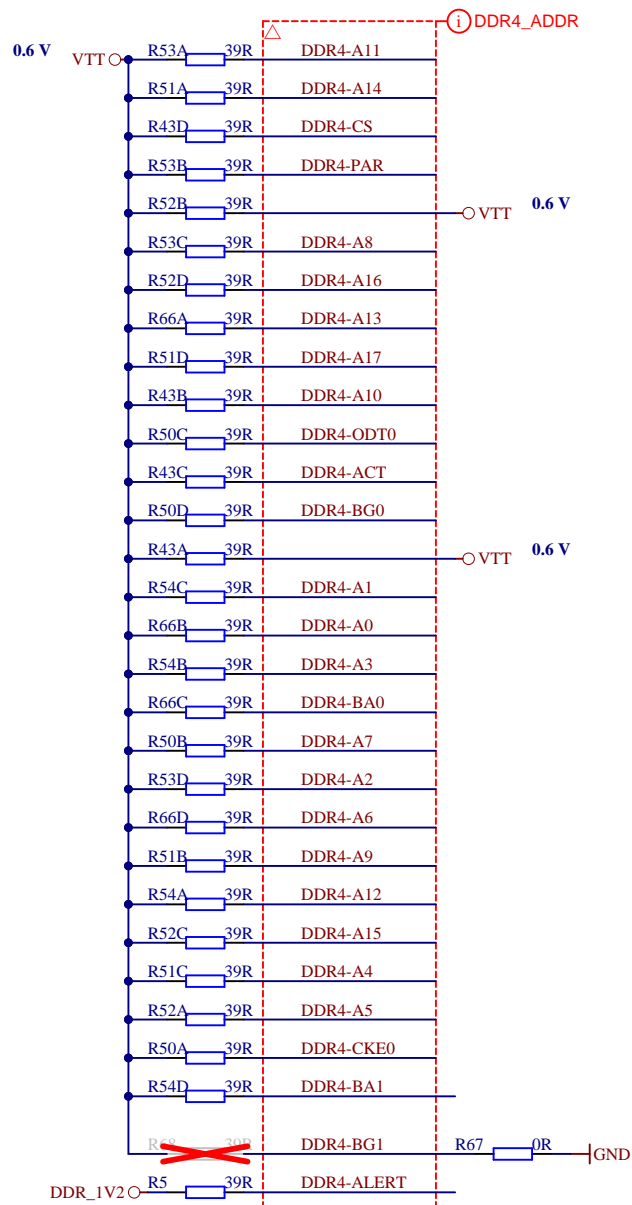



Title: TE0807 – DDR4-RAM_3		
A4	Number: TE0807 4A181-A	Rev. 04
Date: 19.06.2024	Copyright: Trenz Electronic GmbH	Page 25 of 32
Filename: DDR4-RAM_3.SchDoc		



Title: TE0807 - DDR4-RAM_4		
A4	Number: TE0807 4A181-A	Rev. 04
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Filename: DDR4-RAM_4.SchDoc		

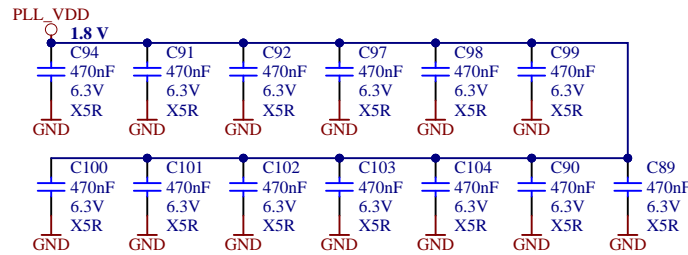
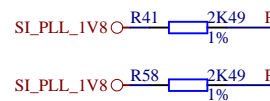
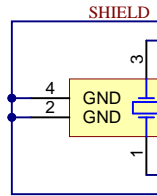
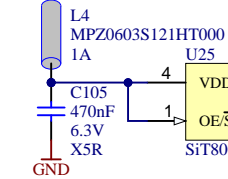




			Title: TE0807 – DDR4-TERM	
			A4	Number: TE0807 4AI81-A
Date: 19.06.2024		Copyright: Trenz Electronic GmbH		Page 27 of 32
Filename: DDR4-TERM.SchDoc				

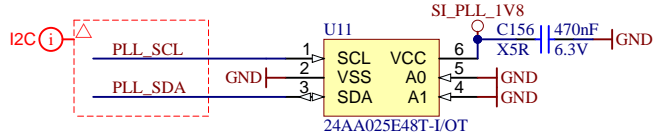
1.8 V

PLL\_VDD



I2C Address: 1101001

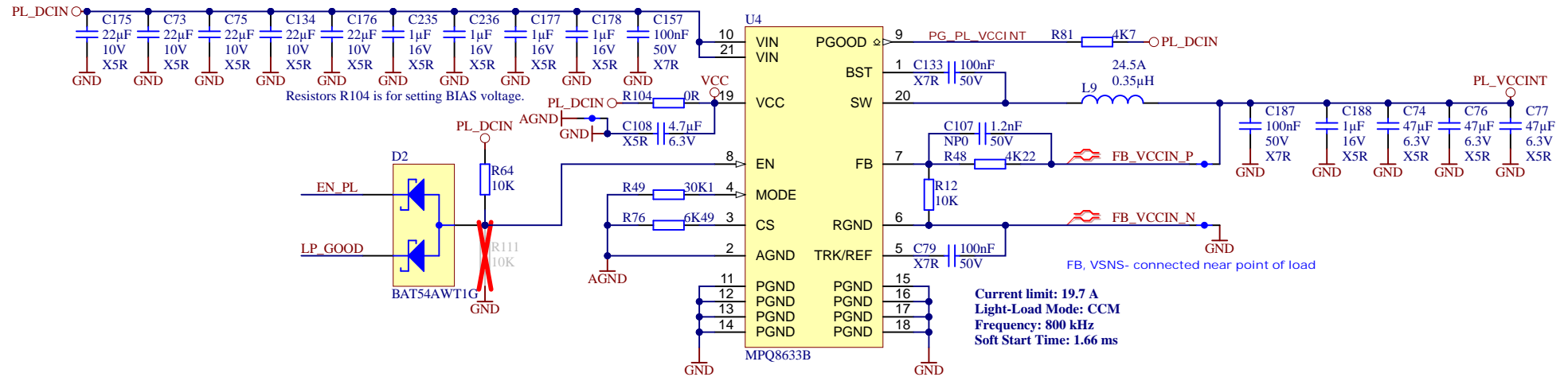
EEPROM for MAC



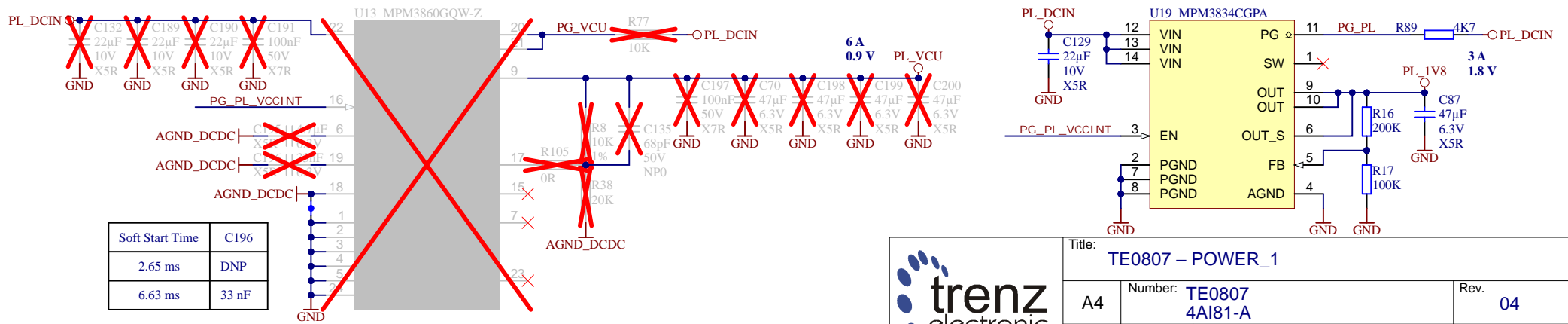
I2C Address: 1010000



Title: TE0807 – Clock		
A4	Number: TE0807 4A181-A	Rev. 04
Date: 19.06.2024	Copyright: Trenz Electronic GmbH	Page 28 of 32
Filename: Clock.SchDoc		



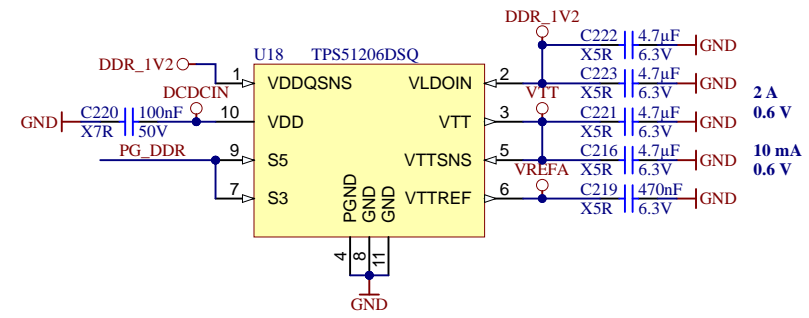
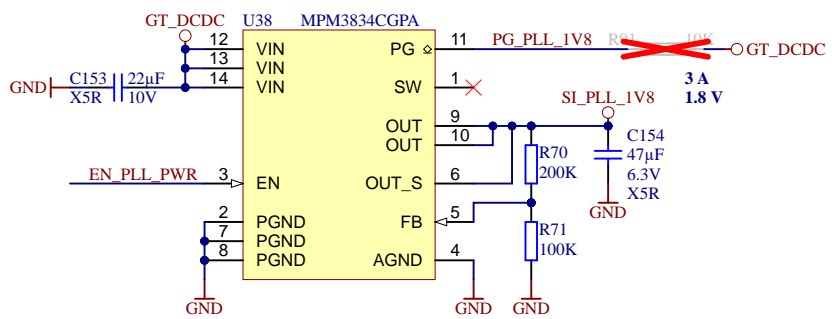
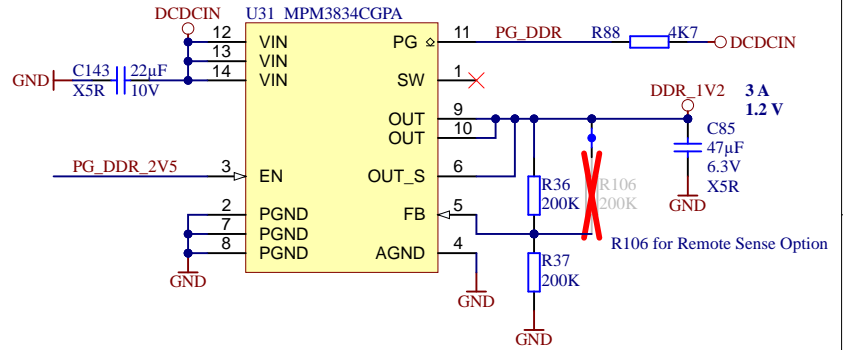
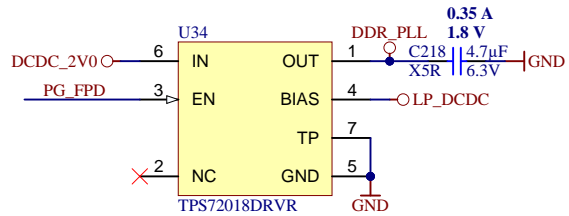
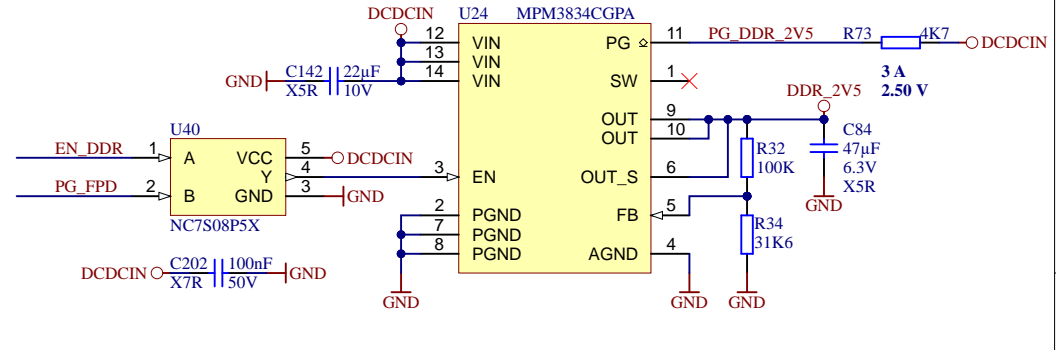
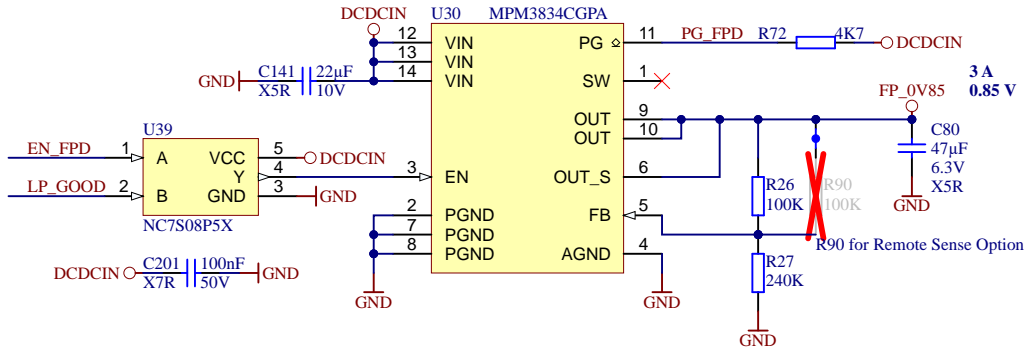
FPGA Speedgrade	R48	R12	PL_VCCINT	C107
-1	4.22 kOhm	10 kOhm	0.853 V	1.2 nF
-2	4.22 kOhm	10 kOhm	0.853 V	1.2 nF
-3	10 kOhm	20 kOhm	0.900 V	560 pF



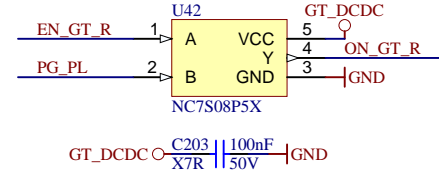
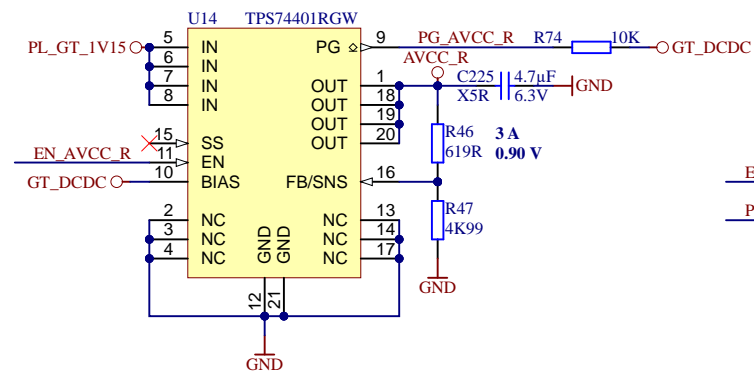
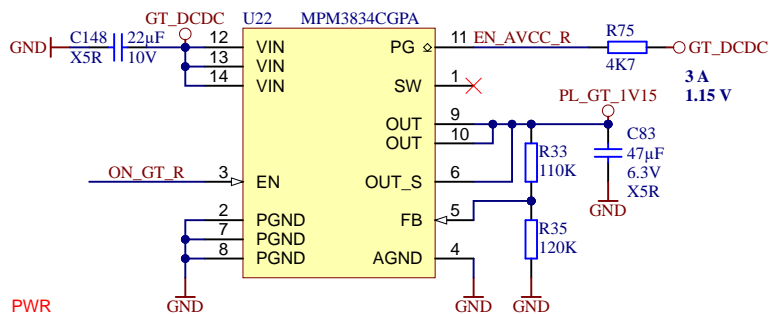
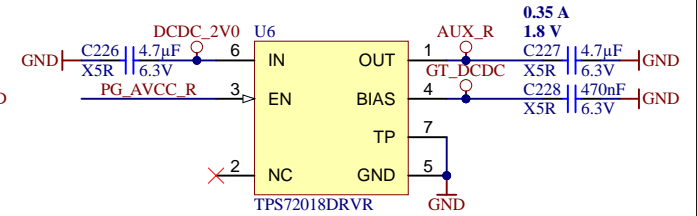
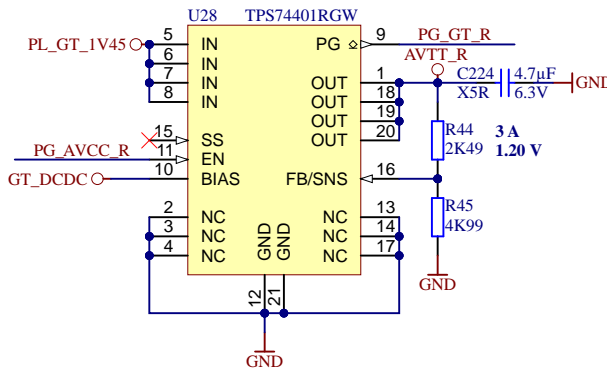
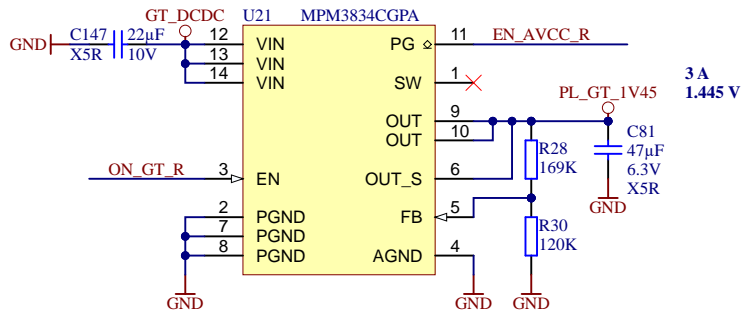
Soft Start Time	C196
2.65 ms	DNP
6.63 ms	33 nF



Title: TE0807 - POWER_1		
A4	Number: TE0807 4AI81-A	Rev. 04
Date: 19.06.2024	Copyright: Trenz Electronic GmbH	Page 29 of 32
Filename: POWER.SchDoc		



Title: TE0807 - POWER_2		
A4	Number: TE0807 4AI81-A	Rev. 04
Date: 19.06.2024	Copyright: Trenz Electronic GmbH	Page 30 of 32
Filename: POWER_2.SchDoc		



**Testpoints on top and bottom:**

Testpoints on top:		Testpoints on bottom:	
LP_0V85	TP4	LP_0V85	TP31
FP_0V85	TP6	FP_0V85	TP15
PS_PLL	TP7	PS_PLL	TP27
PS_GT_1V0	TP8	PS_GT_1V0	TP9
PS_AUX	TP11	PS_AUX	TP29
PS_AVCC	TP13	PS_AVCC	TP30
PS_AVTT	TP14	PS_AVTT	TP28
DDR_PLL	TP19	DDR_PLL	TP18
DDR_2V5	TP20	DDR_2V5	TP16
VREFA	TP22	VREFA	TP34
VTT	TP36	VTT	TP23
PL_VCCINT	TP39	PL_VCCINT	TP12
DCDC_2V0	TP41	DCDC_2V0	TP17
PL_GT_1V45	TP43	PL_GT_1V45	TP44
PL_GT_1V15	TP45	PL_GT_1V15	TP46
AUX_R	TP48	AUX_R	TP24
AVCC_R	TP50	AVCC_R	TP26
AVTT_R	TP52	AVTT_R	TP25
PL_VCU	TP54	PL_VCU	TP33
1V8_REFIN	TP56	1V8_REFIN	TP57
REF_1.25V	TP58	REF_1.25V	TP59
PLL_VDDA	TP62	PLL_VDDA	TP63
PLL_VDD	TP65	PLL_VDD	TP66

**Testpoints on top:**

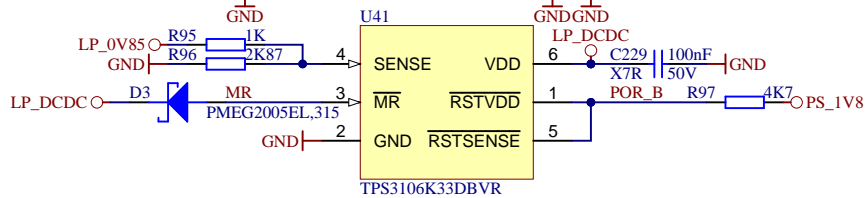
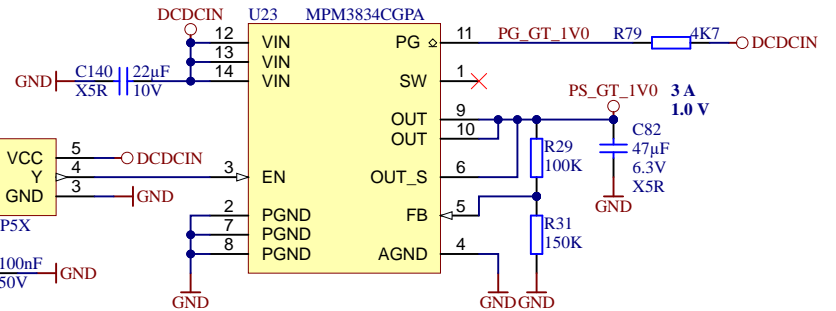
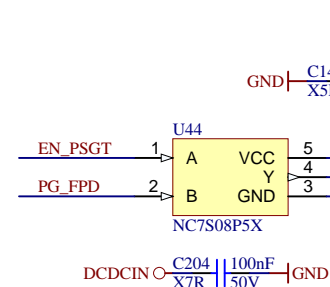
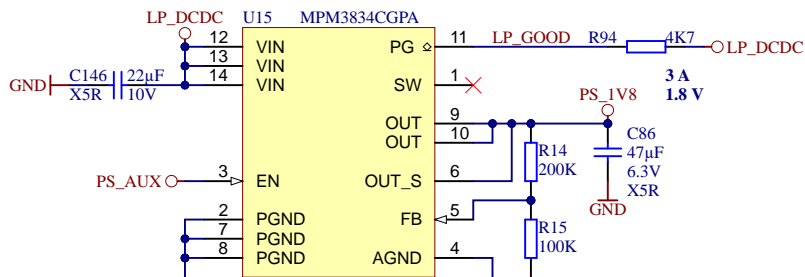
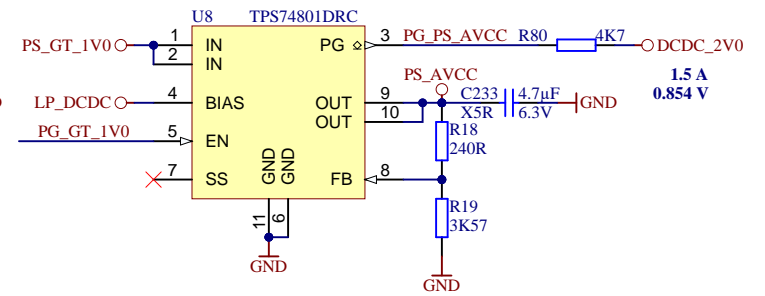
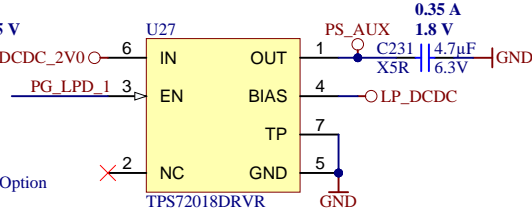
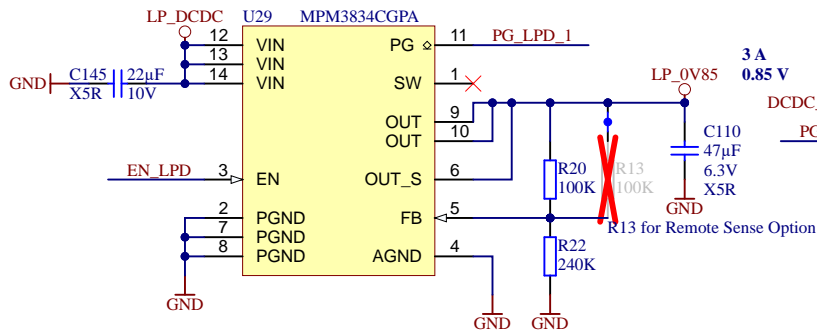
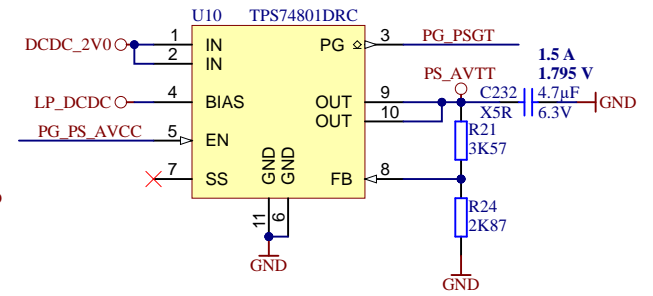
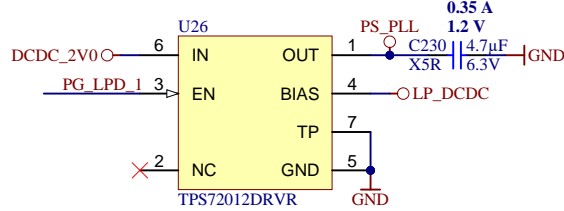
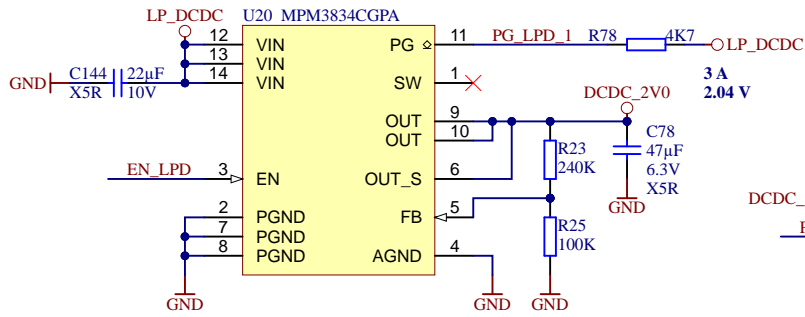
LP_DCDC	TP21
DCDCIN	TP35
PL_DCIN	TP37
GT_DCDC	TP38
PLL_3V3	TP40
PSBATT	TP42
VCCO_47	TP47
VCCO_48	TP49
VCCO_64	TP51
VCCO_65	TP53
VCCO_66	TP55
SI_PLL_1V8	TP60
PS_1V8	TP61
PL_1V8	TP64
DDR_1V2	TP67

**Testpoints on bottom:**

PLL_SCL	TP1
PLL_SDA	TP2
DDR4-TEN	TP3
GND	TP5
GND	TP10
GND	TP32



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Net Name	Voltage Rail	Low Detect
LP_OV85	0.85 V	0.743 V
LP_DCDC	3.3 V	2.941 V



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