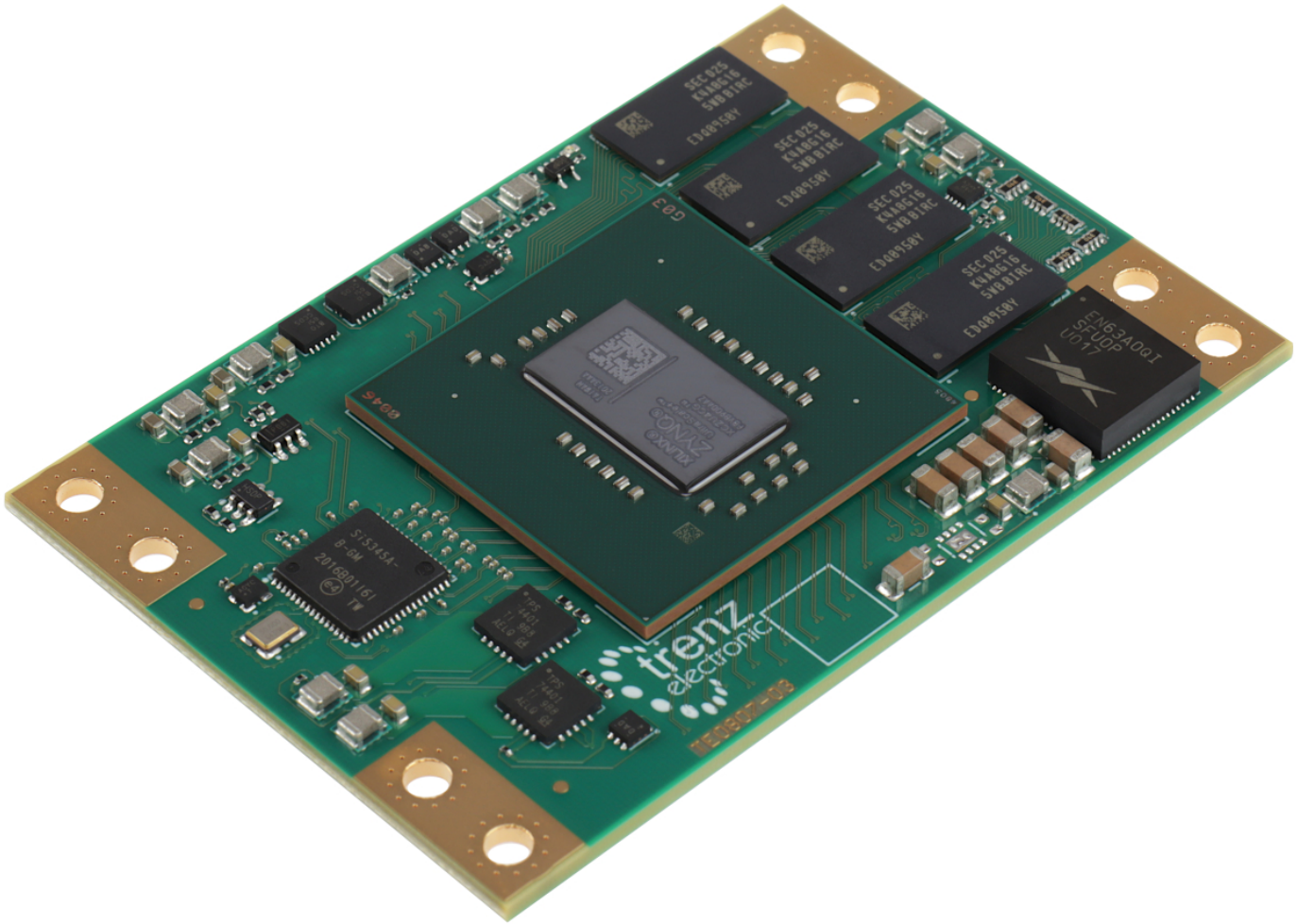

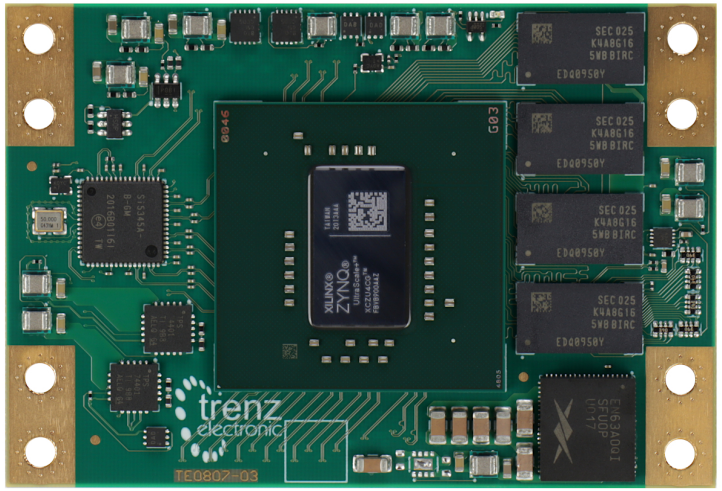

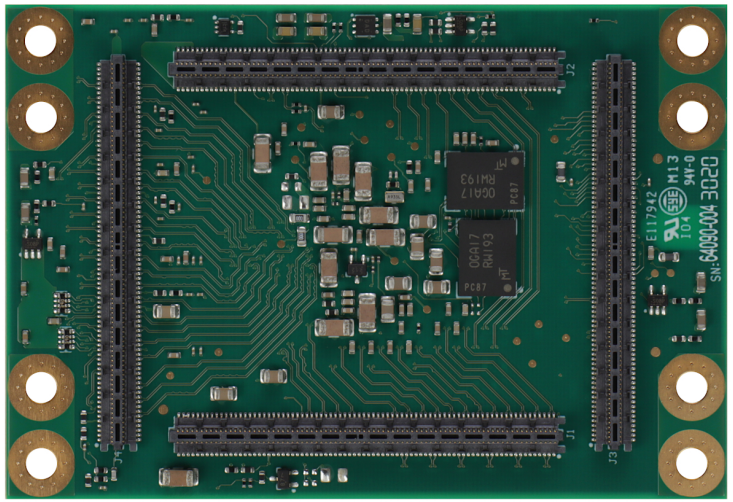

Regarding the usage of our schematics and alike documentation for Trenz module TE0807.

Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified.

TE0807 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

trenz electronic	Title: TE0807 – Legal Notices Modules		
	A4	Number: TE0807 7DE81-A	Rev. 04
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REV	DATE	Description	
-01	-	Initial revision	-
-02	-	1) Added EEPROM U11 (24AA025E48T-I/OT). 2) Added optional resistors R39 / R40 for QSPI flash (default: not populated). 3) Fixed VCU connection (added additional DCDC and capacitors), recommendation from AMD. 4) Changed obsolete DDR4 chips (NT5AD256M16B2-GN -> K4A8G165WB-BIRC). 5) Added net "PG_VCU" to J2 (pin97). 6) Full update LIB.	-
-03	2020-06	1) Fixed ADC connection. 2) Fixed DDR4 connection (support B-die DDR4 chips). 3) Fixed DDR4 connection (alert_n pin connection). 4) Added U16. 5) Added testpoints. 6) Full update LIB.	VT
-04	2024-05	1) Changed DCDC (U4) from EN63A0QI to MPQ8633 and adapted according circuit. 2) Changed DCDC (U13) from TPS82085SIL/MUN3CAD03-SE to MPM3860GQW-Z and adapted according circuit. 3) Changed DCDC (U15 , U19 , U20 , U21 , U22 , U23 , U24 , U29 , U30 , U31 , U38) from TPS82085SIL/MUN3CAD03-SE to MPM3834CGPA and adapted according circuit. 4) Changed voltage rail from 1.35 V to 1.45 V via adaption voltage divider resistor R28 and R30 and changed voltage rail name PL_GT_1V35 to PL_GT_1V45 . 5) Changed voltage rail from 1.05 V to 1.15 V via adaption voltage divider resistors R33 and R35 and changed voltage rail name PL_GT_1V05 to PL_GT_1V15 . 6) Changed PLL (U5) from Si5345A-B to Si5345A-D-GM. 7) Changed inverted buffer SN74LVC1G06DRL to not inverted buffer SN74LVC1G07DRL (U16A / U16B). 8) Added diode D3 between U41 pin 3 net MR and voltage rail LP_DCDC . 9) Added capacitors C213 ... C215 for VTT voltage rail VTT . 10) Replaced DDR4 memory chips to use bigger chip sizes. 11) Connected DDR4-TEN signals together for U2A , U3A , U9A , and U12A and pulled them low via 499 Ohm resistor R103 . Added testpoint TP3 for signal DDR4-TEN. 12) Added remote sense option (default: not fitted): 12.1) R13 for U29 . 12.2) R90 for U30 . 12.3) R106 for U31 . 13) Added decoupling capacitors: 13.1) C136 , C149 for U1B . 13.2) C155 for U1C . 13.3) C151 for U1E . 13.4) C152 for U1D . 13.5) C205 ... C212 , C217 , and C234 for U1N . 13.6) C226 ... C228 for U6 . 13.7) C233 for U8 . 13.8) C232 for U10 . 13.9) C156 for U11 . 13.10) C225 for U14 . 13.11) C150 for U16B . 13.12) C216 , C219 , and C220 ... C223 for U18 . 13.13) C230 for U26 . 13.14) C231 for U27 . 13.15) C224 for U28 . 13.16) C218 for U34 . 13.17) C201 for U39 . 13.18) C202 for U40 . 13.19) C229 for U41 . 13.20) C203 for U42 . 13.21) C204 for U44 . 14) Added pull-up resistors for HOLD (R92) and WP (R93) signals for Flash U7A .	ED/MR

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REV	DATE	Description (continued...)	
-04	2024-05	15) Added pull-up resistors for HOLD (R100) and WP (R102) signals for Flash U17A. 16) Added pull-up resistor (R107) (default: not fitted) and pull-down resistor (R109) (default: fitted) for signal POR_OVERRIDE (U1A). 17) Changed 10 nF capacitor (C112) from 16 V, 0402 to 10 V, 0201. 18) Changed 100 nF capacitor (C37, C79, C95, C96, C130, C131, C133) from 6.3 V, X5R, 0201 to 50 V, X7R, 0402. 19) Changed capacitor (C12, C13, C14, C15, C16, C18, C19, C20, C21, C42, C44, C45, C170, C171) from 4.7 µF to 10 µF. 20) Changed 10 µF capacitor (C65, C66, C67) from 16 V, 0603 to 6.3 V, 0402. 21) Changed 100 µF capacitor (C29, C30, C31, C32, C35, C36, C43, C46, C52, C166, C167, C168, C169) from 6.3 V, 1206 to 4 V, 0805. 22) Changed 47 µF capacitor (C22, C23, C24, C25, C26, C27, C28, C33, C34, C68, C69, C70, C74, C76, C77, C78, C80, C81, C82, C83, C84, C85, C86, C87, C88, C110, C154, C198, C199, C200, C205) from 0805 to 0603. 23) Changed ferrid bead (L1, L2, L3, L4, L5, L7) from BKP0603HS121-T to MPZ0603S121HT000. 24) Changed resistor (R41, R58) from 2 kOhm to 2.49 kOhm. 25) Changed resistor (R74) from 4.7 kOhm, 0201 to 10 kOhm, 0402. 26) Added testpoints TP4, TP6...TP9, TP11, TP13, TP14, TP19...TP22, TP34... TP67. 27) Added Trenz address on PCB. 28) Added CE-, UKCA- RoHS-, and WEEE-logo. 29) Updated components from library. 30) Changed signal trace length. 31) Updated documentation.	ED/MR

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Title: TE0807 – Revision_Changes_2		
A4	Number: TE0807 7DE81-A	Rev. 04
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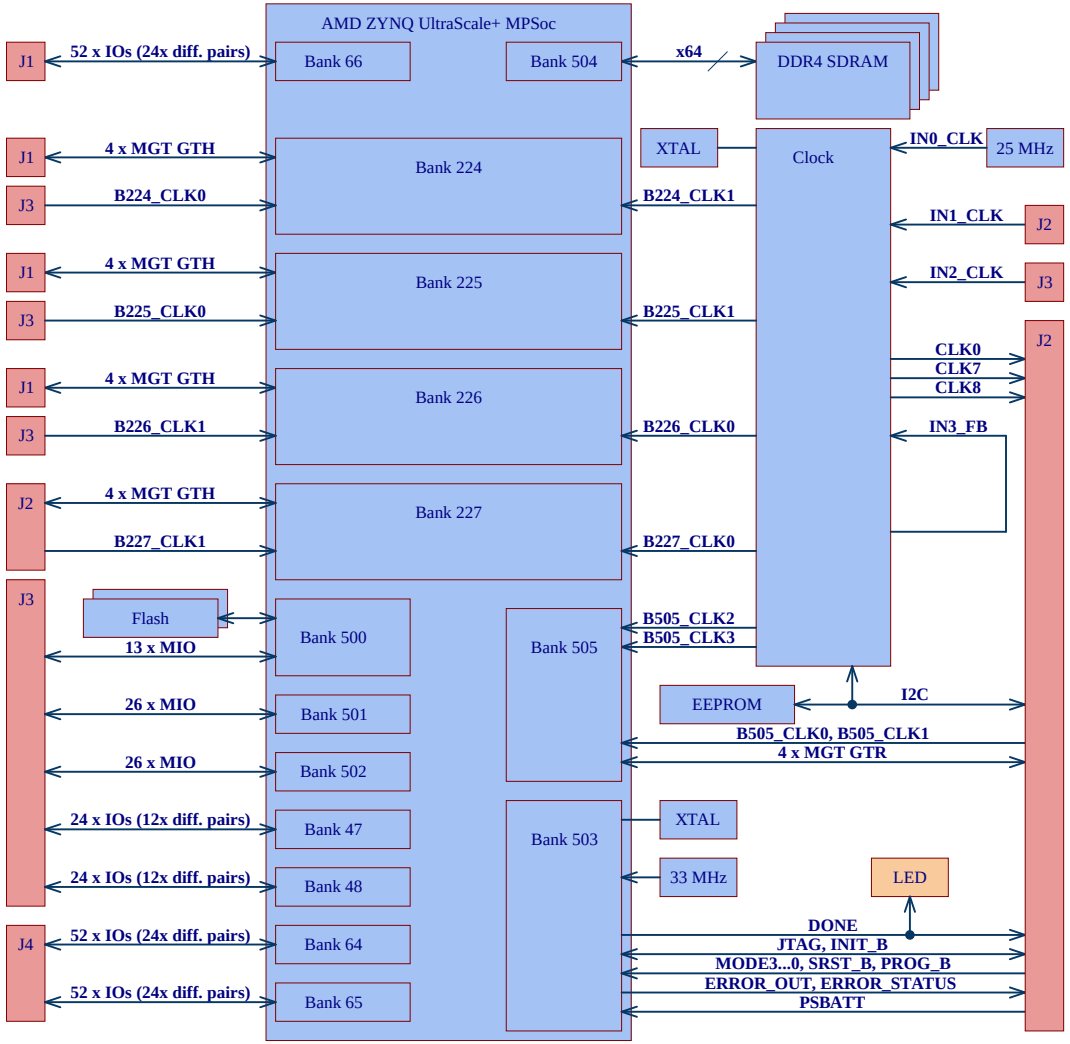

Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
PL_DCIN	IN	3.3 V	+/- 3 %	Micromodule Power	Programmable Logic
LP_DCDC	IN	3.3 V	+/- 3 %	Micromodule Power	Low-Power Domain
GT_DCDC	IN	3.3 V	+/- 3 %	Micromodule Power	GTH/GTY Transceiver
DCDCIN	IN	3.3 V	+/- 5 %	Micromodule Power	Full-Power Domain and GTR
VCCO_64	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 64	-
VCCO_65	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 65	-
VCCO_66	IN	1.0 V - 1.8 V	+/- 3 %	HP IO Bank 66	-
VCCO_47	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 47	-
VCCO_48	IN	1.2 V - 3.3 V	+/- 3 %	HD IO Bank 48	-
PSBATT	IN	1.2 V - 1.5 V	-	RTC / BBRAM	-
PLL_3V3	IN	3.3 V	+/- 5 %	PLL Core Power	-
PL_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Programmable Logic
PS_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Processing System
SI_PLL_1V8	OUT	1.8 V	+/- 3 %	Power for Carrier	Clock Supply
DDR_1V2	OUT	1.2 V	+/- 3 %	Power for Carrier	PS DDR I/O Supply

I2C Address:

Device	I2C ADDR	Note
PLL U5	0x69	-
EEPROM U11	0x50	-

Legend:

- B2B Connector
- LED Interface
- On-board Components

TE0807 | ZU_POWER | POWER | POWER_3
DDR4-TERM | ZU_GT_2 | ZU_PS_POWER | POWER_2 | POWER_4

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Title: TE0807 – Overview		
A4	Number: TE0807 7DE81-A	Rev. 04
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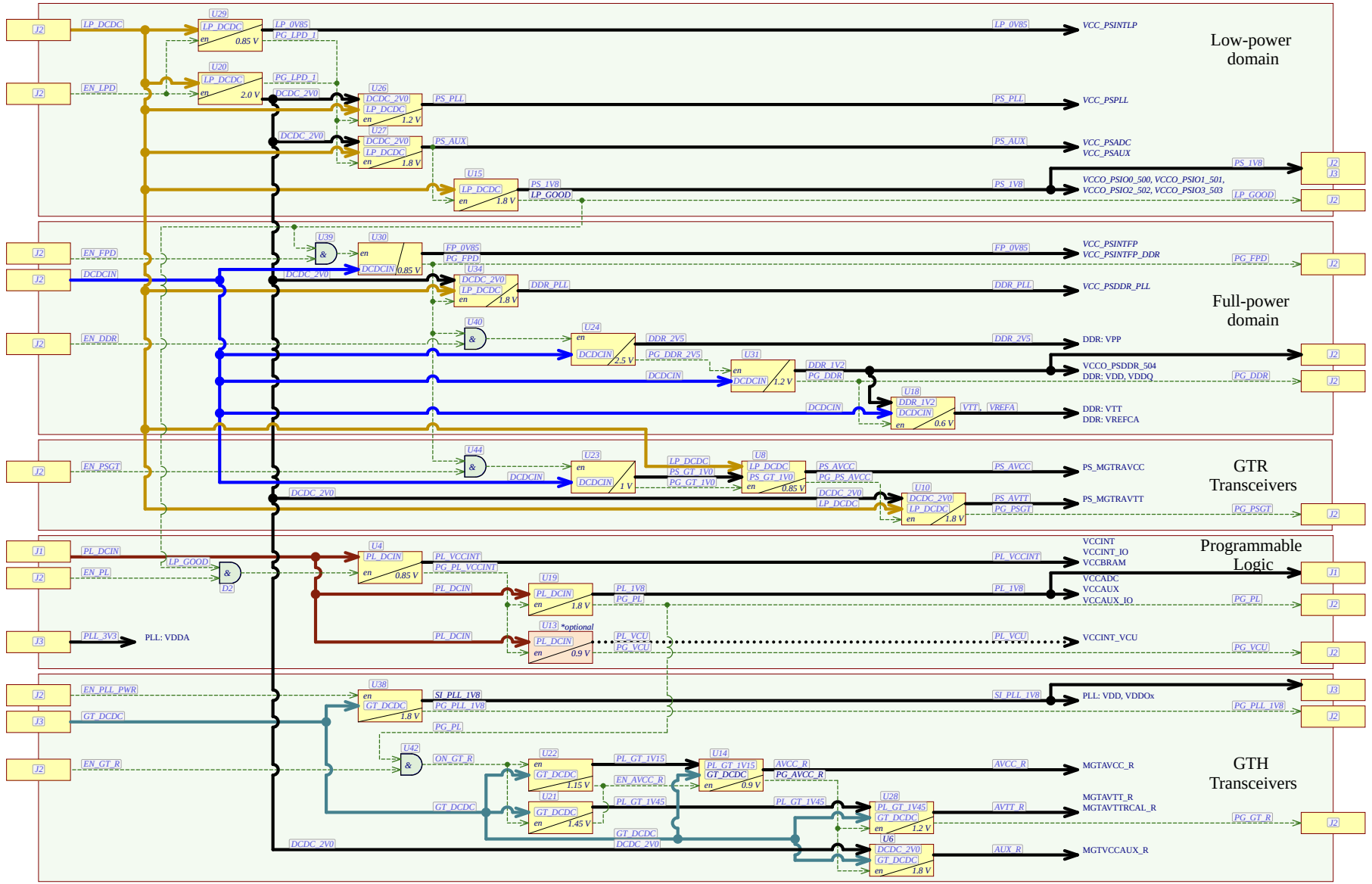

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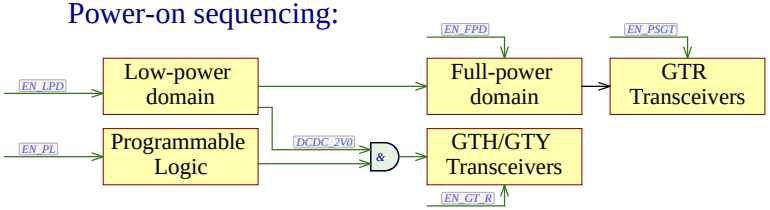

EN_GT_R — Net name

Power bus

Control signal

PL_DCIN 0.9V — Optional power converter

& — Logic AND gate

Title: TE0807 – Power_Diagram			
A3	Nummer: TE0807 7DE81-A		Rev. 04
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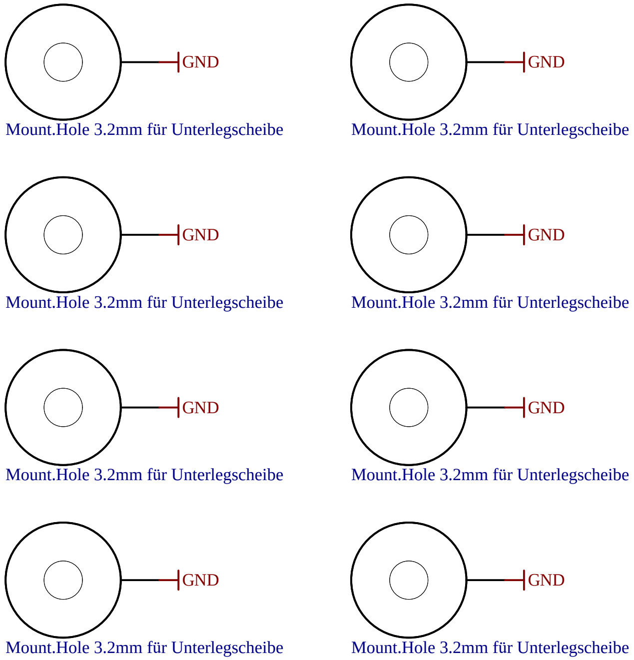
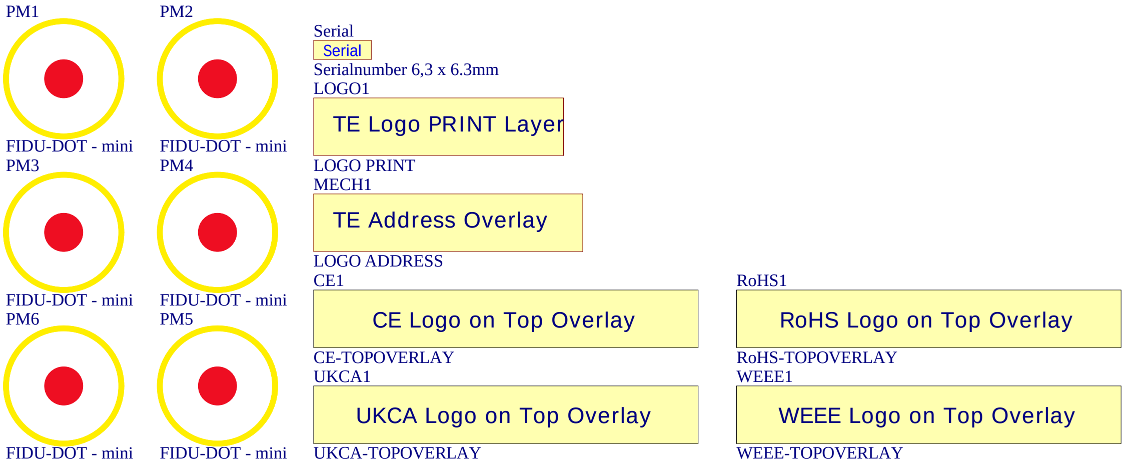
Special notes:





Design drawn by:	ED/MR
Checked by:	MT
Assembly variant:	7DE81-A
Created by:	ED
Modified by:	ED
Modified at:	2024-05-01

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Title: TE0807			
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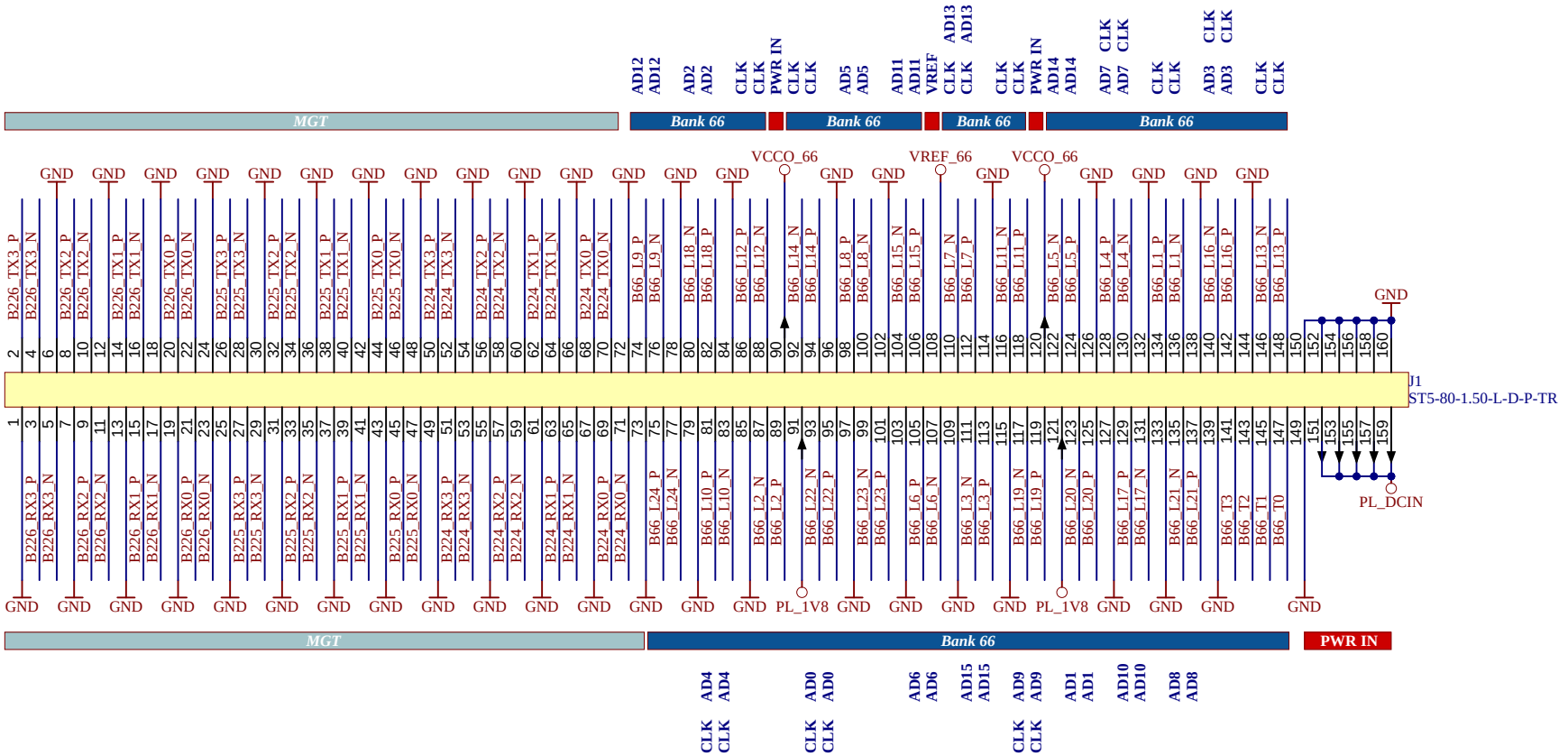
B224 GTH 4 Lanes
B225 GTH 4 Lanes
B226 GTH 4 Lanes
B66 52 IO, 24 LVDS Pairs

Consider AC coupling for MGT signals!



Bank 47 HD	0..VCCO47
Bank 48 HD	0..VCCO48
Bank 64 HP	0..VCCO64
Bank 65 HP	0..VCCO65
Bank 66 HP	0..VCCO66

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Title: TE0807 – Connector J1		
A4	Number: TE0807 7DE81-A	Rev. 04
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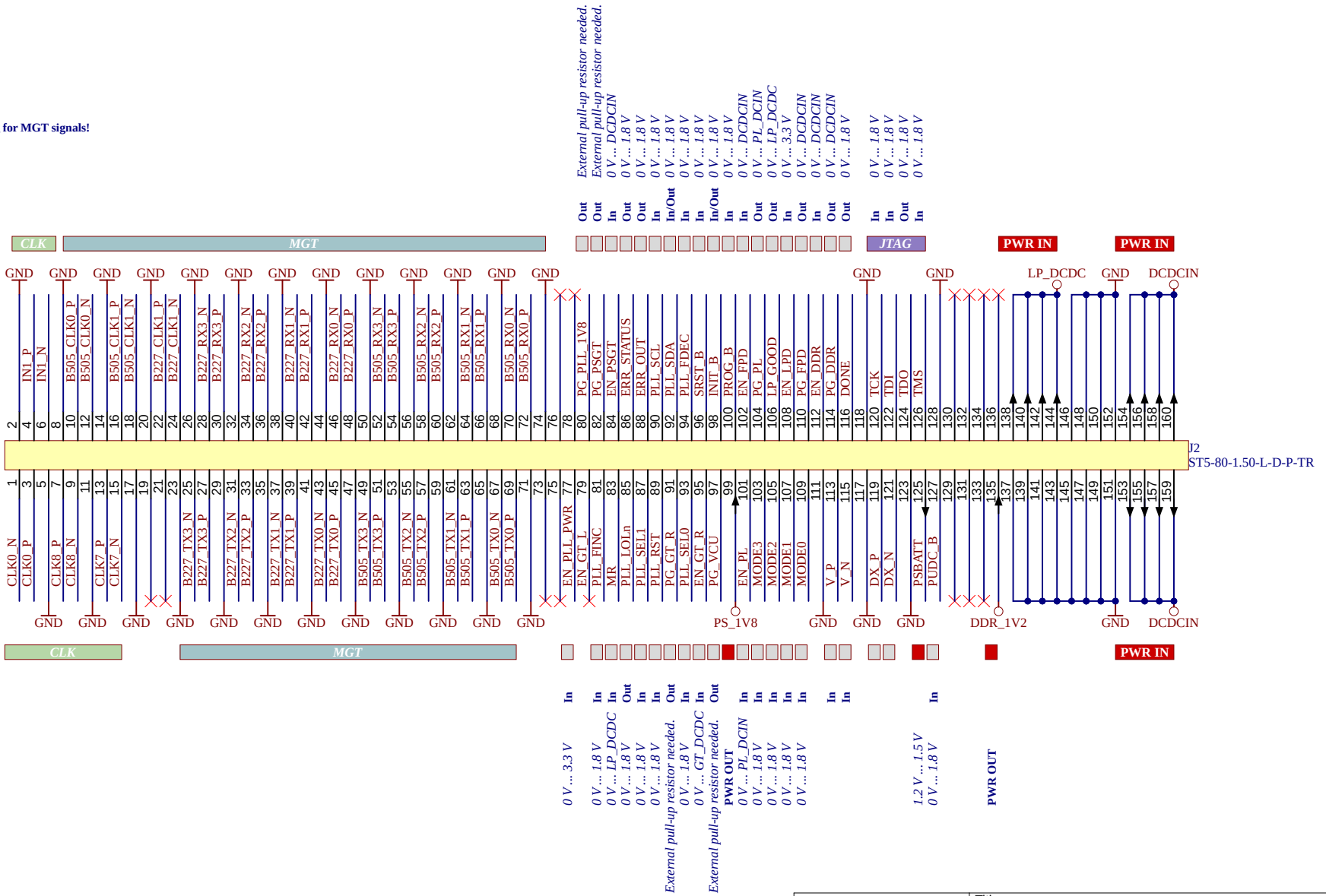
JTAG I2C
PLL CLK IN
3x PLL CLK OUT
B505 GTR 2 CLK IN
B505 GTR 4 Lanes
B227 GTH 4 Lanes
B227 GTH CLK IN

Consider AC coupling for MGT signals!



Bank 47 HD	0..VCCO47
Bank 48 HD	0..VCCO48
Bank 64 HP	0..VCCO64
Bank 65 HP	0..VCCO65
Bank 66 HP	0..VCCO66

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Title: TE0807 – Connector J2		
A4	Number: TE0807 7DE81-A	Rev. 04
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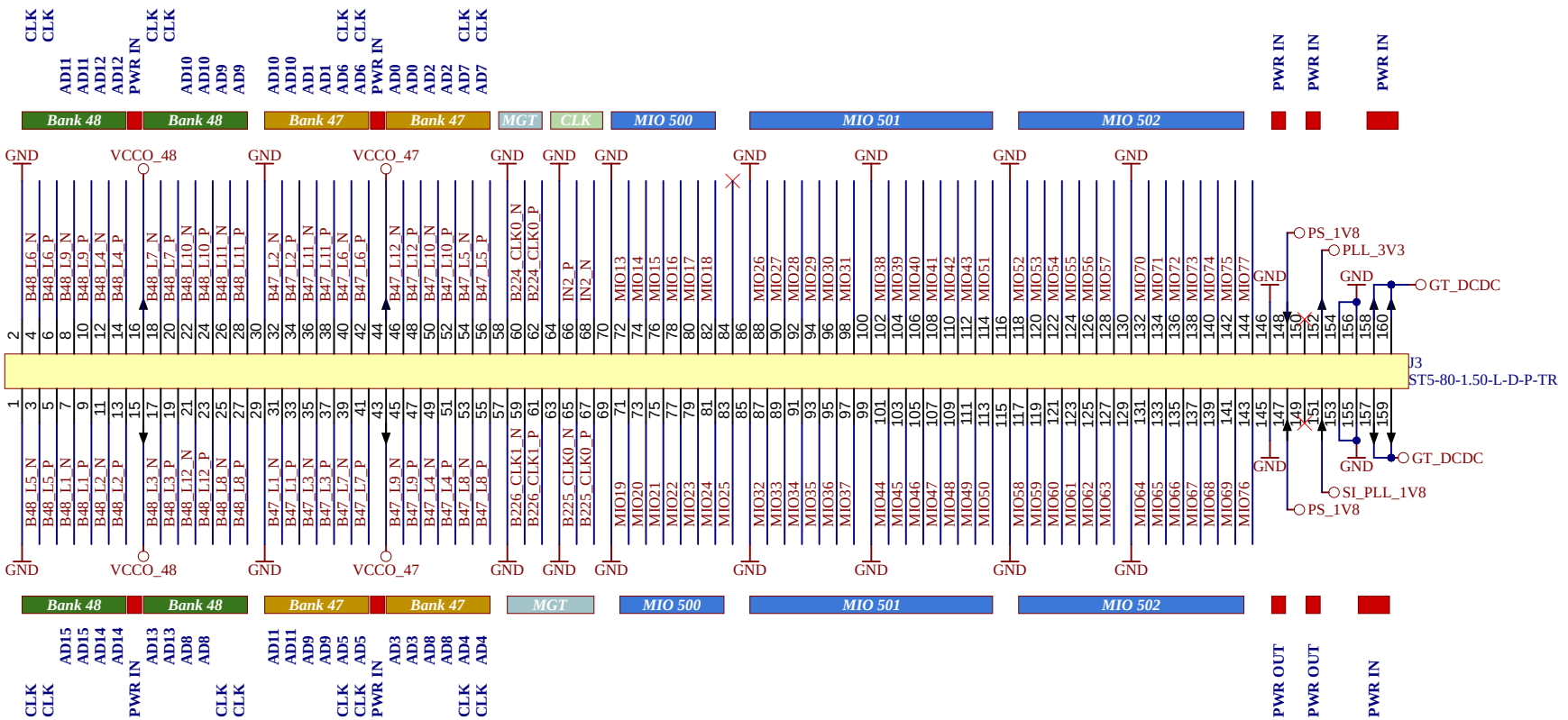
Filename: J2.SchDoc		

B47 24 IO, 12 LVDS Pairs
B48 24 IO, 12 LVDS Pairs
B224 GTH CLK IN
B225 GTH CLK IN
B226 GTH CLK IN
65 MIO
PLL CLK IN



Bank 47 HD 0..VCCO47
Bank 48 HD 0..VCCO48
Bank 64 HP 0..VCCO64
Bank 65 HP 0..VCCO65
Bank 66 HP 0..VCCO66

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Title: TE0807 – Connector J3			
A4	Number: TE0807 7DE81-A		Rev. 04
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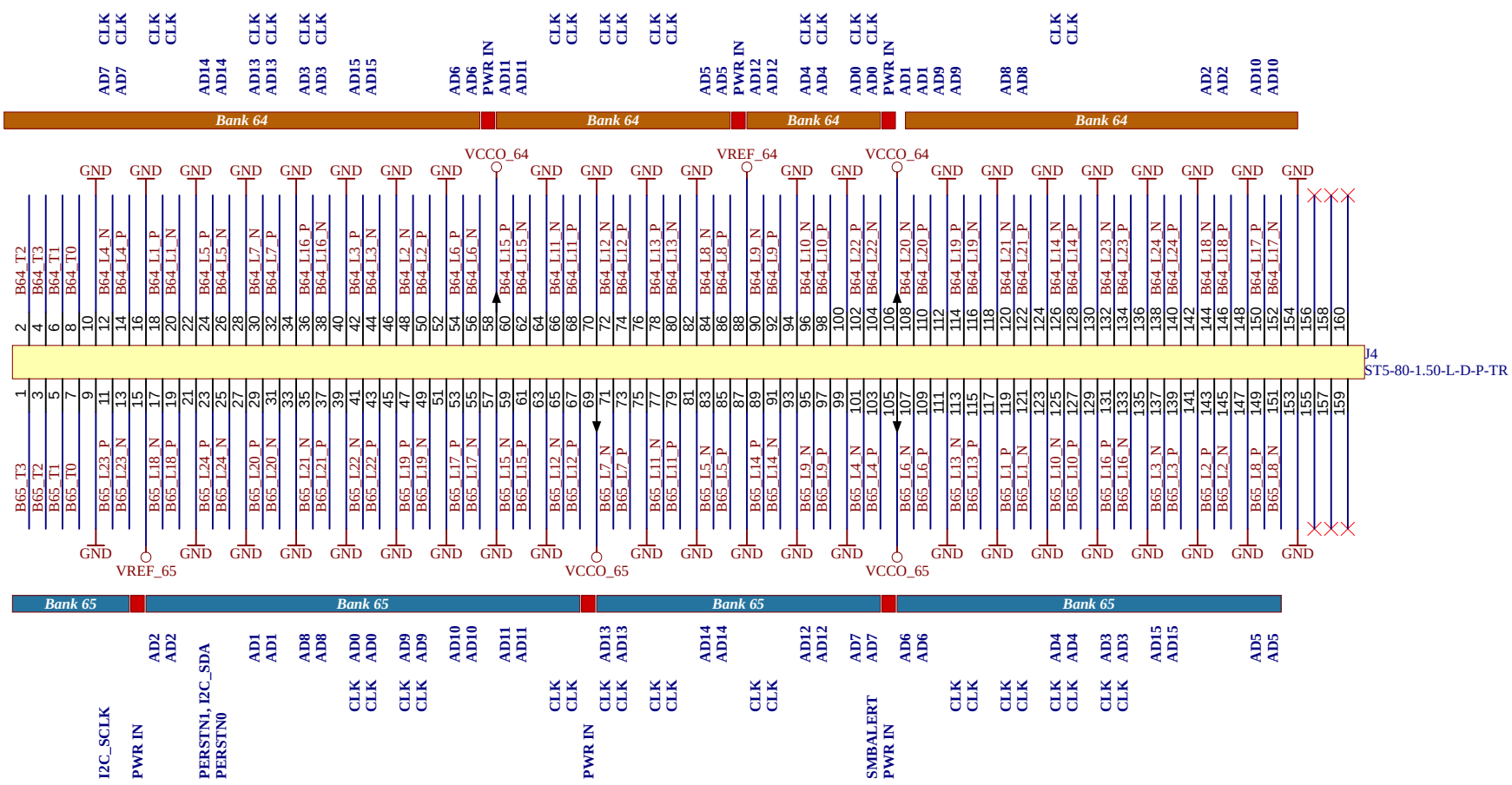
Filename: J3.SchDoc			

B64 52 IO, 24 LVDS Pairs
B65 52 IO, 24 LVDS Pairs



Bank 47 HD 0..VCCO47
Bank 48 HD 0..VCCO48
Bank 64 HP 0..VCCO64
Bank 65 HP 0..VCCO65
Bank 66 HP 0..VCCO66

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Title: TE0807 – Connector J4			
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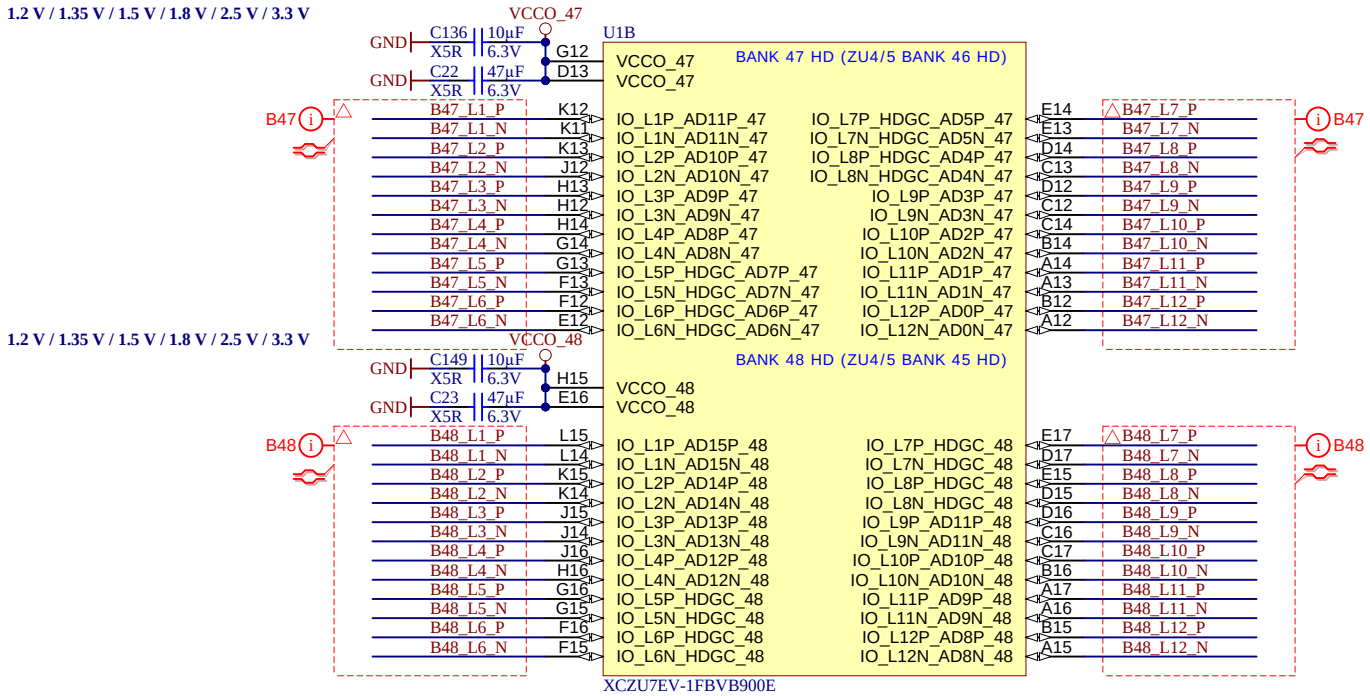
Filename: J4.SchDoc			



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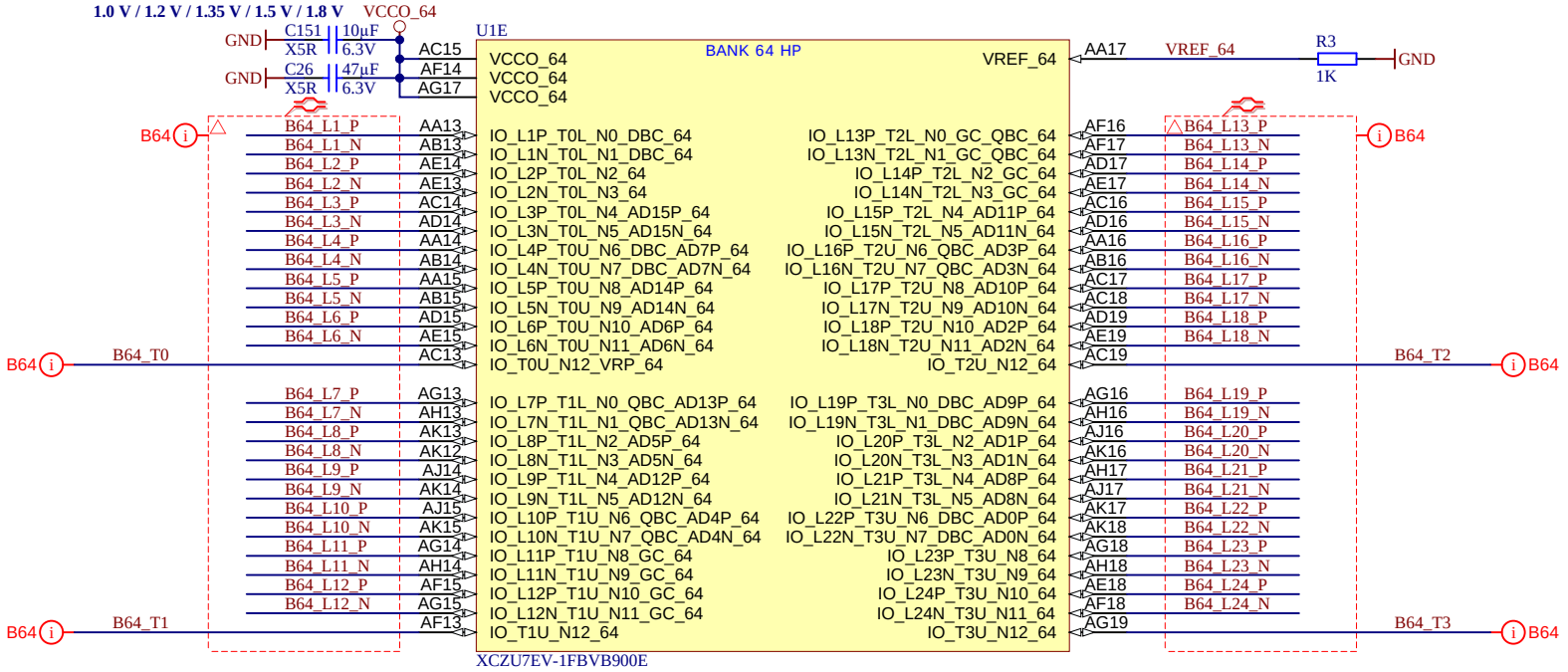
Date: 19.06.2024	Copyright: Trenz Electronic GmbH		Page 11 of 32
Filename: B_HD.SchDoc			



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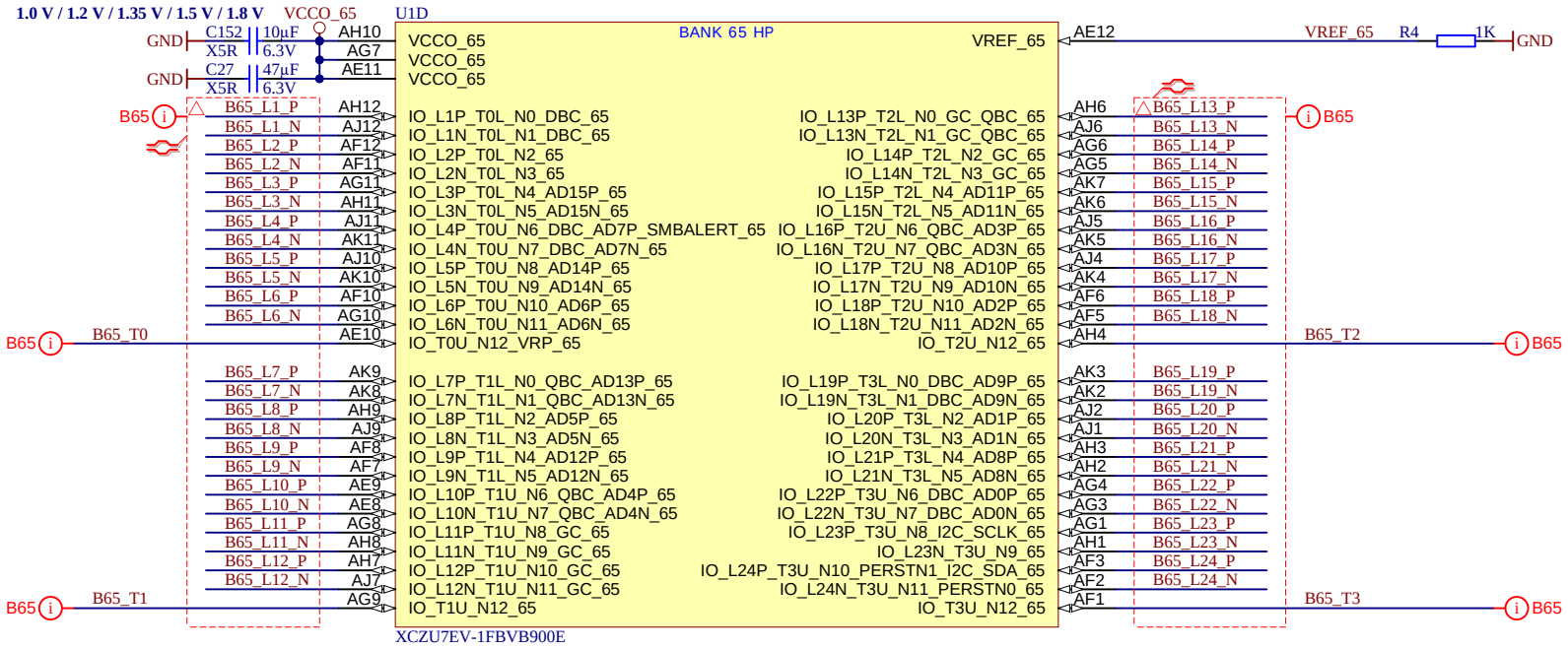
Date: 19.06.2024	Copyright: Trenz Electronic GmbH		Page 12 of 32
Filename: B64.SchDoc			



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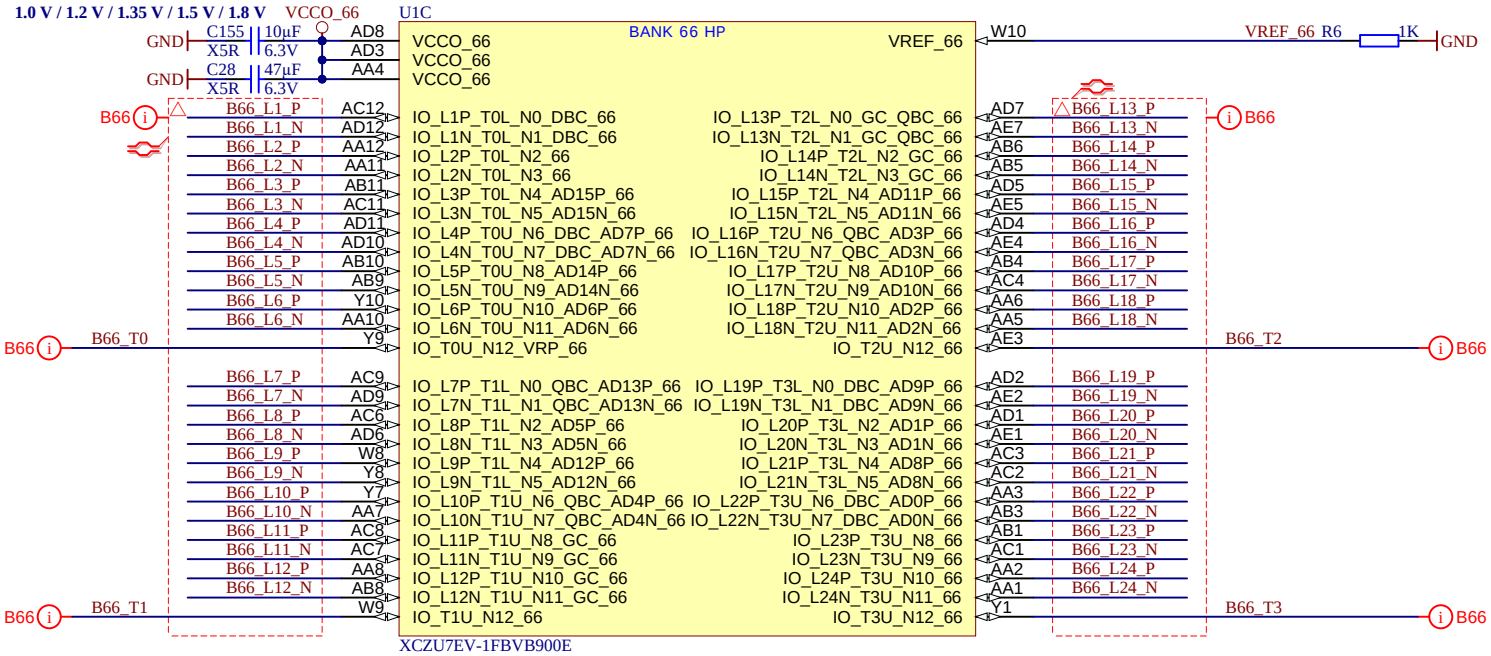
Filename: B65.SchDoc			



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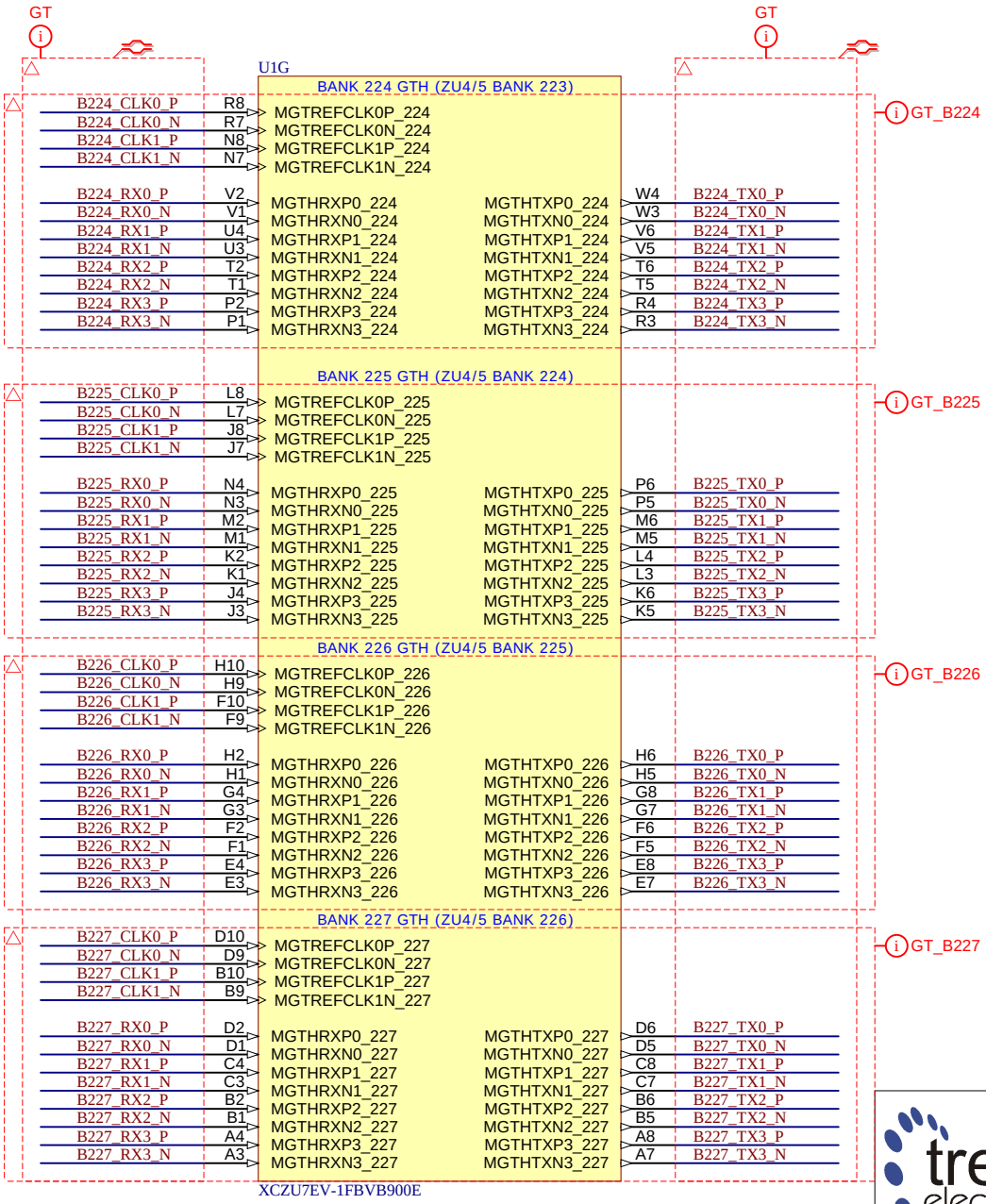
Filename: B66.SchDoc			



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Title: TE0807 – GTH Banks			
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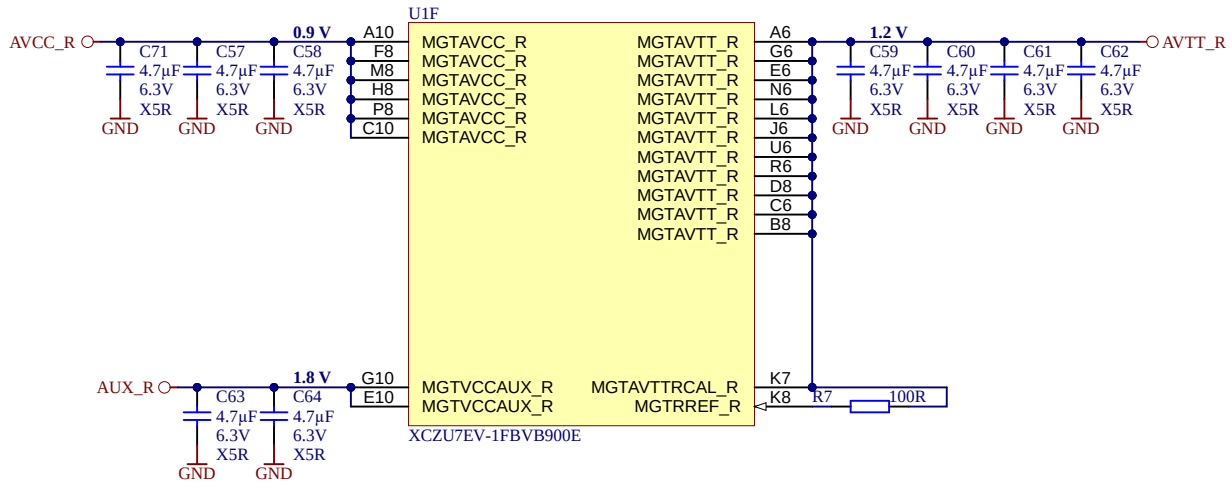
Filename: B_GT.SchDoc			



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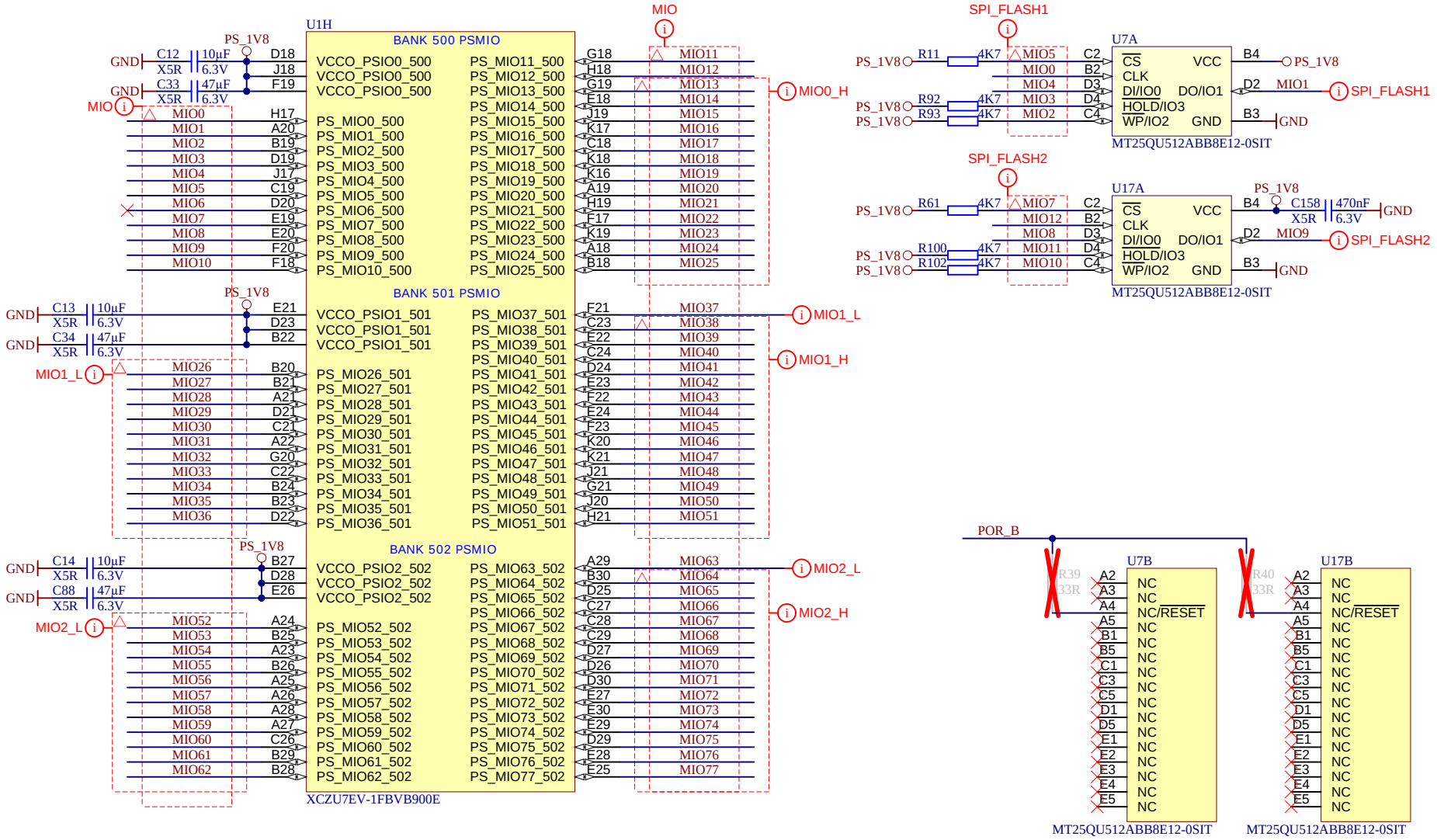
Filename: B_GT_2.SchDoc		



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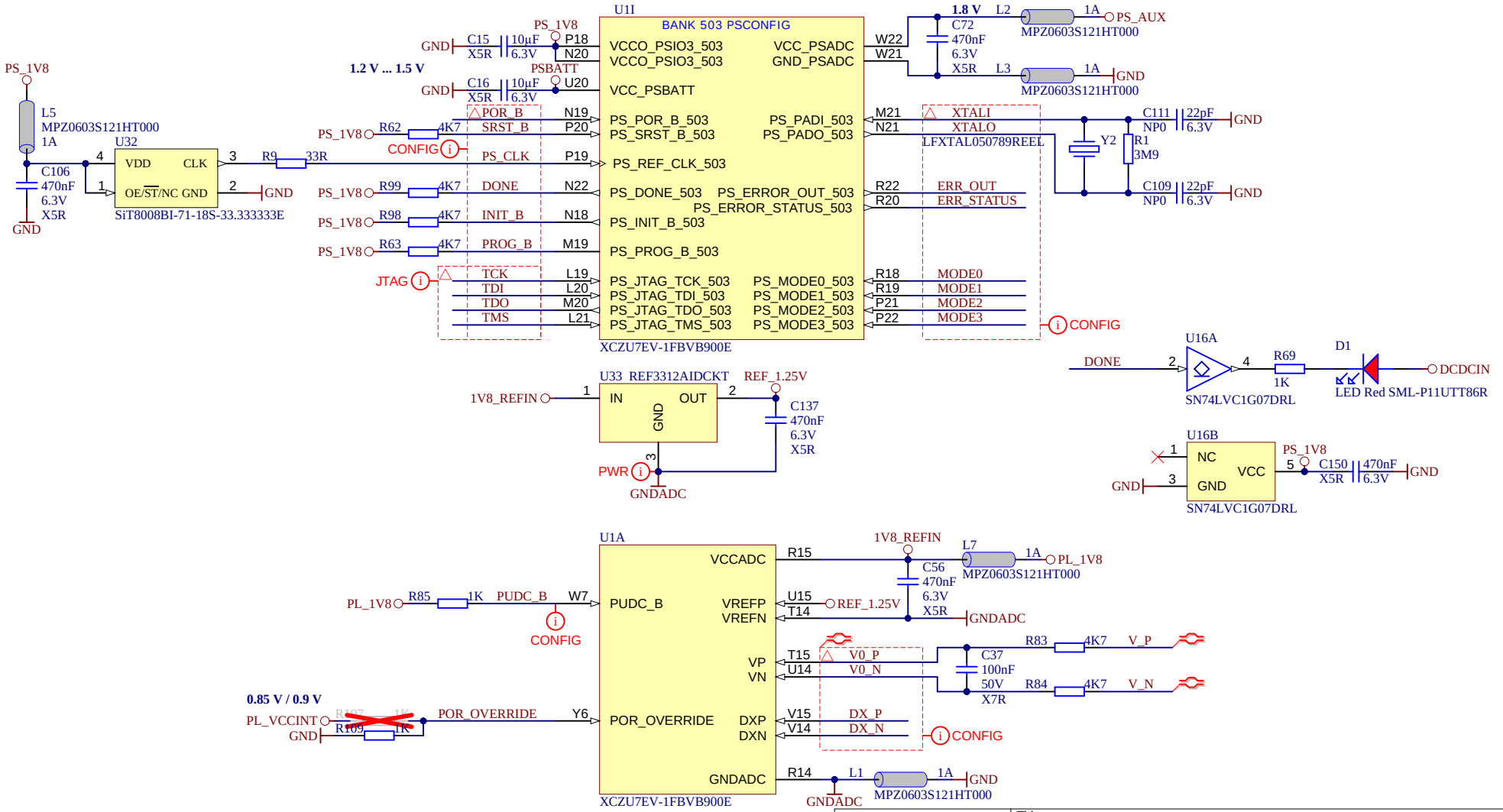
Date: 19.06.2024	Copyright: Trenz Electronic GmbH		Page 17 of 32
Filename: B_MIO.SchDoc			



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Title: TE0807 – Config		
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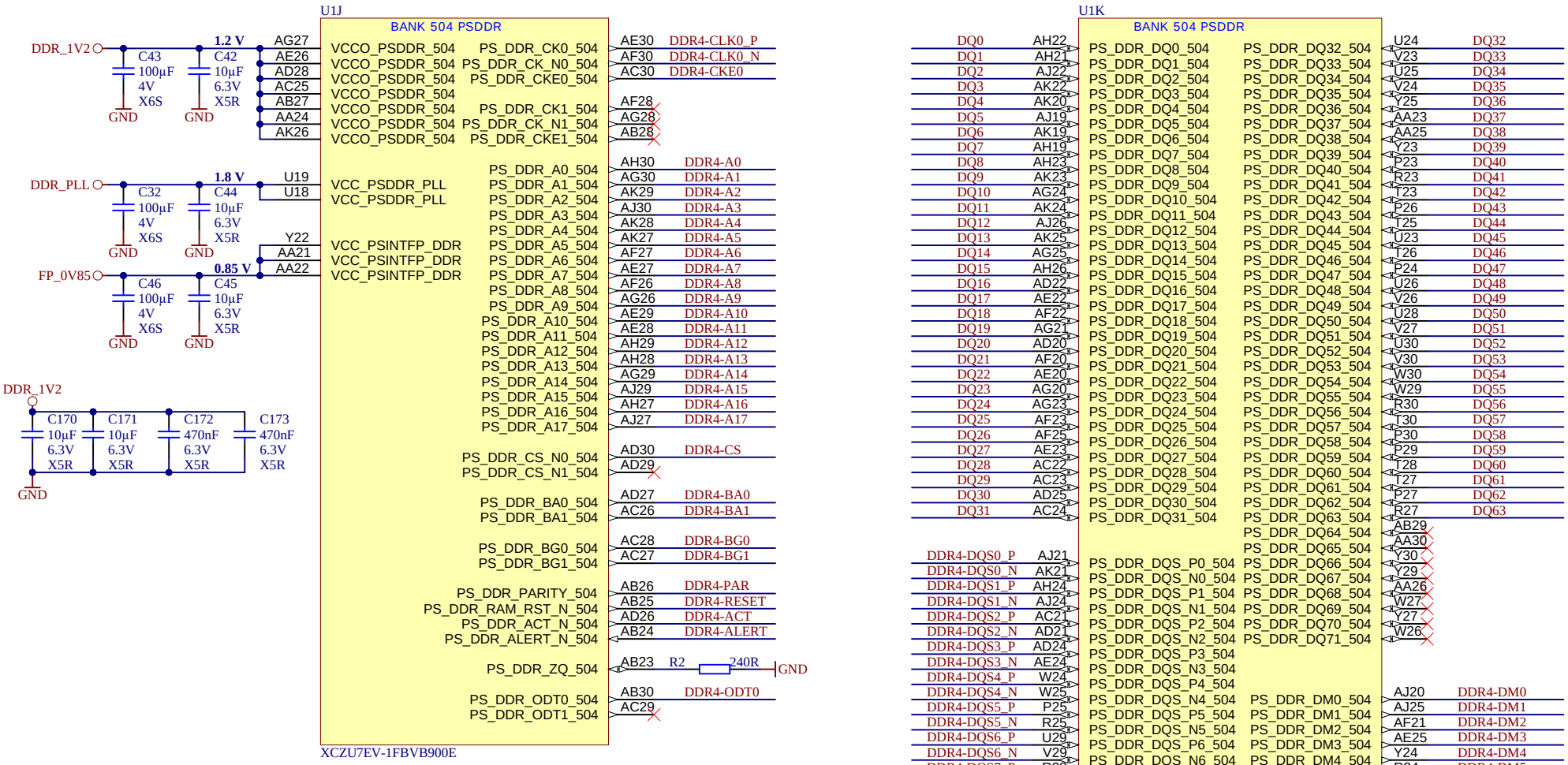
Filename: CONFIG.SchDoc		



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Date: 19.06.2024	Copyright: Trenz Electronic GmbH		Page 19 of 32
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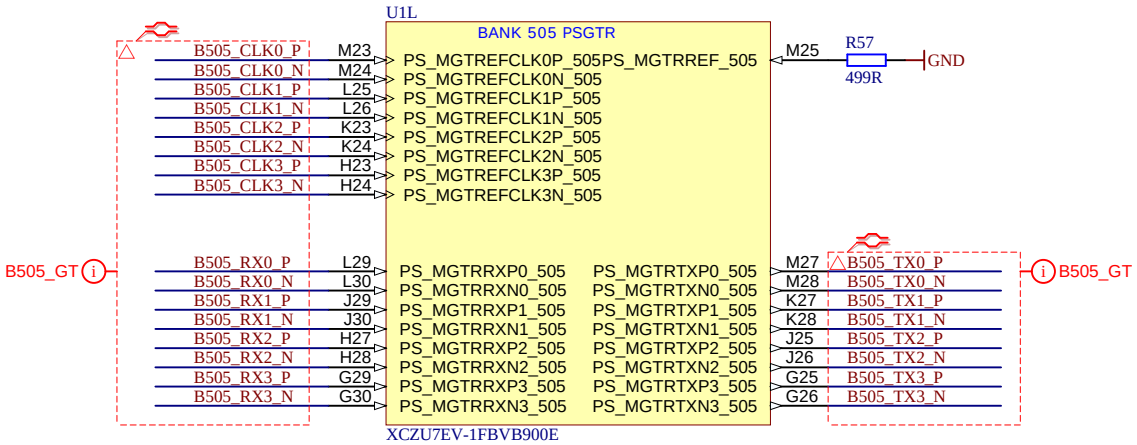

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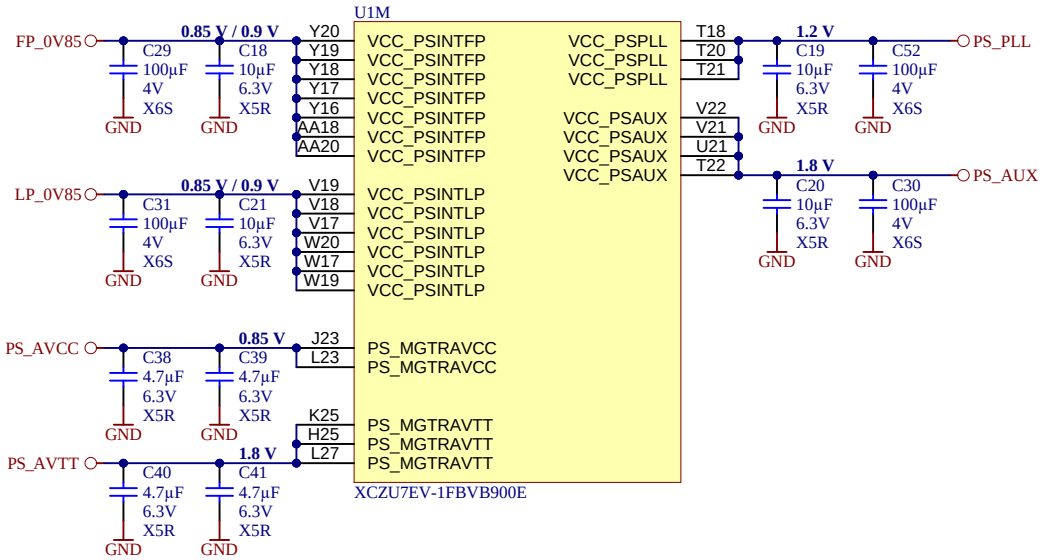
Date: 19.06.2024	Copyright: Trenz Electronic GmbH		Page 20 of 32
Filename: B_PS_GT.SchDoc			



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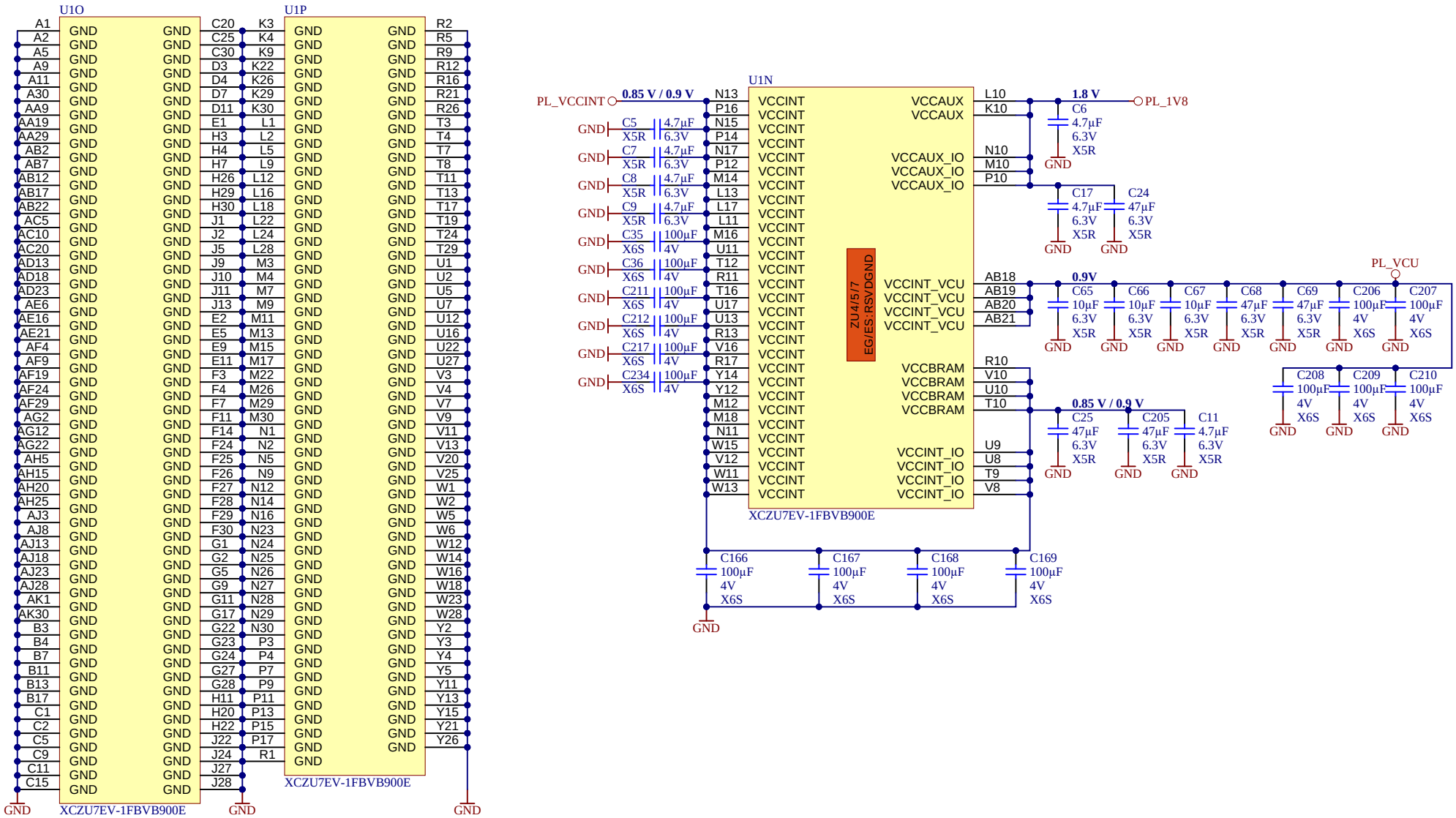
A4	Number: TE0807 7DE81-A		Rev. 04
Date: 19.06.2024	Copyright: Trenz Electronic GmbH		Page 21 of 32
Filename: ZU_PS_POWER.SchDoc			



Title: TE0807 – ZU_POWER			
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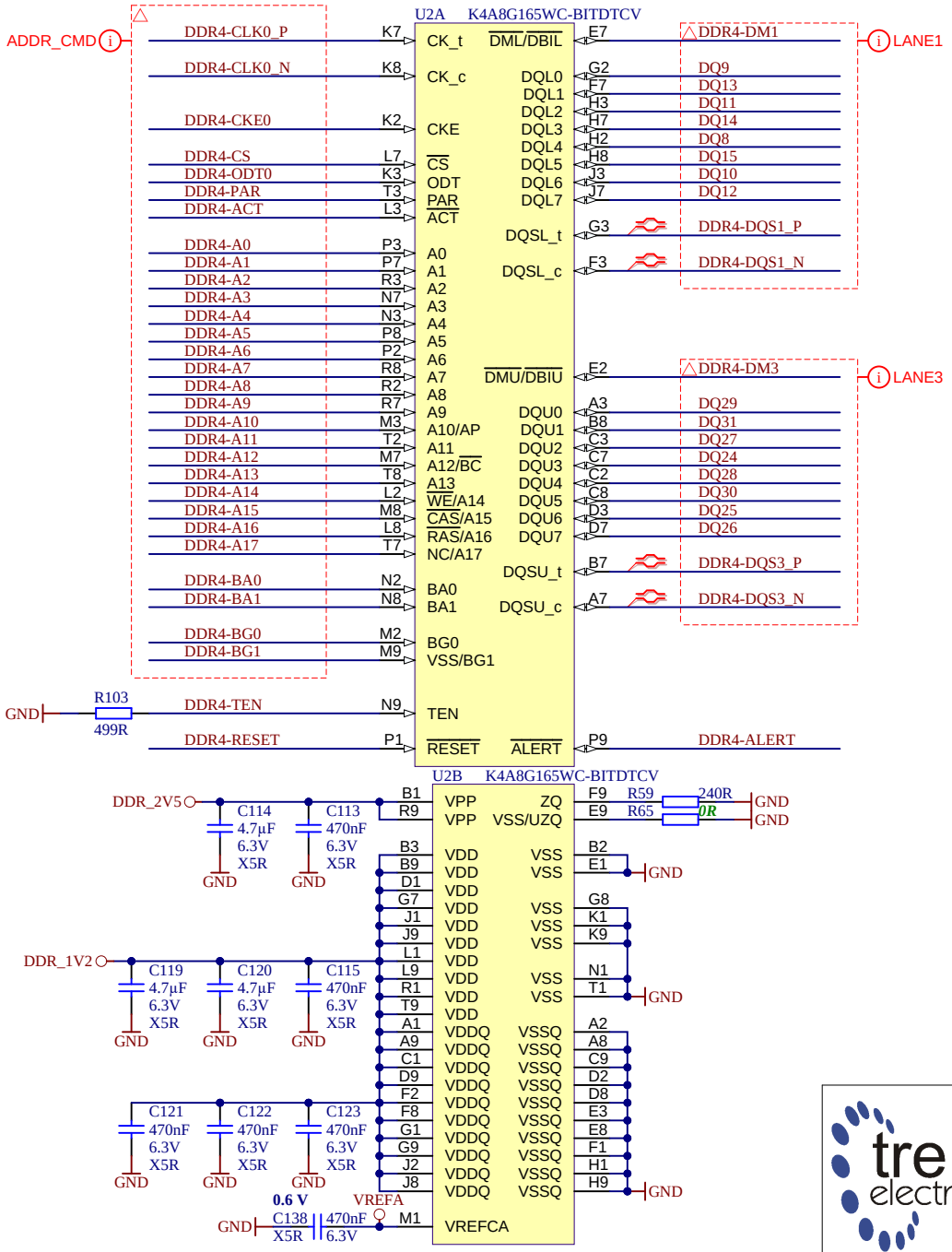
Date: 19.06.2024	Copyright: Trenz Electronic GmbH		Page 22 of 32
Filename: ZU_POWER.SchDoc			



trenz electronic	Title: TE0807 – DDR4-RAM_1		
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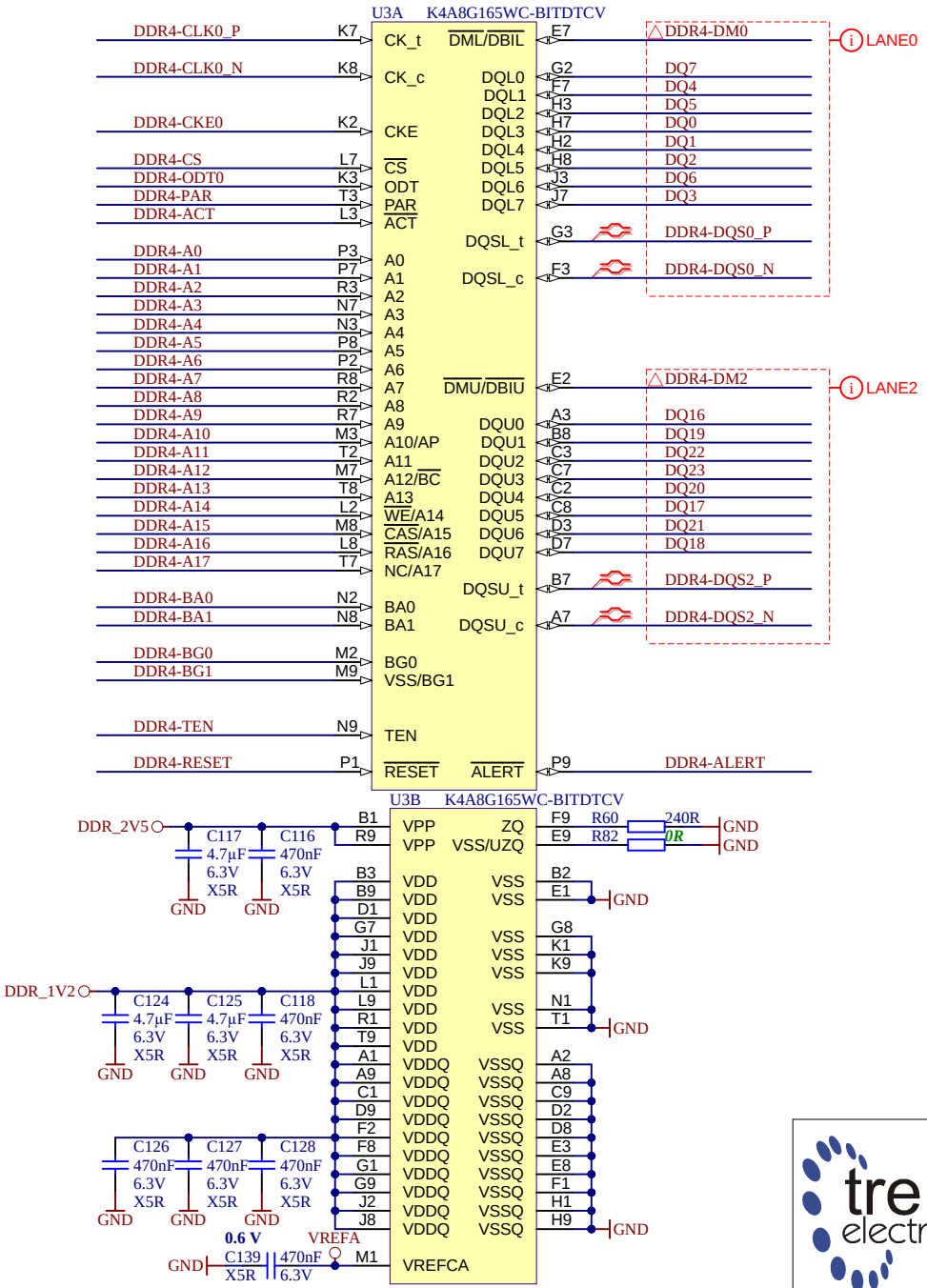
	Date: 19.06.2024	Copyright: Trenz Electronic GmbH	Page 23 of 32
	Filename: DDR4-RAM.SchDoc		



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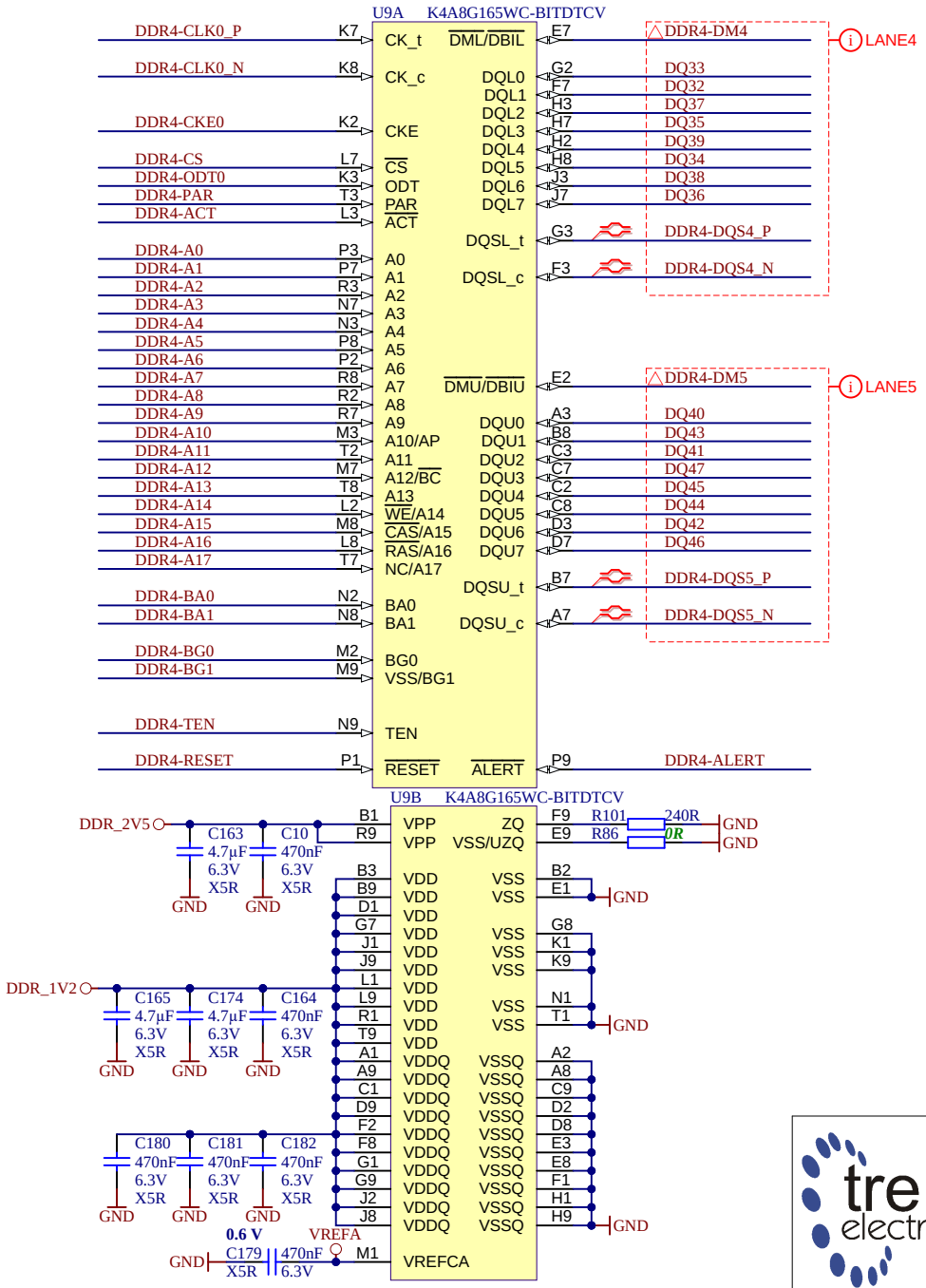
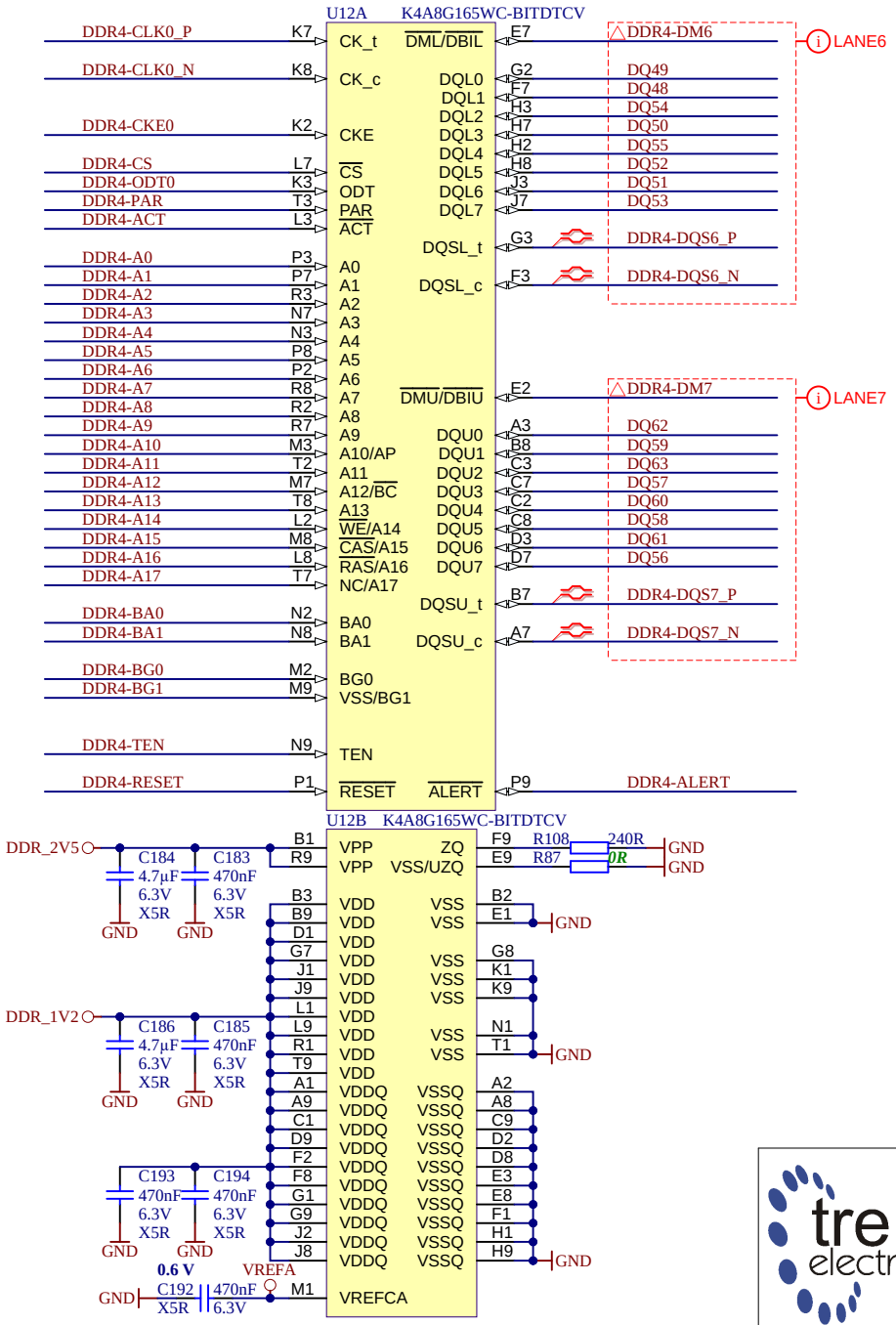
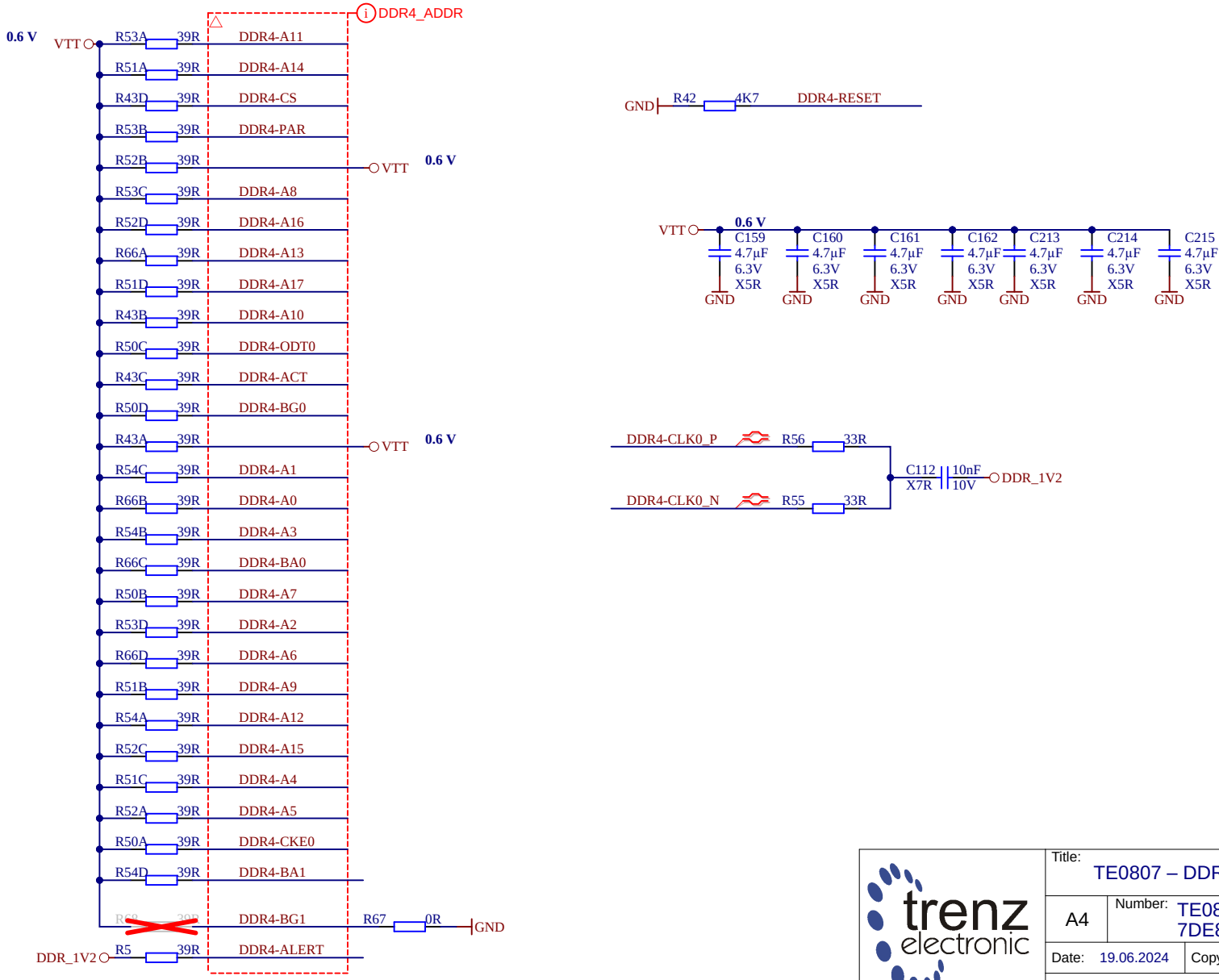
	Date: 19.06.2024	Copyright: Trenz Electronic GmbH	Page 24 of 32
	Filename: DDR4-RAM_2.SchDoc		



	Title: TE0807 – DDR4-RAM_3		
A4	Number: TE0807 7DE81-A		Rev. 04
Date: 19.06.2024	Copyright: Trenz Electronic GmbH		Page 25 of 32
Filename: DDR4-RAM_3.SchDoc			



Title: TE0807 – DDR4-RAM_4			
A4	Number: TE0807 7DE81-A		Rev. 04
Date: 19.06.2024	Copyright: Trenz Electronic GmbH		Page 26 of 32
Filename: DDR4-RAM_4.SchDoc			



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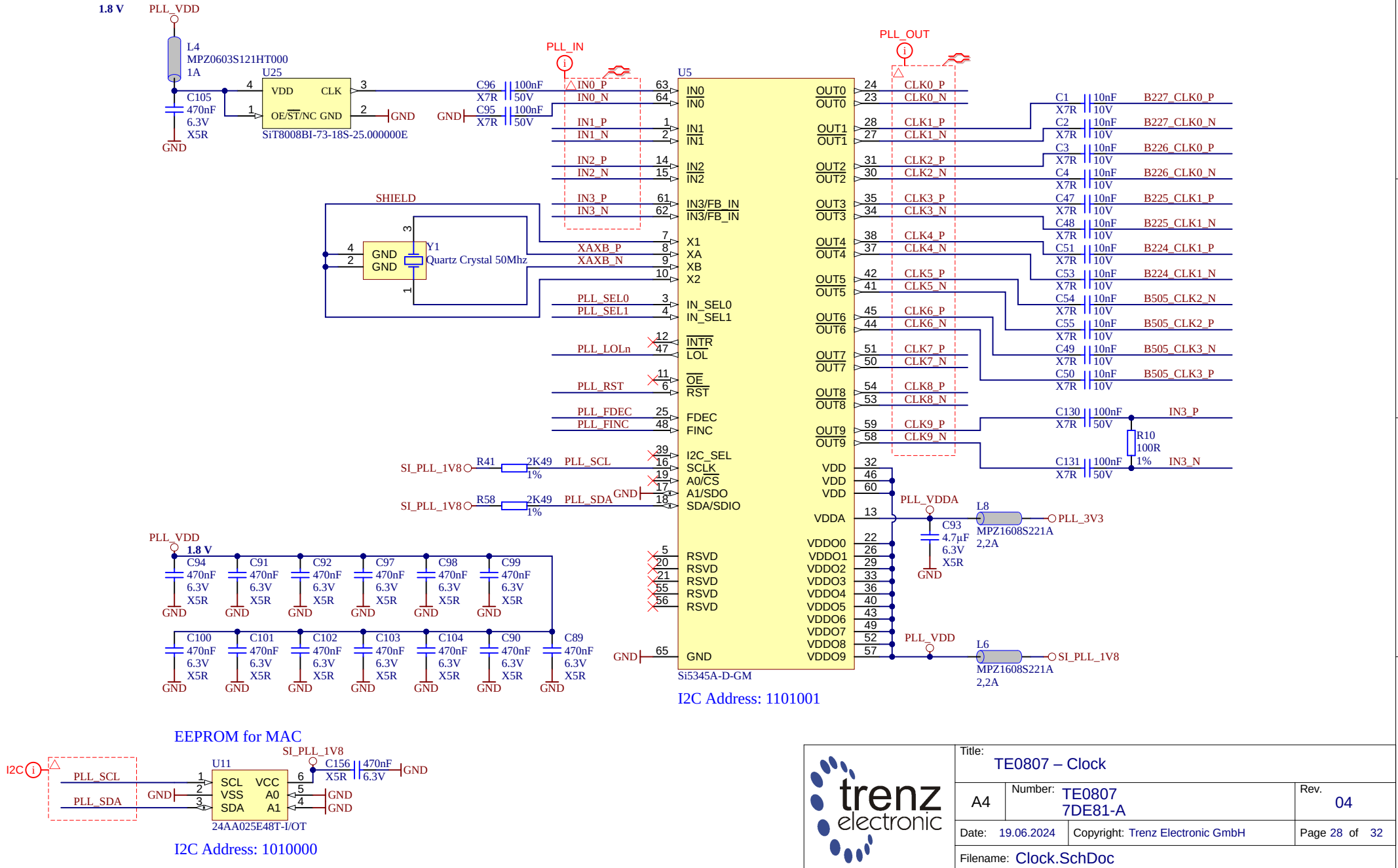
Title: TE0807 – DDR4-TERM		
A4	Number: TE0807 7DE81-A	Rev. 04
Date: 19.06.2024	Copyright: Trenz Electronic GmbH	Page 27 of 32
Filename: DDR4-TERM.SchDoc		


1.8 V
PLL_VDD
L4
MPZ0603S121HT000
1A
C105
470nF
6.3V
X5R
GND
U25
VDD
CLK
OE/ST/NC
GND
SiT8008BI-73-18S-25.000000E
C96
100nF
X7R
50V
C95
100nF
X7R
50V
PLL_IN
PLL_OUT
U5
IN0_P
IN0_N
IN1_P
IN1_N
IN2_P
IN2_N
IN3_P
IN3_N
IN3/FB_IN
IN3/FB_IN
SHIELD
Y1
Quartz Crystal 50Mhz
XAXB_P
XAXB_N
X1
XA
XB
X2
PLL_SEL0
PLL_SEL1
IN_SEL0
IN_SEL1
PLL_LOLn
INTR
LOL
PLL_RST
OE
RST
PLL_FDEC
PLL_FINC
FDEC
FINC
SI_PLL_1V8
R41
2K49
1%
PLL_SCL
I2C_SEL
SCLK
R58
PLL_SDA
A0/CS
A1/SDO
SDA/SDIO
RSVD
GND
OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
OUT9
CLK0_P
CLK0_N
CLK1_P
CLK1_N
CLK2_P
CLK2_N
CLK3_P
CLK3_N
CLK4_P
CLK4_N
CLK5_P
CLK5_N
CLK6_P
CLK6_N
CLK7_P
CLK7_N
CLK8_P
CLK8_N
CLK9_P
CLK9_N
VDD
VDDA
VDDO0
VDDO1
VDDO2
VDDO3
VDDO4
VDDO5
VDDO6
VDDO7
VDDO8
VDDO9
Si5345A-D-GM
I2C Address: 1101001
C1
C2
C3
C4
C47
C48
C51
C53
C54
C55
C49
C50
10nF
X7R
10V
B227_CLK0_P
B227_CLK0_N
B226_CLK0_P
B226_CLK0_N
B225_CLK1_P
B225_CLK1_N
B224_CLK1_P
B224_CLK1_N
B505_CLK2_N
B505_CLK2_P
B505_CLK3_N
B505_CLK3_P
C130
C131
100nF
X7R
50V
IN3_P
IN3_N
R10
100R
1%
PLL_VDDA
L8
MPZ1608S221A
2,2A
PLL_3V3
C93
4.7µF
6.3V
X5R
L6
SI_PLL_1V8
C94
C91
C92
C97
C98
C99
C100
C101
C102
C103
C104
C90
C89
470nF
6.3V
X5R
EEPROM for MAC
I2C
U11
SCL
VSS
SDA
VCC
A0
A1
C156
24AA025E48T-I/OT
I2C Address: 1010000
trenz electronic
Title: TE0807 – Clock
A4
Number: TE0807 7DE81-A
Rev. 04
Date: 19.06.2024
Copyright: Trenz Electronic GmbH
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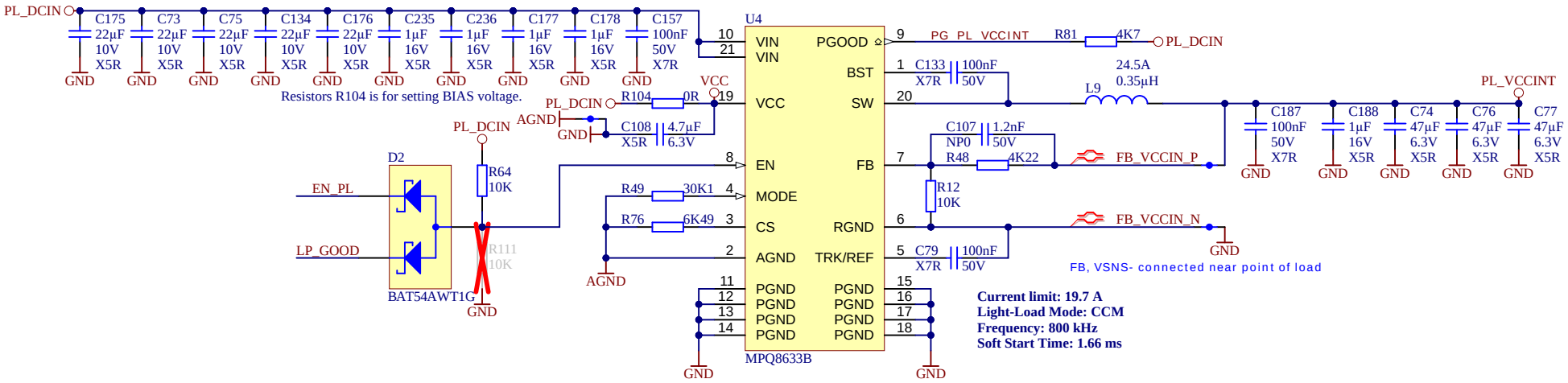
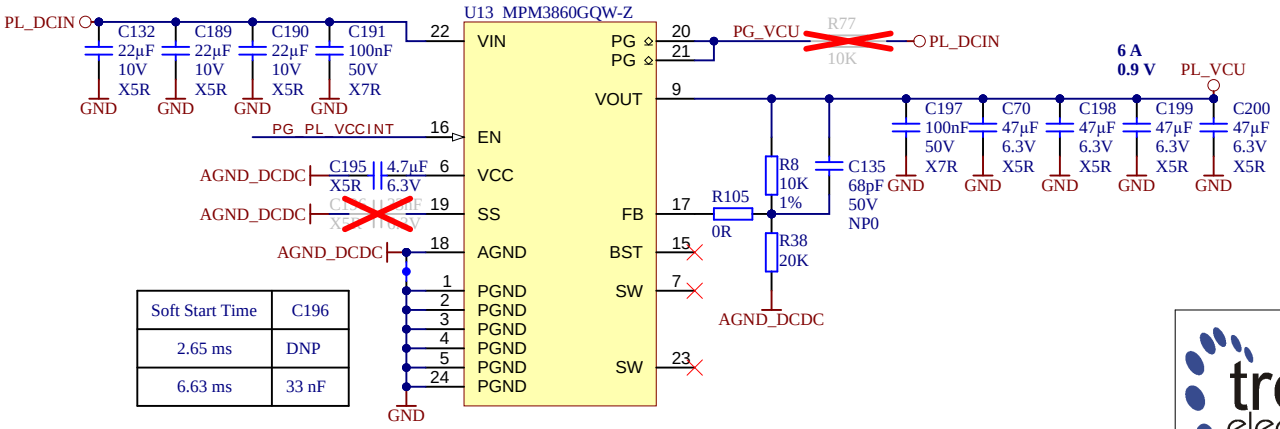
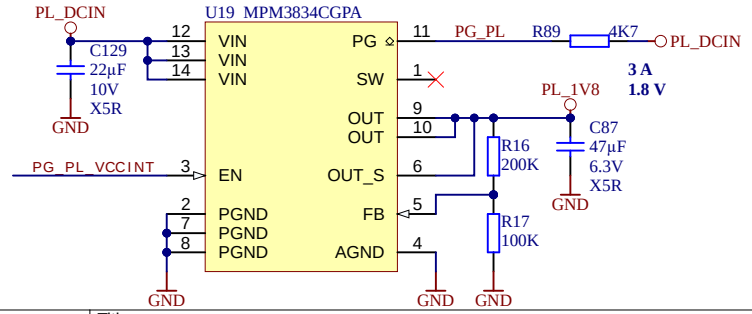
Filename: Clock.SchDoc



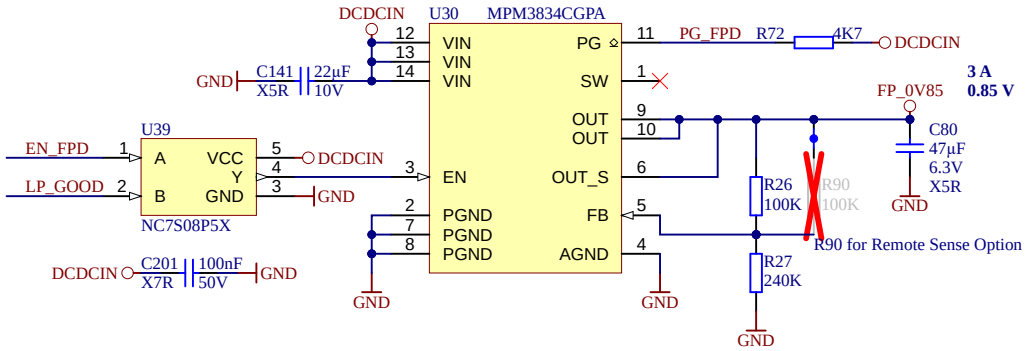
FPGA Speedgrade	R48	R12	PL_VCCINT	C107
-1	4.22 kOhm	10 kOhm	0.853 V	1.2 nF
-2	4.22 kOhm	10 kOhm	0.853 V	1.2 nF
-3	10 kOhm	20 kOhm	0.900 V	560 pF

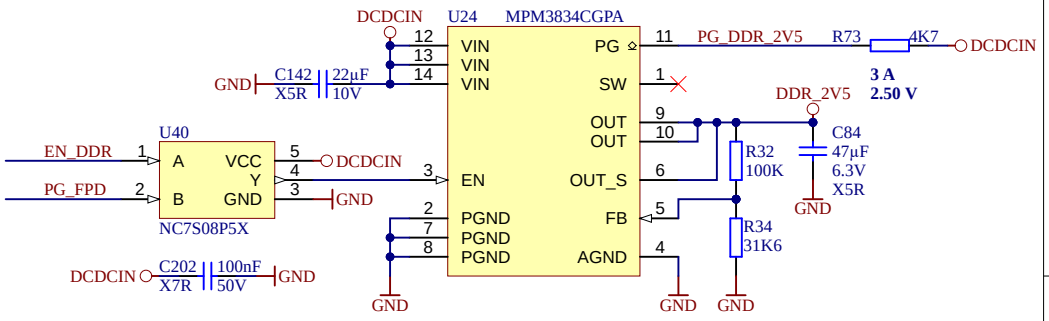


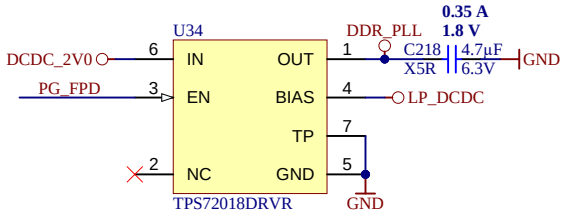
Soft Start Time	C196
2.65 ms	DNP
6.63 ms	33 nF

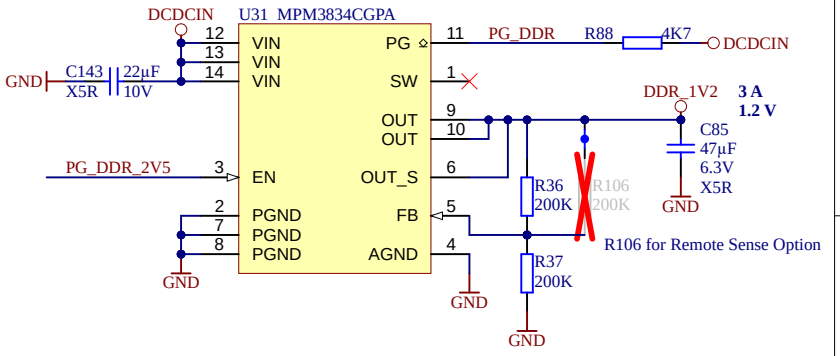


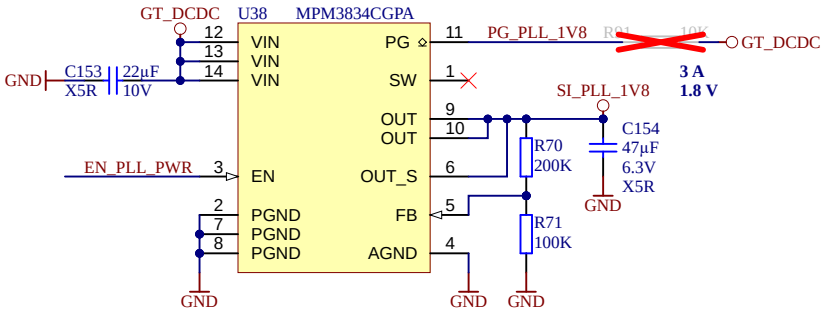
Title: TE0807 – POWER_1			
A4	Number: TE0807 7DE81-A		Rev. 04
Date: 19.06.2024	Copyright: Trenz Electronic GmbH		Page 29 of 32
Filename: POWER.SchDoc			

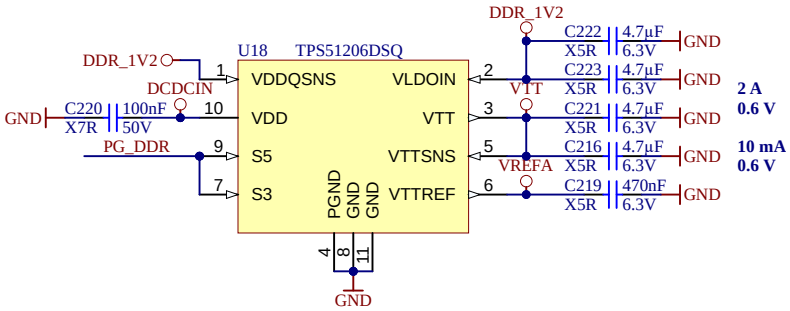

DCDCIN
U30
MPM3834CGPA
VIN
VIN
VIN
PG
SW
OUT
OUT
EN
OUT_S
PGND
PGND
PGND
FB
AGND
PG_FPD
R72
4K7
DCDCIN
3 A
0.85 V
FP_0V85
C80
47µF
6.3V
X5R
R26
100K
R90
100K
R90 for Remote Sense Option
R27
240K
GND
C141
22µF
10V
X5R
U39
NC7S08P5X
EN_FPD
LP_GOOD
A
B
VCC
Y
GND
C201
100nF
50V
X7R

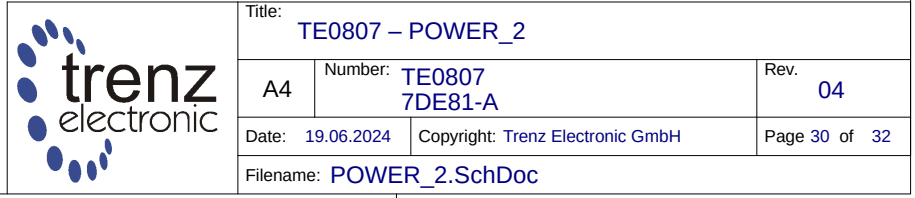

DCDCIN
U24
MPM3834CGPA
VIN
VIN
VIN
PG
SW
OUT
OUT
EN
OUT_S
PGND
PGND
PGND
FB
AGND
PG_DDR_2V5
R73
4K7
DCDCIN
3 A
2.50 V
DDR_2V5
C84
47µF
6.3V
X5R
R32
100K
R34
31K6
GND
C142
22µF
10V
X5R
U40
NC7S08P5X
EN_DDR
PG_FPD
A
B
VCC
Y
GND
C202
100nF
50V
X7R


U34
TPS72018DRVR
DCDC_2V0
PG_FPD
IN
EN
NC
OUT
BIAS
TP
GND
DDR_PLL
0.35 A
1.8 V
C218
4.7µF
6.3V
X5R
LP_DCDC
GND


DCDCIN
U31
MPM3834CGPA
VIN
VIN
VIN
PG
SW
OUT
OUT
EN
OUT_S
PGND
PGND
PGND
FB
AGND
PG_DDR
R88
4K7
DCDCIN
DDR_1V2
3 A
1.2 V
C85
47µF
6.3V
X5R
R36
200K
R106
200K
R106 for Remote Sense Option
R37
200K
GND
C143
22µF
10V
X5R
PG_DDR_2V5


GT_DCDC
U38
MPM3834CGPA
VIN
VIN
VIN
PG
SW
OUT
OUT
EN
OUT_S
PGND
PGND
PGND
FB
AGND
PG_PLL_1V8
GT_DCDC
3 A
1.8 V
SI_PLL_1V8
C154
47µF
6.3V
X5R
R70
200K
R71
100K
GND
C153
22µF
10V
X5R
EN_PLL_PWR


DDR_1V2
U18
TPS51206DSQ
VDDQSNS
VDD
S5
S3
VLDOIN
VTT
VTTSNS
VTTREF
PGND
GND
GND
DDR_1V2
DCDCIN
PG_DDR
C220
100nF
50V
X7R
C222
4.7µF
6.3V
X5R
C223
4.7µF
6.3V
X5R
C221
4.7µF
6.3V
X5R
C216
4.7µF
6.3V
X5R
C219
470nF
6.3V
X5R
VTT
VREFA
2 A
0.6 V
10 mA
0.6 V
GND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electronic
Title:
TE0807 – POWER_2
A4
Number:
TE0807
7DE81-A
Rev.
04
Date:
19.06.2024
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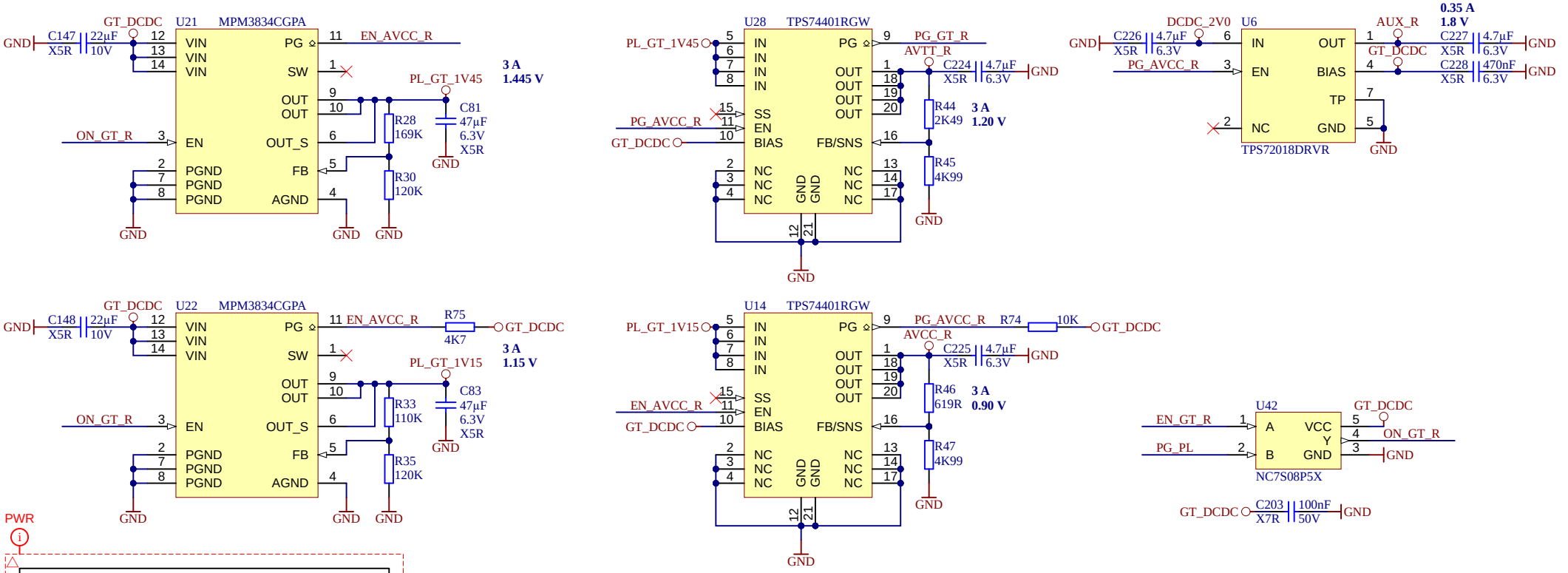
Filename:
POWER_2.SchDoc



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Title: TE0807 – POWER_3		
A4	Number: TE0807 7DE81-A	Rev. 04
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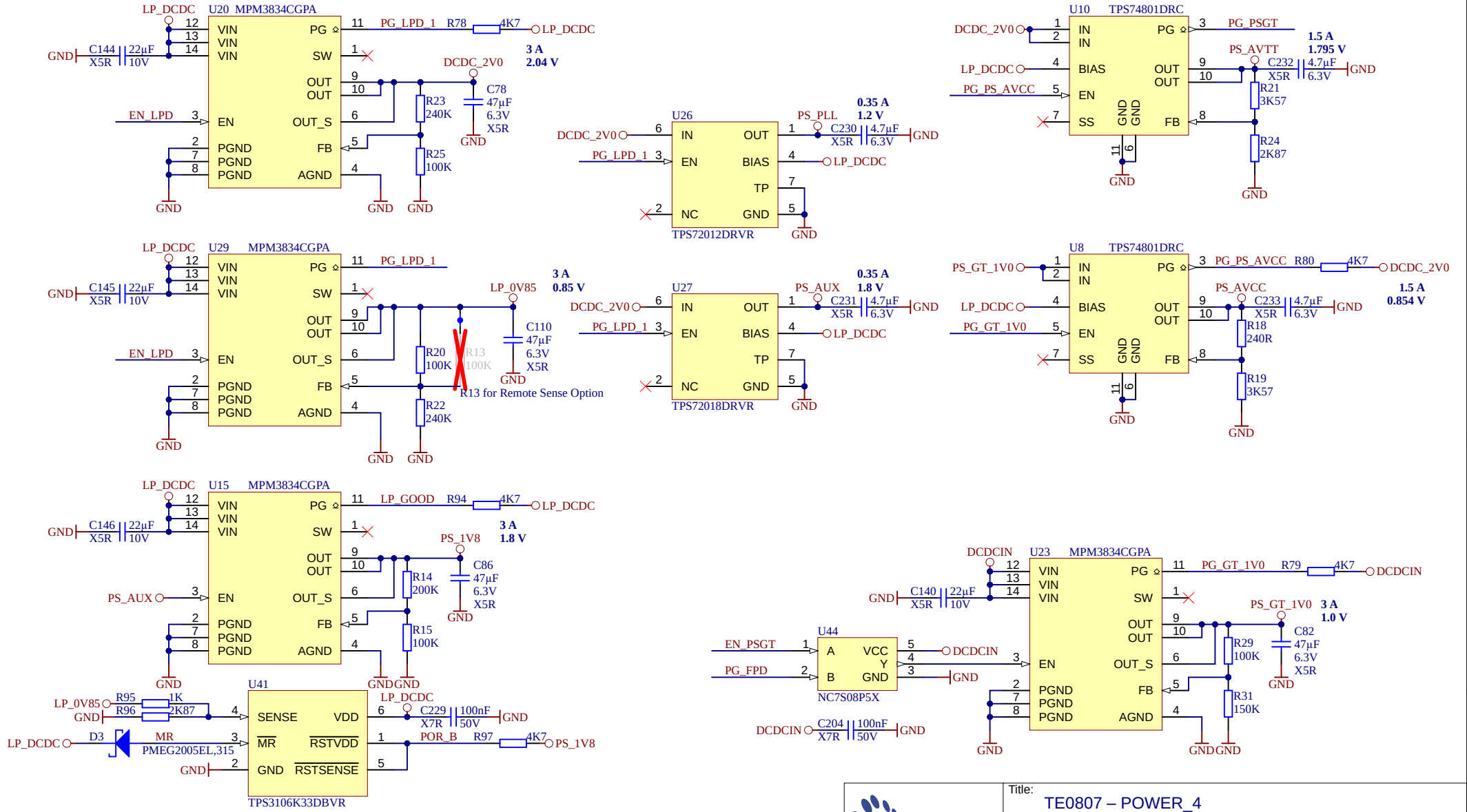
Filename: POWER_3.SchDoc		



Net Name	Voltage Rail	Low Detect
LP_0V85	0.85 V	0.743 V
LP_DCDC	3.3 V	2.941 V

Title: TE0807 – POWER_4		
A4	Number: TE0807 7DE81-A	Rev. 04
Date: 19.06.2024	Copyright: Trenz Electronic GmbH	Page 32 of 32
Filename: POWER_4.SchDoc		