



TE0807 Test Board

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Online version of this manual and other related documents can be found at <https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation>

Overview

Design Example with minimum PS Setup (DDR, QSPI, UART0) only for custom boards or easier debug via SDK.

Key Features

- QSPI
- SDK
- Custom Carrier (with other MIO settings as TEBF0808)

Revision History

Date	Vivado	Project Built	Authors	Description
2017-11-14	2017.2	TE0807-test_board_noprebuilt-vivado_2017.2-build_05_20171114115524.zip TE0807-test_board-vivado_2017.2-build_05_20171114115511.zip	John Hartfiel	initial release

Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Requirements

Software

Software	Version	Note
Vivado	2017.2	needed
SDK	2017.2	needed

Hardware

Basic description of TE Board Part Files is available on [TE Board Part Files](#).

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	Notes
TE0807-01-ES2	es2	REV01	

Note: Design contains also Board Part Files for TE0803+TEBF0808 configuration, this board part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
Custom PCB	use simple Board Part files, if MIO connected is different to TEBF0808
TEBF0808	Used as reference carrier.
TEBT0808	Change UART0 to UART1 (MIO68...69) and regenerate design

Additional HW Requirements:

Additional Hardware	Notes
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Content

For general structure and of the reference design, see [Project Delivery](#)

Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI

Additional Sources

Type	Location	Notes
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Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- [TE0807 Test Board](#)

Design Flow



Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

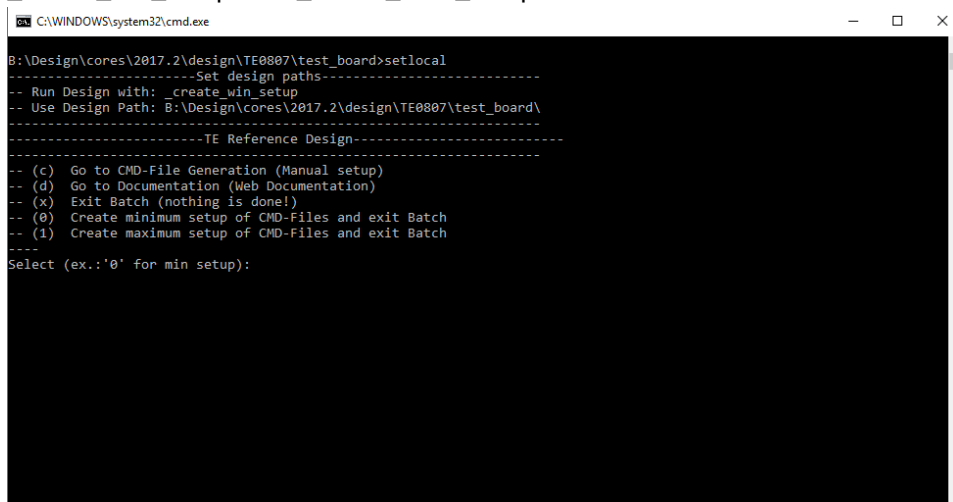
See also:

- [Vivado/SDK/SDSoC#XilinxSoftware-BasicUserGuides](#)
- [Vivado Projects](#)
- [Project Delivery.](#)

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: [Project Delivery Currently limitations of functionality](#)

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x:\<design name>)
4. Create Project
 - a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guiemode.cmd"

Note: Select correct one, see [TE Board Part Files](#)

Use Board Part Files, which **did not** contains with *_tebf0808

5. Create HDF and export to prebuilt folder

- a. Run on Vivado TCL: `TE::hw_build_design -export_prebuilt`

Note: Script generate design and export files into `\prebuilt\hardware\<short dir>`. Use GUI is the same, except file export to prebuilt folder

6. Generate Programming Files with HSI/SDK

- a. Run on Vivado TCL: `TE::sw_run_hsi`

Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"

- b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: `TE::sw_run_sdk`

Note: See [SDK Projects](#)

Launch

Programming



Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: [Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging](#)

QSPI

1. Select JTAG as Boot Mode (see Carrier Description and ZynqMP TRM)
2. Connect JTAG to Host PC
3. Power On
4. Open Vivado Hardware Manager with Auto Connect
5. Right Click to FPGA Device XCU... and select Add Configuration Memory Device
 - a. Select correct Flash Typ (see schematics or FPGAFLASHTYP on test_board/board_files/TE0808_board_files.csv)
6. Open Program Configuration Memory Device
 - a. Configuration file: test_board/prebuilt/boot_image/<short dir>/hello_te0803/Boot.bin
 - b. Zynq FSBL: test_board/prebuilt/software/<short dir>/zynqmp_fsbl.elf
 - c. Program Device Flash

Use SDK instead of Vivado is also possible, see: [SDK Projects#Xilinx%22HelloWorld%22onZynqMP](#)

SD

This does not work, because SD controller is not selected on PS.

JTAG

Load configuration and Application with SDK Debugger into device, see:

- [SDK Projects](#)
- [SDK Projects#DebugSoftwareApplication](#)

Usage

QSPI Boot:

1. Prepare HW like described on section [Programming](#)
2. Connect UART USB (most cases same as JTAG)

3. Select QSPI Card as Boot Mode

Note: See TRM of the Carrier, which is used.

4. Power On PCB

Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from QSPI into OCM, 2. FSBL loads Application into DDR

Debugging:

- [SDK Projects](#)
- [SDK Projects#DebugSoftwareApplication](#)

System Design - Vivado

Block Design



PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
UART0	MIO, please select other one, if you have connected uart to second controller or other MIO

Constrains

Basic module constrains

```
_i_bitgen.xdc

set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

Design specific constrain

Not needed.

Software Design - SDK/HSI

For SDK project creation, follow instructions from:

[SDK Projects](#)

Application

FSBL

Xilinx default FSBL

Hello TE0803

Hello TE0803 is a Xilinx Hello World example as endless loop instead of one console output.


Additional Software

No additional software is needed.

Appx. A: Change History and Legal Notices

Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2019-02-07	 v.9 Unbekanntes Makro: 'metadata'	John Hartfiel	<ul style="list-style-type: none">Release 2017.2
	All	John Hartfiel	

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