TE0807 Test Board

Revision v.9

Exported on 2019-05-06

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0807+Test+Board

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Online version of this manual and other related documents can be found at https://wiki.trenz-electronic.de/display/PD/Trenz+Electronic+Documentation

4 Overview

Design Example with minimum PS Setup (DDR, QSPI, UART0) only for custom boards or easier debug via SDK.

4.1 Key Features

- QSPI
- SDK
- Custom Carrier (minimum PS Design with available module components only)
- Special FSBL for QSPI Programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2019-02-08	2018.2	TE0807-test_board_noprebuilt-vivado_2018.2-build_04_20190207111539.zip TE0807-test_board-vivado_2018.2-build_04_20190207111524.zip	John Hartfiel	• new assembly variant
2018-09-04	2018.2	TE0807-test_board_noprebuilt-vivado_2018.2-build_03_20180904121458.zip TE0807-test_board-vivado_2018.2-build_03_20180904121522.zip	John Hartfiel	• additional notes for FSBL generated with Win SDK • changed *.bif

Date	Vivado	Project Built	Authors	Description
2018-01-18	2017.4	TE0807-test_board_noprebuilt-vivado_2017.4-build_05_20180118152119.zip TE0807-test_board-vivado_2017.4-build_05_20180118152104.zip	John Hartfiel	• rework Board Part Files
2017-11-14	2017.2	TE0807-test_board_noprebuilt-vivado_2017.2-build_05_20171114115524.zip TE0807-test_board-vivado_2017.2-build_05_20171114115511.zip	John Hartfiel	• initial release

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vivado	2017.8	needed
SDK	2017.8	needed

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[1]

1 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	Others	Notes
TE0807-01-ES2	es2	REV01	2GB	64MB		
TE0807-02-07EV-1E	7ev_1e	REV02	4GB	64MB		

Note: Design contains also Board Part Files for TE0807+TEBF0808 configuration, this boart part files are not used for this reference design.

Design supports following carriers:

Carrier Model	Notes
Custom PCB	use simple Board Part files, if MIO connected is different to TEBF0808
TEBF0808	Used as reference carrier.
TEBT0808	Change UART0 to UART1 (MIO68...69) and regenerate design

Additional HW Requirements:

Additional Hardware	Notes

4.5 Content

For general structure and of the reference design, see Project Delivery[2]

4.5.1 Design Sources

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for SDK/HSI and apps_list.csv with settings for HSI

2 https://wiki.trenz-electronic.de/display/PD/Project+Delivery

4.5.2 Additional Sources

Type	Location	Notes

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.hdf	Exported Vivado Hardware Specification for SDK/HSI and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0807 "Test Board" Reference Design[3]

3 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0807/Reference_Design/2018.2/test_board

5 Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

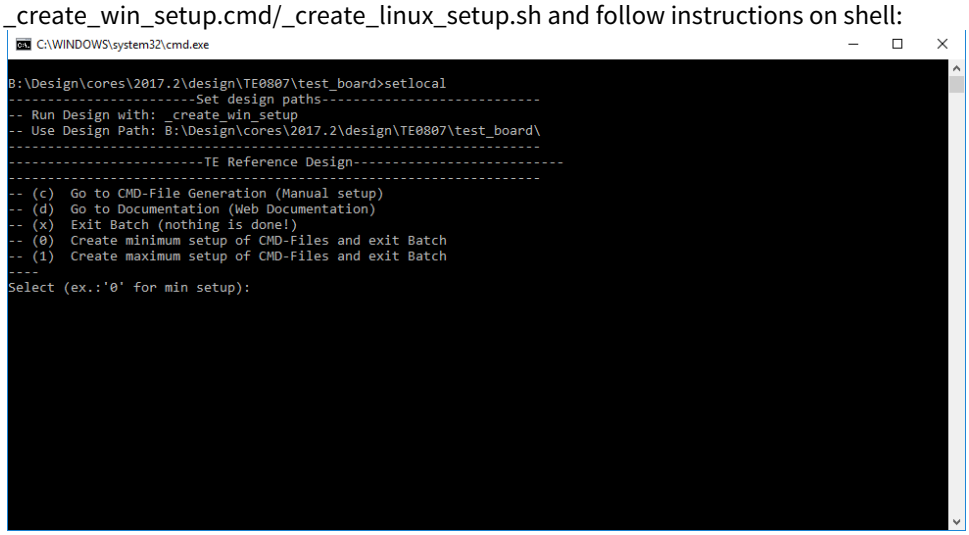
See also:

- Vivado/SDK/SDSoC[4]
- Vivado Projects[5]
- Project Delivery.[6]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[7]

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter for minimum setup
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project
   a. Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
      Note: Select correct one, see TE Board Part Files [8] Important: Use Board Part Files, which **did not** ends with *_tebf0808
5. Create HDF and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
      Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Generate Programming Files with HSI/SDK

4 https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=14746264#Vivado/SDK/SDSoC-XilinxSoftware-BasicUserGuides
5 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects
6 https://wiki.trenz-electronic.de/display/PD/Project+Delivery
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery#ProjectDelivery-Currentlylimitationsoffunctionality
8 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

a. Run on Vivado TCL: TE::sw_run_hsi
   Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_sdk
   Note: See SDK Projects[9]

9 https://wiki.trenz-electronic.de/display/PD/SDK+Projects

6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging[10]

6.1.1 QSPI

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash_binfile -swapp hello_te0807
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup

Use SDK instead of Vivado is also possible, see: SDK Projects#Xilinx%22HelloWorld%22onZynqMP[11]

6.1.2 SD

This does not work, because SD controller is not selected on PS.

6.1.3 JTAG

Load configuration and Application with SDK Debugger into device, see:

- SDK Projects[12]
- SDK Projects[13]

6.2 Usage

QSPI Boot:

1. Prepare HW like described on section Programming(see page 13)
2. Connect UART USB (most cases same as JTAG)
3. Select QSPI Card as Boot Mode
   Note: See TRM of the Carrier, which is used.
4. Power On PCB
   Note: 1. ZynqMP Boot ROM loads PMU Firmware and FSBL from QSPI into OCM, 2. FSBL loads Application into DDR

Debugging:

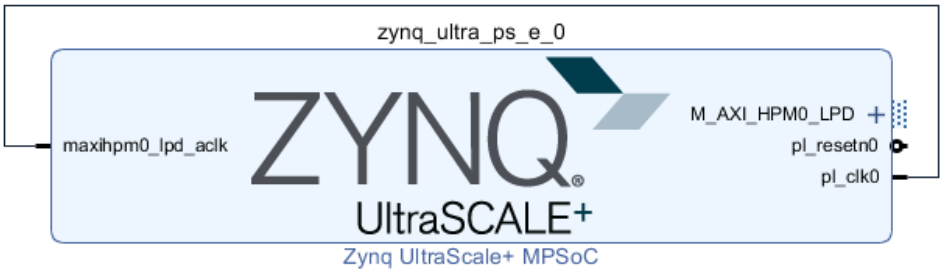
10 https://wiki.trenz-electronic.de/pages/viewpage.action?pageId=14746264#Vivado/SDK/SDSoC-XilinxSoftwareProgrammingandDebugging
11 https://wiki.trenz-electronic.de/display/PD/SDK+Projects#SDKProjects-Xilinx"HelloWorld"onZynqMP
12 https://wiki.trenz-electronic.de/display/PD/SDK+Projects
13 https://wiki.trenz-electronic.de/display/PD/SDK+Projects#SDKProjects-DebugSoftwareApplication

- SDK Projects[14]
- SDK Projects[15]

14 https://wiki.trenz-electronic.de/display/PD/SDK+Projects
15 https://wiki.trenz-electronic.de/display/PD/SDK+Projects#SDKProjects-DebugSoftwareApplication

7 System Design - Vivado

7.1 Block Design



7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
UART0	MIO, please select other one, if you have connected uart to second controller or other MIO
SWDT0..1	
TTC0..3	

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen.xdc

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN PULLNONE [current_design]
```

7.2.2 Design specific constrain

Not needed.

8 Software Design - SDK/HSI

For SDK project creation, follow instructions from:

SDK Projects[16]

8.1 Application

Template location: ./sw_lib/sw_apps/

8.1.1 zynqmp_fsbl

Xilinx default FSBL

8.1.2 zynqmp_fsbl_flash

TE modified 2017.4 FSBL

Changes:

- Set FSBL Boot Mode to JTAG
- Disable Memory initialisation

8.1.3 hello_te0807

Hello TE0807 is a Xilinx Hello World example as endless loop instead of one console output.

16 https://wiki.trenz-electronic.de/display/PD/SDK+Projects

9 Additional Software

No additional software is needed.

10 Appx. A: Change History and Legal Notices

10.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2019-02-07	v.9(see page 6) Unbekanntes Makro: 'metadata'	John Hartfiel[17]	• new assembly variant
04.09.2018	v.7	John Hartfiel	• Release 2018.2
2018-02-08	v.5	John Hartfiel	• Release 2017.4
2017-11-14	v.3	John Hartfiel	• Release 2017.2
	All	John Hartfiel[18]	

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10.3 Data privacy

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17 https://wiki.trenz-electronic.de/display/~j.hartfiel
18 https://wiki.trenz-electronic.de/display/~j.hartfiel

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WEEE

19 http://guidance.echa.europa.eu/
20 https://echa.europa.eu/candidate-list-table
21 http://www.echa.europa.eu/

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2018-09-18