

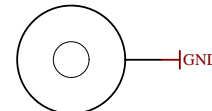
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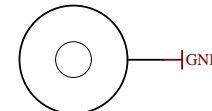
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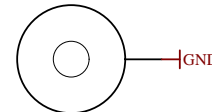
U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_DDR4-TERM DDR4-TERM.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	U_POWER_3 POWER_3.SchDoc
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	
U_B_GT_2 B_GT_2.SchDoc	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	



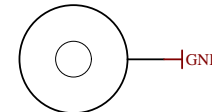
Mount.Hole 3.2mm für Unterlegscheibe



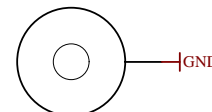
Mount.Hole 3.2mm für Unterlegscheibe



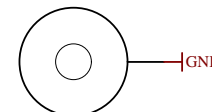
Mount.Hole 3.2mm für Unterlegscheibe



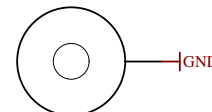
Mount.Hole 3.2mm für Unterlegscheibe



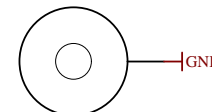
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe

FIDU-DOT - small FIDU-DOT - small



PM1 FIDU-DOT - small PM2 FIDU-DOT - small



PM3 FIDU-DOT - small PM4 FIDU-DOT - small



PM5 PM6

LOGO1

TE Logo PRINT Layer

LOGO PRINT

Serial

Serial

Serialnumber 6,3 x 6.3mm



Title: TE0808		
A4	Number: TE0808 ES2	Rev. 03
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Filename: TE0808.SchDoc		

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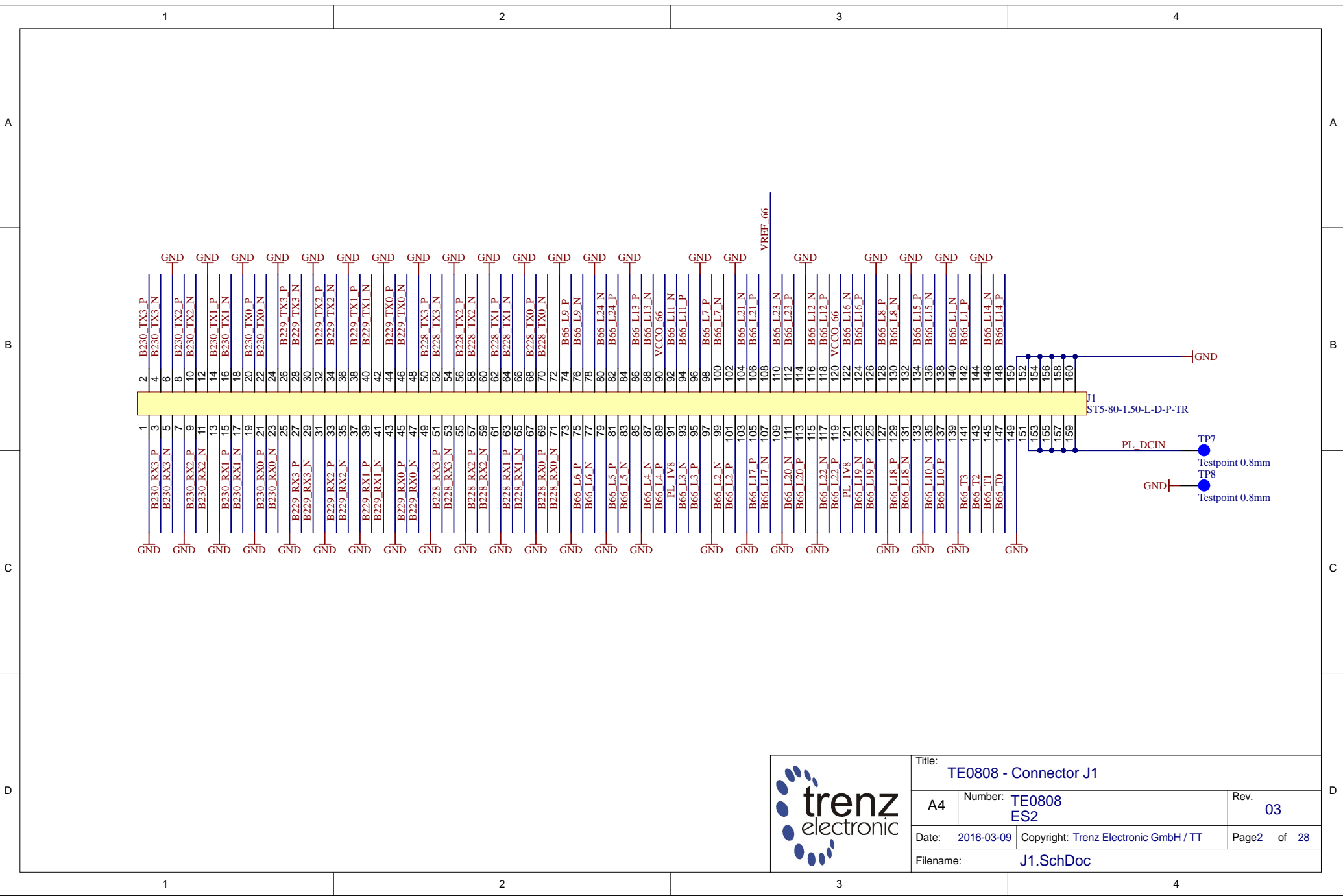
B

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Title: TE0808 - Connector J1		
A4	Number: TE0808 ES2	Rev. 03
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page2 of 28
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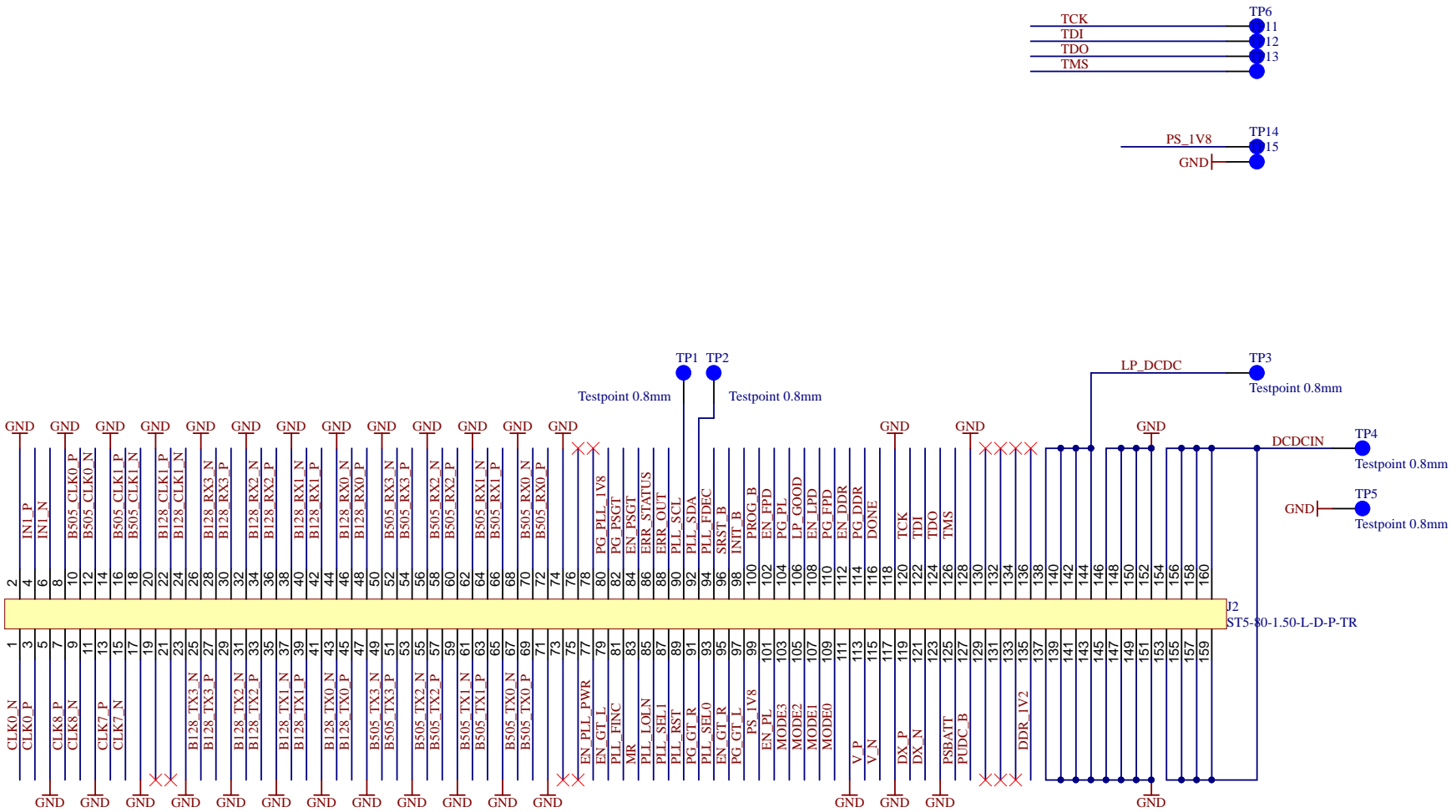
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Title: TE0808 - Connector J2		
A4	Number: TE0808 ES2	Rev. 03
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page3 of 28
Filename: J2.SchDoc		

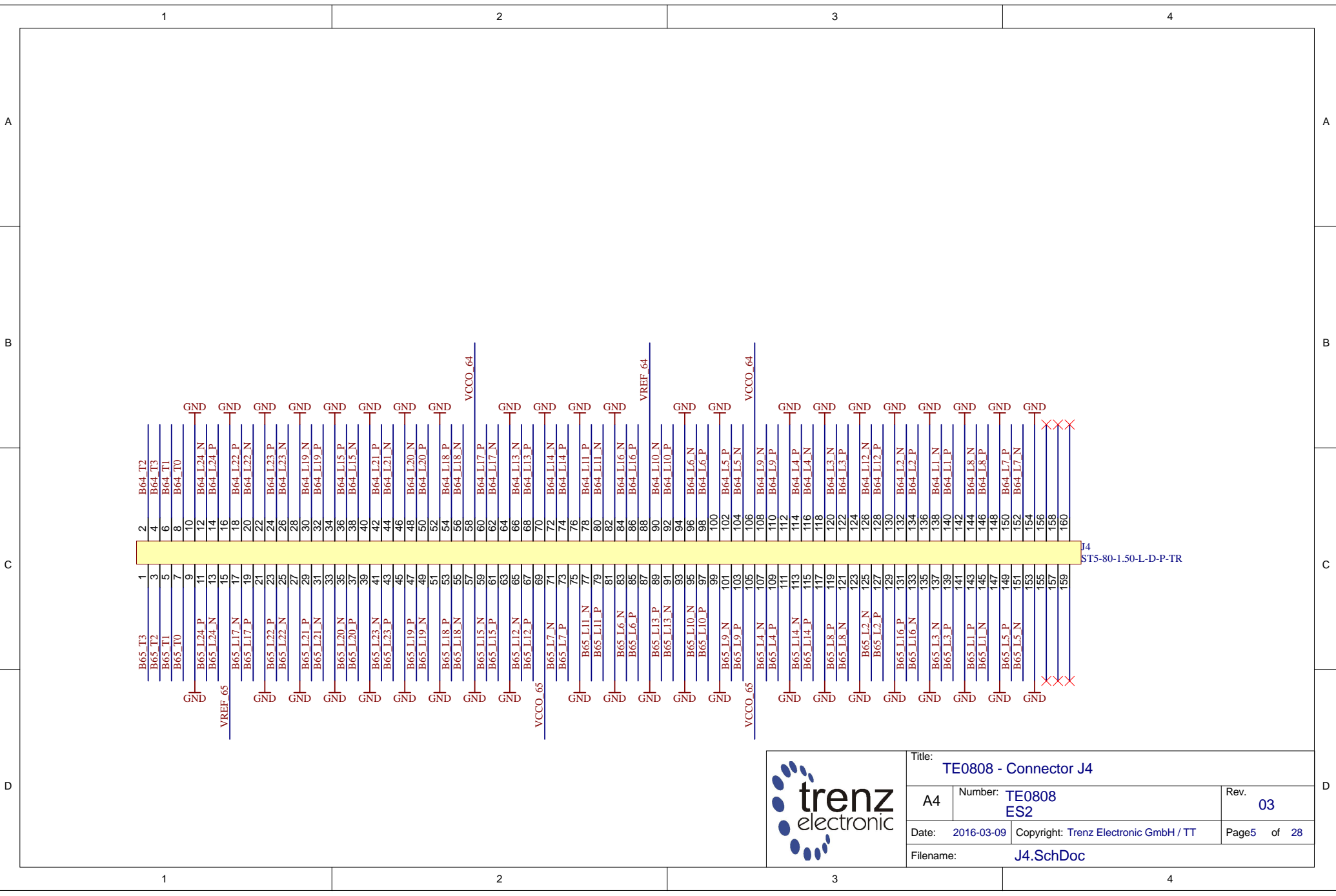
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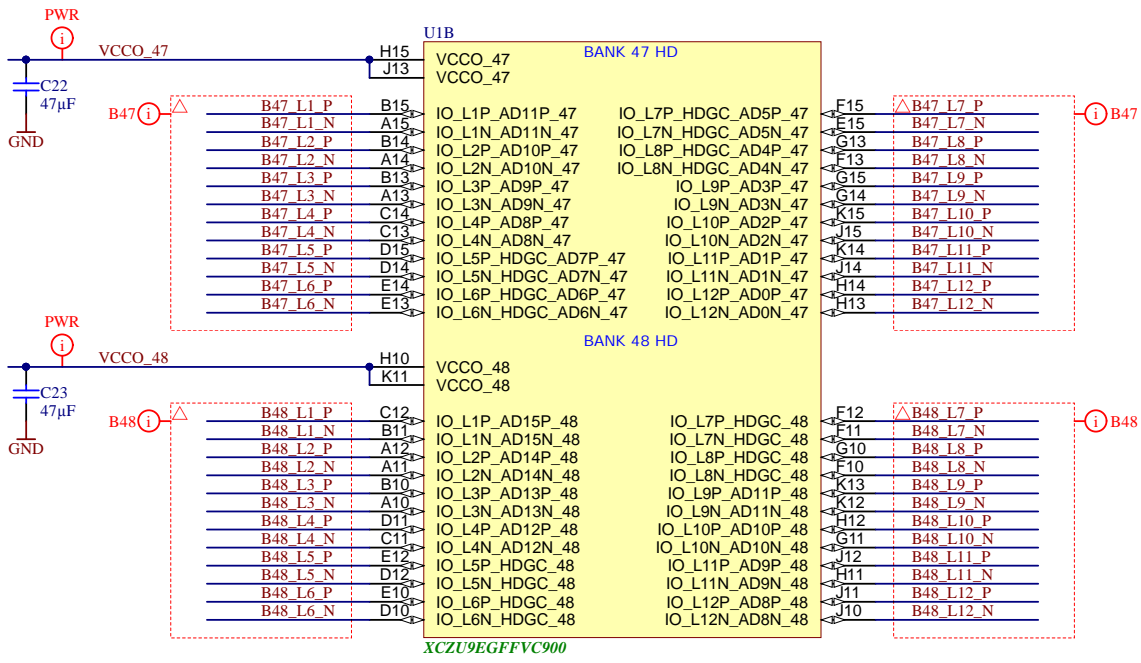
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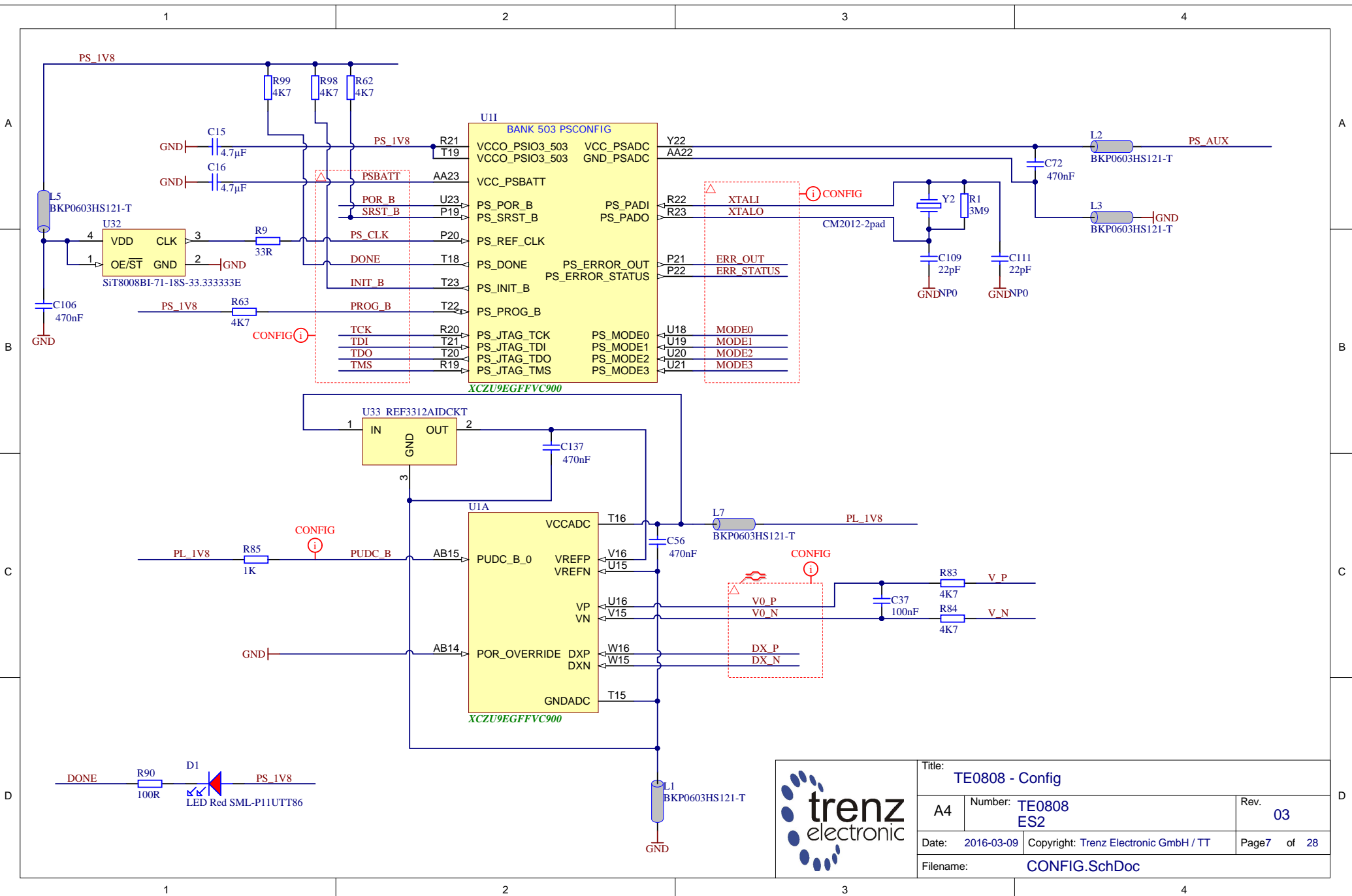



J4  
ST5-80-1.50-L-D-P-TR

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	Date: <b>2016-03-09</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>
	Rev. <b>03</b>	
Filename: <b>J4.SchDoc</b>		Page5 of 28



	Title: TE0808 - B47HD and B48HD		
	A4	Number: TE0808 ES2	Rev. 03
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			Title: TE0808 - Config	
			A4	Number: TE0808 ES2
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Filename: CONFIG.SchDoc				

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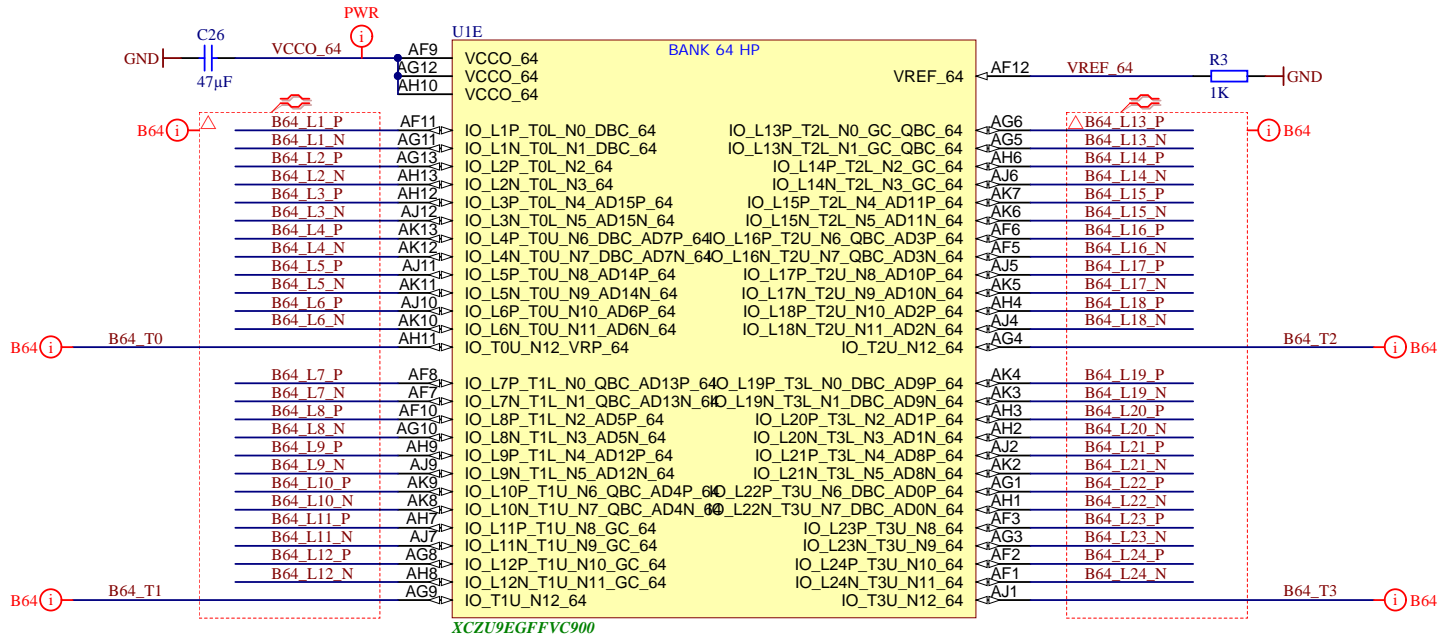

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Title: TE0808 - B64		
A4	Number: TE0808 ES2	Rev. 03
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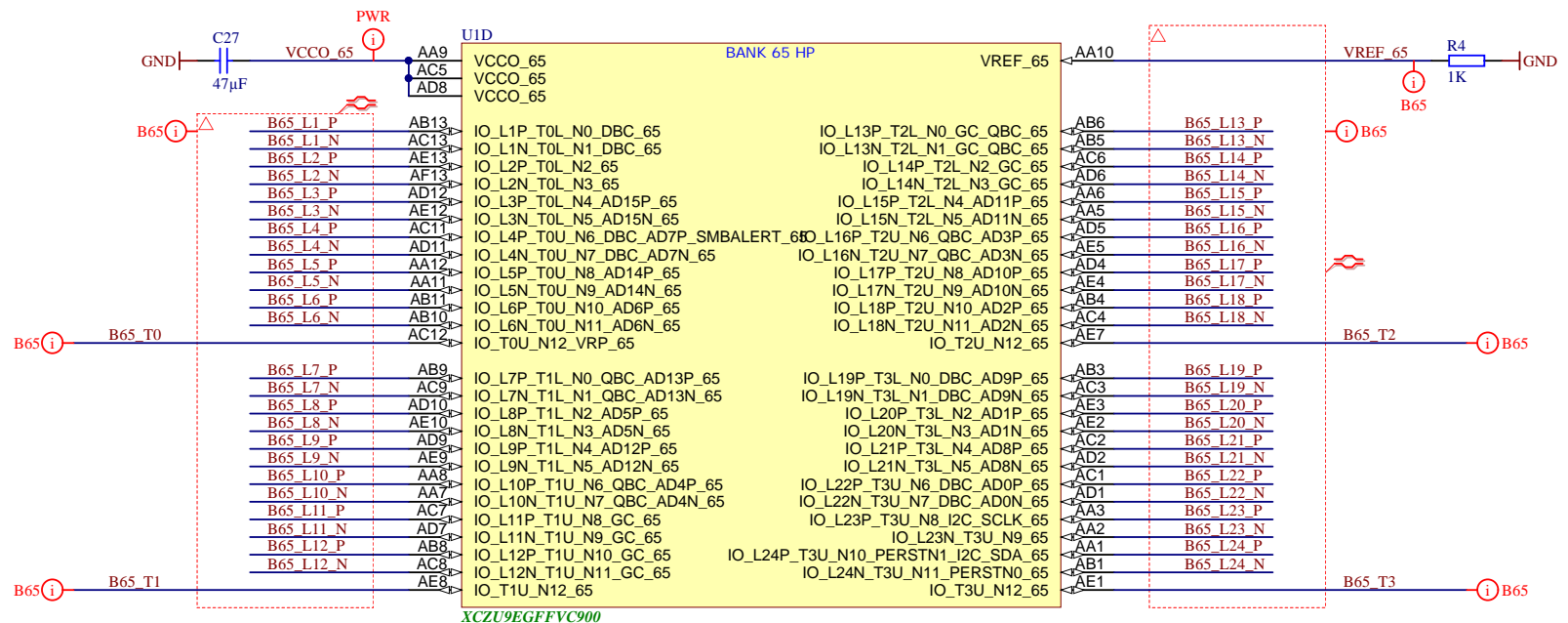
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XCZU9EGFFVC900

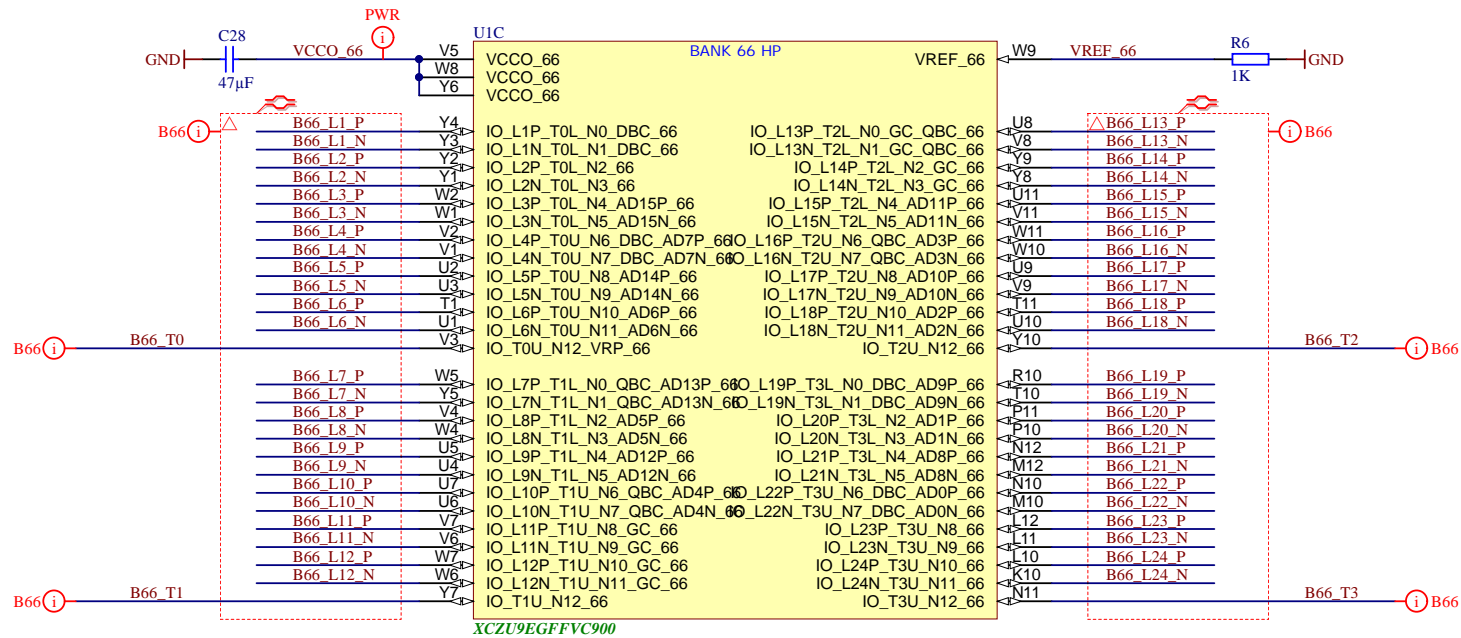
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	A4	Number: TE0808 ES2	Rev. 03
	Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page9 of 28
	Filename: B65.SchDoc		

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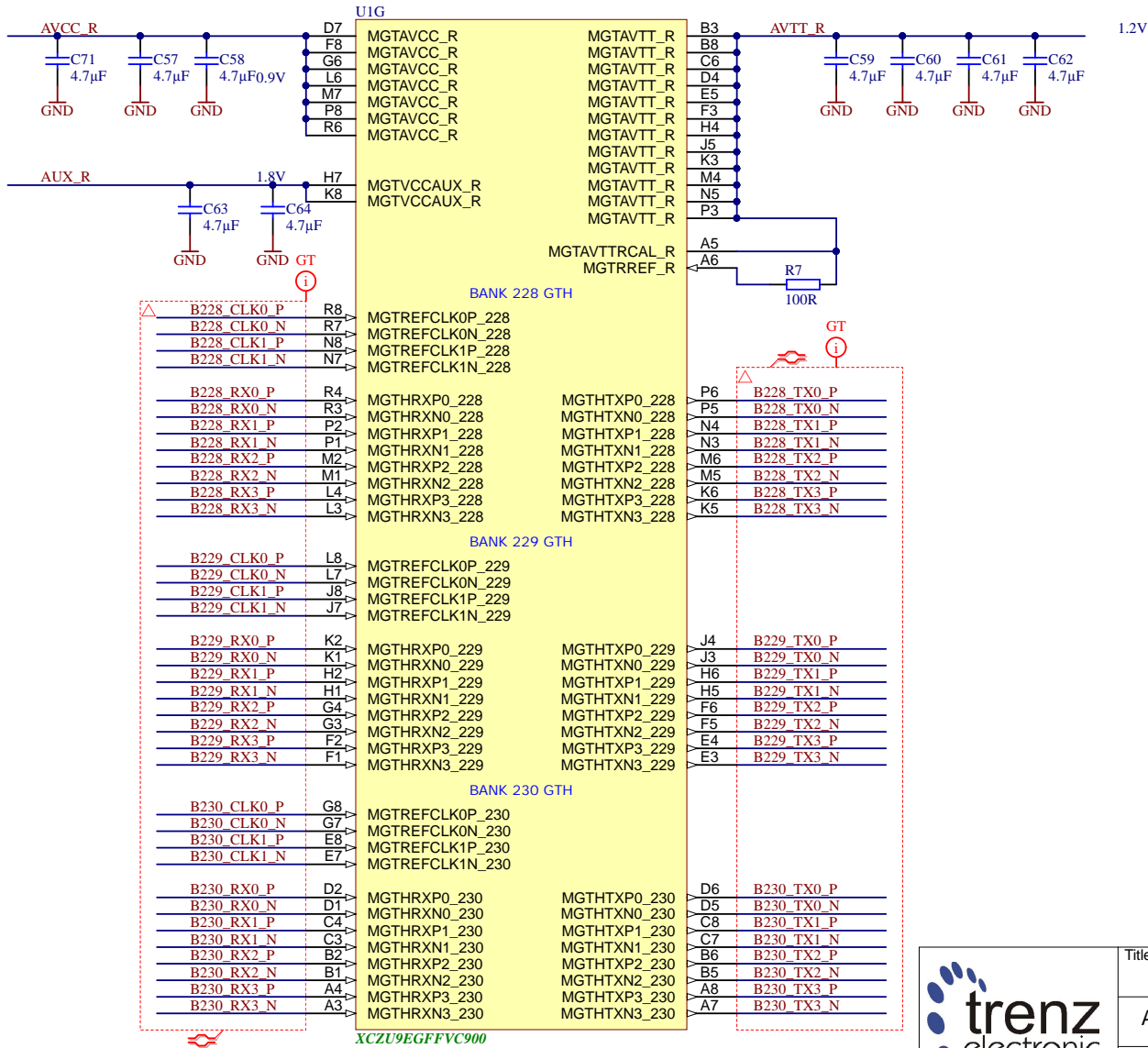
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Title: TE0808 - B66		
A4	Number: TE0808 ES2	Rev. 03
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Title: TE0808 - B228GTH_B229GTH_B230GTH		
A4	Number: TE0808 ES2	Rev. 03
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Filename: B_GT.SchDoc		

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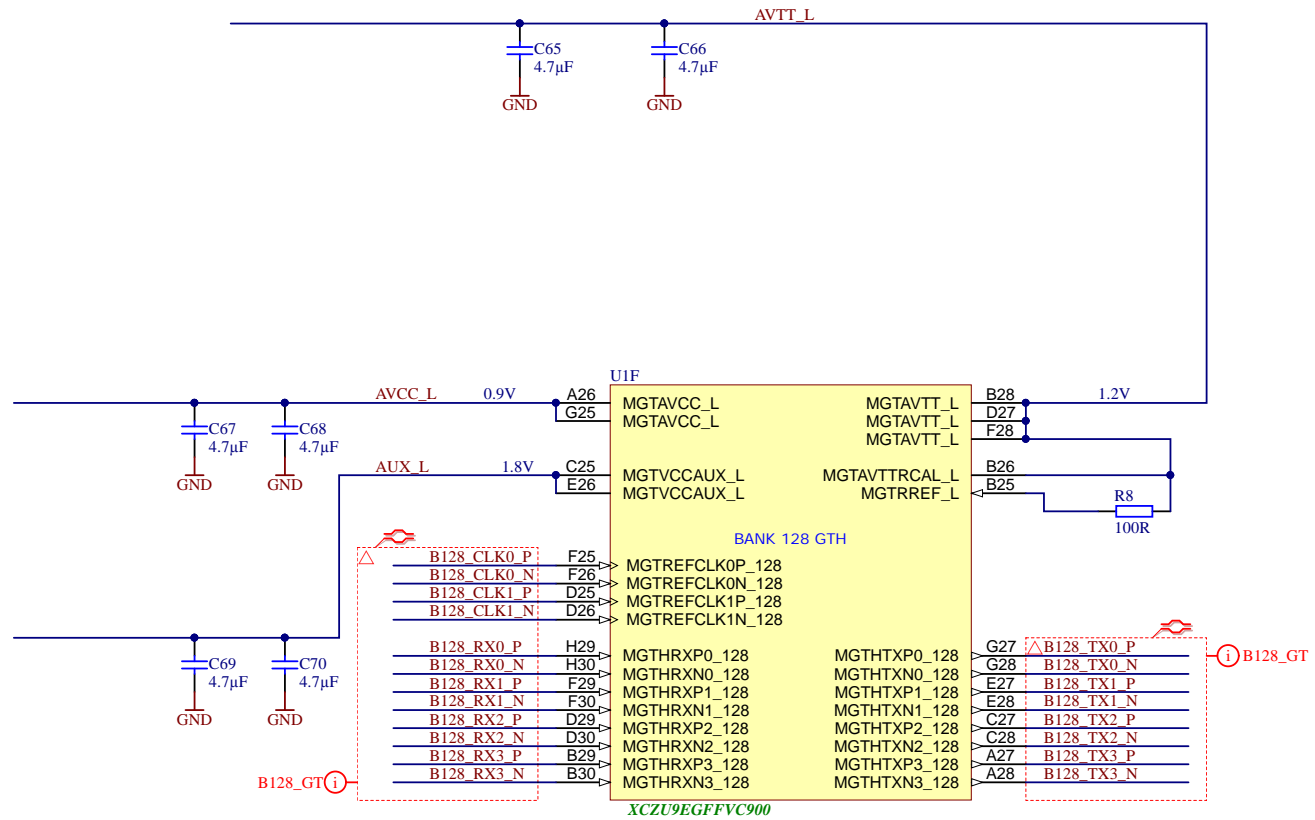
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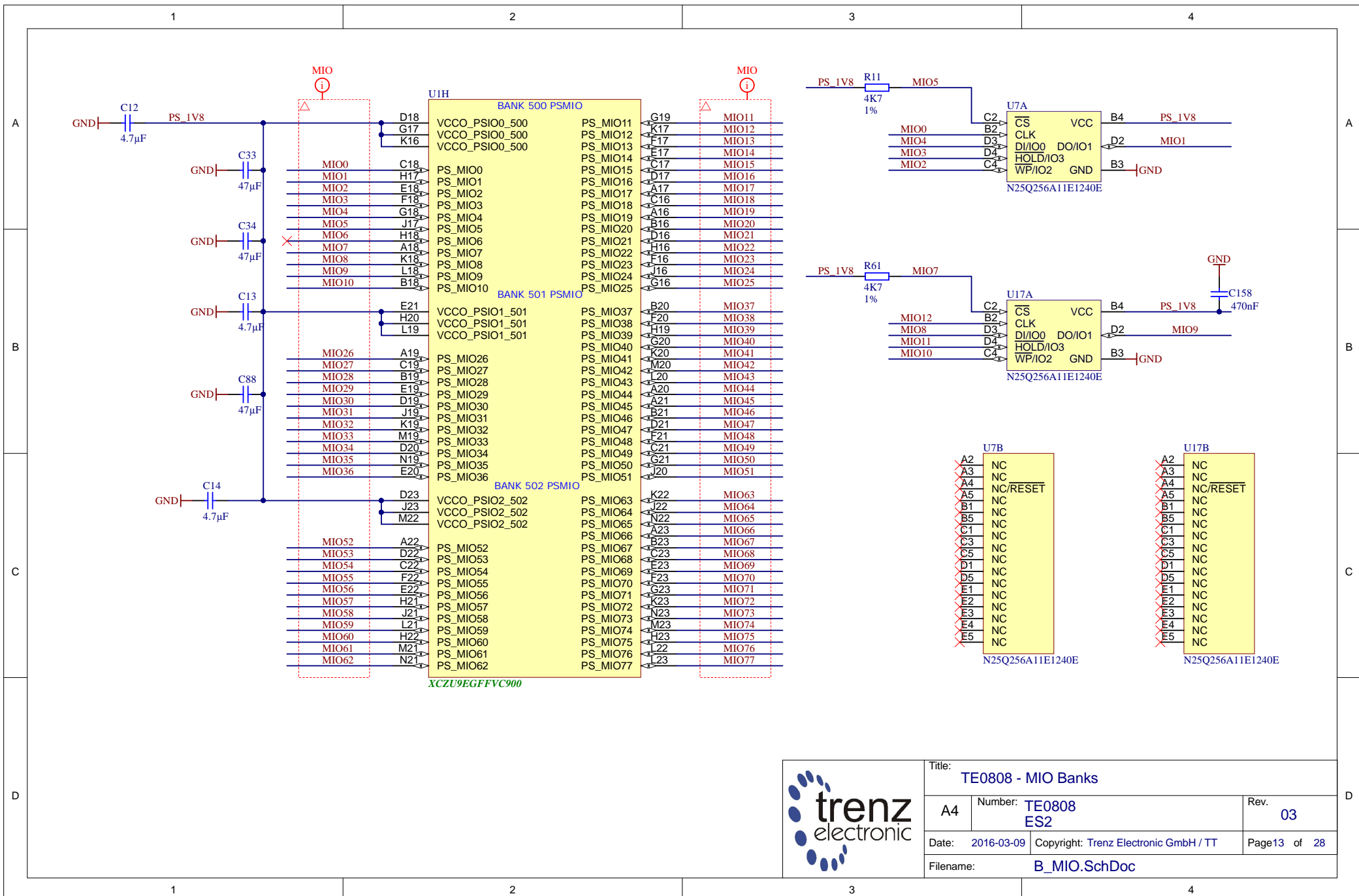
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A4	Number: TE0808 ES2	Rev. 03
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 12 of 28
Filename: B_GT_2.SchDoc		

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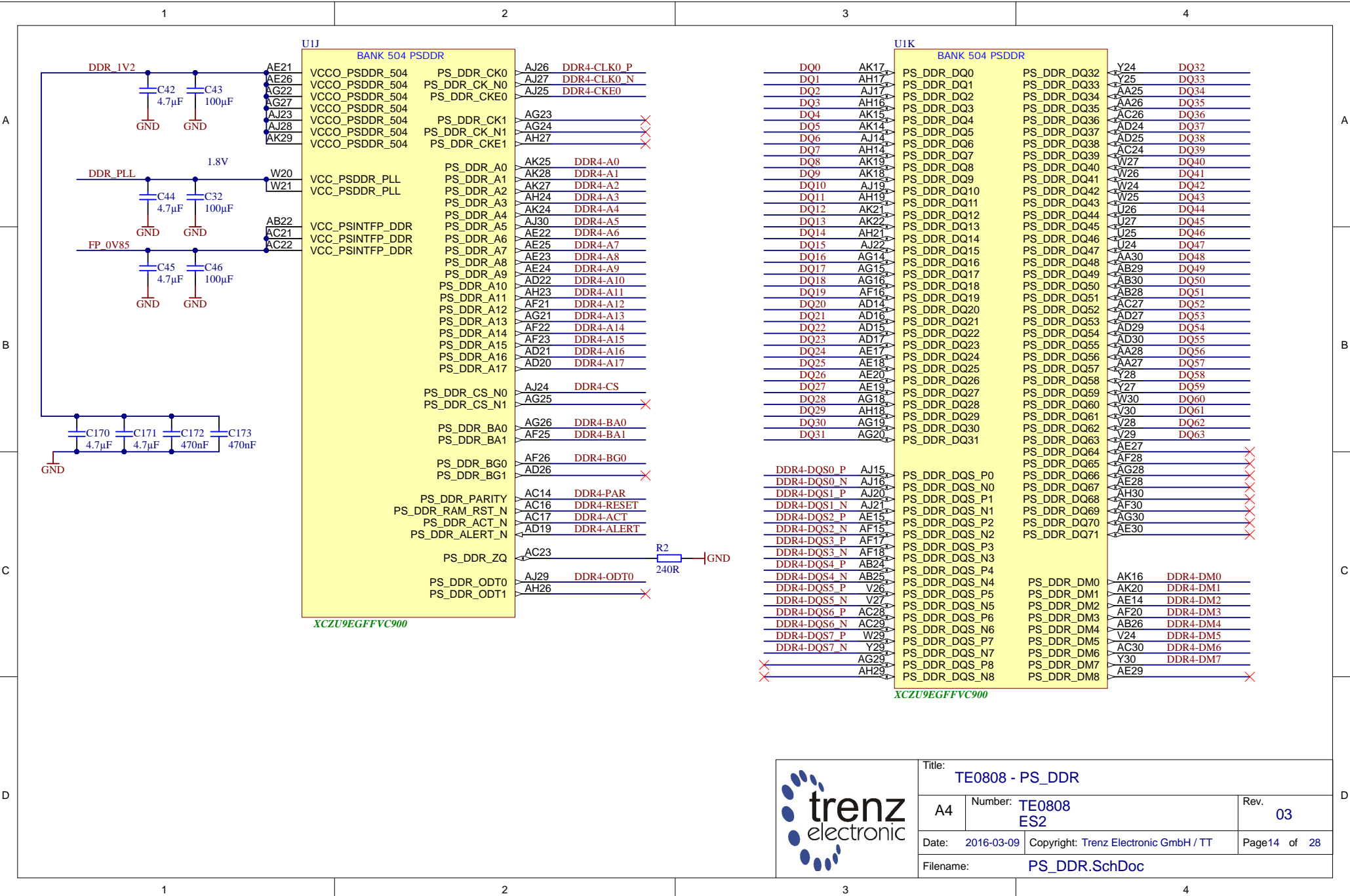
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	Title: <b>TE0808 - MIO Banks</b>		
	A4	Number: <b>TE0808 ES2</b>	Rev. <b>03</b>
	Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page13 of 28
	Filename: <b>B_MIO.SchDoc</b>		



**UIJ**  
**BANK 504 PSDDR**

VCCO_PSDDR_504	PS_DDR_CK0	AJ26	DDR4-CLK0_P
VCCO_PSDDR_504	PS_DDR_CK_N0	AJ27	DDR4-CLK0_N
VCCO_PSDDR_504	PS_DDR_CKE0	AJ25	DDR4-CKE0
VCCO_PSDDR_504		AG23	
VCCO_PSDDR_504	PS_DDR_CK1	AG24	
VCCO_PSDDR_504	PS_DDR_CK_N1	AH27	
VCCO_PSDDR_504		AH27	
	PS_DDR_A0	AK25	DDR4-A0
	PS_DDR_A1	AK28	DDR4-A1
	PS_DDR_A2	AK27	DDR4-A2
	PS_DDR_A3	AH24	DDR4-A3
	PS_DDR_A4	AK24	DDR4-A4
	PS_DDR_A5	AJ30	DDR4-A5
	PS_DDR_A6	AE22	DDR4-A6
	PS_DDR_A7	AE25	DDR4-A7
	PS_DDR_A8	AE23	DDR4-A8
	PS_DDR_A9	AE24	DDR4-A9
	PS_DDR_A10	AD22	DDR4-A10
	PS_DDR_A11	AH23	DDR4-A11
	PS_DDR_A12	AF21	DDR4-A12
	PS_DDR_A13	AG21	DDR4-A13
	PS_DDR_A14	AF22	DDR4-A14
	PS_DDR_A15	AF23	DDR4-A15
	PS_DDR_A16	AD21	DDR4-A16
	PS_DDR_A17	AD20	DDR4-A17
	PS_DDR_CS_N0	AJ24	DDR4-CS
	PS_DDR_CS_N1	AG25	
	PS_DDR_BA0	AG26	DDR4-BA0
	PS_DDR_BA1	AF25	DDR4-BA1
	PS_DDR_BG0	AF26	DDR4-BG0
	PS_DDR_BG1	AD26	
	PS_DDR_PARITY	AC14	DDR4-PAR
	PS_DDR_RAM_RST_N	AC16	DDR4-RESET
	PS_DDR_ACT_N	AC17	DDR4-ACT
	PS_DDR_ALERT_N	AD19	DDR4-ALERT
	PS_DDR_ZQ	AC23	
	PS_DDR_ODT0	AJ29	DDR4-ODT0
	PS_DDR_ODT1	AH26	

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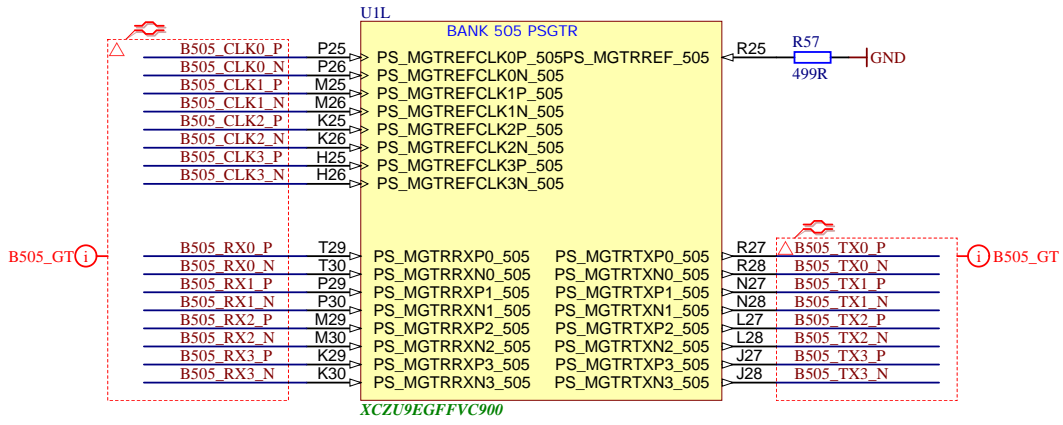
**UIK**  
**BANK 504 PSDDR**


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PS_DDR_DQ1	AH17	PS_DDR_DQ1	PS_DDR_DQ33	Y25	DQ33
PS_DDR_DQ2	AJ17	PS_DDR_DQ2	PS_DDR_DQ34	AA25	DQ34
PS_DDR_DQ3	AH16	PS_DDR_DQ3	PS_DDR_DQ35	AA26	DQ35
PS_DDR_DQ4	AK15	PS_DDR_DQ4	PS_DDR_DQ36	AC26	DQ36
PS_DDR_DQ5	AK14	PS_DDR_DQ5	PS_DDR_DQ37	AD24	DQ37
PS_DDR_DQ6	AJ14	PS_DDR_DQ6	PS_DDR_DQ38	AD25	DQ38
PS_DDR_DQ7	AH14	PS_DDR_DQ7	PS_DDR_DQ39	AC24	DQ39
PS_DDR_DQ8	AK19	PS_DDR_DQ8	PS_DDR_DQ40	W27	DQ40
PS_DDR_DQ9	AK18	PS_DDR_DQ9	PS_DDR_DQ41	W26	DQ41
PS_DDR_DQ10	AJ19	PS_DDR_DQ10	PS_DDR_DQ42	W24	DQ42
PS_DDR_DQ11	AH19	PS_DDR_DQ11	PS_DDR_DQ43	W25	DQ43
PS_DDR_DQ12	AH19	PS_DDR_DQ12	PS_DDR_DQ44	U26	DQ44
PS_DDR_DQ13	AK22	PS_DDR_DQ13	PS_DDR_DQ45	U27	DQ45
PS_DDR_DQ14	AH21	PS_DDR_DQ14	PS_DDR_DQ46	U25	DQ46
PS_DDR_DQ15	AJ22	PS_DDR_DQ15	PS_DDR_DQ47	U24	DQ47
PS_DDR_DQ16	AG14	PS_DDR_DQ16	PS_DDR_DQ48	AA30	DQ48
PS_DDR_DQ17	AG15	PS_DDR_DQ17	PS_DDR_DQ49	AB29	DQ49
PS_DDR_DQ18	AG16	PS_DDR_DQ18	PS_DDR_DQ50	AB30	DQ50
PS_DDR_DQ19	AF16	PS_DDR_DQ19	PS_DDR_DQ51	AB28	DQ51
PS_DDR_DQ20	AD14	PS_DDR_DQ20	PS_DDR_DQ52	AC27	DQ52
PS_DDR_DQ21	AD16	PS_DDR_DQ21	PS_DDR_DQ53	AD27	DQ53
PS_DDR_DQ22	AD15	PS_DDR_DQ22	PS_DDR_DQ54	AD29	DQ54
PS_DDR_DQ23	AD17	PS_DDR_DQ23	PS_DDR_DQ55	AD30	DQ55
PS_DDR_DQ24	AE17	PS_DDR_DQ24	PS_DDR_DQ56	AA28	DQ56
PS_DDR_DQ25	AE18	PS_DDR_DQ25	PS_DDR_DQ57	AA27	DQ57
PS_DDR_DQ26	AE20	PS_DDR_DQ26	PS_DDR_DQ58	Y28	DQ58
PS_DDR_DQ27	AE19	PS_DDR_DQ27	PS_DDR_DQ59	Y27	DQ59
PS_DDR_DQ28	AG18	PS_DDR_DQ28	PS_DDR_DQ60	W30	DQ60
PS_DDR_DQ29	AH18	PS_DDR_DQ29	PS_DDR_DQ61	V30	DQ61
PS_DDR_DQ30	AG19	PS_DDR_DQ30	PS_DDR_DQ62	V28	DQ62
PS_DDR_DQ31	AG20	PS_DDR_DQ31	PS_DDR_DQ63	V29	DQ63
PS_DDR_DQS_P0	AJ15	PS_DDR_DQS_P0	PS_DDR_DQ64	AE27	
PS_DDR_DQS_N0	AJ16	PS_DDR_DQS_N0	PS_DDR_DQ65	AF28	
PS_DDR_DQS_P1	AJ20	PS_DDR_DQS_P1	PS_DDR_DQ66	AG28	
PS_DDR_DQS_N1	AJ21	PS_DDR_DQS_N1	PS_DDR_DQ67	AE28	
PS_DDR_DQS_P2	AE15	PS_DDR_DQS_P2	PS_DDR_DQ68	AH30	
PS_DDR_DQS_N2	AF15	PS_DDR_DQS_N2	PS_DDR_DQ69	AF30	
PS_DDR_DQS_P3	AF17	PS_DDR_DQS_P3	PS_DDR_DQ70	AG30	
PS_DDR_DQS_N3	AF18	PS_DDR_DQS_N3	PS_DDR_DQ71	AE30	
PS_DDR_DQS_P4	AB24	PS_DDR_DQS_P4			
PS_DDR_DQS_N4	AB25	PS_DDR_DQS_N4	PS_DDR_DM0	AK16	DDR4-DM0
PS_DDR_DQS_P5	V26	PS_DDR_DQS_P5	PS_DDR_DM1	AK20	DDR4-DM1
PS_DDR_DQS_N5	V27	PS_DDR_DQS_N5	PS_DDR_DM2	AE14	DDR4-DM2
PS_DDR_DQS_P6	AC28	PS_DDR_DQS_P6	PS_DDR_DM3	AF20	DDR4-DM3
PS_DDR_DQS_N6	AC29	PS_DDR_DQS_N6	PS_DDR_DM4	AB26	DDR4-DM4
PS_DDR_DQS_P7	W29	PS_DDR_DQS_P7	PS_DDR_DM5	V24	DDR4-DM5
PS_DDR_DQS_N7	Y29	PS_DDR_DQS_N7	PS_DDR_DM6	AC30	DDR4-DM6
PS_DDR_DQS_P8	AG29	PS_DDR_DQS_P8	PS_DDR_DM7	Y30	DDR4-DM7
PS_DDR_DQS_N8	AH29	PS_DDR_DQS_N8	PS_DDR_DM8	AE29	

XCZU9EGFFVC900



Title: TE0808 - PS_DDR		
A4	Number: TE0808 ES2	Rev. 03
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	Title: TE0808 - PS_GT		
	A4	Number: TE0808 ES2	Rev. 03
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	Filename: B_PS_GT.SchDoc		

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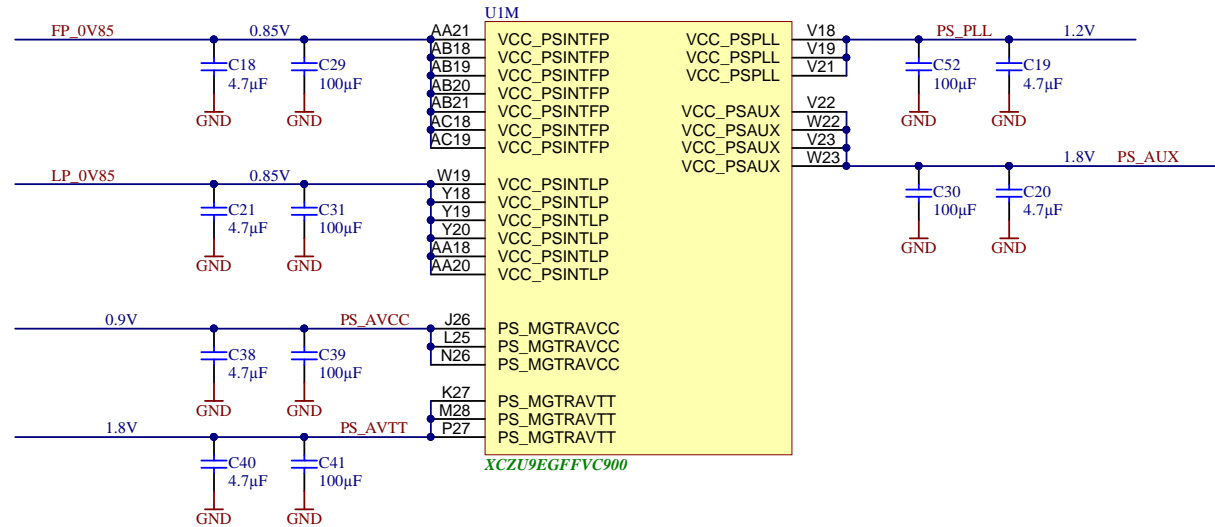
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		A4	Number: TE0808 ES2
Date: 2016-03-09		Copyright: Trenz Electronic GmbH / TT	
Filename: ZU_PS_POWER.SchDoc		Page 16 of 28	

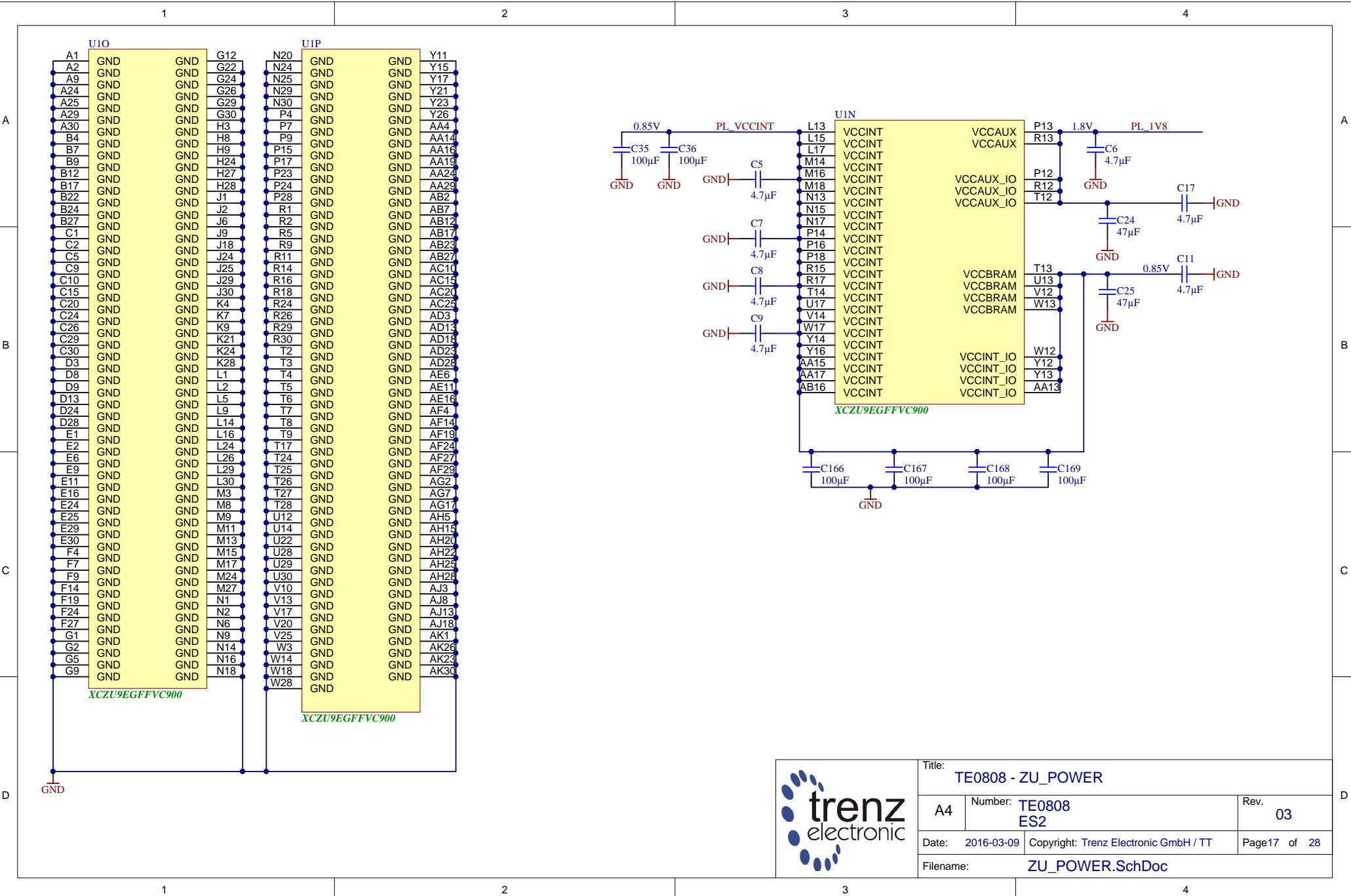
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Title: TE0808 - ZU_POWER		
A4	Number: TE0808 ES2	Rev. 03
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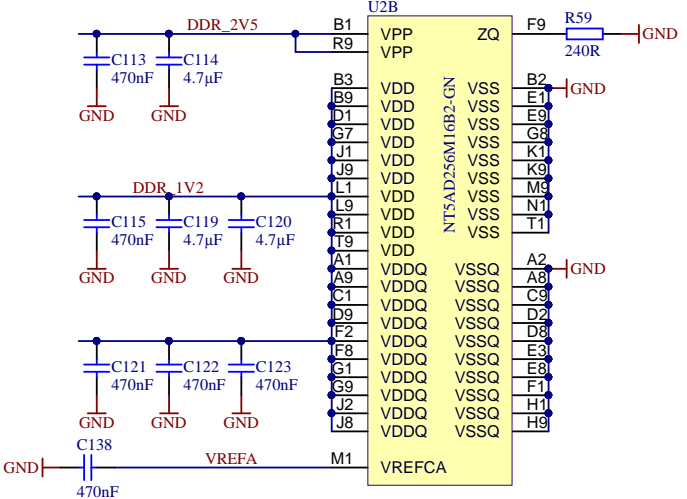
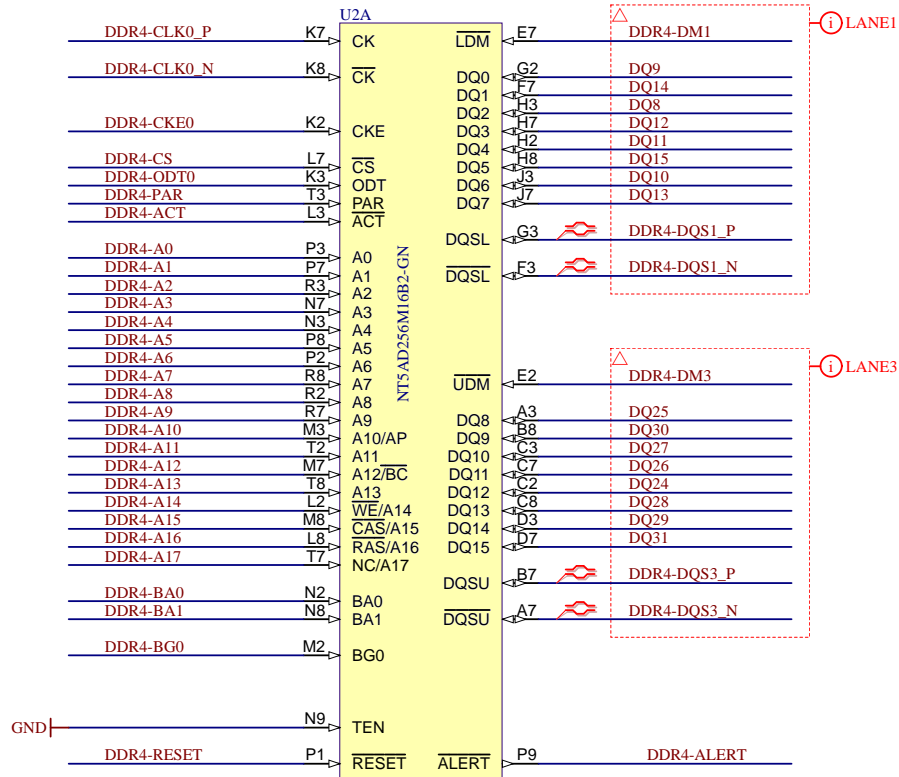
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Title: TE0808 - DDR4_1_RAM		
A4	Number: TE0808 ES2	Rev. 03
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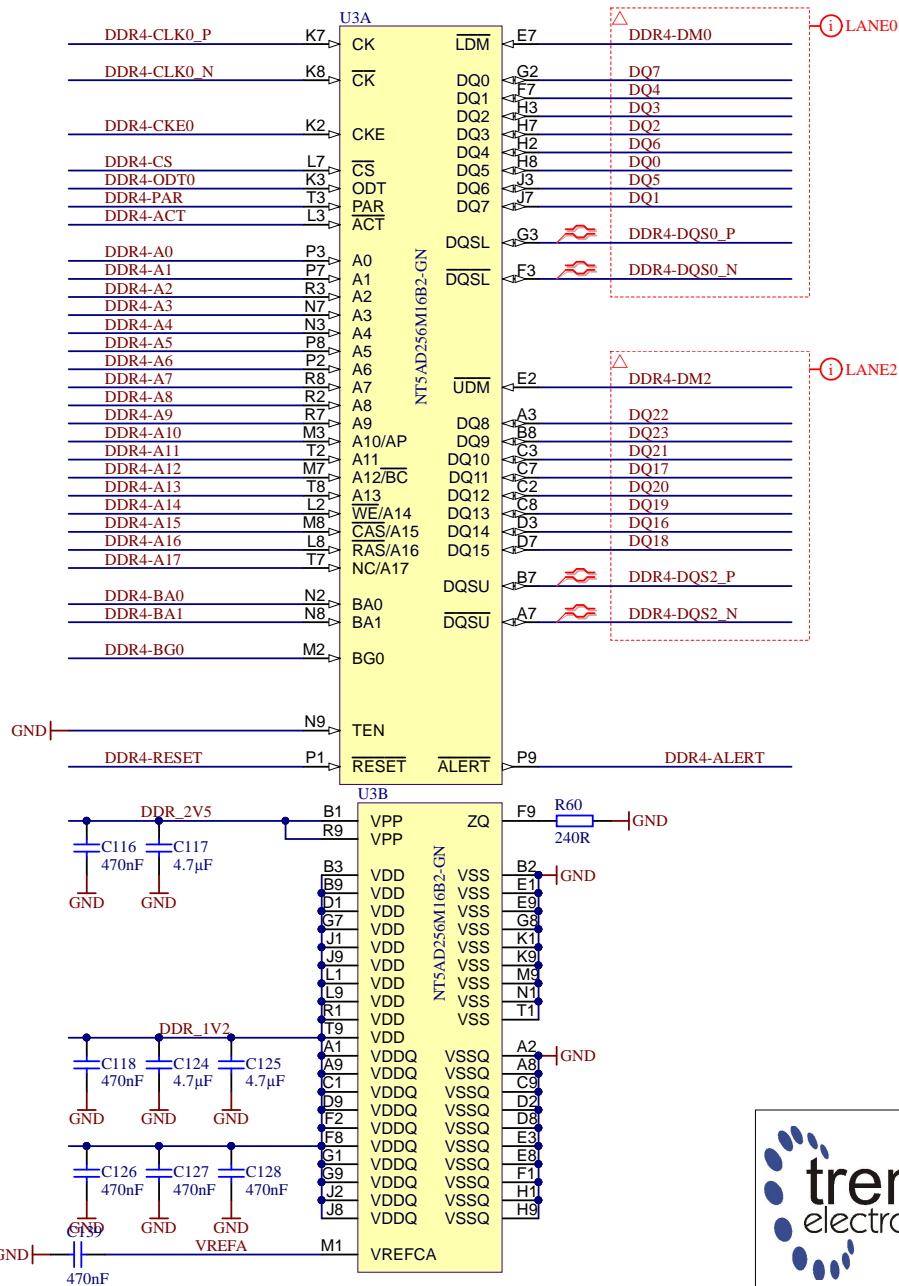

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Title: TE0808 - DDR4_2_RAM		
A4	Number: TE0808 ES2	Rev. 03
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Filename: DDR4-RAM_2.SchDoc		

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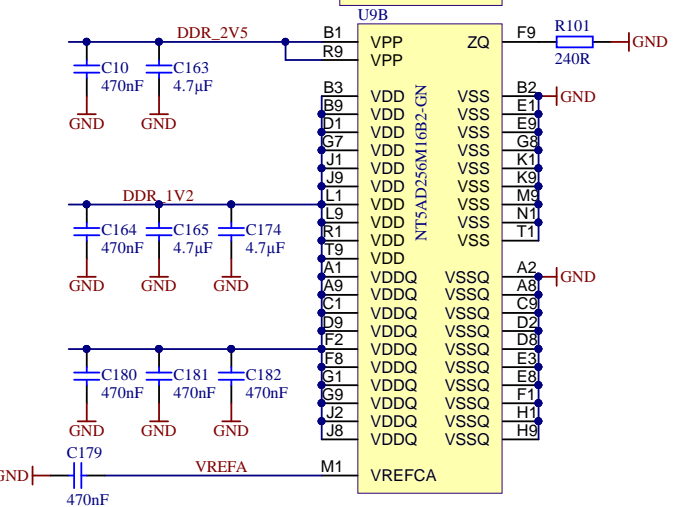
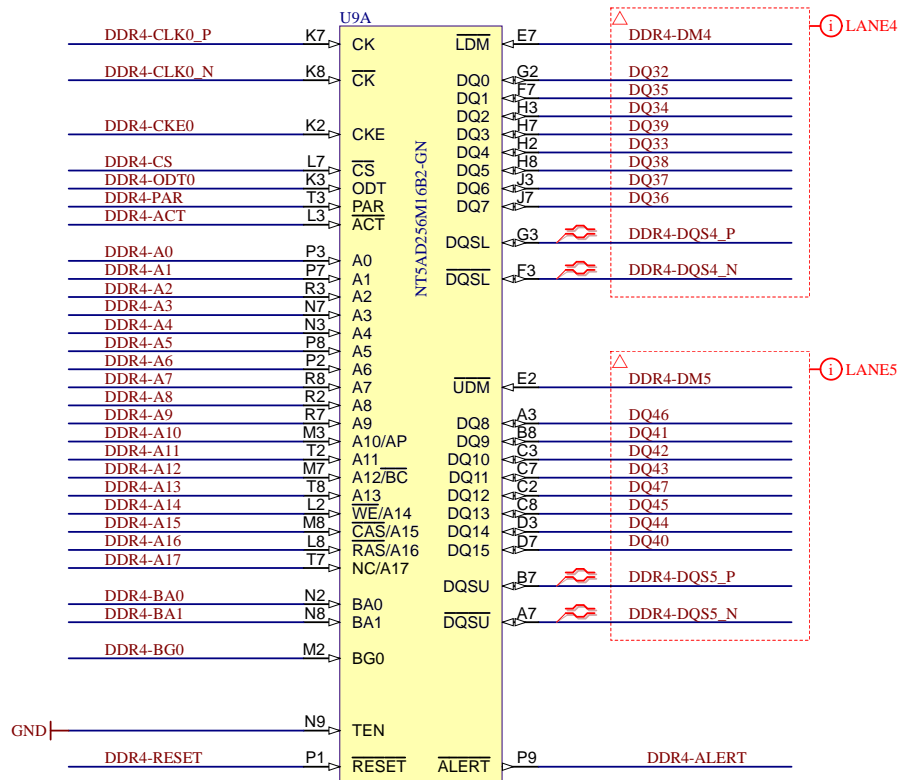

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Title: TE0808 - DDR4_3_RAM		
A4	Number: TE0808 ES2	Rev. 03
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Filename: DDR4-RAM_3.SchDoc		

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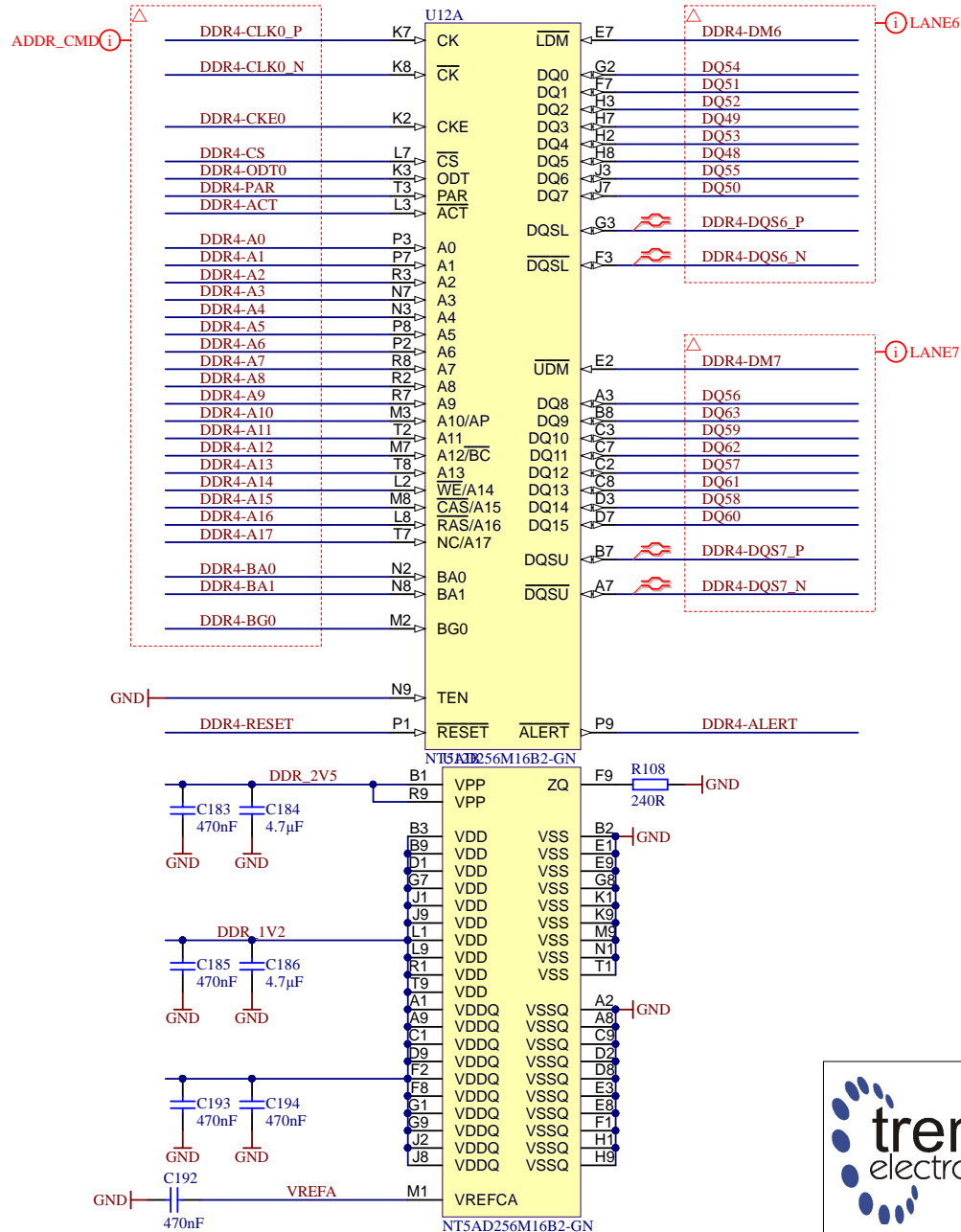
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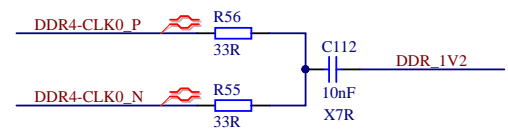
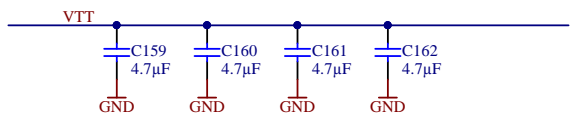
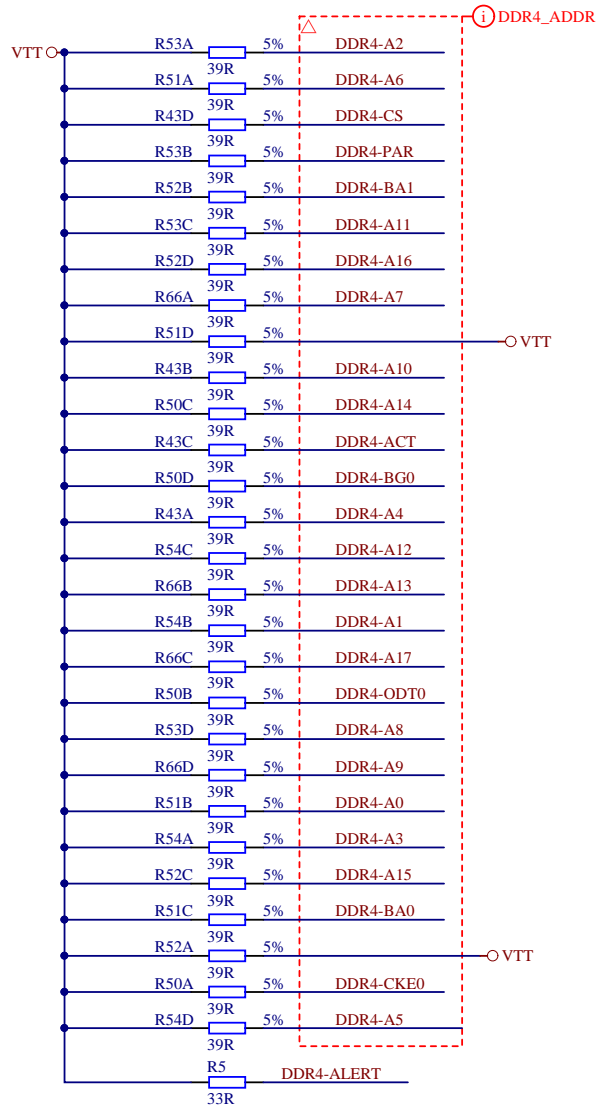
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Filename: DDR4-RAM_4.SchDoc		

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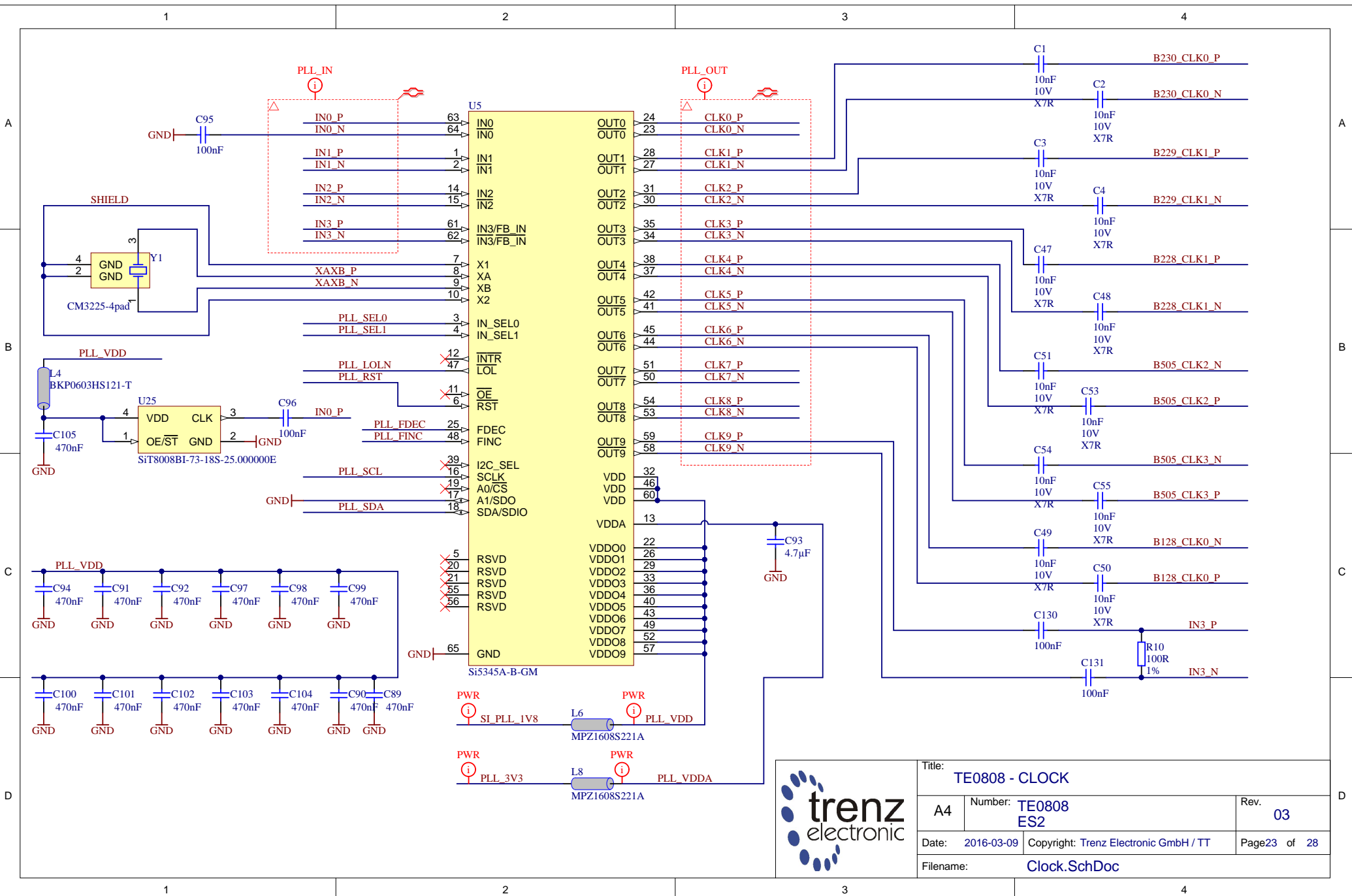
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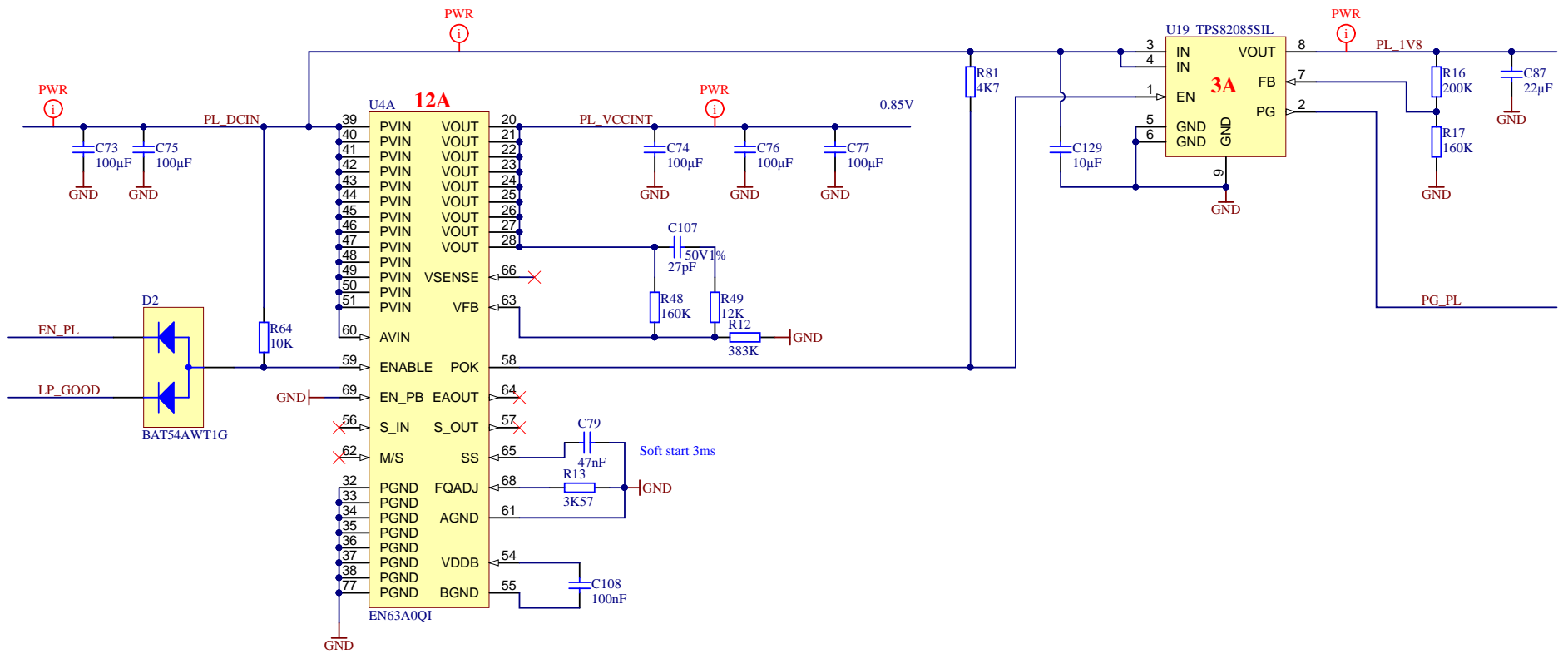
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Title: TE0808 - DDR4_TERM		
A4	Number: TE0808 ES2	Rev. 03
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Filename: DDR4-TERM.SchDoc		



Title: TE0808 - CLOCK		
A4	Number: TE0808 ES2	Rev. 03
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page23 of 28
Filename: Clock.SchDoc		



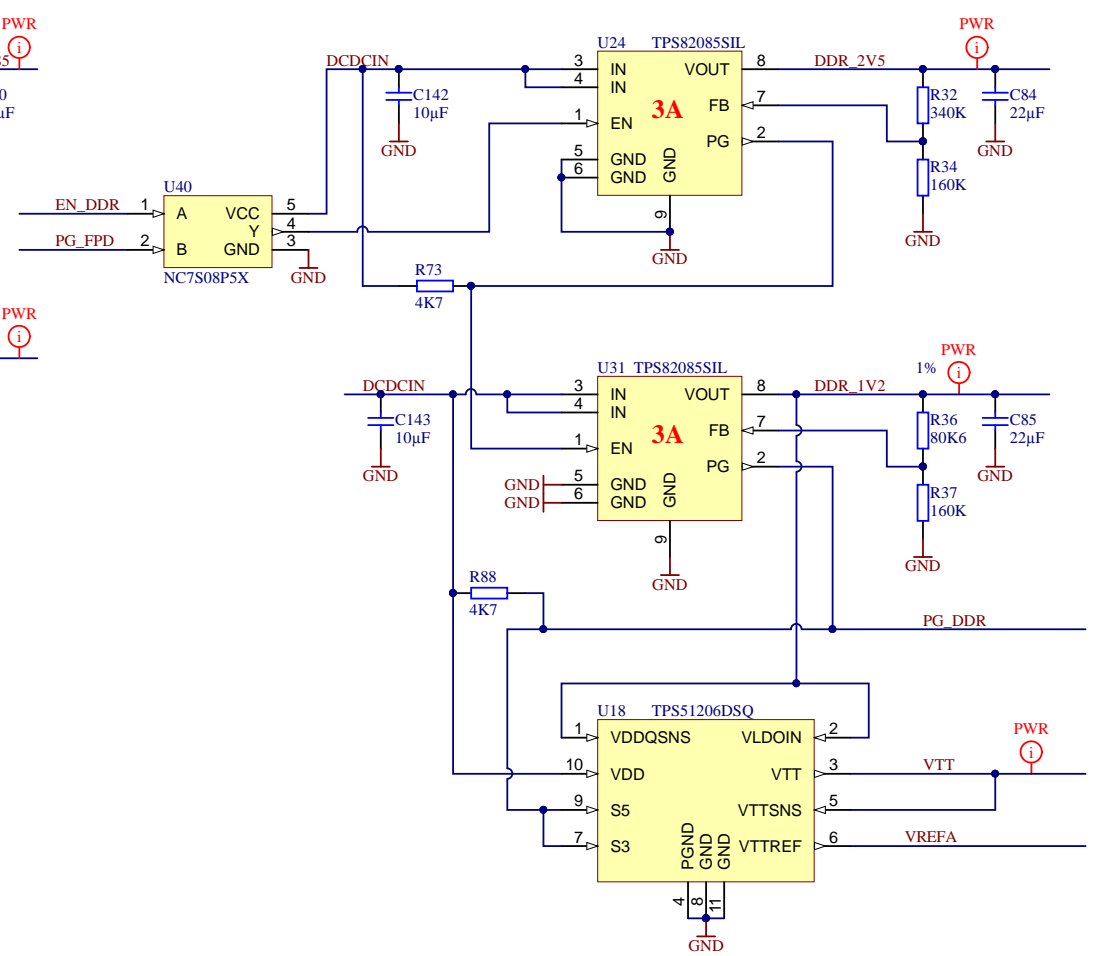
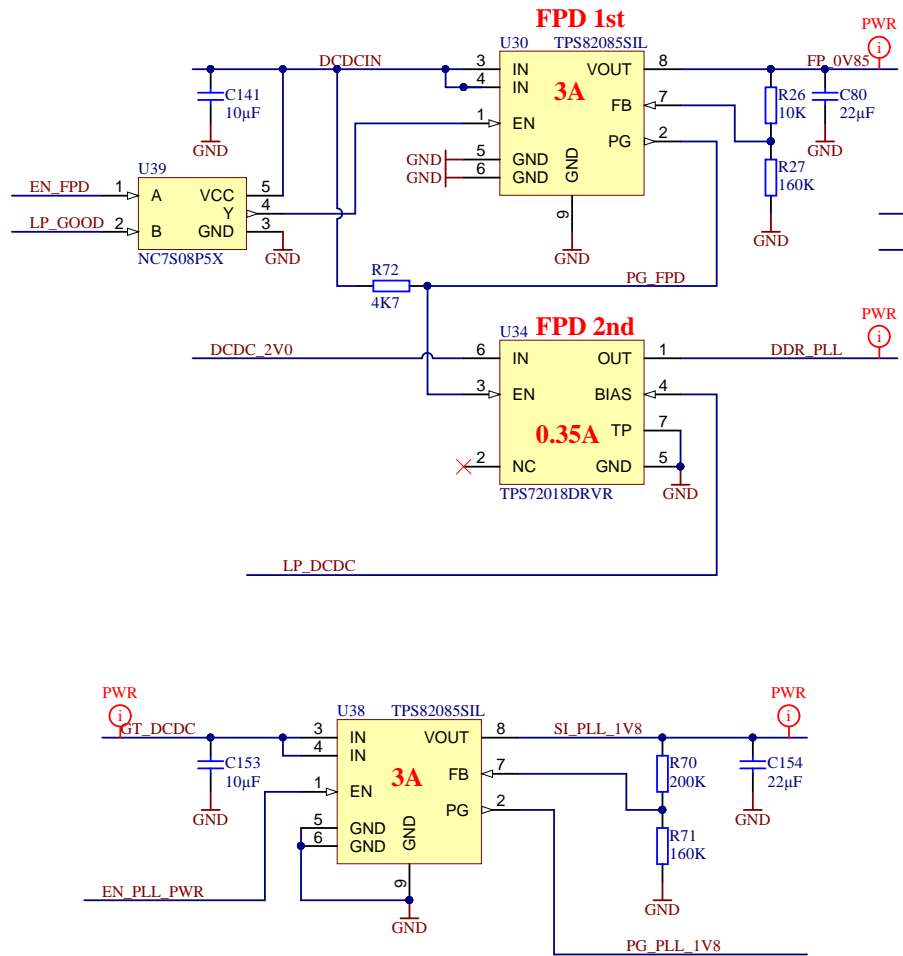
1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC(SW)	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76

EN63A0QI

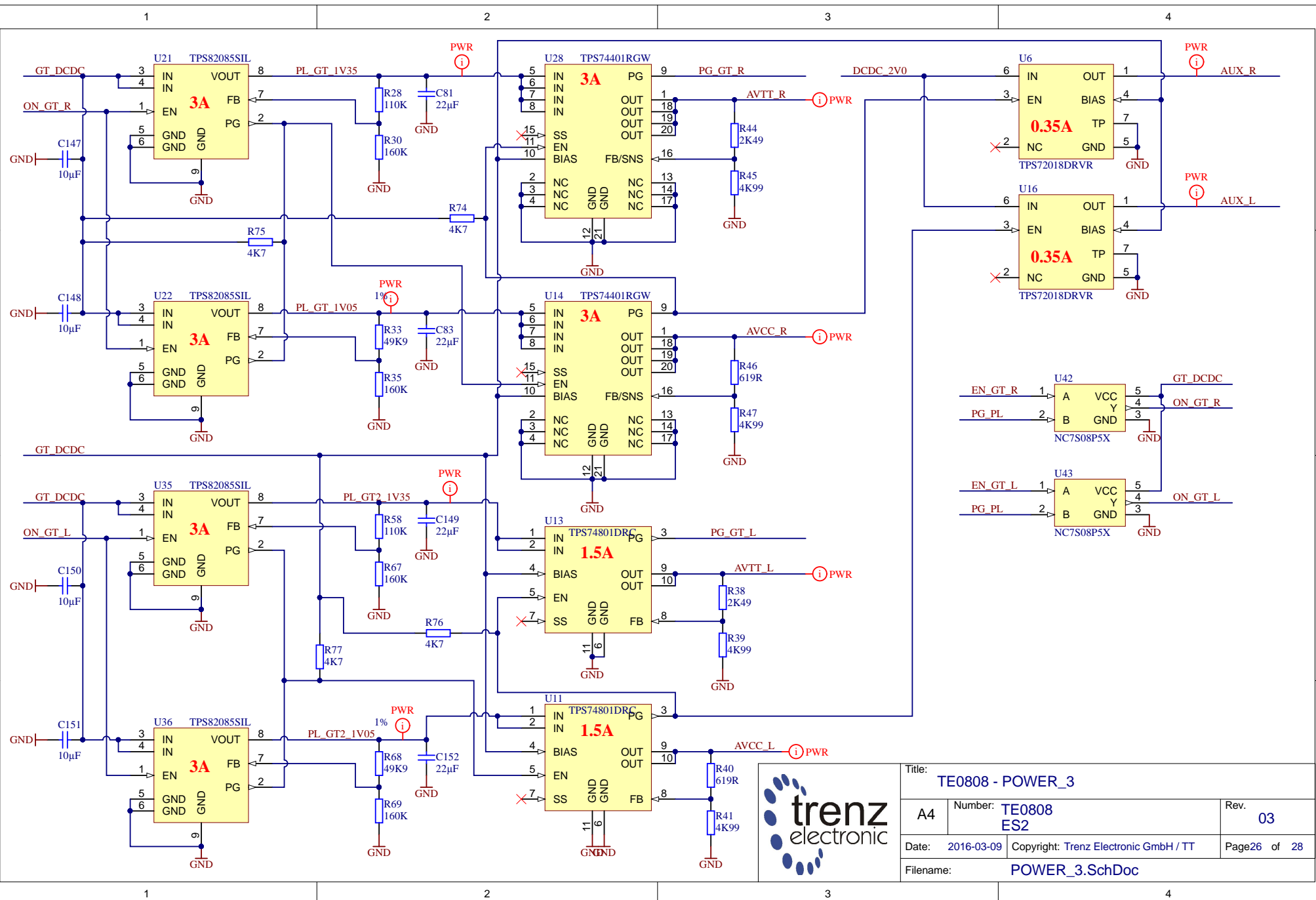


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A4	Number: TE0808 ES2	Rev. 03
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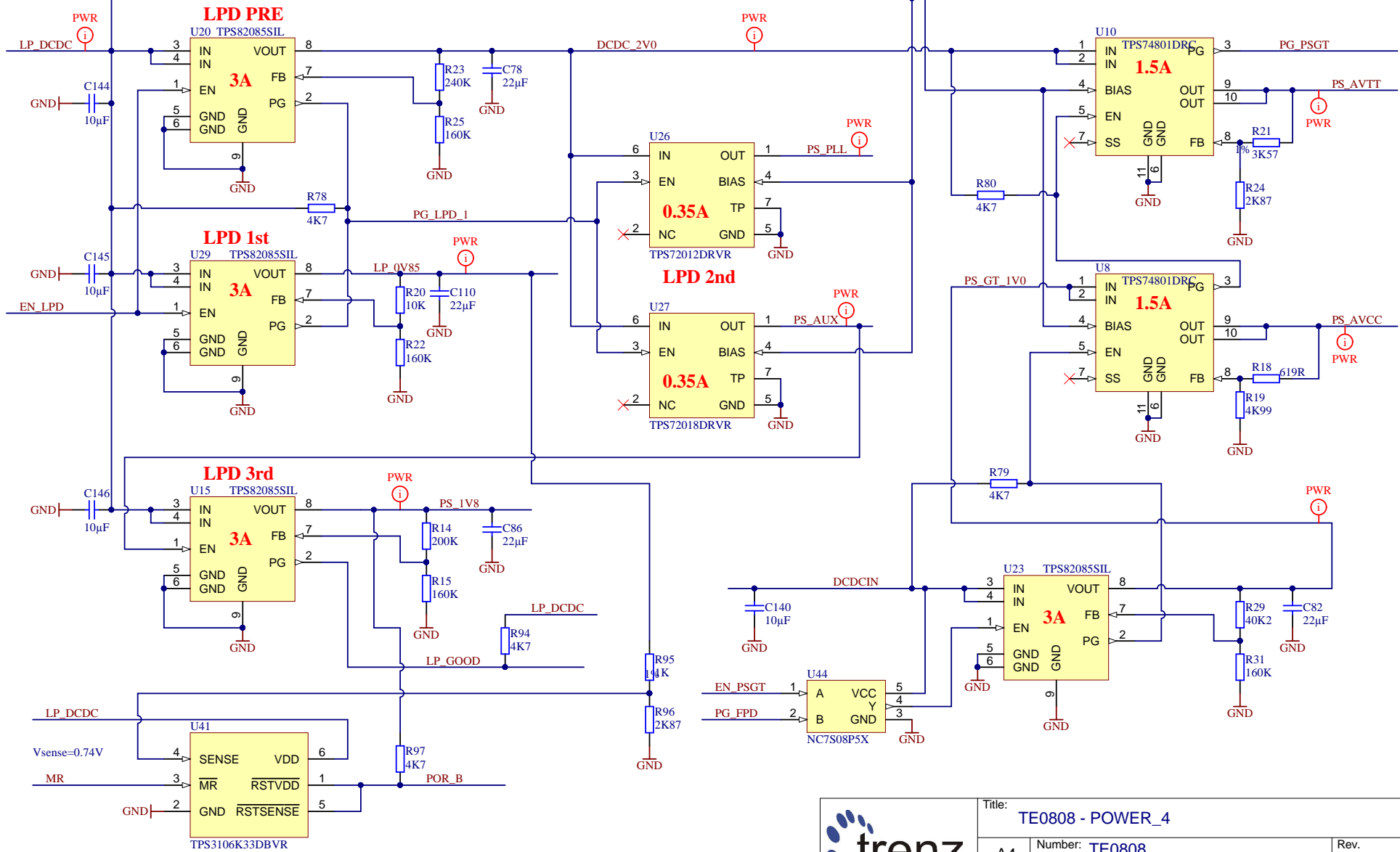





	Title: TE0808 - POWER_2	
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	Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT
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			Title: TE0808 - POWER_4	
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CHANGES REV02 to REV03

- 1) added diode D2, resistor R64
- 2) full update lib
- 3) removed U37 (NC7S08P5X)

A

A

B

B

C

C

D

D



Title: TE0808 - Changes list		
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