



TE0808 TRM

Revision: V1

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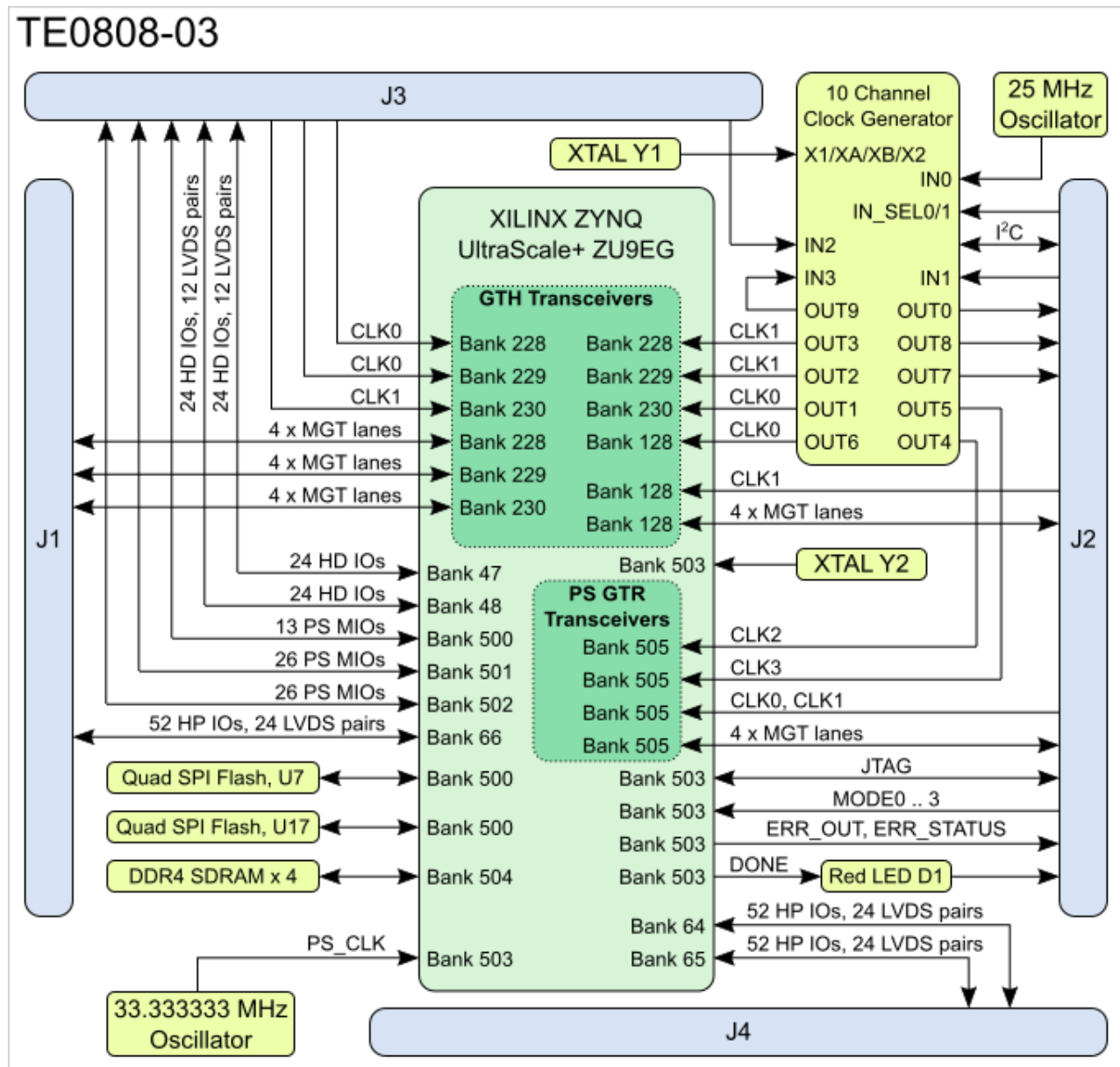
Overview

Refer to "https://shop.trenz-electronic.de/en/Download/?path=Trenz_Electronic/TE0808" for downloadable version of this manual and the rest of available documentation. The Trenz Electronic TE0808 is an industrial-grade MPSoC module integrating a Xilinx Zynq UltraScale+, max. 8 GByte DDR4 SDRAM with 64-Bit width, max. 512 MByte Flash memory for configuration and operation, 20 Gigabit transceivers, and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/O's is provided via rugged high-speed stacking connections.

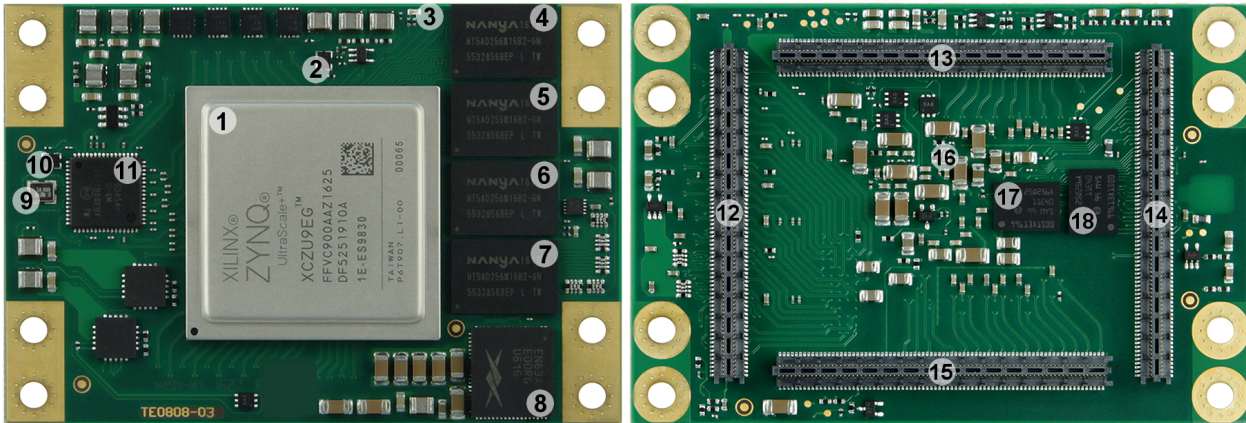


Current TE0808 boards are equipped with ES1 silicon. Erratas and functional restrictions may exist, please check Xilinx documentation and contact your local Xilinx FAE for restrictions.

Block Diagram



Main Components



1. Xilinx ZYNQ UltraScale+ XCZU9EG MPSoC, U1
2. Low-power programmable oscillator @ 33.333333 MHz (PS_CLK), U32
3. Red LED (DONE), D1
4. 256Mx16 DDR4-2400 SDRAM, U12
5. 256Mx16 DDR4-2400 SDRAM, U9
6. 256Mx16 DDR4-2400 SDRAM, U2
7. 256Mx16 DDR4-2400 SDRAM, U3
8. 12A PowerSoC DC-DC converter, U4
9. Quartz crystal, Y1
10. Low-power programmable oscillator @ 25.000000 MHz (IN0 for U5), U25
11. 10-channel programmable clock generator, U5
12. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J4
13. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J2
14. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J3
15. Ultra fine 0.50 mm pitch, Razor Beam™ LP Slim Terminal Strip with 160 contacts, J1
16. Quartz crystal, Y2
17. 256 Mbit serial NOR Flash memory, U7
18. 256 Mbit serial NOR Flash memory, U17

Key Features

- MPSoC: ZYNQ UltraScale+ ZU9EG 900 pin package
- Memory
 - 64-Bit DDR4, 8 GByte maximum
 - Dual SPI boot Flash in parallel, 512 MByte maximum
- User I/O
 - 65 x MIO, 48 x HD (all), 156 x HP (3 banks)
 - Serial transceiver: 4 x GTR + 16 x GTH
 - Transceiver clocks inputs and outputs
 - PLL clock generator inputs and outputs

- Size: 52 x 76 mm, 3 mm mounting holes for skyline heat spreader
- B2B connectors: 4 x 160 pin
- Si5345 - 10 output PLL
- All power supplies on board, single 3.3V power source required
 - 14 on-board DC-DC regulators and 13 LDOs
 - LP, FP, PL separately controlled power domains
- Support for all boot modes (except NAND) and scenarios
- Support for any combination of PS connected peripherals

Initial Delivery State

Storage device name	Content	Notes
SPI Flash main array	Not programmed	-
eFUSE Security	Not programmed	-
Si5345 OTP ROM	Not programmed	

Signals, Interfaces and Pins

Board to Board (B2B) I/Os

I/O signals connected to the MPSoC's I/O banks and B2B connectors:

Bank	Type	B2B Connector	I/O Signal Count	Voltage	Direction	Notes
47	HD	J3	24	VCCO47	Input/Output	Supplied from the baseboard, 3.3V maximum.
48	HD	J3	24	VCCO48	Input/Output	Supplied from the baseboard, 3.3V maximum.
64	HP	J4	52	VCCO64	Input/Output	Supplied from the baseboard, 1.8V maximum.
65	HP	J4	52	VCCO65	Input/Output	Supplied from the baseboard, 1.8V maximum.
66	HP	J1	52	VCCO66	Input/Output	Supplied from the baseboard, 1.8V maximum.
128	GTH	J2	16 (4 lanes)		Input/Output	
128	GTH_CLK	J2	2		Input	
228	GTH	J1	16 (4 lanes)		Input/Output	
228	GTH_CLK	J3	2		Input	
229	GTH	J1	16 (4 lanes)		Input/Output	
229	GTH_CLK	J3	2		Input	
230	GTH	J1	16 (4 lanes)		Input/Output	
230	GTH_CLK	J3	2		Input	
500	MIO	J3	13	1.8V	Input/Output	
501	MIO	J3	26	1.8V	Input/Output	
502	MIO	J3	26	1.8V	Input/Output	
503	JTAG	J2	4		Input/Output	
505	GTR	J2	16 (4 lanes)		Input/Output	
505	GTR_CLK	J2	4		Input	

All MIO banks are powered from on-module DC-DC power rail. All PL I/O Banks have separate VCCO pins in the B2B connectors, valid VCCO should be supplied from the baseboard.

For detailed information about the B2B pin-out, please refer to the [Pin-out](#) table.

JTAG Interface

JTAG access to the Xilinx UltraScale+ MPSoC is provided through B2B connector J2.

JTAG Signal	B2B Connector Pin
TCK	J2-120
TDI	J2-122
TDO	J2-124
TMS	J2-126

LEDs

TE0808 has one red LED (D1) which reflects MPSoC's DONE signal. This LED goes ON when power has been applied to the module and stays ON until MPSoC FPGA is configured properly.

Programmable Clock Generator

Following table illustrates on-board Si5345A programmable clock generator chip inputs and outputs:

Input/Output	Connected to	Frequency	Notes
IN0	On-board Oscillator	25 MHz	Main reference for the PLL
IN1	B2B Connector	User	AC decoupling required on base
IN2	B2B Connector	User	AC decoupling required on base
IN3	OUT9	User	Loop-back from OUT9
OUT0	B2B Connector	User	Default off.
OUT1	B230 CLK0	User	Default off.
OUT2	B229 CLK1	User	Default off.
OUT3	B228 CLK1	User	Default off.
OUT4	B505 CLK2	User	Default off.
OUT5	B505 CLK3	User	Default off.
OUT6	B128 CLK0	User	Default off.
OUT7	B2B Connector	User	Default off.
OUT8	B2B Connector	User	Default off.
OUT9	IN3	User	Default off.
XA/XB	Quartz	50.000 MHz	not used as time reference



Si5345 OTP ROM is not programmed by default at delivery, so it is customers responsibility to either configure Si5345 during FSBL or then use SiLabs programmer and burn the OTP ROM with customer fixed clock setup.

Si5345 OTP can only be programmed two times, as different user configurations may required different setup TE0808 is normally shipped with blank OTP.

For more information [Si5345 at SiLabs](#)

Clocking

Clock	Frequency	Note
PS_CLK	33.3333 MHz	PS main clock
PS_PAD (RTC)	32.768 kHz	Clock for PS RTC

B2B connectors

Order number	REF Number	Samtec Numer	Type	Contribution to stacking height	Datasheet	Comment
27017	REF-189545-01	ST5-80-1.00-L-D-P-TR	Module connector	1 mm	st5-xx-x.xx-x-d-p-tr-mkt.pdf st5.pdf	Assembly option on request
27220	REF-192552-02	ST5-80-1.50-L-D-P-TR	Module connector	1.5 mm	REF-192552-02.pdf	Standard connector used on modules
27018	REF-189545-02	SS5-80-3.00-L-D-K-TR	Baseboard connector	3 mm	ss5-xx-x.xx-x-d-k-tr-mkt.pdf ss5.pdf	Assembly option on request
27219	REF192552-01	SS5-80-3.50-L-D-K-TR	Baseboard connector	3.5 mm	REF-192552-01.pdf	Standard connector used on modules

SS5-ST5 Product Specification: [ss5-st5.pdf](#)

Technical Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference Document
Supply voltage			V	
Storage temperature (ambient)			°C	

Recommended Operating Conditions

Parameter	Min	Max	Units	Reference Document
Supply voltage			V	

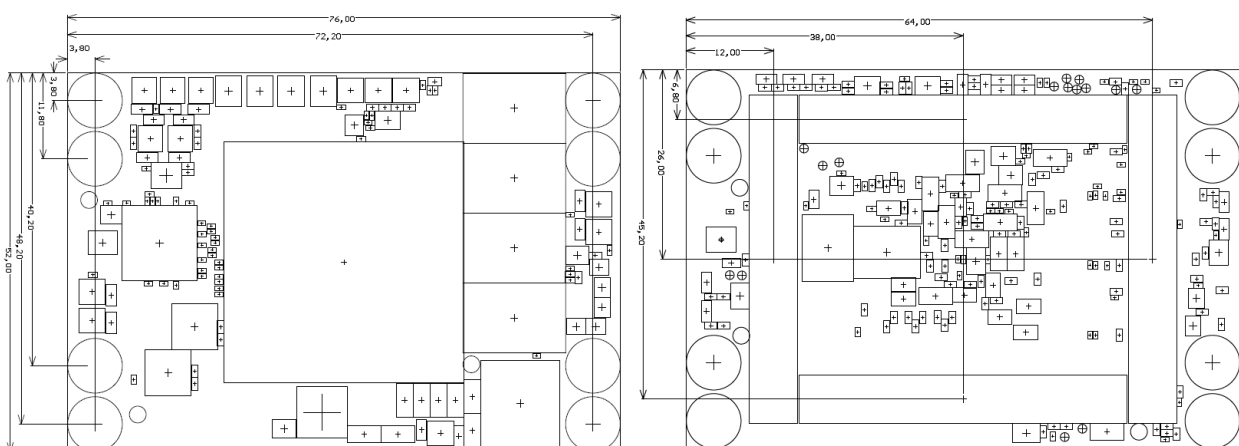


Assembly variants for higher storage temperature range are available on request.

Physical Dimensions

- Module size: 52 mm x 76 mm. Please download the assembly diagram for exact numbers
- Mating height with standard connectors: 4mm
- PCB thickness: 1.6mm
- Highest part on PCB: approx. 3mm. Please download the step model for exact numbers

All dimensions are given in millimeters.



Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial grade: -40°C to +85°C.

The module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

Weight

.. g - Plain module

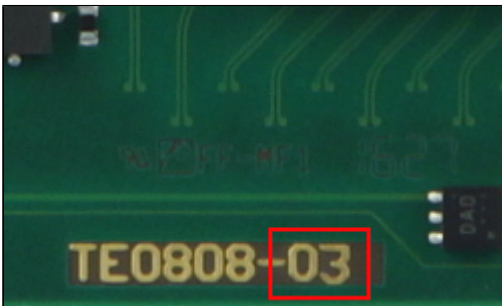
.. g - Set of bolts and nuts

Revision History

Hardware Revision History

Date	Revision	Notes	Link to PCN	Documentation Link
	03	Second production release		TE0808-03
2016-03-09	02	First production release		TE0808-02
	01	Prototypes		

Hardware revision number is written on the PCB board together with the module model number separated by the dash.



Document Change History

Date	Revision	Contributors	Description
2017-02-06	V1	Jan Kumann	Initial document.

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