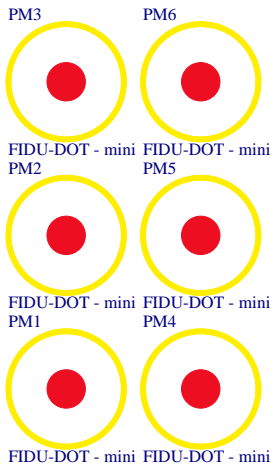
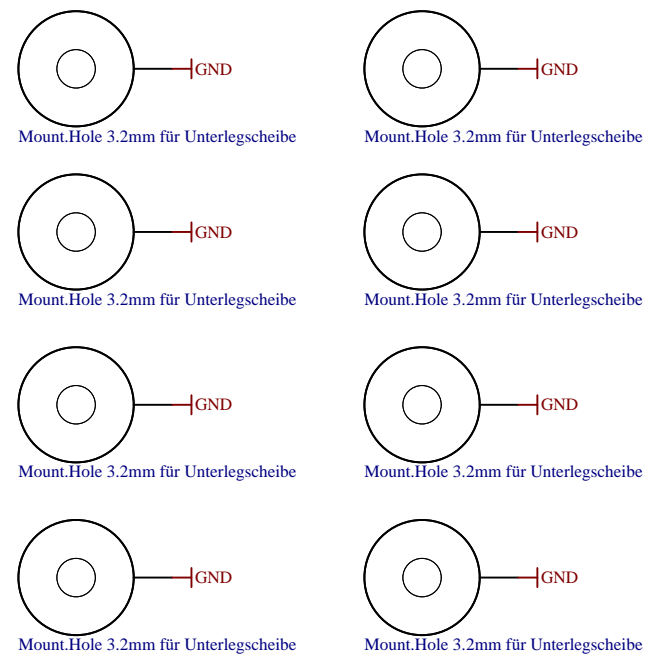


U_J1 J1.SchDoc	U_B_PS_GT B_PS_GT.SchDoc	U_DDR4-TERM DDR4-TERM.SchDoc
U_J2 J2.SchDoc	U_PS_DDR PS_DDR.SchDoc	U_ZU_POWER ZU_POWER.SchDoc
U_J3 J3.SchDoc	U_B_MIO B_MIO.SchDoc	U_ZU_PS_POWER ZU_PS_POWER.SchDoc
U_J4 J4.SchDoc	U_B_HD B_HD.SchDoc	U_POWER POWER.SchDoc
U_DDR4-TERM DDR4-TERM.SchDoc	U_Clock Clock.SchDoc	U_POWER_2 POWER_2.SchDoc
U_B64 B64.SchDoc	U_CONFIG CONFIG.SchDoc	U_POWER_3 POWER_3.SchDoc
U_B65 B65.SchDoc	U_DDR4-RAM DDR4-RAM.SchDoc	U_POWER_4 POWER_4.SchDoc
U_B66 B66.SchDoc	U_DDR4-RAM_2 DDR4-RAM_2.SchDoc	U_RC Revision_Changes.SchDoc
U_B_GT B_GT.SchDoc	U_DDR4-RAM_3 DDR4-RAM_3.SchDoc	
U_B_GT_2 B_GT_2.SchDoc	U_DDR4-RAM_4 DDR4-RAM_4.SchDoc	

Special notes:

*U41 Power supervisor TPS3106K33DBVR replaced by Schottky diodes SBAS70-04LT1G*



Serial  
Serialnummer 6,3 x 6.3mm

MECHI  
TE Address Overlay

LOGO ADDRESS

LOGO1  
TE Logo PRINT Layer

LOGO PRINT

Design drawn by:	VY
Checked by:	MR
Assembly variant:	6BI21-X
Created by:	VY
Modified by:	VY
Modified at:	2020-06-08



Title: TE0808		
A4	Number: TE0808 6BI21-X	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 1 of 28
Filename: TE0808.SchDoc		

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A

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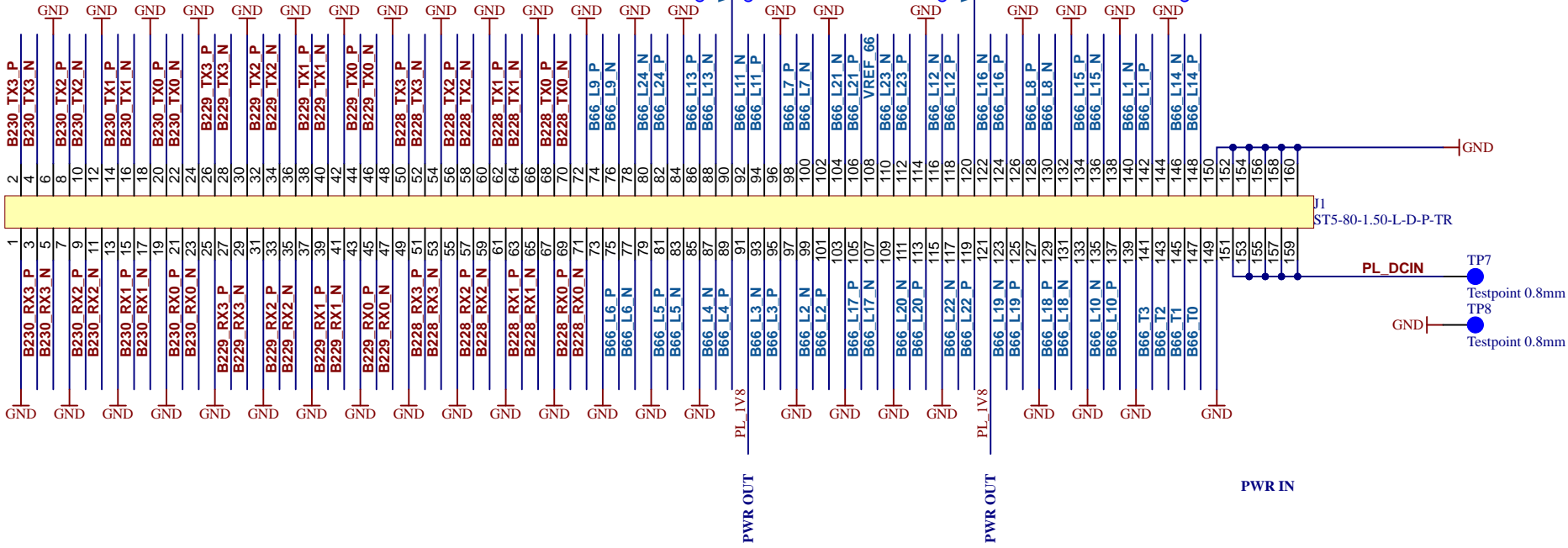

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Title: TE0808 - Connector J1		
A4	Number: TE0808 6BI21-X	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 2 of 28
Filename: J1.SchDoc		

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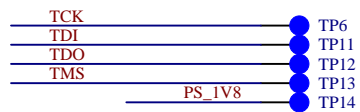
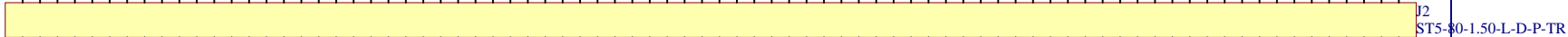
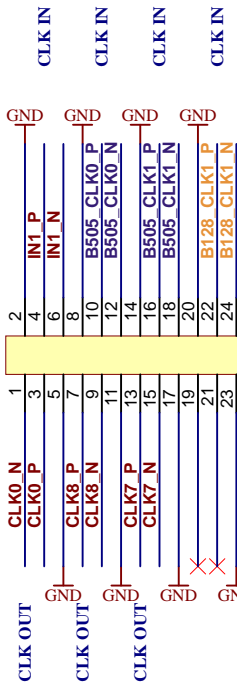
B

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D



(External pull-up R required)  
 (External pull-up R required)  
 (On board pull-up R)  
 (On board pull-up R)  
 (On board pull-up R)  
 (On board pull-up R)  
 (On board pull-up R)  
 (On board pull-up R)  
 (On board pull-up R)  
 (On board pull-up R)  
 (On board pull-up R)

(External pull-up R required)  
 (External pull-up R required)  
 (On board pull-up R)



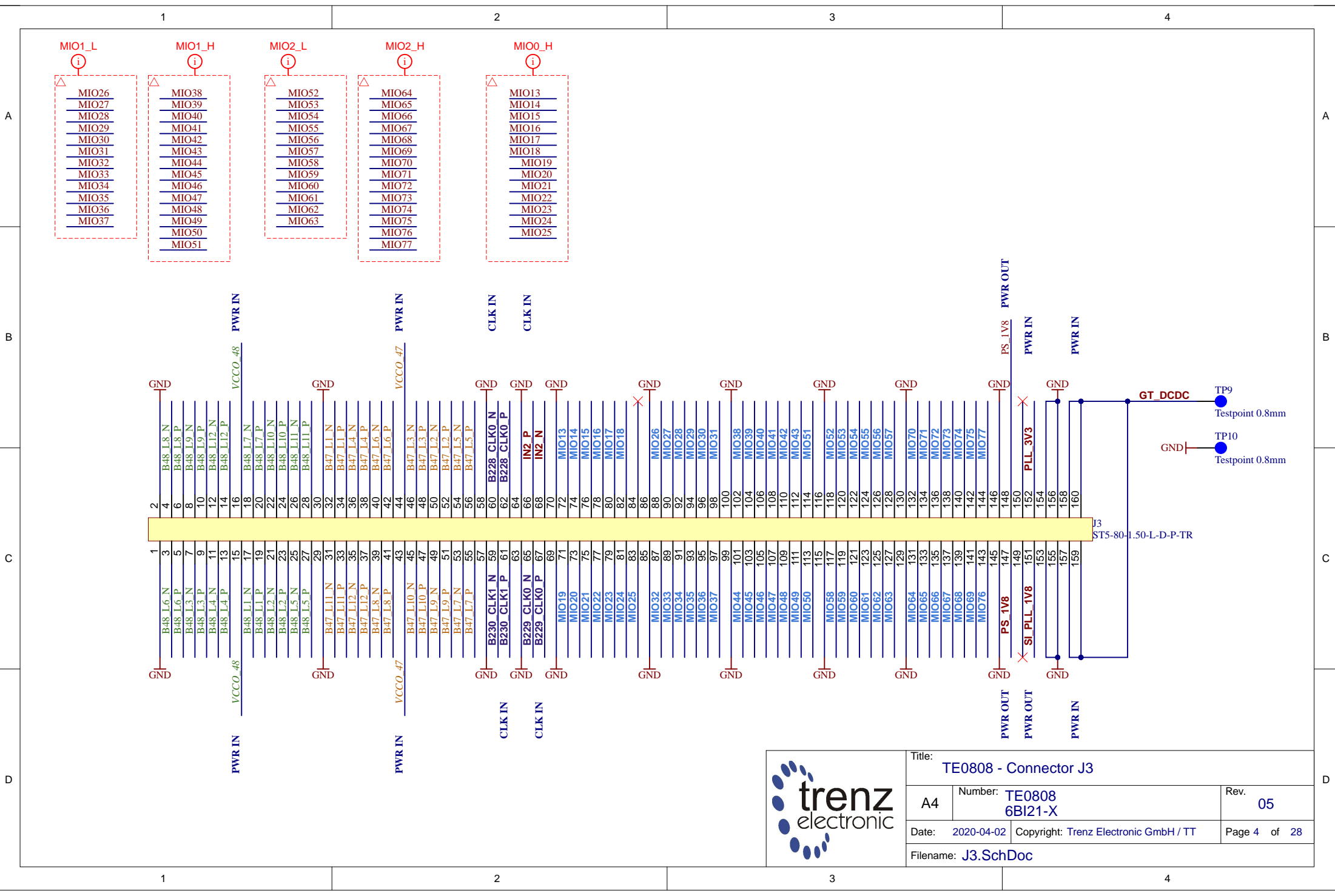
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A4	Number: TE0808 6BI21-X	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 3 of 28
Filename: J2.SchDoc		

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Title: TE0808 - Connector J3		
A4	Number: TE0808 6BI21-X	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 4 of 28
Filename: J3.SchDoc		



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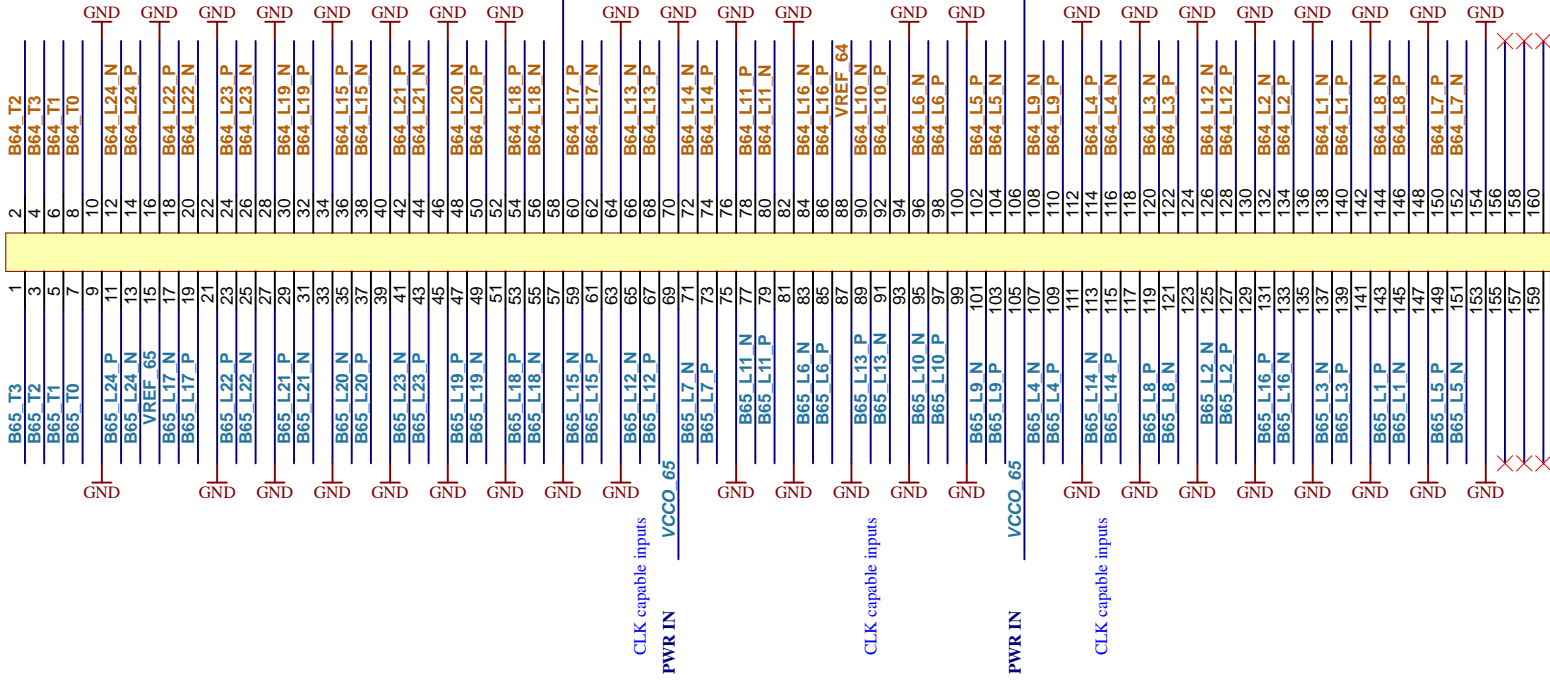
B

C

C

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D



J4 ST5-80-1.50-L-D-P-TR



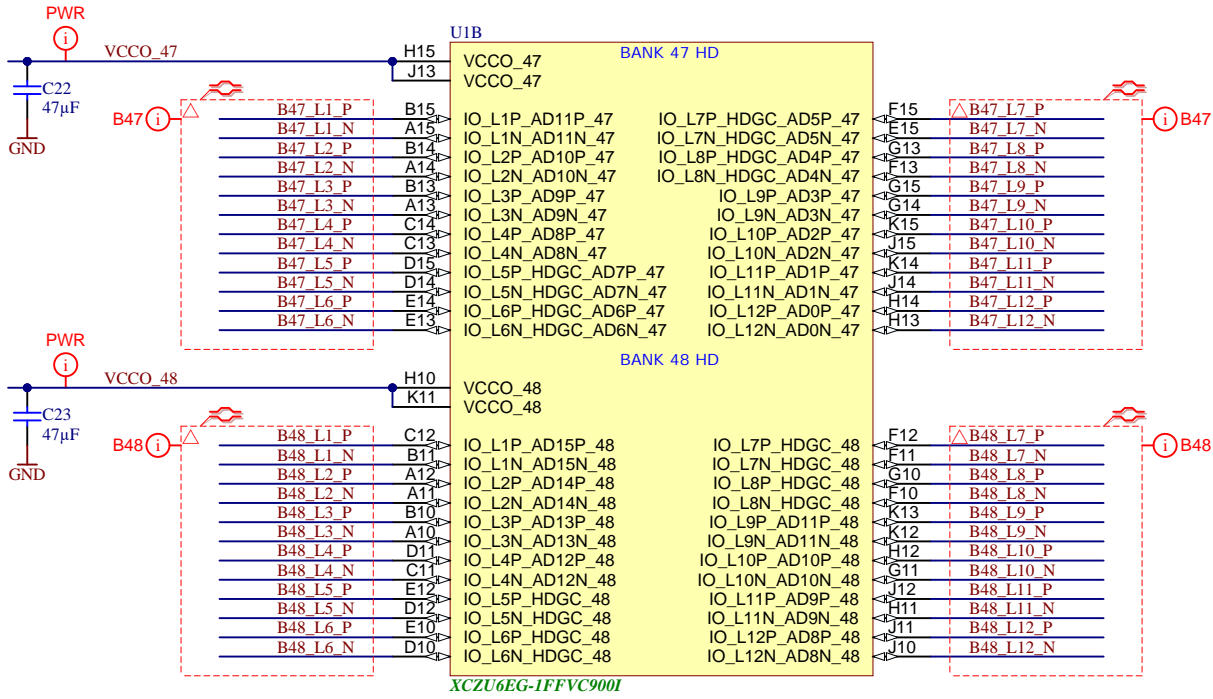
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Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 5 of 28
Filename: J4.SchDoc		

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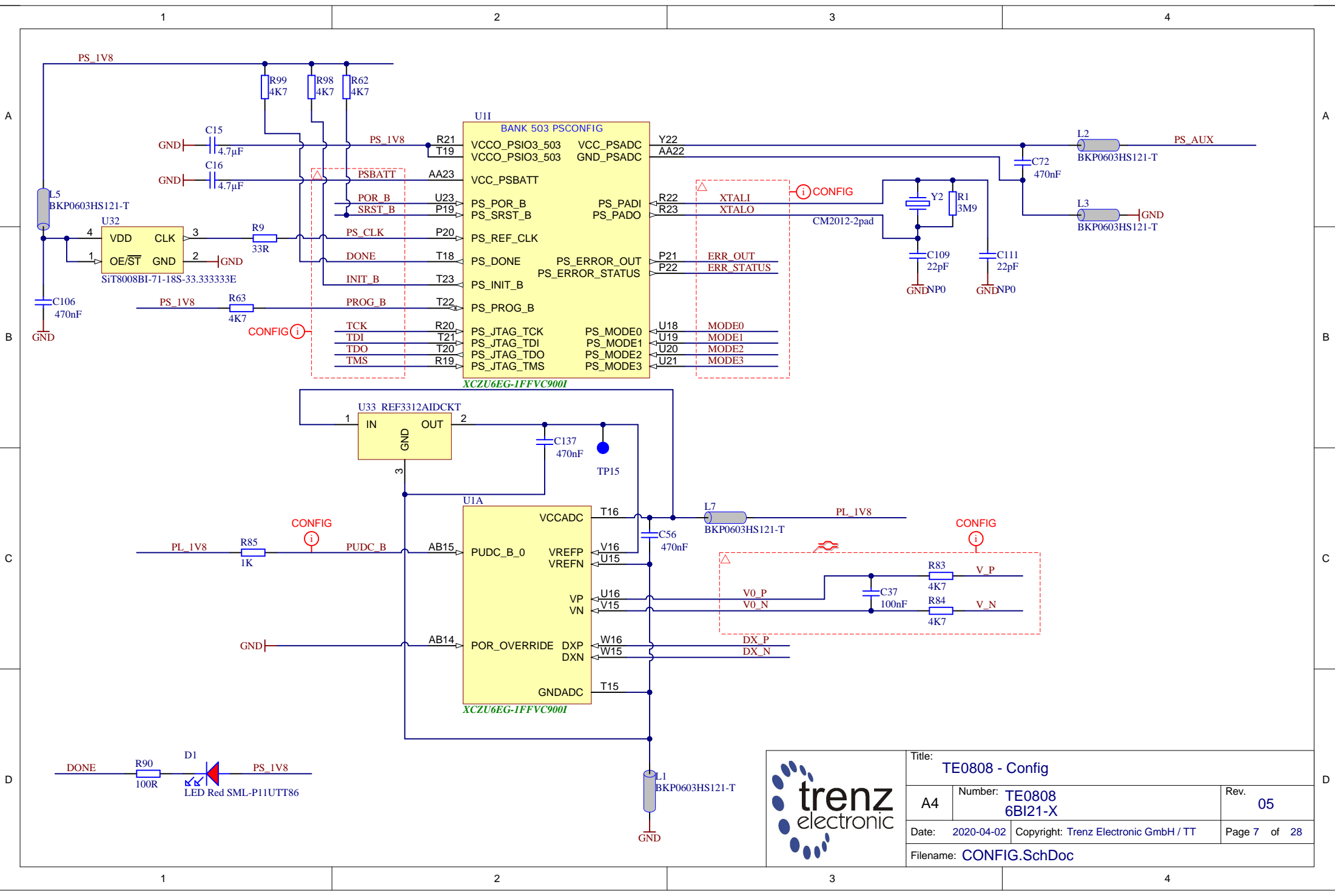
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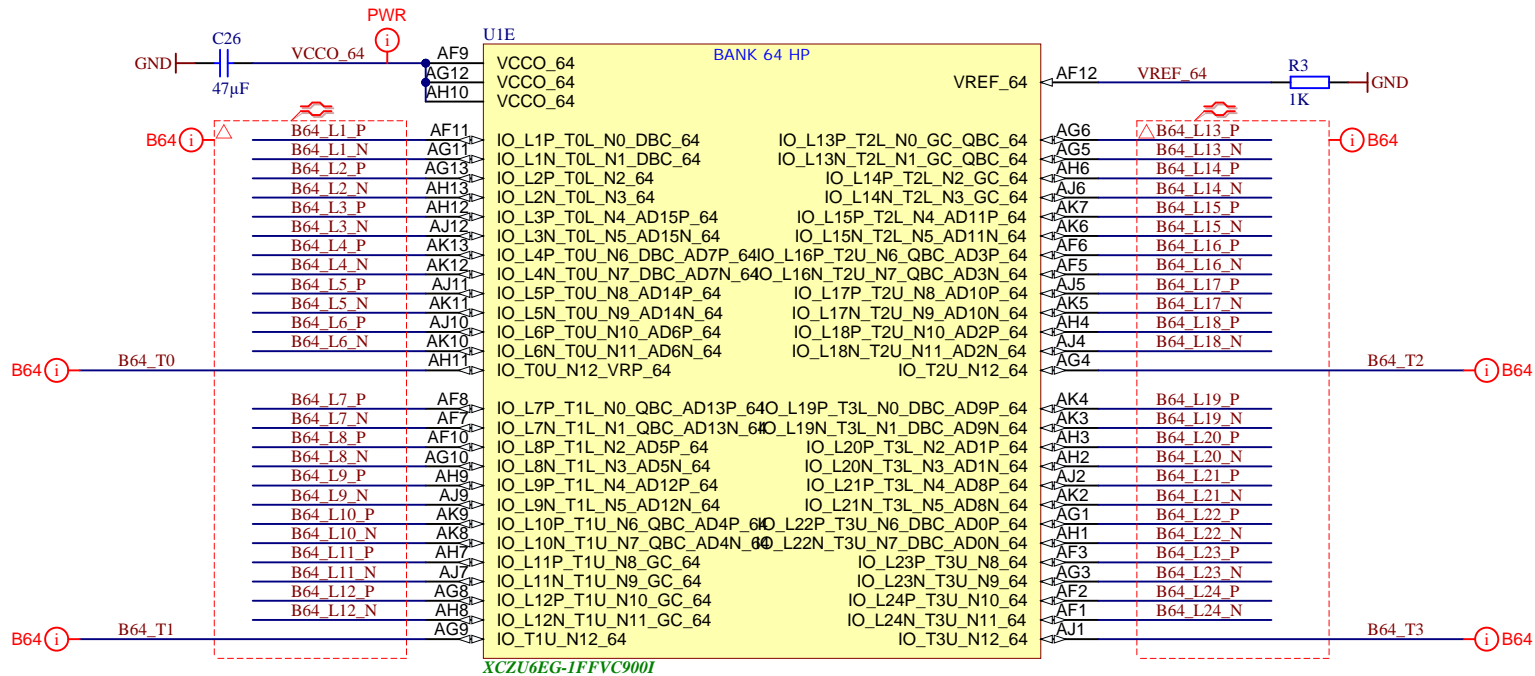
XCZU6EG-1FFVC9001



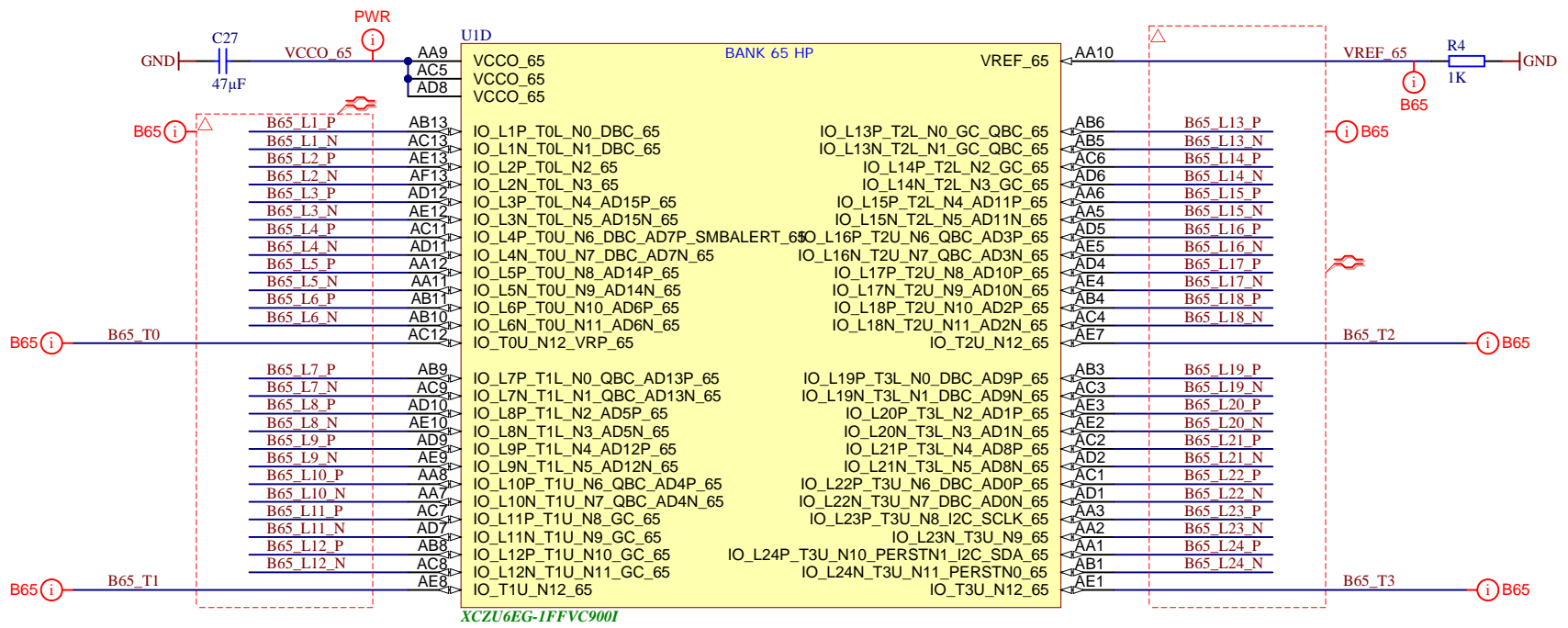
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Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 6 of 28
Filename: B_HD.SchDoc		



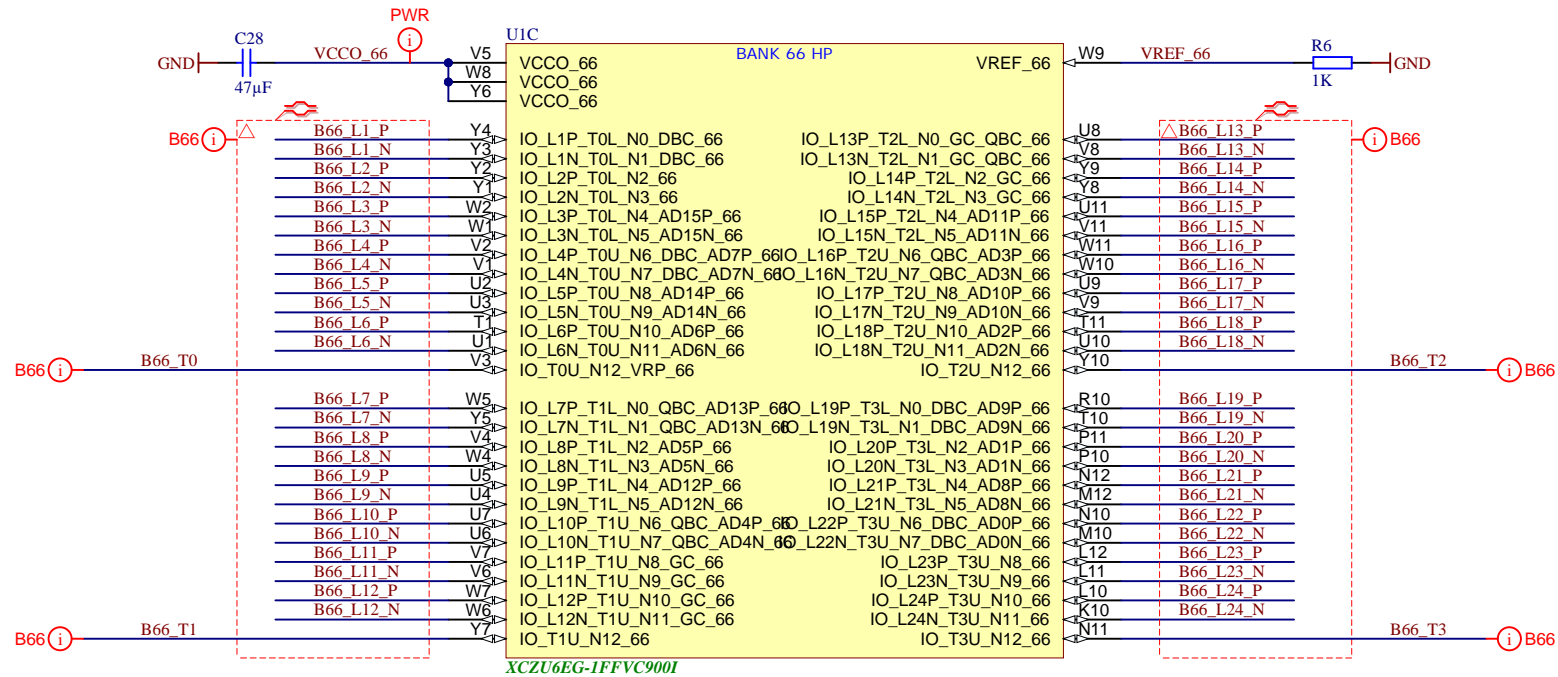
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A4	Number: TE0808 6BI21-X	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 7 of 28
Filename: CONFIG.SchDoc		



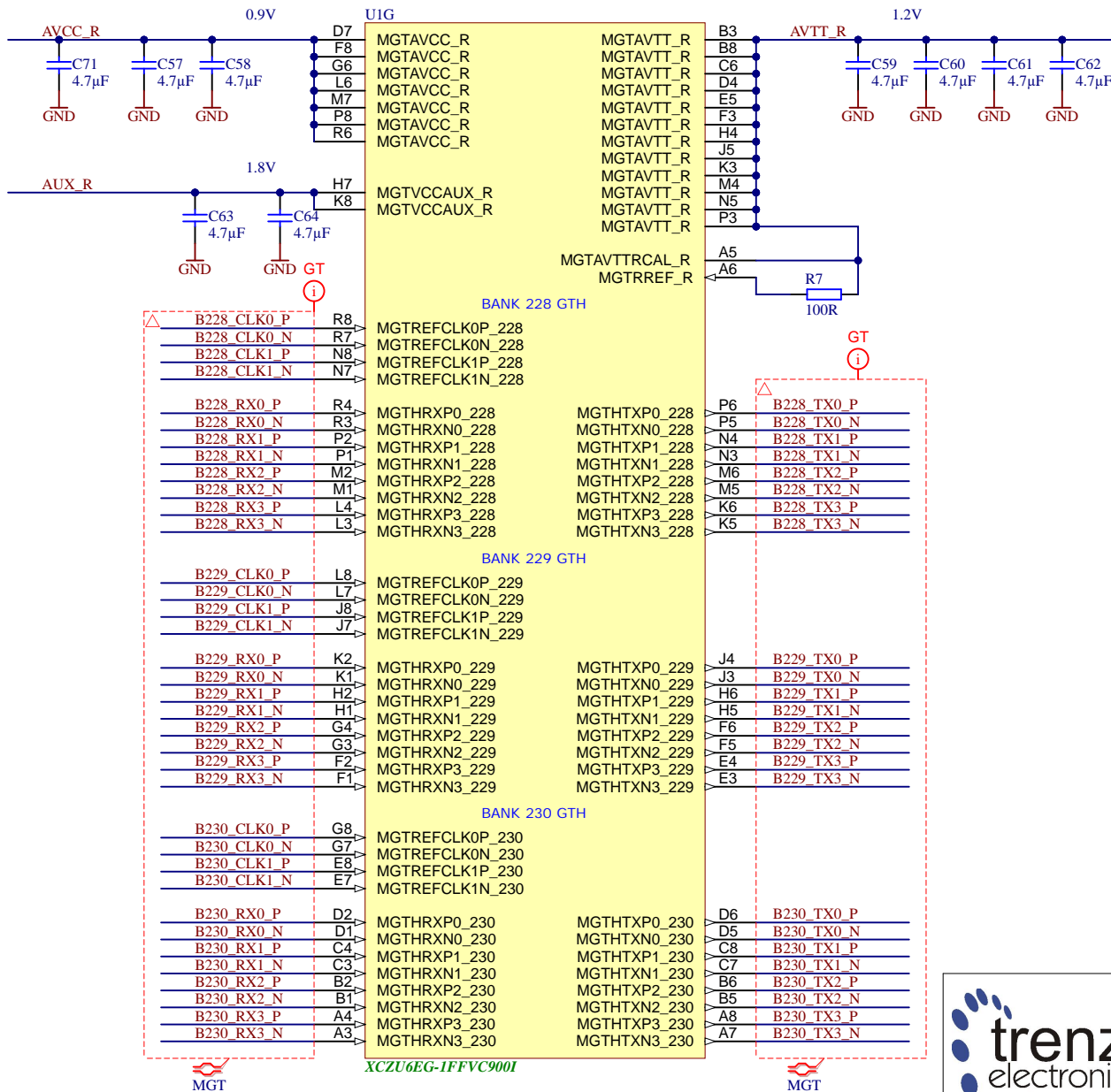
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A4	Number: <b>TE0808 6BI21-X</b>	Rev. <b>05</b>
Date: <b>2020-04-02</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>8</b> of <b>28</b>
Filename: <b>B64.SchDoc</b>		



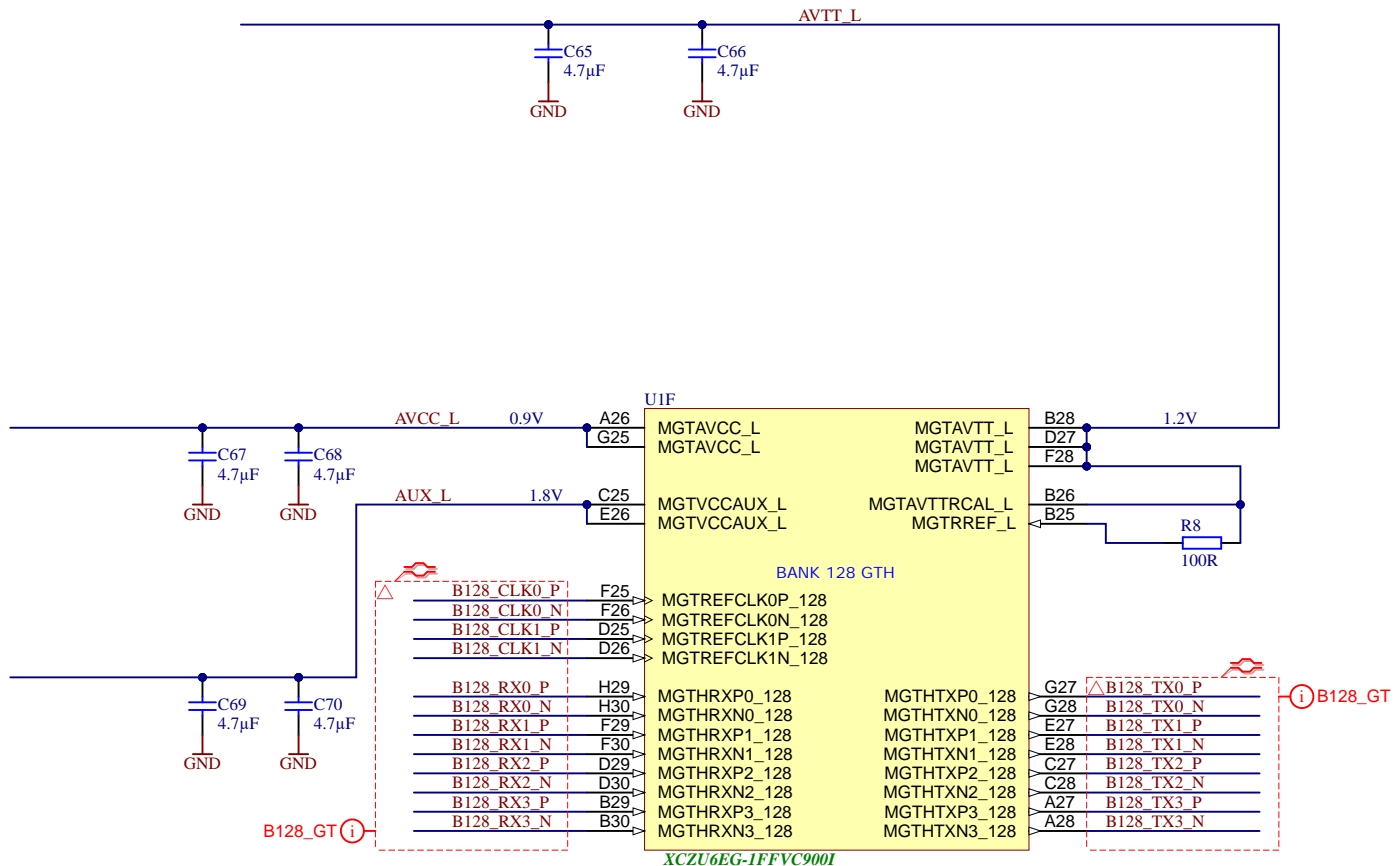
Title: TE0808 - B65		
A4	Number: TE0808 6BI21-X	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 9 of 28
Filename: B65.SchDoc		



Title: <b>TE0808 - B66</b>		
A4	Number: <b>TE0808 6BI21-X</b>	Rev. <b>05</b>
Date: <b>2020-04-02</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	
Page <b>10</b> of <b>28</b>		
Filename: <b>B66.SchDoc</b>		

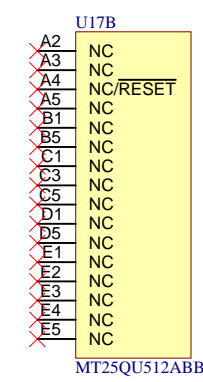
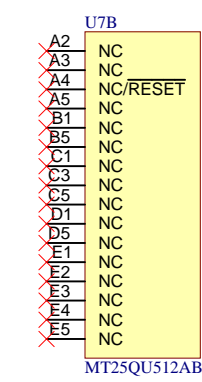
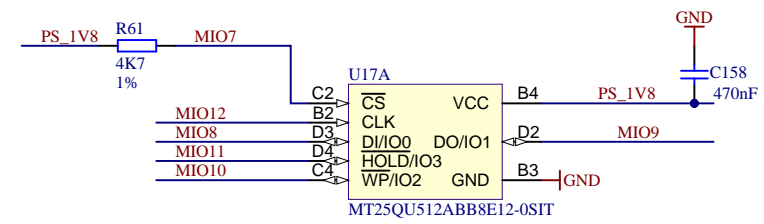
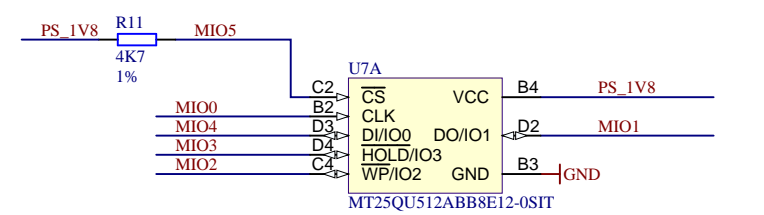
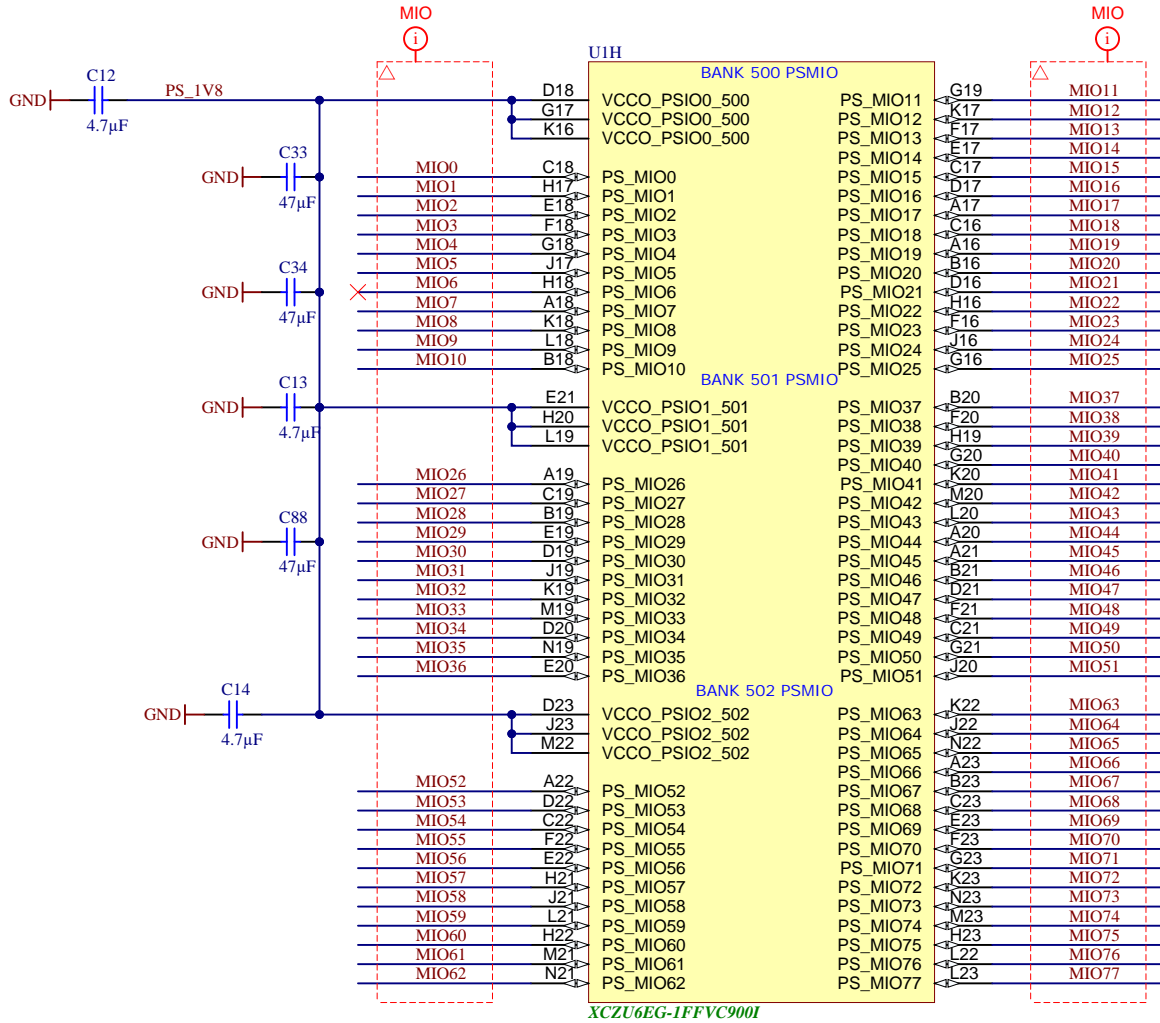


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Date: <b>2020-04-02</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	
Page <b>11</b> of <b>28</b>		
Filename: <b>B_GT.SchDoc</b>		

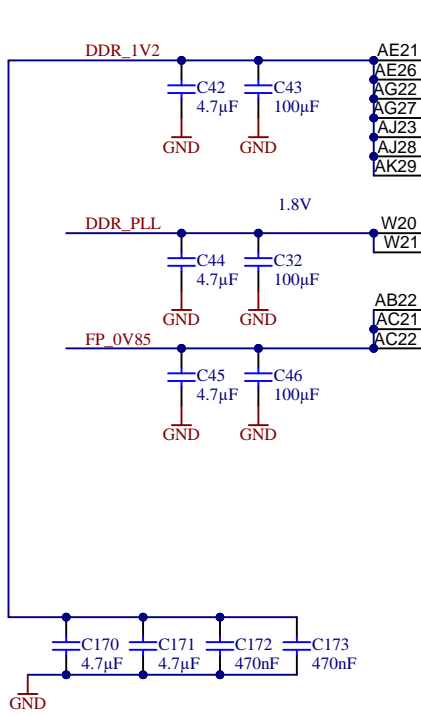


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	A4	Number: TE0808 6BI21-X
	Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT
	Filename: B_GT_2.SchDoc	
	Rev. 05	Page 12 of 28





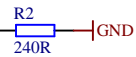
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	Date: <b>2020-04-02</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	
	Filename: <b>B_MIO.SchDoc</b>		Page <b>13</b> of <b>28</b>



**UIJ BANK 504 PSDDR**

AE21	VCCO_PSDDR_504	PS_DDR_CK0	AJ26	DDR4-CLK0_P
AE26	VCCO_PSDDR_504	PS_DDR_CK_N0	AJ27	DDR4-CLK0_N
AG22	VCCO_PSDDR_504	PS_DDR_CKE0	AJ25	DDR4-CKE0
AG27	VCCO_PSDDR_504			
AJ23	VCCO_PSDDR_504	PS_DDR_CK1	AG23	
AJ28	VCCO_PSDDR_504	PS_DDR_CK_N1	AG24	
AK29	VCCO_PSDDR_504	PS_DDR_CKE1	AH27	
		PS_DDR_A0	AK25	DDR4-A0
		PS_DDR_A1	AK28	DDR4-A1
		PS_DDR_A2	AK27	DDR4-A2
		PS_DDR_A3	AH24	DDR4-A3
		PS_DDR_A4	AK24	DDR4-A4
		PS_DDR_A5	AJ30	DDR4-A5
		PS_DDR_A6	AE22	DDR4-A6
		PS_DDR_A7	AE25	DDR4-A7
		PS_DDR_A8	AE23	DDR4-A8
		PS_DDR_A9	AE24	DDR4-A9
		PS_DDR_A10	AD22	DDR4-A10
		PS_DDR_A11	AH23	DDR4-A11
		PS_DDR_A12	AF21	DDR4-A12
		PS_DDR_A13	AG21	DDR4-A13
		PS_DDR_A14	AF22	DDR4-A14
		PS_DDR_A15	AF23	DDR4-A15
		PS_DDR_A16	AD21	DDR4-A16
		PS_DDR_A17	AD20	DDR4-A17
		PS_DDR_CS_N0	AJ24	DDR4-CS
		PS_DDR_CS_N1	AG25	
		PS_DDR_BA0	AG26	DDR4-BA0
		PS_DDR_BA1	AF25	DDR4-BA1
		PS_DDR_BG0	AF26	DDR4-BG0
		PS_DDR_BG1	AD26	DDR4-BG1
		PS_DDR_PARITY	AC14	DDR4-PAR
		PS_DDR_RAM_RST_N	AC16	DDR4-RESET
		PS_DDR_ACT_N	AC17	DDR4-ACT
		PS_DDR_ALERT_N	AD19	DDR4-ALERT
		PS_DDR_ZQ	AC23	
		PS_DDR_ODT0	AJ29	DDR4-ODT0
		PS_DDR_ODT1	AH26	

*XCZU6EG-1FFVC9001*



**UIK BANK 504 PSDDR**

DQ0	AK17	PS_DDR_DQ0	PS_DDR_DQ32	Y24	DQ32
DQ1	AH17	PS_DDR_DQ1	PS_DDR_DQ33	Y25	DQ33
DQ2	AJ17	PS_DDR_DQ2	PS_DDR_DQ34	AA25	DQ34
DQ3	AH16	PS_DDR_DQ3	PS_DDR_DQ35	AA26	DQ35
DQ4	AK15	PS_DDR_DQ4	PS_DDR_DQ36	AC26	DQ36
DQ5	AK14	PS_DDR_DQ5	PS_DDR_DQ37	AD24	DQ37
DQ6	AJ14	PS_DDR_DQ6	PS_DDR_DQ38	AD25	DQ38
DQ7	AH14	PS_DDR_DQ7	PS_DDR_DQ39	AC24	DQ39
DQ8	AK19	PS_DDR_DQ8	PS_DDR_DQ40	W27	DQ40
DQ9	AK18	PS_DDR_DQ9	PS_DDR_DQ41	W26	DQ41
DQ10	AJ19	PS_DDR_DQ10	PS_DDR_DQ42	W24	DQ42
DQ11	AH19	PS_DDR_DQ11	PS_DDR_DQ43	W25	DQ43
DQ12	AK21	PS_DDR_DQ12	PS_DDR_DQ44	U26	DQ44
DQ13	AK22	PS_DDR_DQ13	PS_DDR_DQ45	U27	DQ45
DQ14	AH21	PS_DDR_DQ14	PS_DDR_DQ46	U25	DQ46
DQ15	AJ22	PS_DDR_DQ15	PS_DDR_DQ47	U24	DQ47
DQ16	AG12	PS_DDR_DQ16	PS_DDR_DQ48	AA30	DQ48
DQ17	AG15	PS_DDR_DQ17	PS_DDR_DQ49	AB29	DQ49
DQ18	AG16	PS_DDR_DQ18	PS_DDR_DQ50	AB30	DQ50
DQ19	AF16	PS_DDR_DQ19	PS_DDR_DQ51	AB28	DQ51
DQ20	AD14	PS_DDR_DQ20	PS_DDR_DQ52	AC27	DQ52
DQ21	AD16	PS_DDR_DQ21	PS_DDR_DQ53	AD27	DQ53
DQ22	AD15	PS_DDR_DQ22	PS_DDR_DQ54	AD29	DQ54
DQ23	AD17	PS_DDR_DQ23	PS_DDR_DQ55	AD30	DQ55
DQ24	AE17	PS_DDR_DQ24	PS_DDR_DQ56	AA28	DQ56
DQ25	AE18	PS_DDR_DQ25	PS_DDR_DQ57	AA27	DQ57
DQ26	AE20	PS_DDR_DQ26	PS_DDR_DQ58	Y28	DQ58
DQ27	AE19	PS_DDR_DQ27	PS_DDR_DQ59	Y27	DQ59
DQ28	AG18	PS_DDR_DQ28	PS_DDR_DQ60	W30	DQ60
DQ29	AH18	PS_DDR_DQ29	PS_DDR_DQ61	V30	DQ61
DQ30	AG19	PS_DDR_DQ30	PS_DDR_DQ62	V28	DQ62
DQ31	AG20	PS_DDR_DQ31	PS_DDR_DQ63	V29	DQ63
			PS_DDR_DQ64	AE27	
			PS_DDR_DQ65	AF28	
			PS_DDR_DQ66	AG28	
			PS_DDR_DQ67	AE28	
			PS_DDR_DQ68	AH30	
			PS_DDR_DQ69	AF30	
			PS_DDR_DQ70	AG30	
			PS_DDR_DQ71	AE30	
			PS_DDR_DM0	AK16	DDR4-DM0
			PS_DDR_DM1	AK20	DDR4-DM1
			PS_DDR_DM2	AE14	DDR4-DM2
			PS_DDR_DM3	AF20	DDR4-DM3
			PS_DDR_DM4	AB26	DDR4-DM4
			PS_DDR_DM5	V24	DDR4-DM5
			PS_DDR_DM6	AC30	DDR4-DM6
			PS_DDR_DM7	Y30	DDR4-DM7
			PS_DDR_DM8	AE29	

*XCZU6EG-1FFVC9001*



Title: TE0808 - PS_DDR		
A4	Number: TE0808 6BI21-X	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 14 of 28
Filename: PS_DDR.SchDoc		

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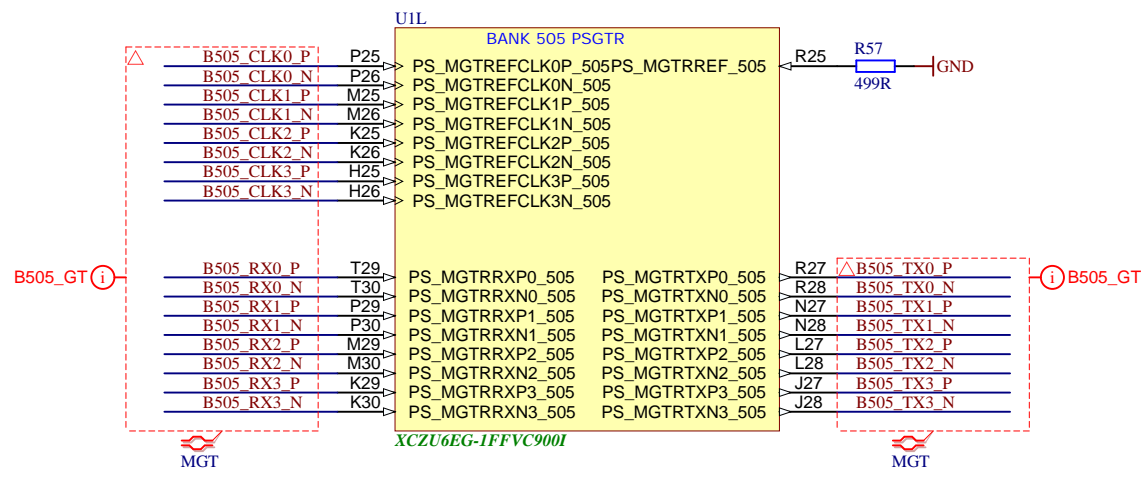
B

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Title: TE0808 - PS_GT		
A4	Number: TE0808 6BI21-X	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 15 of 28
Filename: B_PS_GT.SchDoc		

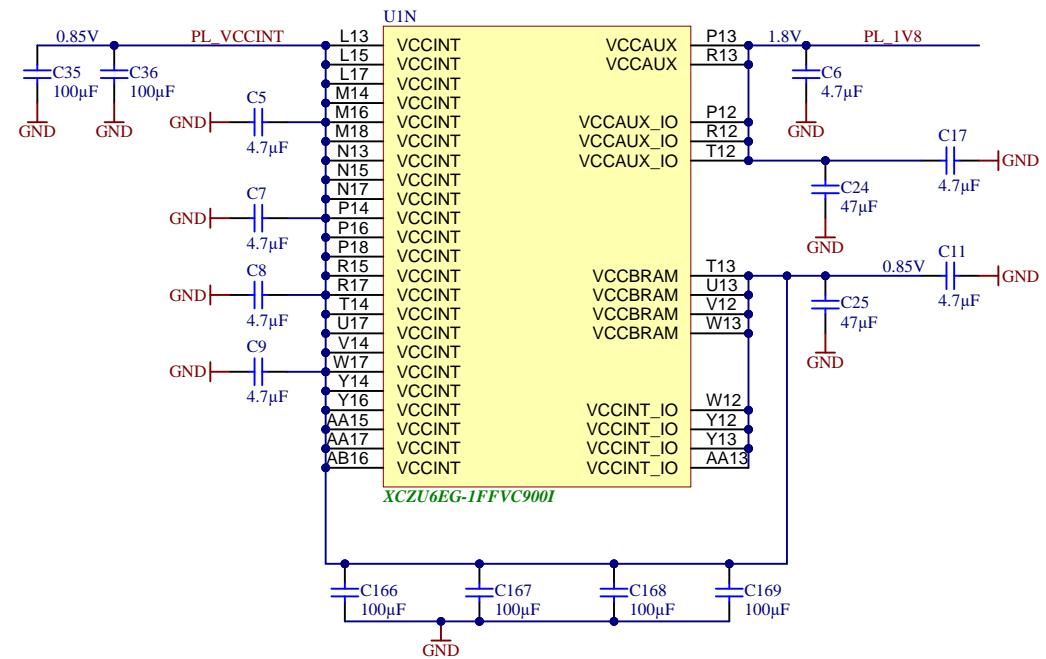
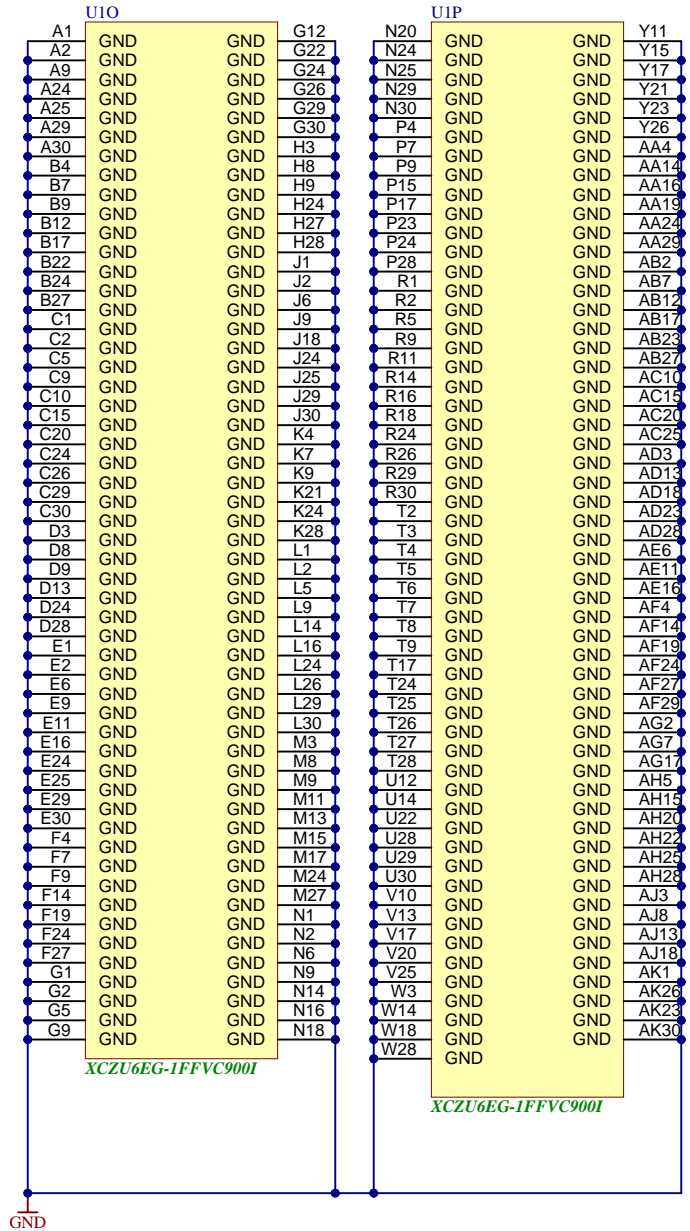
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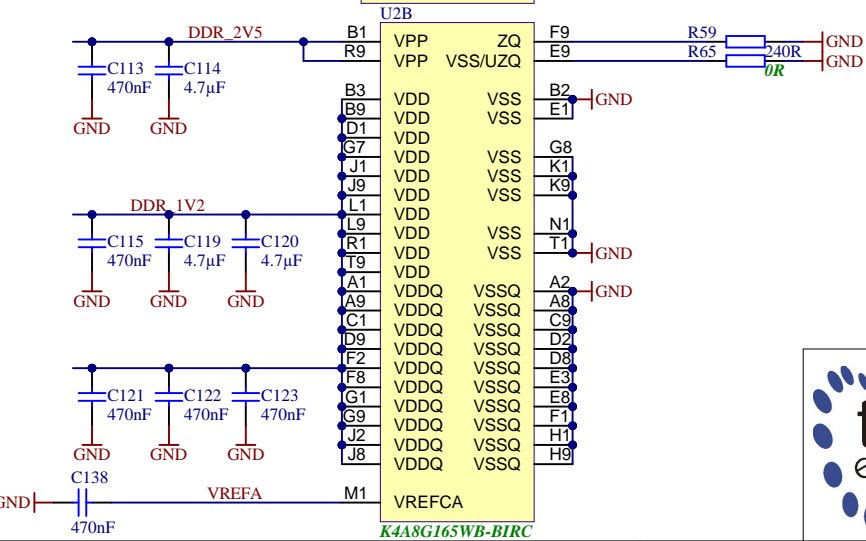
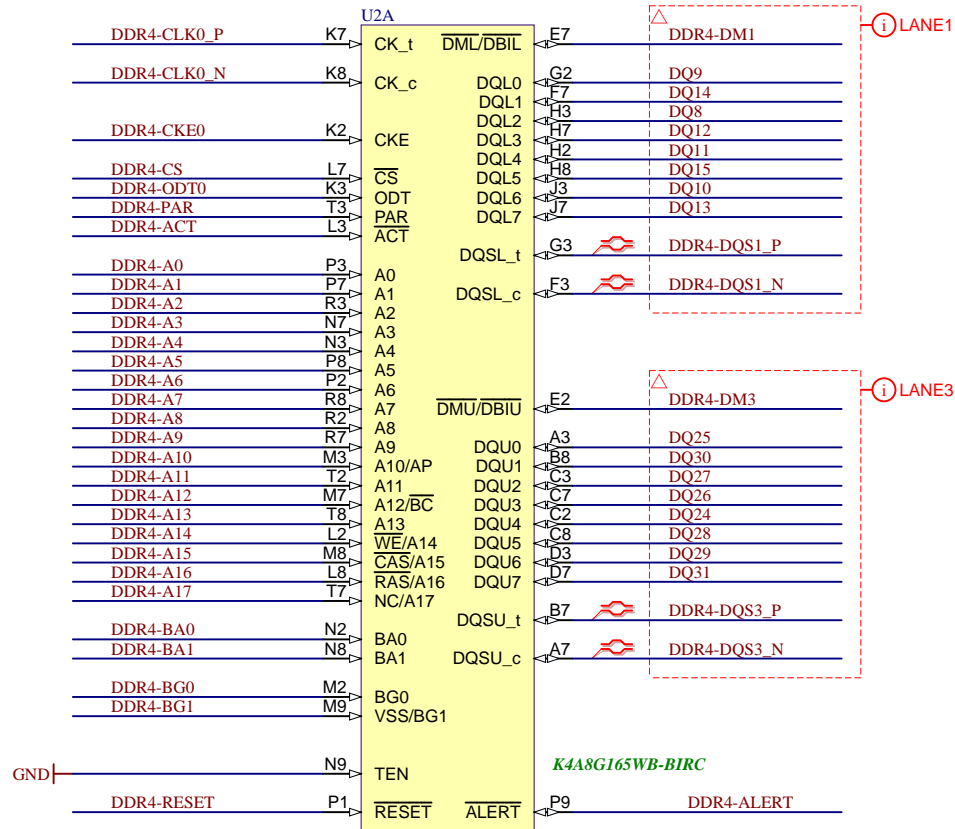
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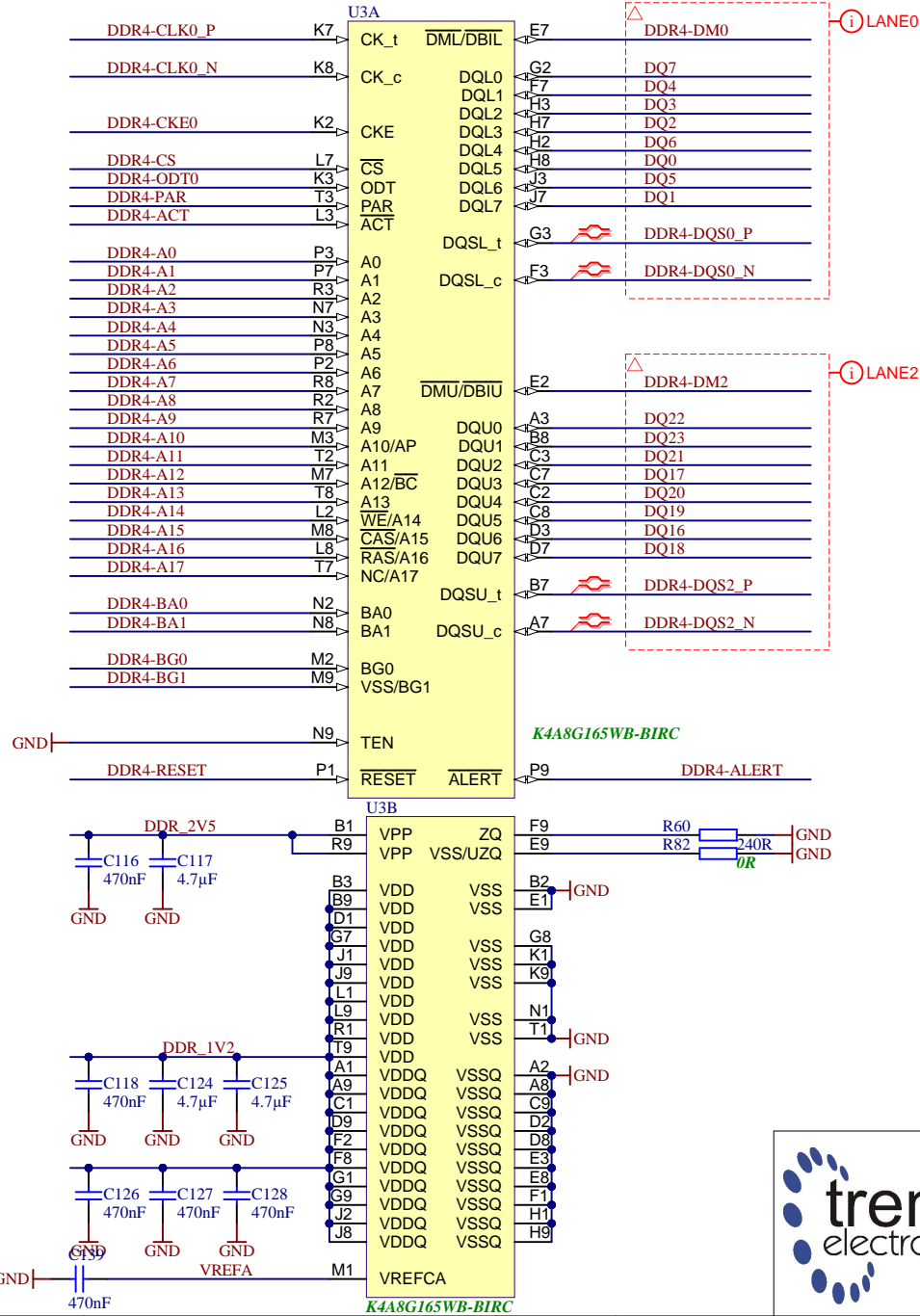




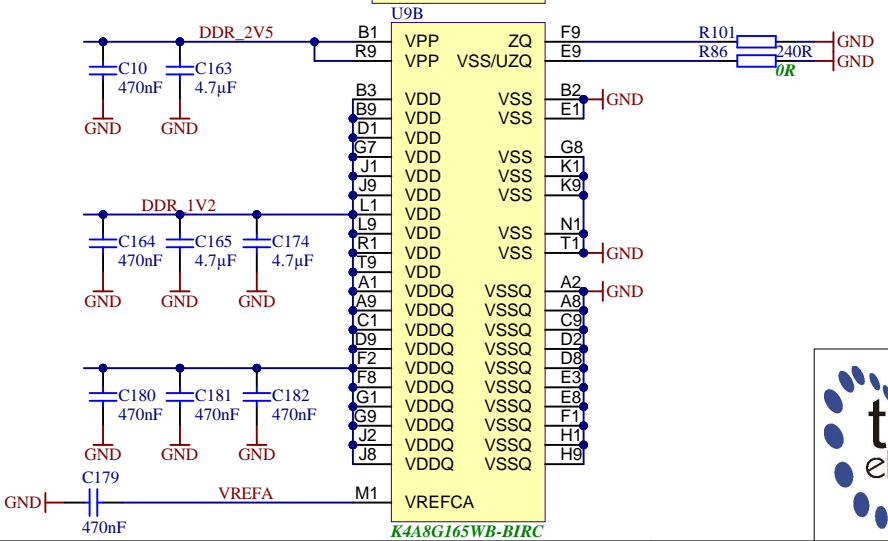
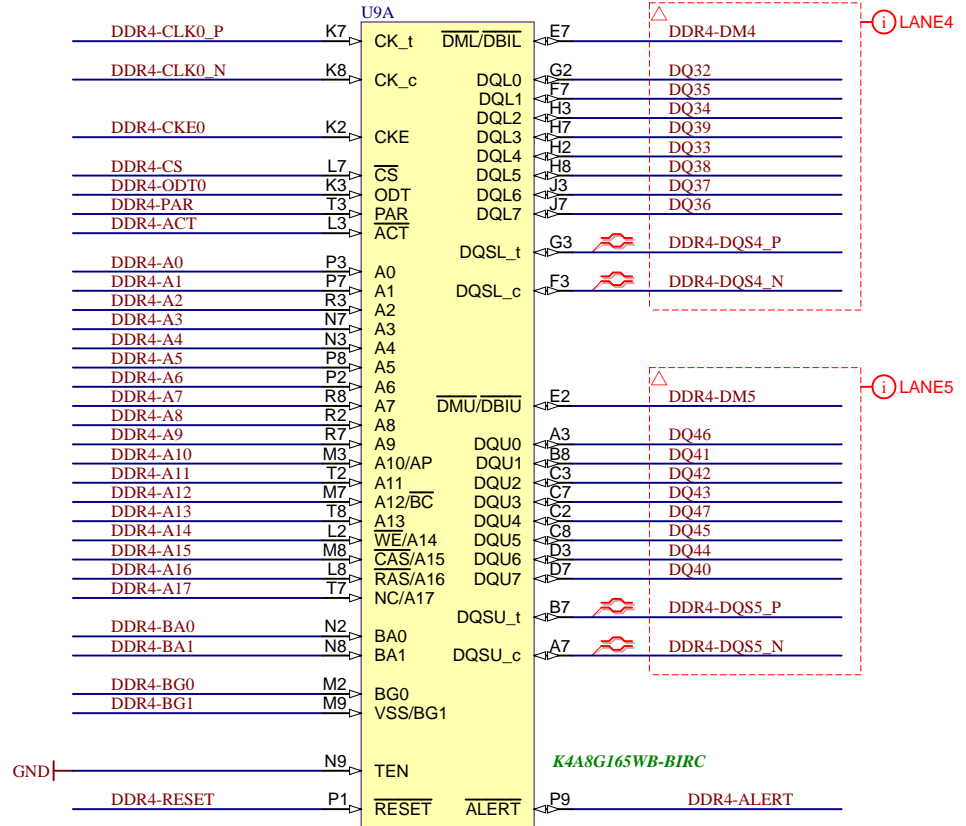
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Date: 2020-04-02		Copyright: Trenz Electronic GmbH / TT		Page 17 of 28
Filename: ZU_POWER.SchDoc				



Title: TE0808 - DDR4_1_RAM		
A4	Number: TE0808 6BI21-X	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 18 of 28
Filename: DDR4-RAM.SchDoc		

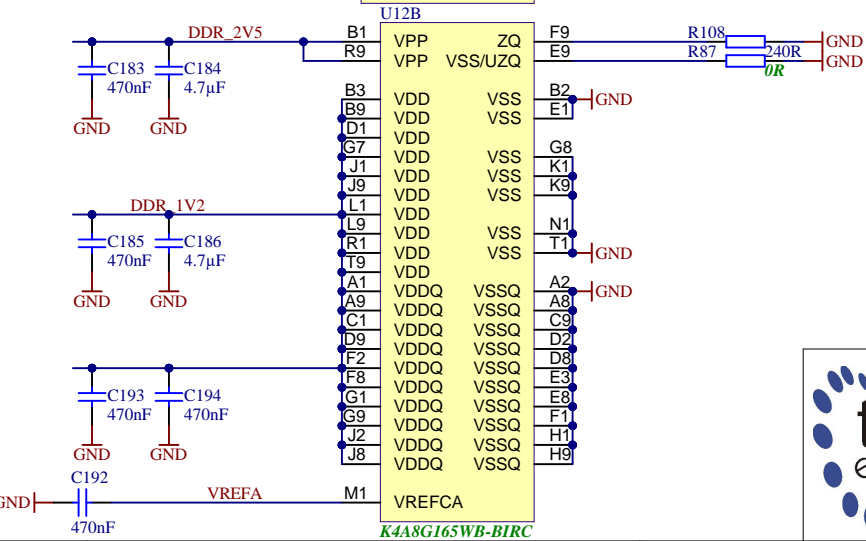
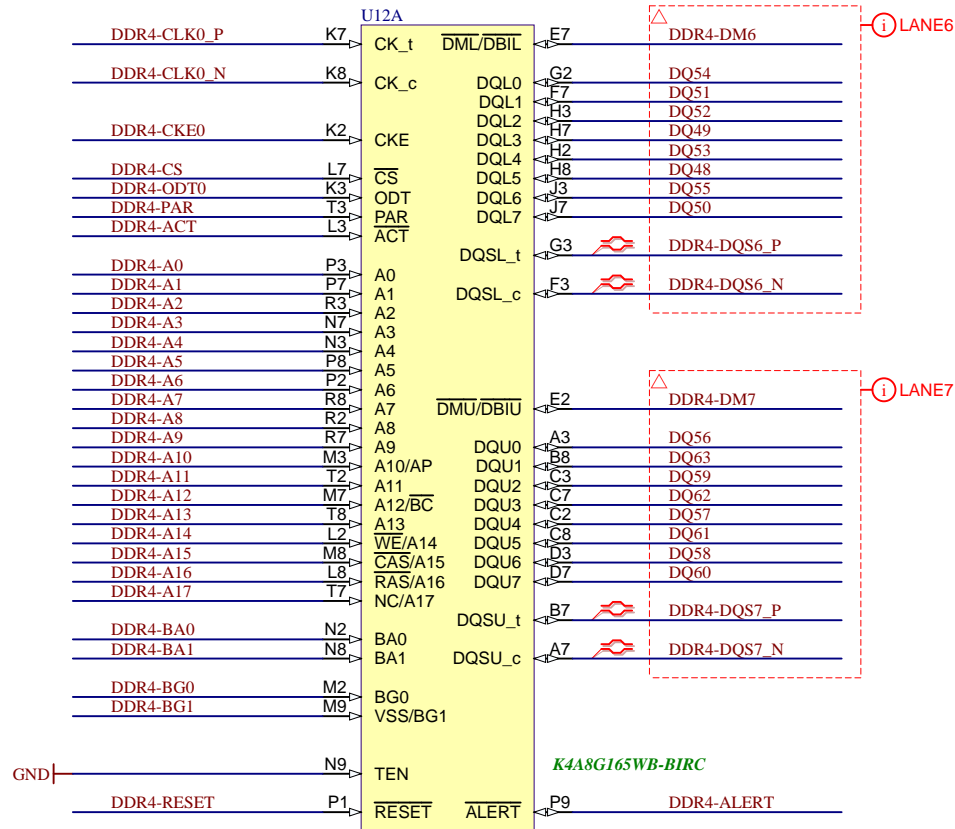


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Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 19 of 28
Filename: DDR4-RAM_2.SchDoc		

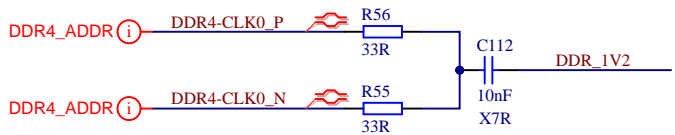
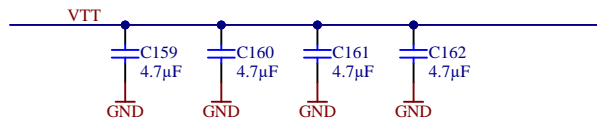
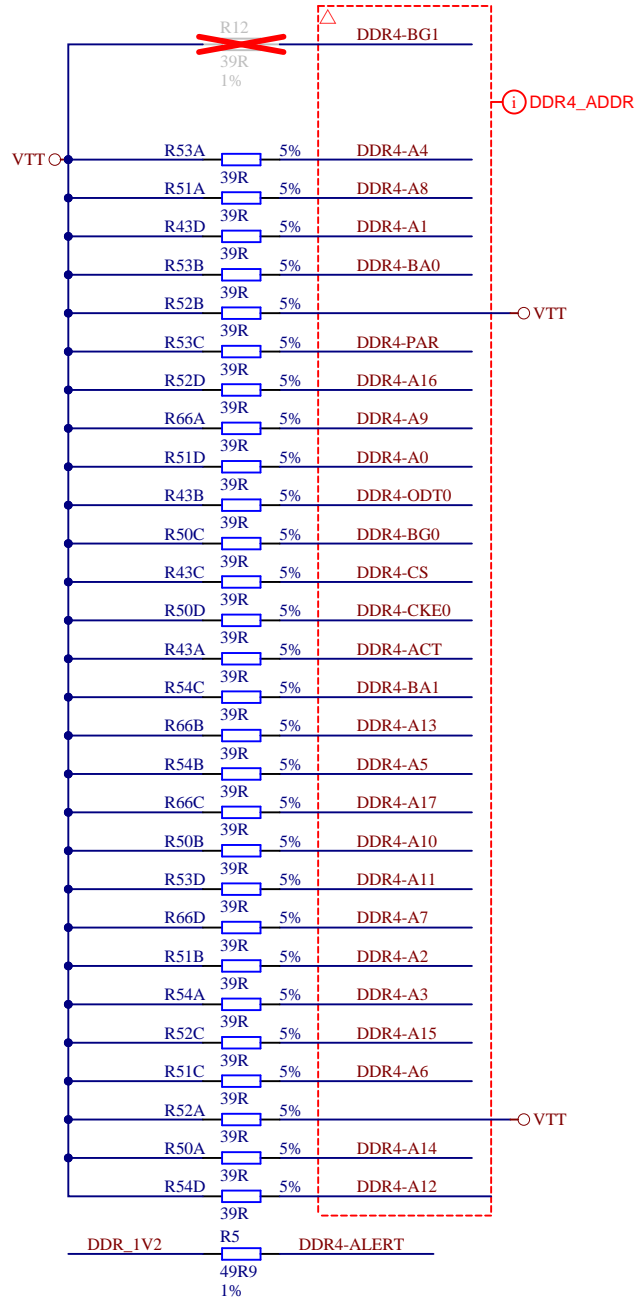


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Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 20 of 28
Filename: DDR4-RAM_3.SchDoc		

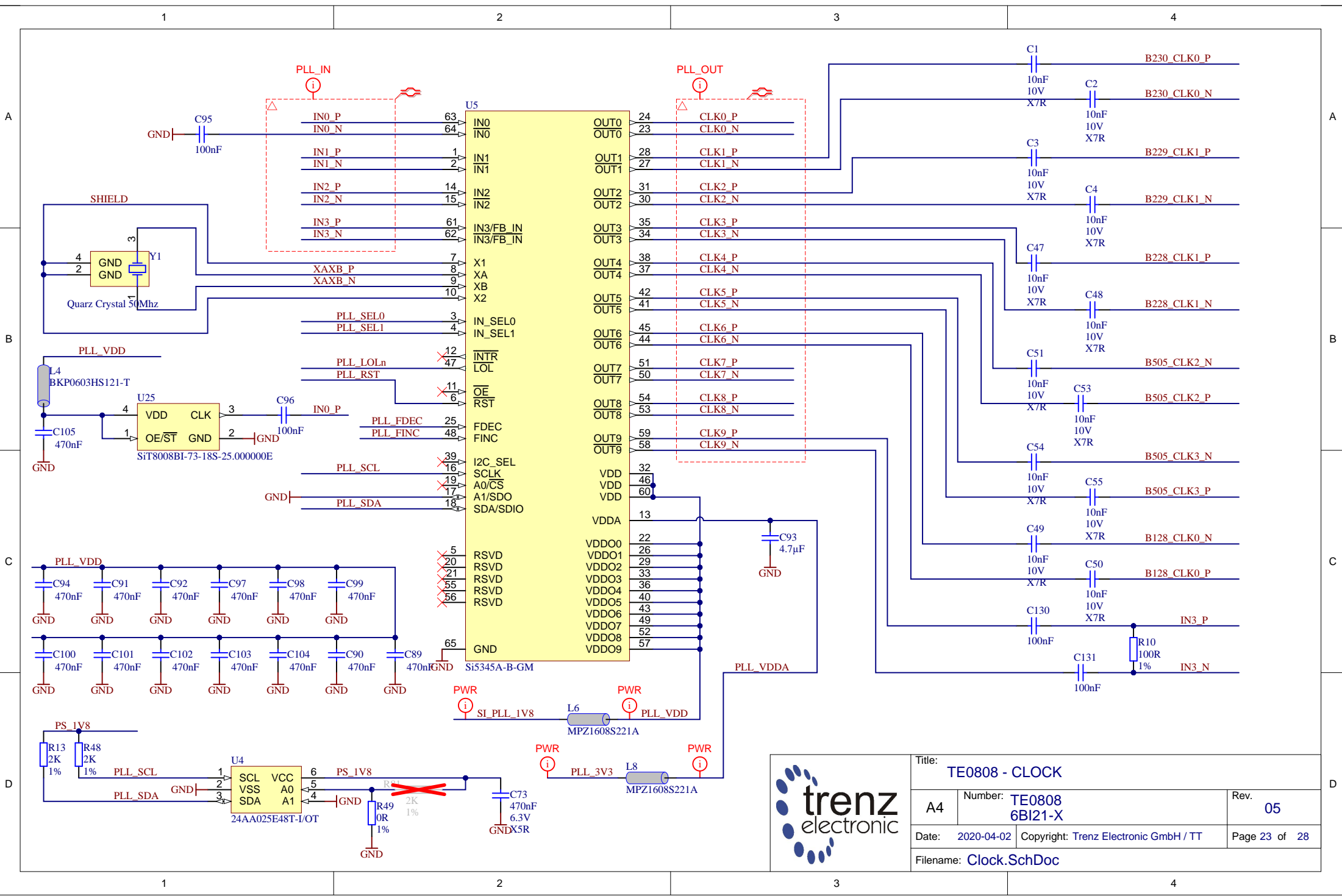




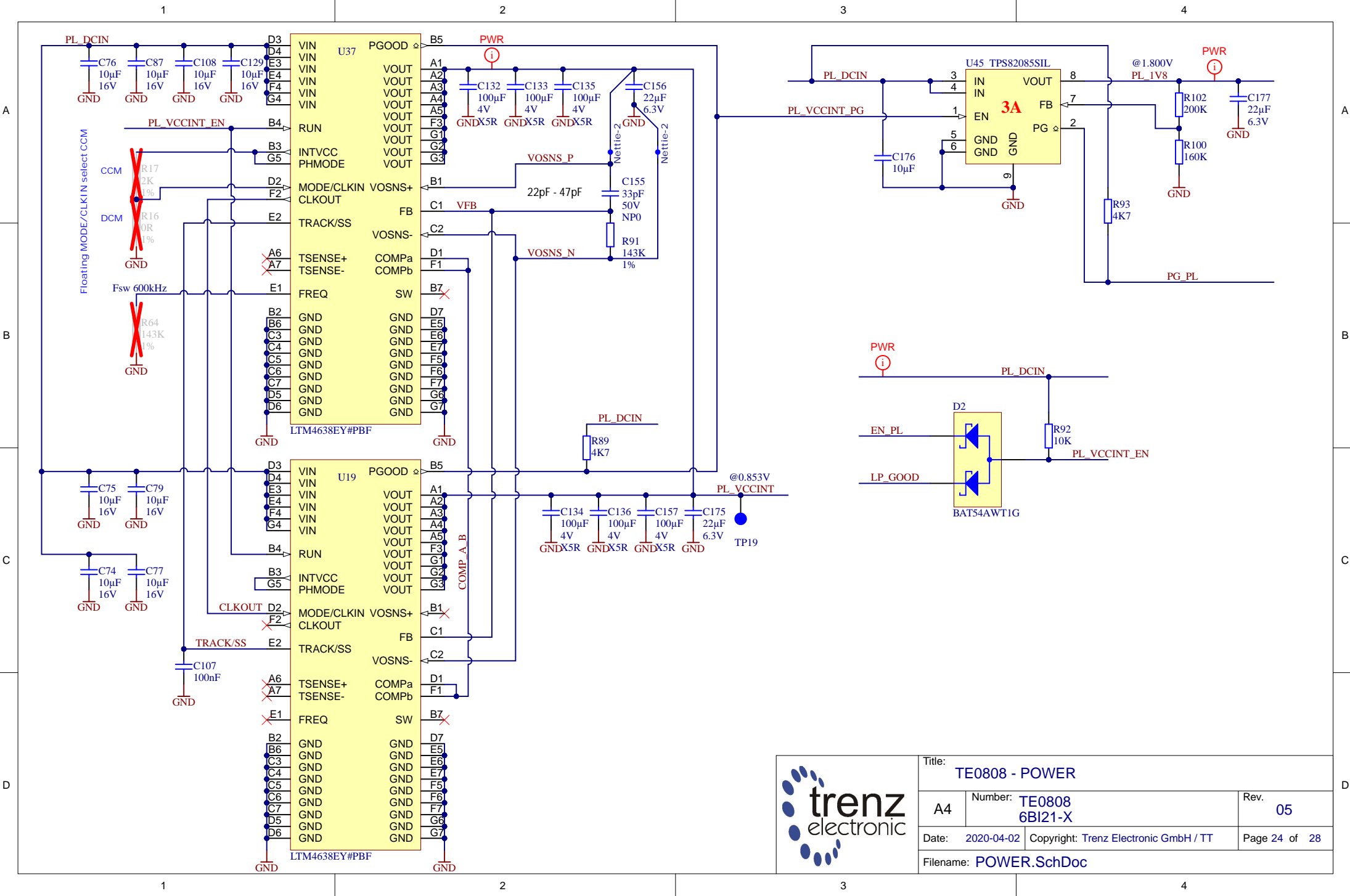
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Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 21 of 28
Filename: DDR4-RAM_4.SchDoc		



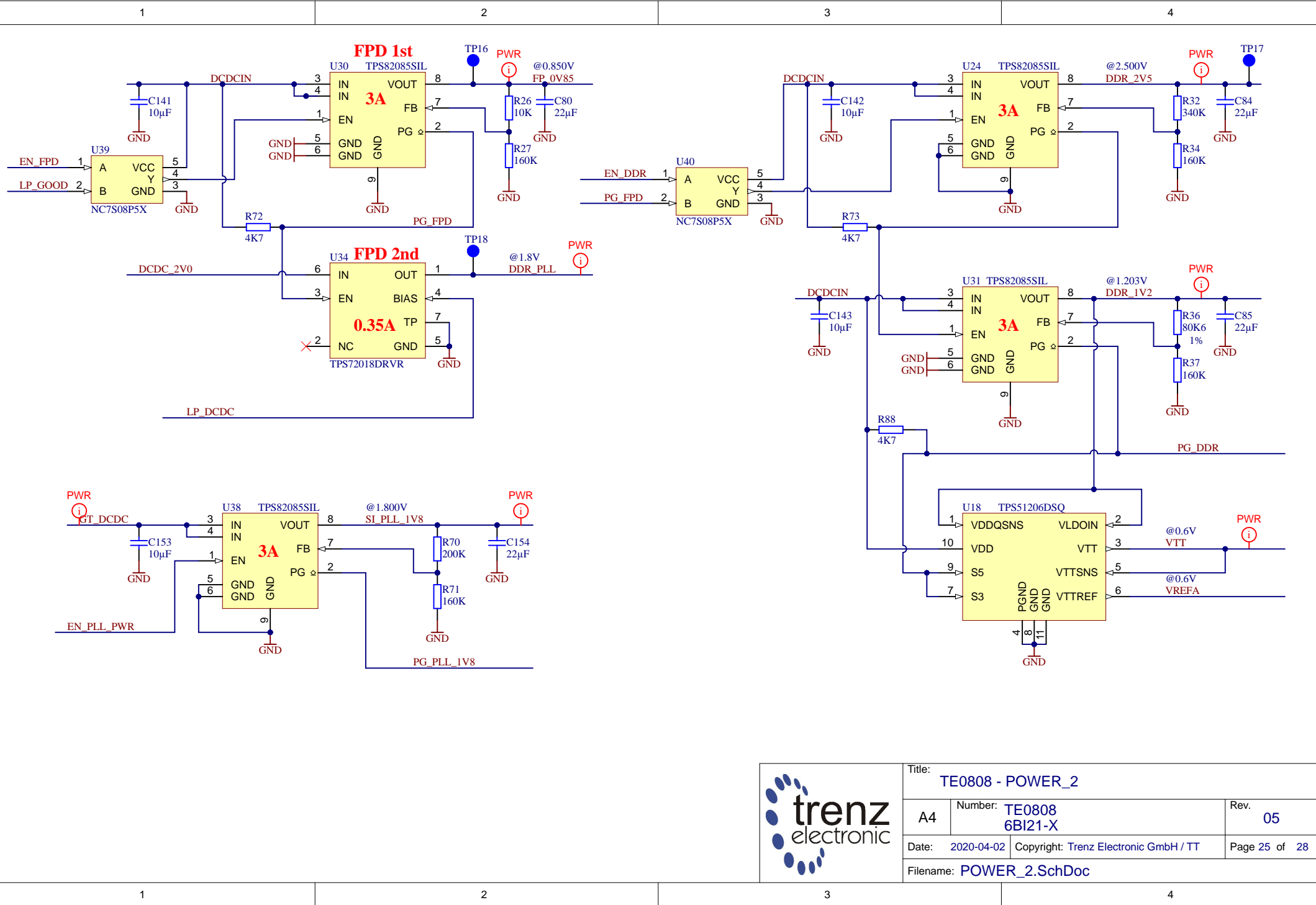
Title: TE0808 - DDR4_TERM		
A4	Number: TE0808 6BI21-X	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 22 of 28
Filename: DDR4-TERM.SchDoc		




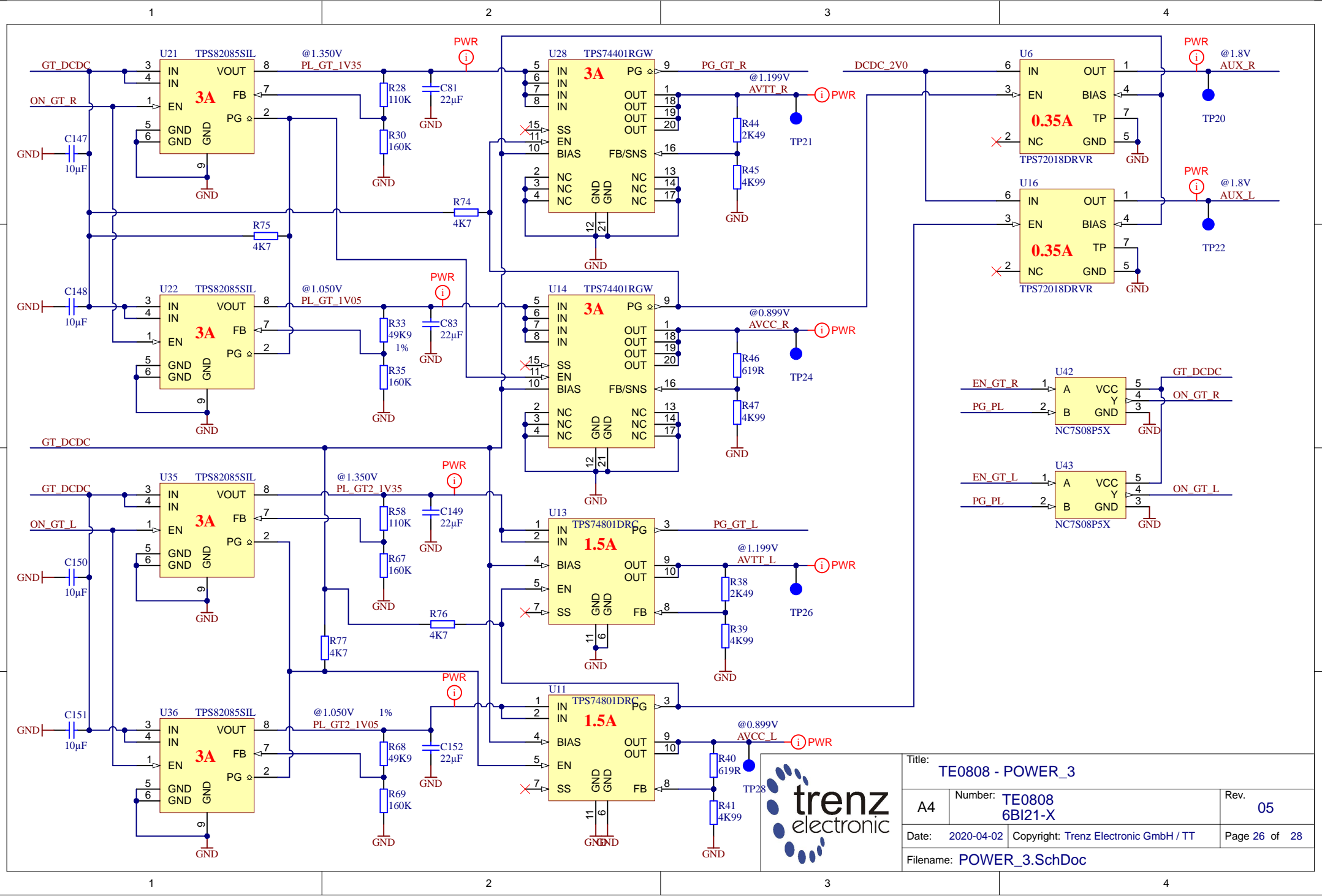
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Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 23 of 28
Filename: Clock.SchDoc		



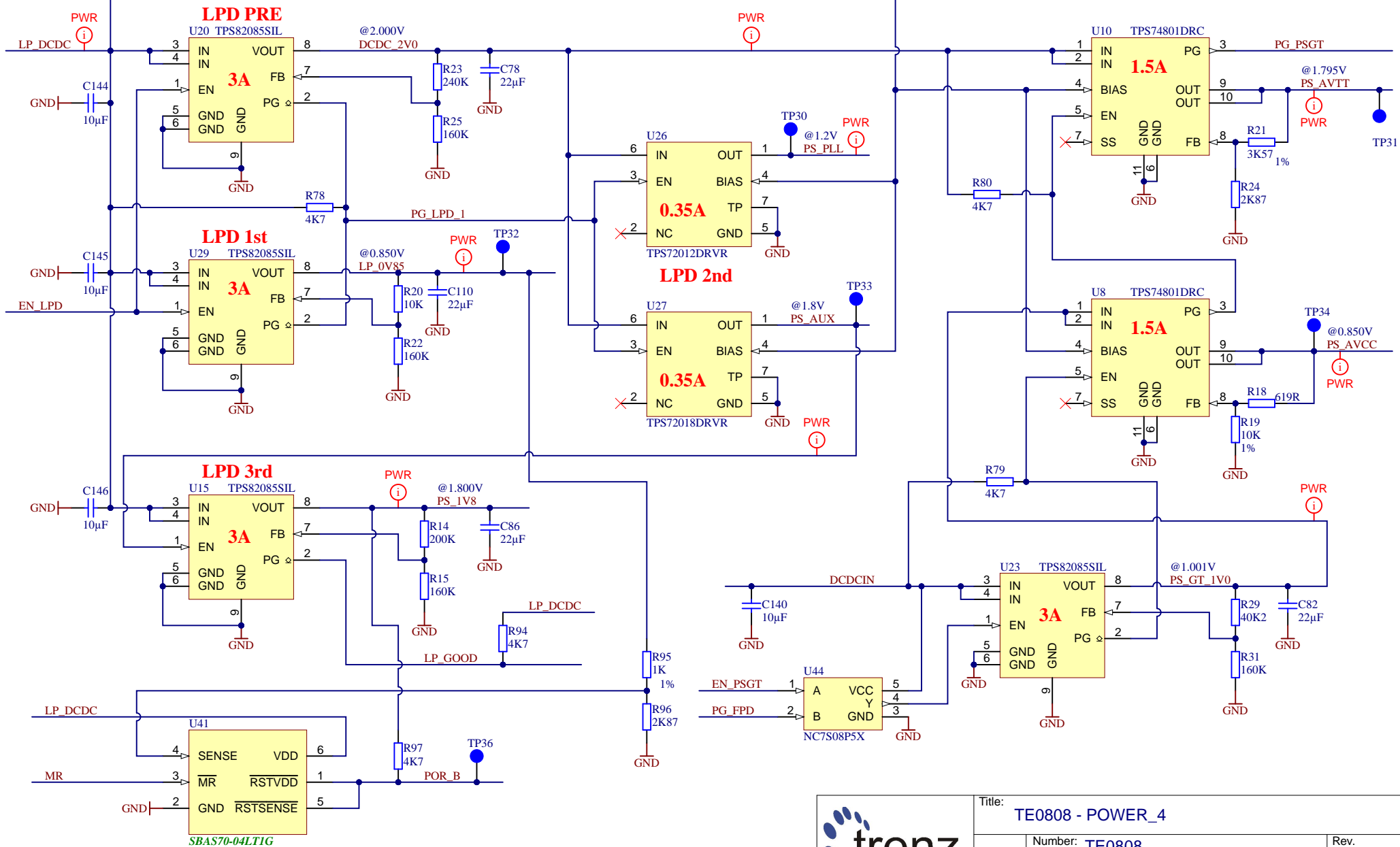
Title: TE0808 - POWER		
A4	Number: TE0808 6BI21-X	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 24 of 28
Filename: POWER.SchDoc		



		Title: TE0808 - POWER_2	
		A4	Number: TE0808 6BI21-X
Date: 2020-04-02		Copyright: Trenz Electronic GmbH / TT	
Filename: POWER_2.SchDoc		Page 25 of 28	



Title: TE0808 - POWER_3		
A4	Number: TE0808 6BI21-X	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 26 of 28
Filename: POWER_3.SchDoc		



POR\_B is "0" when LP\_OV85 lower 0.74V



Title: TE0808 - POWER_4		
A4	Number: TE0808 6BI21-X	Rev. 05
Date: 2020-04-02	Copyright: Trenz Electronic GmbH / TT	Page 27 of 28
Filename: POWER_4.SchDoc		

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Revision 04:

- 1. Added resistors R65,R82,R86,R87 (240R) for each DDR4-chip for supporting DDP DDR4 chips
- 2. Full library update

Revision 04a (09.06.2020):


- 1. VY: R19 value was changed to 10K (was: 4K99) to set PS\_MGTRAVCC 0.85V

Revision 05:

- 1. VY: revised PL\_VCCINT power supply. PCB: revised routing and components placement;
- 2. VY: added signal BG1 for DDP DDR4 IC. Added support of new packages. PCB: revised routing and components placement;
- 3. VY: R5 pulled up to 1.2V. R5 value changed to 49.9R;
- 4. VY: added test points;
- 5. VY: added MAC EEPROM U48. I2C bus PLL\_SCL/SDA. Added pull up resistor to I2C bus;
- 6. VY: PCB - revised FPGA location. Package placed 1.5mm closer to connector J3;
- 7. VY: PCB - updated silkscreen. Added company address, CE and WEEE symbols;
- 8. VY: PCB - updated signal trace lengths.

29.11.2022

- 9. Chnaged note near J2.97 and net PG\_GT\_L from "On board pull-up R" to "External pull-up R Required"

		Title: TE0808 - Changes list		
		A4	Number: TE0808 6BI21-X	Rev. 05
		Date: 2020-04-02	Copyright: Trenz Electronic GmbH	Page 28 of 28
		Filename: Revision_Changes.SchDoc		

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4